Design Guide: TIDA-050096

Scalable, High-Current, Parallel Automotive Reference Design

Description

This reference design demonstrates two methods for paralleling the TPS7B7702-Q1 linear regulator to achieve higher load currents which can be required in common applications such as phantom power supplies. The first approach uses external operational amplifiers (op amps) to parallel four TPS7B7702-Q1 channels, delivering up to 1.2A to the load. This technique is scalable and more linear regulator channels can be paralleled for additional current. The second approach uses ballast resistors to parallel two TPS7B7702-Q1 channels, providing up to 500mA of output current.

Resources

TIDA-050096	Design Folder
TPS7B7702-Q1	Product Folder
OPA388-Q1	Product Folder
LMV321A-Q1	Product Folder

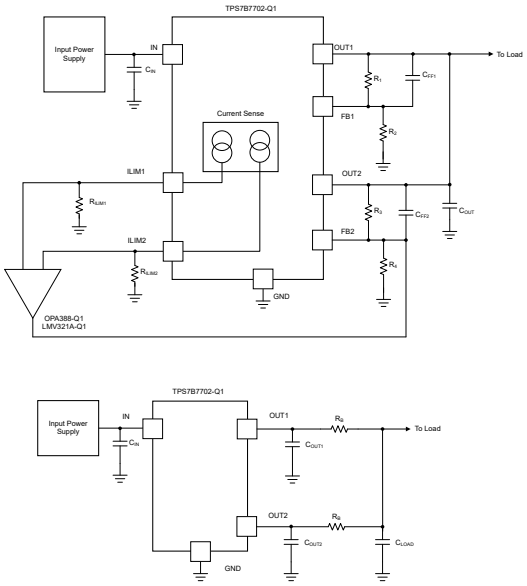
Ask the TI E2E™ support experts

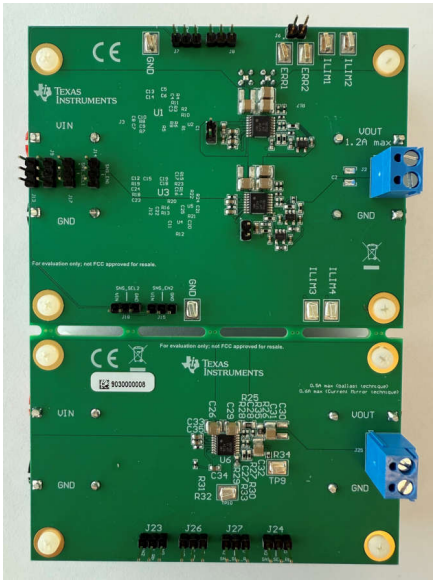
Features

- Output current: Up to 500mA
  - Using ballast resistors and two TPS7B7702-Q1 linear regulator channels
- Output current: Scalable
  - Using op amps; 1.2A capability is demonstrated using four TPS7B7702-Q1 linear regulator channels
- Integrated protection and diagnostics
- 4.5V to 40V wide input voltage range, 45V load dump
- Adjustable current-limit with external resistor

Applications

- Digital cockpit processing unit
- Telematics control unit
- Surround view system ECU
- Automotive head unit
- Unboosted audio amplifier with ANC





1 System Description

Low-noise low-dropout regulators (LDO) are required in many applications to make sure that power supply noise does not couple into the signal chain. The requirements for LDO output current continue to increase as new sensors require additional current or different loads are combined to save space. Using a single LDO for the supply is not always possible due to power dissipation limitations or output current capability. The TIDA-050096 reference design solves this issue by using multiple LDOs configured to share current in parallel. There are two methods for paralleling the TPS7B7702-Q1 in this reference design:

1. **Operational Amplifiers**: The first method uses op amps to parallel multiple TPS7B7702-Q1 channels. A wide range of op amps can be used to parallel the TPS7B7702-Q1, including the OPA388-Q1 and LMV321A-Q1. Up to four TPS7B7702-Q1 channels are paralleled in this reference design, using op amps, to deliver up to 1.2A to the load while maintaining all of the key features of a single TPS7B7702-Q1 channel. This approach can be scaled above four LDO channels; however, there is no limit to the number of channels that can be placed in parallel using this technique.
2. **Ballast Resistors**: The second method uses ballast resistors, which can be designed either as discrete resistors or as copper traces on the printed-circuit board (PCB). In some applications, the harness resistance inherent in the system can also be used as part as all of the ballast resistance. Although there is no theoretical limit to the number of TPS7B7702-Q1 LDO channels that can be paralleled using this technique, Texas Instruments recommends limiting the number to two channels. This is recommended because the error voltage, or difference between the output of each individual LDO[1], increases with output voltage as a result of the gain set by the feedback resistors. At higher voltages, the increased gain amplifies the error voltage, leading to larger ballast resistance values - potentially exceeding 1Ω for the TPS7B7702-Q1. Increasing ballast resistance can lead to an impractical approach given the adverse impact on load regulation.

1.1 Key System Specifications

Table 1-1. Key System Specifications (Parallel LDO Using Op Amps)

PARAMETER	SPECIFICATIONS
Input Voltage Range	4.5V to 40V
Output Voltage Range	1.5V to 35V
Optimized for Input Voltage, V_{IN}	12V
Optimized for Output Voltage, V_{OUT}	10V
Maximum Output Current	Scalable
	600mA is capable with 2 × TPS7B7702-Q1 channels using op amps
	900mA is capable with 3 × TPS7B7702-Q1 channels using op amps
	1.2A is capable with 4 × TPS7B7702-Q1 channels using op amps
V_{OUT} Transient Deviation, 600mA to 1.2A to 600mA, 4 parallel channels, 1A/µs (typical)(1)	+135mV_{PK}/–113mV_{PK}
V_{OUT} Transient Deviation, 600mA to 1.2A to 600mA, 4 parallel channels, 0.1A/µs (typical)(1)	+132mV_{PK}/–109mV_{PK}
V_{OUT} Transient Deviation, 450mA to 900mA to 450mA, 1A/µs (typical)(1)	+114mV_{PK}/–96mV_{PK}
V_{OUT} Transient Deviation, 450mA to 900mA to 450mA, 0.1A/µs (typical)(1)	+113mV_{PK}/–94mV_{PK}
V_{OUT} Transient Deviation, 300mA to 600mA to 300mA, 1A/µs (typical)(1)	+85mV_{PK} /–78mV_{PK}
V_{OUT} Transient Deviation, 300mA to 600mA to 300mA, 0.1A/µs (typical)(1)	+82mV_{PK} /–79mV_{PK}
Load Regulation	+16.7mV/A

(1) Each TPS7B7702-Q1 LDO has one 10µF ceramic capacitor on the OUT pin to GND.

Table 1-2. Key System Specifications (Parallel LDO Using Ballast Resistors)

PARAMETER	SPECIFICATIONS
Input Voltage Range	4.5V to 40V
Output Voltage Range	1.5V to 35V
Optimized for Input Voltage, V_{IN}	12V
Optimized for Output Voltage, V_{OUT}	10V
Maximum Output Current(1)	500mA (2 × TPS7B7702-Q1(2) channels using ballast resistors)
V_{OUT} Transient Deviation, 300mA to 600mA to 300mA, C_{FF} = Uninstalled, 1A/µs (typical)(1)	+135mV_{PK}/–326mV_{PK}
V_{OUT} Transient Deviation, 300mA to 600mA to 300mA, C_{FF} = 22nF, 1A/µs (typical)(1)	+28mV_{PK}/–226mV_{PK}
V_{OUT} Transient Deviation, 300mA to 600mA to 300mA, C_{FF} = Uninstalled, 0.1A/µs (typical)(1)	+139mV_{PK}/–323mV_{PK}
V_{OUT} Transient Deviation, 300mA to 600mA to 300mA, C_{FF} = 22nF, 0.1A/µs (typical)(1)	+29mV_{PK}/–223mV_{PK}
Ballast Resistor	1.33Ω
Load Regulation	–662mV/A

(1) Theoretically, there is no limit to the number of LDO channels which can be paralleled using ballast resistors. The reference voltage presents a significant error term in parallel LDOs and while the internal reference is shared among the two LDO channels inside the TPS7B7702-Q1 package, this is not true for separate TPS7B7702-Q1 packages. For this reason, TI recommends limiting the number of parallel TPS7B7702-Q1 LDO channels to two when using the ballast resistor technique.

(2) Each TPS7B7702-Q1 LDO has one 10µF ceramic capacitor on the OUT pin to GND, before the ballast resistor. There is one additional 10µF ceramic capacitor after the ballast resistor.

2 System Overview

2.1 Block Diagram

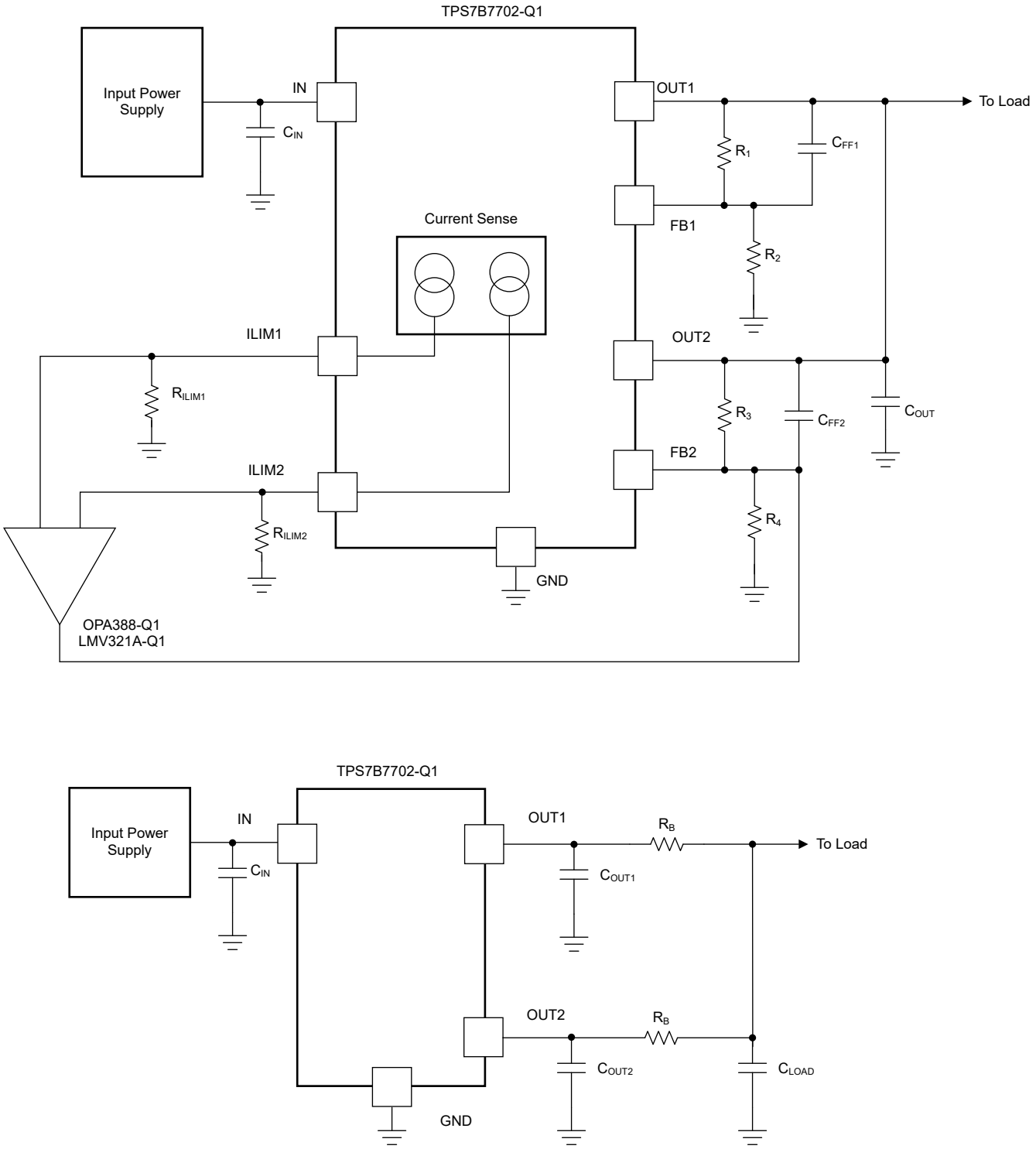


Figure 2-1. Block Diagram: Op-Amp Technique (Top) and Ballast Resistor Technique (Bottom)

2.2 Design Considerations

This reference design showcases two different techniques to paralleling the TPS7B7702-Q1 channels. One technique uses operational amplifiers to parallel multiple LDO channels while the second technique uses ballast resistors to parallel the LDO channels. Details of these different techniques, and design considerations of these techniques are discussed in Section 2.2.2 and Section 2.2.3.

2.2.1 Fault Detection and Protection

The TPS7B7702-Q1 includes both analog current sense and digital fault pins for full diagnostics of different fault conditions.

The current-sense voltage scale is selected based on the output-current range of interest. Figure 2-2 shows a recommended setting that allows for full diagnostics of each fault. Before the device goes into current-limit mode, the output current-sense voltage is linearly proportional to the actual load current. During a thermal-shutdown (TSD) and short-to-battery (STB) condition, the current-sense voltage is set to the fault voltage level that is specified in the *electrical characteristics* table of the *TPS7B770x-Q1, Automotive, Single- and Dual-Channel Antenna LDO With Current Sense* (TPS7B7702-Q1) data sheet.

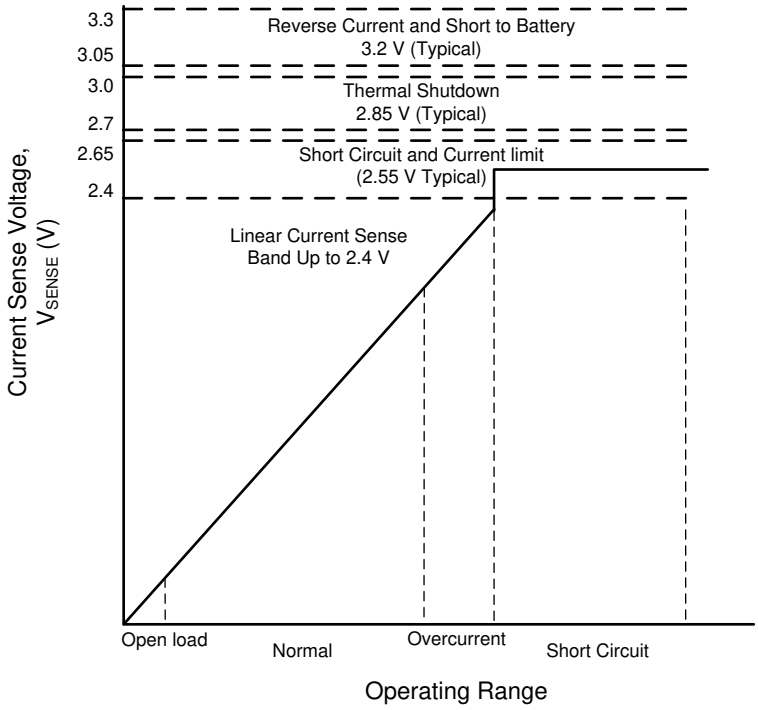


Figure 2-2. Functionality of the Current Sense Output

2.2.2 Theory of Operation - Parallel LDOs Using Op Amps

This topology senses the load current drawn from each LDO channel and uses this information to parallel multiple LDO channels together. This technique is applicable only to adjustable output LDOs. When paralleling LDOs using op amps, one LDO, called the *primary LDO*, controls the overall output. Each additional LDO channel that is paralleled is referred to as a *secondary LDO*. In this configuration, the output of an amplifier is connected to the feedback pin of each secondary LDO, allowing the primary LDO to control the overall output. Any number of secondary LDOs can be paralleled using this method, enabling the total available current to be the sum of the currents of the individual LDOs - provided the current sensing remains accurate. The TPS7B770x-Q1 current sensing has a worst-case tolerance of ±8%, which sets a practical limit on the total current that can be reliably drawn in worst-case conditions.

The compensation for the op-amp circuit is critical to maintain system stability. In this reference design, the op amp is configured as a simple integrator. An isolation resistor (R_{ISO}) is placed in series between the op amp and the FB pin to prevent the op amp from being capacitively loaded down, which can otherwise cause the op amp to become unstable (see reference [8]). Figure 2-3 shows the final op-amp circuit is provided.

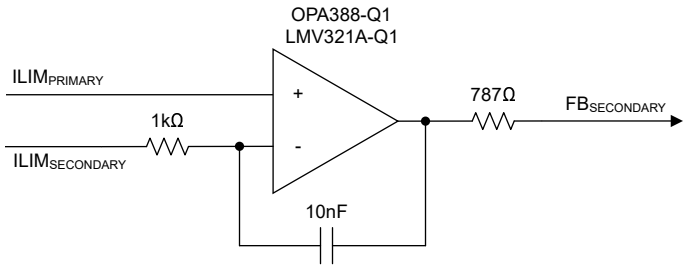


Figure 2-3. Final Op-Amp Circuit

Load transient response measurements are provided (see Section 3.3), demonstrating the stability of the circuit. Additionally, power-supply rejection ratio (PSRR) and other measurements are included to further validate the robustness of the design (again, see Section 3.3).

2.2.3 Theory of Operation - Parallel LDOs Using Ballast Resistors

Ballast resistors provide an easy way to connect multiple voltage sources together to supply power to a common load. Minimizing the voltage difference, called the error voltage V_E, at the output of each individual LDO is critical. As LDO accuracy improves, the size of the ballast resistor can be reduced.

Each TPS7B7702-Q1 has two internal LDO channels which share an internal reference. This eliminates the dominant source of error in paralleled LDOs using ballast resistors, which is the difference among reference voltages. The remaining sources of error come from the ballast resistors, the internal output field-effect transistor (FET), and the amplifier. These errors show up as the offset voltage, which is also a function of line and load. The offset voltage, combined with the tolerance in the setpoint feedback resistors, make up the total error V_E of each LDO. To achieve the smallest current-sharing error between the different LDOs, use 0.1% (or better) tolerance feedback resistors. The offset voltage is magnified by the internal error amplifier gain, which is set as a function of the necessary output voltage to determine V_{OUT}. In this reference design, all ballast resistors are configured to be the same value, for simplicity.

Traditionally, the ballast resistance is chosen using Equation 1 to set the current imbalance I_{MAX} of the parallel LDOs.

$$R_B = \frac{\underset{1<x<n}{max} V_{En} - \underset{1<x<n}{min} V_{En}}{\Delta I_{MAX}} \quad (1)$$

This formula does not account for the load voltage, V_{LOAD}, which is also a requirement for most modern power supplies designed with parallel LDOs. Texas Instruments has modernized the design and analysis of parallel LDOs using ballast resistors (see references [4] and [6]), and a downloadable software tool has been developed to design R_B for our LDOs against a set of system requirements (see reference [5]). The parallel TPS7B7702-Q1 devices using ballast resistors are designed by using the downloadable software tool to assess the system requirements and design the necessary ballast resistance.

TPS7B7702

LDO Specifications

Parameter	Value	Units	Optional User Entry	Units
V_E, high	63.503278	mVdc	63.50327828	mVdc
V_E, low	-63.44464	mVdc	-63.44464286	mVdc
Thermal Impedance T_{JA}	40.3	°C / W		°C / W
V_{REF}	1.233	Vdc		

Parallel LDO System Requirements

Parameter	Value	Units		
T_A	25	°C		°C
Maximum T_J per LDO	125	°C		°C
V_{IN}	12	Vdc	12	Vdc
V_{OUT}	10.048	Vdc	10.048	Vdc
Allowable load regulation	0.5	Vdc	0.5	Vdc
System Noise Requirement (10 Hz - 100 kHz)	167	µVrms		µVrms
Total System Load:	0.5	A	0.5	A
Minimum Ballast Resistance needed	423.15974	mΩ		
Optimum Ballast Resistance	1655.1184	mΩ		
Ballast Resistance Selected	1330	mΩ	1330	mΩ
	N =			
Minimum number of parallel LDO's required:	2			

Figure 2-4. Screenshot Showing the Parallel LDO Using Ballast Resistors Calculator

In addition to I_{OUTn} and V_{LOAD}, other system requirements can require using a parallel LDO topology such as noise, PSRR, dropout and thermal limitations. In brief, parallel LDOs using ballast resistors:

1. Reduce the system noise by a factor of the square root of the number of LDOs in parallel
2. Increase the system PSRR when compared with using a single LDO
3. Reduce the dropout requirement by spreading the load current across multiple LDOs
4. Decrease the junction temperature of the linear regulator by spreading the power dissipation across multiple LDOs

For a detailed discussion on all of these system requirements, how parallel LDOs using ballast resistors can increase performance, and how many parallel LDOs are needed for the system requirements, see reference [4], [5], and [6].

Ballast resistors are typically employed as either a PCB trace or a discrete resistor. In general, PCB trace resistors favor applications which are low cost. PCB trace resistors are also a good choice for applications which operate in a narrow temperature range or experience very high temperatures. Trace resistors are an excellent choice where multiple low-current devices are paralleled together (such as are seen in high-voltage LDOs, which are typically limited in the available output currents).

Discrete resistors are a good choice for applications which require maximum performance (where output voltage tolerance and transient responses are critical). A discrete resistor approach also favors applications where high-current devices are being paralleled (such as low-voltage LDOs, where high-current devices are readily available). Designing with a discrete ballast resistor becomes challenging when ambient temperatures exceed 125°C, and it is difficult to use discrete ballast resistors above 150°C. For a detailed discussion on ballast resistor analysis and design, see reference [4].

Table 2-1. PCB Trace Resistor vs Discrete Resistor Summary

BALLAST RESISTOR OPTION	ASSOCIATED COST	TOLERANCE	PARASITIC INDUCTANCE	HIGH-TEMPERATURE OPERATION
PCB Trace Resistor	*None* after the PCB trace resistor design is complete	Wide: Resistor value nearly doubles across the operating temperature range	Increases with PCB trace length	Only limited by the Tg of the FR4
Discrete Resistor	Must be sourced, purchased, and installed on each PCB	Tight: discrete resistors come in 100ppm or lower tolerances	Low	Large resistor package sizes (0805 or 1206) can be required at higher temperatures

2.3 Highlighted Products

2.3.1 TPS7B7702-Q1, Automotive, Dual-Channel Antenna Low Dropout (LDO) Regulator With Current Sense

The TPS7B770x-Q1 family of devices feature a single and dual, high-voltage low-dropout regulator (LDO) with current sensing, designed to operate with a wide input-voltage range from 4.5V to 40V (45V load dump protection). These devices provide power to the low-noise amplifiers of the active antenna through a coax cable with 300mA per channel current. Each channel also provides an adjustable output voltage from 1.5V to 20V.

These devices provide diagnostics through the current sense and error pins. To monitor the load current, a high-side current-sense circuitry provides a proportional analog output to the sensed load current. The accurate current sense allows detection of open, normal, and short-circuit conditions without the need for further calibration. Current sense can be multiplexed between channels and devices to save analog-to-digital converter (ADC) resources. Each channel also implements adjustable current limit with an external resistor.

An integrated reverse polarity diode eliminates the need for an external diode. These devices feature standard thermal shutdown, short-to-battery protection on the output, and reverse current protection. Each channel has internal inductive clamp protection on the output during inductive switch off.

These devices operate over a –40°C to +125°C ambient temperature range.

2.3.2 OPAx388 Automotive, Precision, Zero-Drift, Zero-Crossover, True Rail-to-Rail, Input/Output Operational Amplifiers

The OPA388-Q1 and OPA2388-Q1 (OPAx388-Q1) are automotive, low-noise, fast-settling, zero-drift, precision operational amplifiers that provide rail-to-rail input and output operation. Excellent ac performance, combined with only 0.25µV of offset and 0.005µV/°C of drift overtemperature, make the OPAx388-Q1 a great choice for driving high-resolution, analog-to-digital converters (ADCs) with high accuracy. Zero-crossover technology minimizes any offset change over the common-mode range. The combination of low drift and very low 1/f noise allow the OPAx388-Q1 to monitor and detect faulty conditions without compromising signal integrity.

These devices are specified over the industrial temperature range of –40°C to +125°C.

2.3.3 LMV321A-Q1 Automotive Low-Voltage Rail-to-Rail Output Operational Amplifier

The LMV3xxA-Q1 family includes single (LMV321A-Q1), dual (LMV358A-Q1), and quad-channel (LMV324A-Q1) low-voltage (2.5V to 5.5V) automotive operational amplifiers (op amps) with rail-to-rail output swing capabilities. These op amps provide a cost-effective method for space-constrained applications such as infotainment and lighting where low-voltage operation and high capacitive-load drive are required. The capacitive-load drive of the LMV3xxA-Q1 family is 500pF, and the resistive open-loop output impedance makes stabilization easier with much higher capacitive loads. These op amps are designed specifically for low-voltage operation (2.5V to 5.5V) with performance specifications similar to the LMV3xx-Q1 devices.

The robust design of the LMV3xxA-Q1 family simplifies circuit design. The op amps feature unity-gain stability, an integrated RFI and EMI rejection filter, and no-phase reversal in overdrive conditions.

The LMV3xxA-Q1 family is available in industry-standard packages such as SOIC, MSOP, SOT-23, and TSSOP packages.

3 Hardware, Testing Requirements, and Test Results

3.1 Hardware Requirements

3.2 Test Setup

The TIDA-050096 reference design showcases two methods to paralleling the TPS7B7702-Q1 LDOs. All components needed for evaluation are populated: input, output, V_{CC}, sense and feedforward capacitors are installed, as well as error, current limit, feedback, and sense resistors are also installed. See also the *TPS7B770x-Q1, Automotive, Single- and Dual-Channel Antenna LDO With Current Sense* data sheet for guidance on selecting these components. The TIDA-050096 reference design is configured for 12V input, 10V output, with a range of load-current options.

The first method to parallel the TPS7B7702-Q1 LDOs uses op amps to current share the LDOs. Two different op amps are used to characterize performance of the reference design (OPA388-Q1 and LMV321A-Q1). The compensation capacitors and resistors to maintain stability with the addition of the new feedback loop are installed. The TIDA-050096 reference design supports up to four paralleled LDO channels to obtain up to 1.2A output current with all of the features already included in the single TPS7B7701-Q1 LDO.

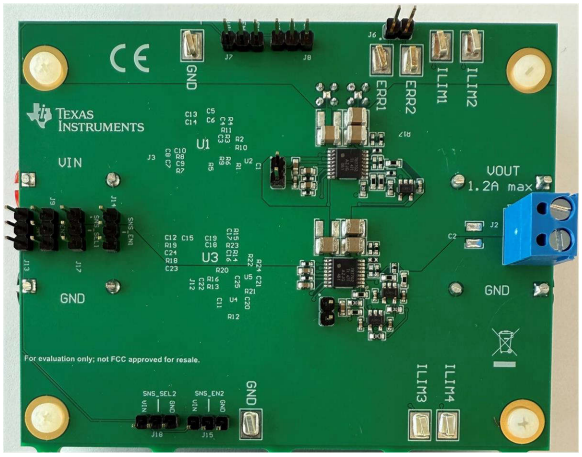


Figure 3-1. 2 ×–4 × Parallel LDO Channels Using Op Amps and Current Sensing

Four LDO channels is not the limit with this technique. If more current is needed in the end application, additional LDO channels can be paralleled using the op-amp technique, as necessary.

The second method to parallel the TPS7B7702-Q1 LDOs uses ballast resistors. Recommended ballast resistors are installed, as well as an extra load capacitor. While there is no fundamental limit to the number of LDOs which can be paralleled using ballast resistors, because a single reference cannot be shared among TPS7B7702-Q1 devices in different packages, the paralleled LDOs across packages experience an increased error voltage. This increase in error voltage directly correlates to an increase in ballast resistance. TI recommends limiting the number of parallel TPS7B7702-Q1 channels to the two LDOs inside the package and if more LDOs are needed, to use the op-amp parallel method.

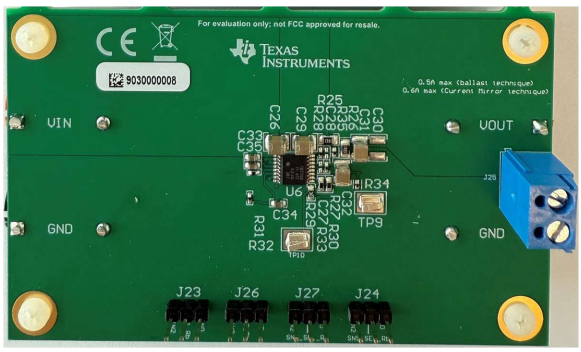


Figure 3-2. 2 × Parallel LDO Channels Using Ballast Resistors

The TPS7B7702-Q1 LDO channels can be enabled or disabled by using the 3-pin headers (J7, J8, J9, J13 for the op-amp method, or J23 and J26 for the ballast resistor method).

- Tie the center pin of the 3-pin header to Vin to enable the device
- Tie the center pin of the 3-pin header to a GND to disable the device

Test points are provided to measure the ILIM voltage of each LDO channel to confirm each is sharing the load current equally. A 2-pin header connects V_{CC} of the TPS7B7702-Q1 to the positive power rail of the op amp, and can be used to measure the current draw of the op amp. The V_{CC} pin can source up to 15mA current draw from external circuitry. J2 (parallel LDOs using op amps) or J25 (parallel LDOs using ballast resistors) can be used to connect external loading for evaluation.

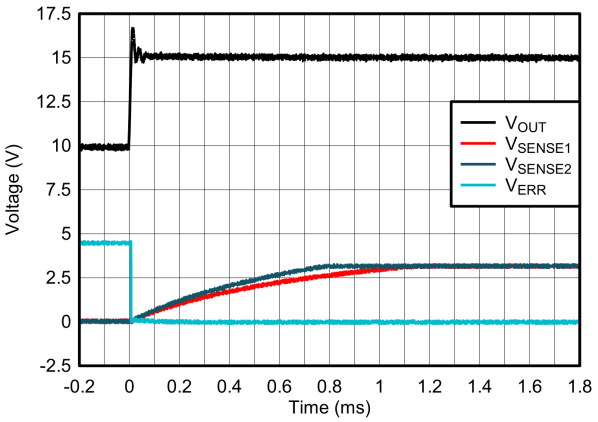
The parallel LDOs using op-amp designs include additional connectors for evaluation. MMCX connectors are available to measure V_{IN} and V_{OUT}. Test points are available to measure V_{ERR} for each package (V_{ERR1} for the top IC and V_{ERR2} for the bottom IC). A 2-pin header can be used to short V_{ERR1} to V_{ERR2} which is how the measurements in this design guide are captured.

3.3 Test Results - Parallel LDOs Using Op Amps

The test results in this section are taken under the following conditions:

V_{IN} = 12V, V_{OUT} = 10V, C_{INn} = 10µF, C_{OUTn} = 10µF, C_{FFn} = 22nF, V_{ERR} = V_{ERR1} = V_{ERR2},
Op-Amp = OPA388-Q1 (unless otherwise noted).

3.3.1 Short to Battery



V_{ERR} = V_{ERR1}

Figure 3-3. 2 × LDO Channels

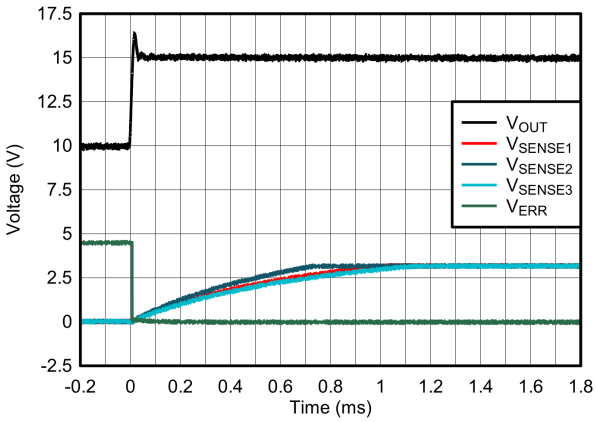


Figure 3-4. 3 × LDO Channels

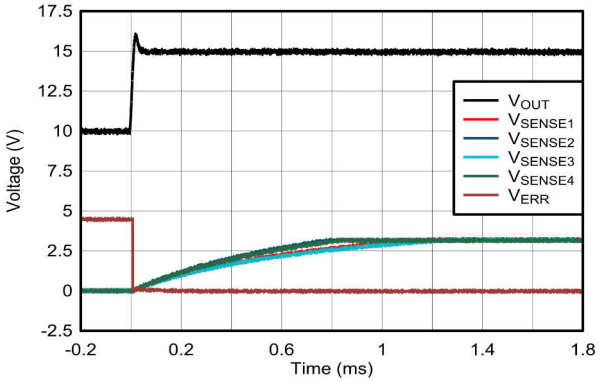
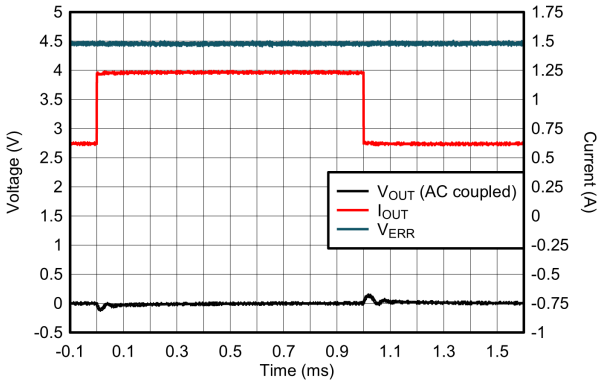


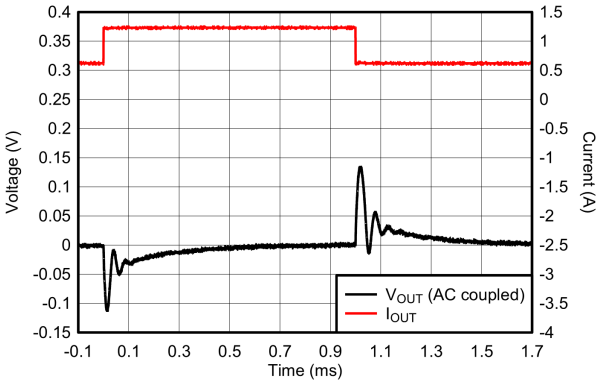
Figure 3-5. 4 × LDO Channels

3.3.2 Load Transient Response



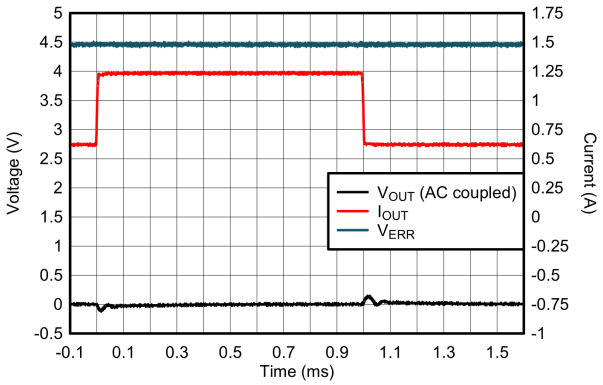
I_{OUT} = 600mA to 1.2A to 600mA, SR = 1A/µs

Figure 3-6. 4 × LDO Channels Load Transient



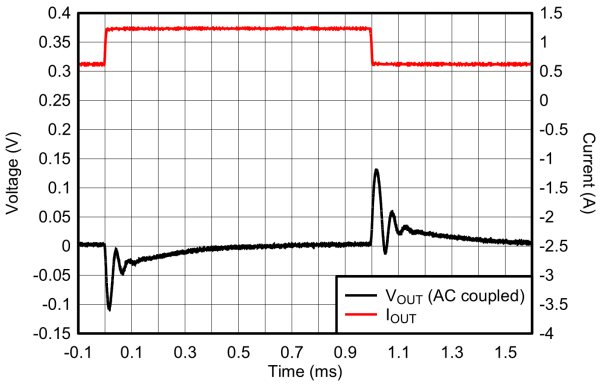
I_{OUT} = 600mA to 1.2A to 600mA, SR = 1A/µs

Figure 3-7. 4 × LDO Channels Load Transient (Zoomed in)



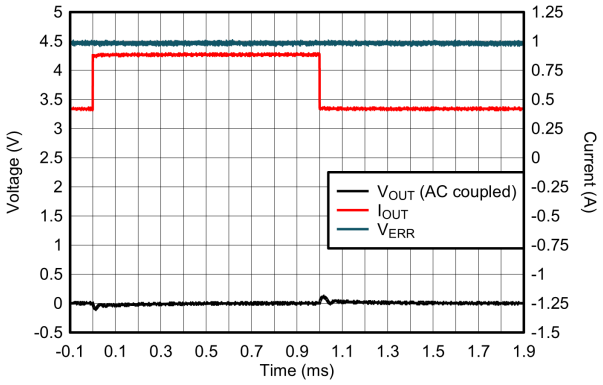
I_{OUT} = 600mA to 1.2A to 600mA, SR = 0.1A/µs

Figure 3-8. 4 × LDO Channels Load Transient



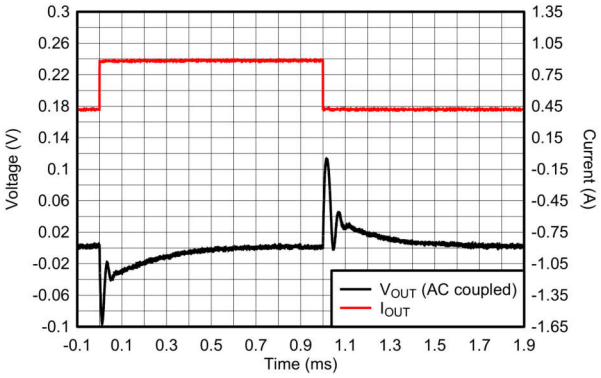
I_{OUT} = 600mA to 1.2A to 600mA, SR = 0.1A/µs

Figure 3-9. 4 × LDO Channels Load Transient (Zoomed in)



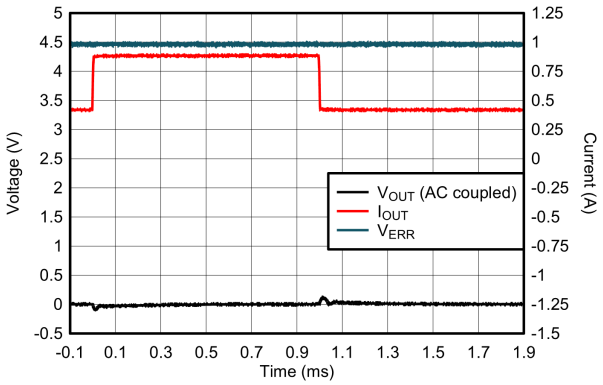
I_{OUT} = 450mA to 900mA to 450mA, SR = 1A/µs

Figure 3-10. 3 × LDO Channels Load Transient



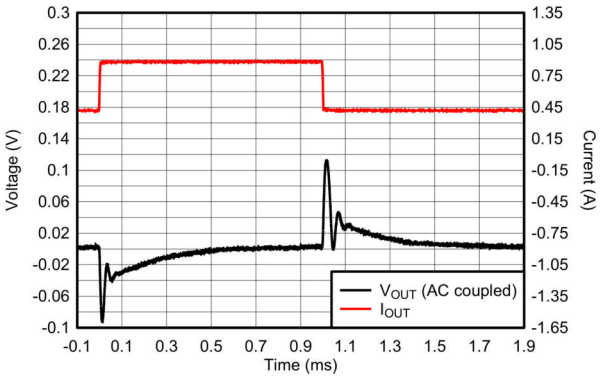
I_{OUT} = 450mA to 900mA to 450mA, SR = 1A/µs

Figure 3-11. 3 × LDO Channels Load Transient (Zoomed in)



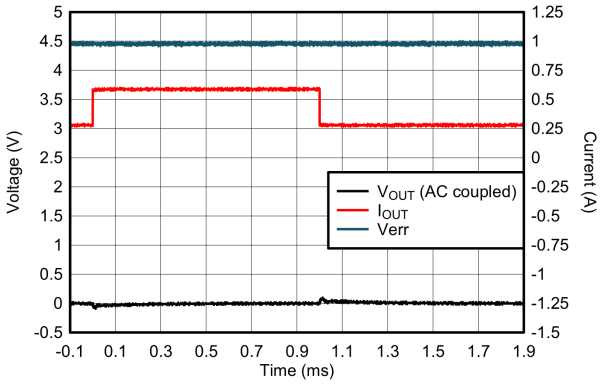
I_{OUT} = 450mA to 900mA to 450mA, SR = 0.1A/µs

Figure 3-12. 3 × LDO Channels Load Transient



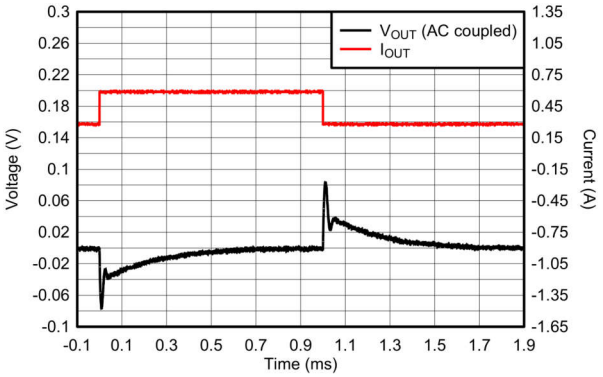
I_{OUT} = 450mA to 900mA to 450mA, SR = 0.1A/µs

Figure 3-13. 3 × LDO Channels Load Transient (Zoomed in)



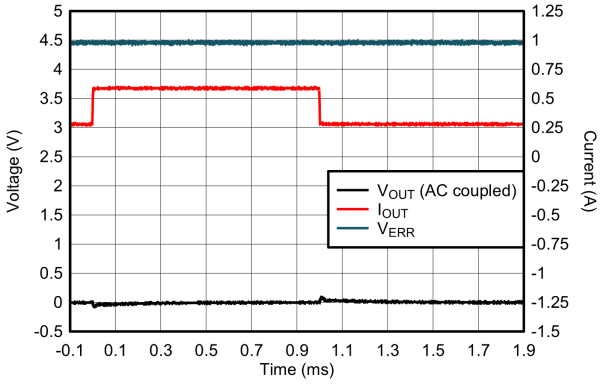
I_{OUT} = 300mA to 600mA to 300mA, SR = 1A/µs, V_{ERR} = V_{ERR1}

Figure 3-14. 2 × LDO Channels Load Transient



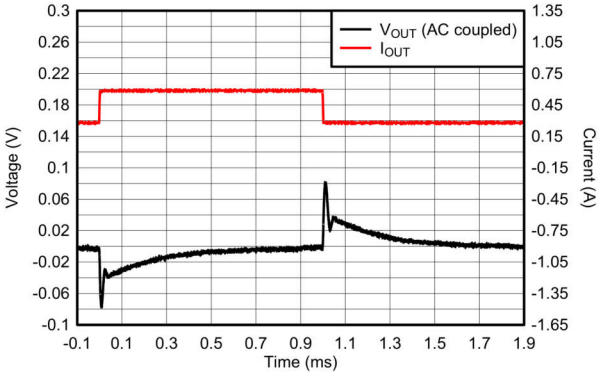
I_{OUT} = 300mA to 600mA to 300mA, SR = 1A/µs

Figure 3-15. 2 × LDO Channels Load Transient (Zoomed in)



I_{OUT} = 300mA to 600mA to 300mA, SR = 0.1A/µs, V_{ERR} = V_{ERR1}

Figure 3-16. 2 × LDO Channels Load Transient



I_{OUT} = 300mA to 600mA to 300mA, SR = 0.1A/µs

Figure 3-17. 2 × LDO Channels Load Transient (Zoomed in)

3.3.3 Current Limit

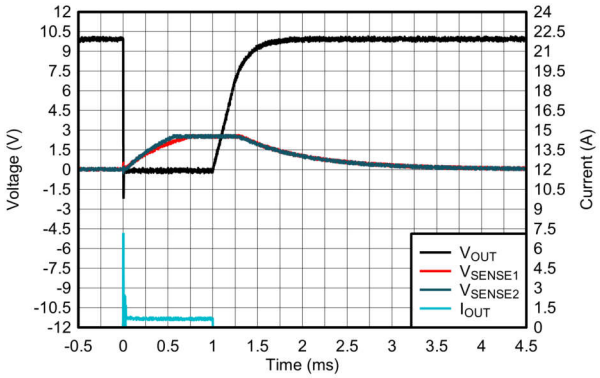


Figure 3-18. 2 x LDO Channels

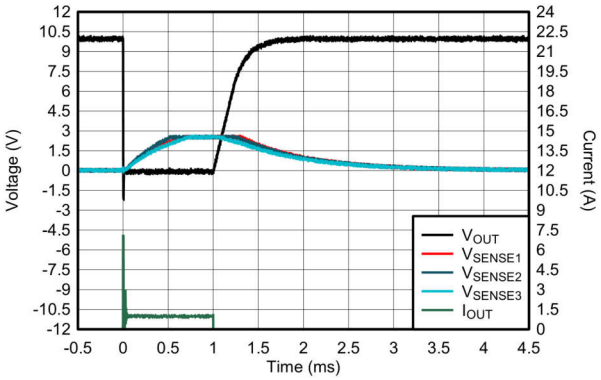


Figure 3-19. 3 x LDO Channels

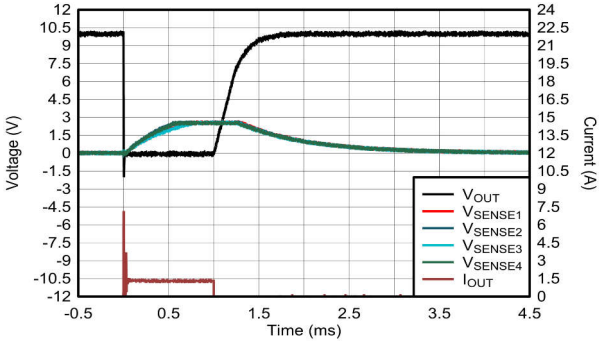
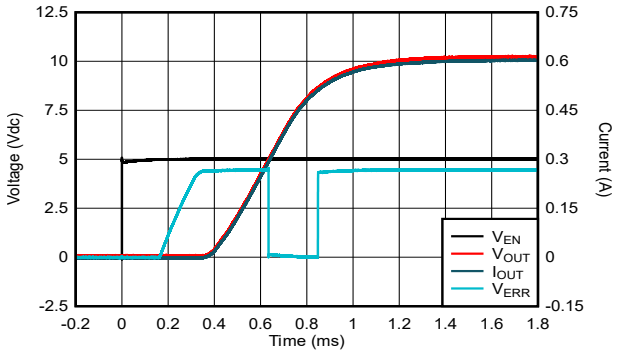


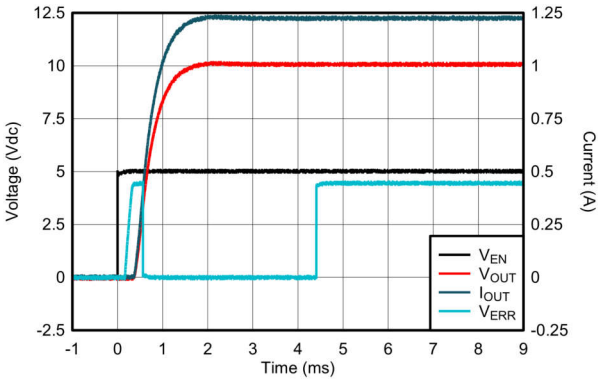
Figure 3-20. 4 x LDO Channels

3.3.4 Start-Up



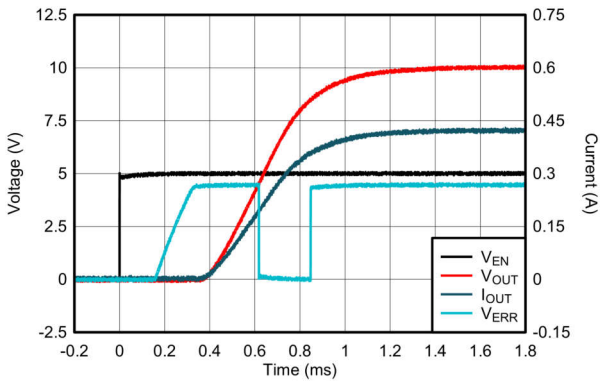
V_{IN} = 12V, I_{OUT} = 600mA, 4 x LDO channels

Figure 3-21. Start-Up Into a 600mA Load



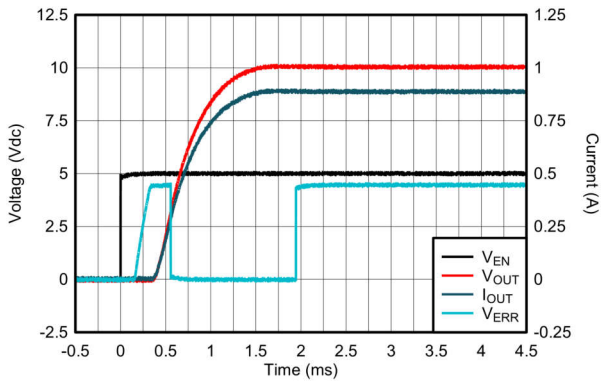
V_{IN} = 12V, I_{OUT} = 1.2A, 4 x LDO channels

Figure 3-22. Start-Up Into a 1.2A Load



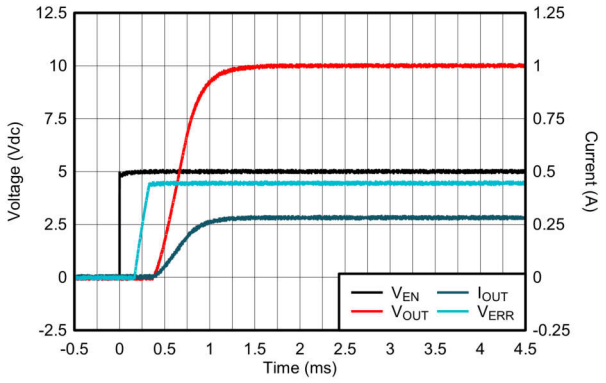
V_{IN} = 12V, I_{OUT} = 415mA, 3 x LDO channels

Figure 3-23. Start-Up Into a 415mA Load



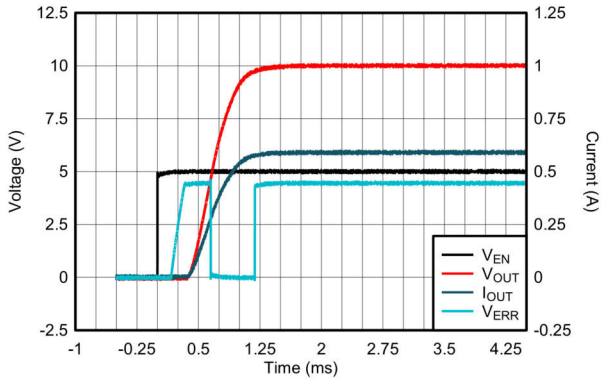
V_{IN} = 12V, I_{OUT} = 870mA, 3 x LDO channels

Figure 3-24. Start-Up Into a 870mA Load



V_{IN} = 12V, I_{OUT} = 275mA, V_{ERR} = V_{ERR1}, 2 x LDO channels

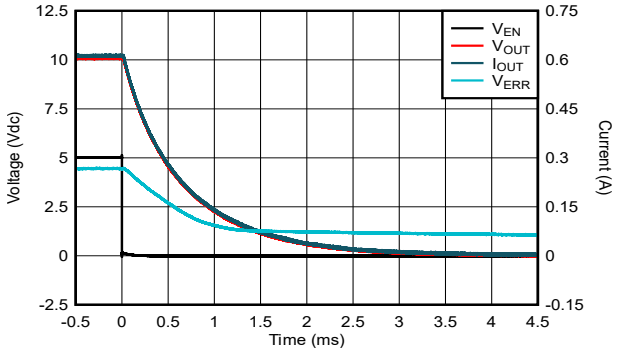
Figure 3-25. Start-Up Into a 275mA Load



V_{IN} = 12V, I_{OUT} = 580mA, V_{ERR} = V_{ERR1}, 2 x LDO channels

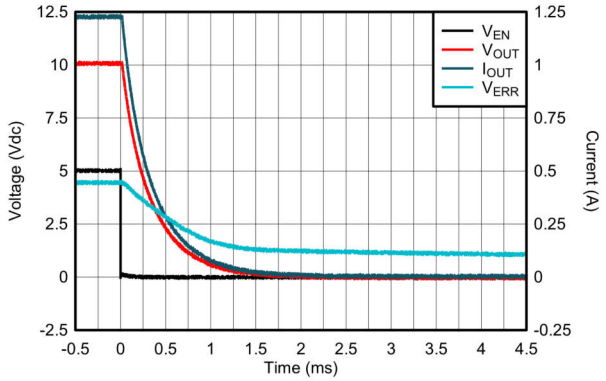
Figure 3-26. Start-Up Into a 580mA Load

3.3.5 Shutdown



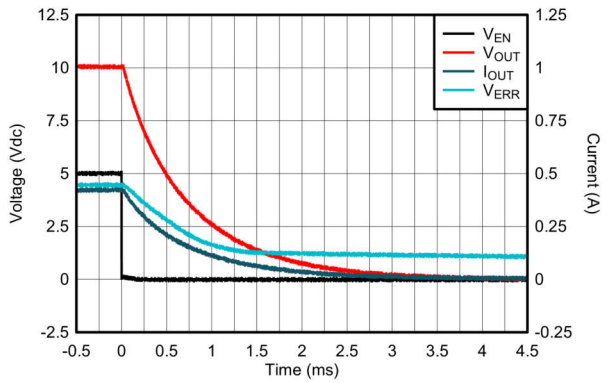
V_{IN} = 12V, I_{OUT} = 600mA, 4 x LDO channels

Figure 3-27. Shutdown Into a 600mA Load



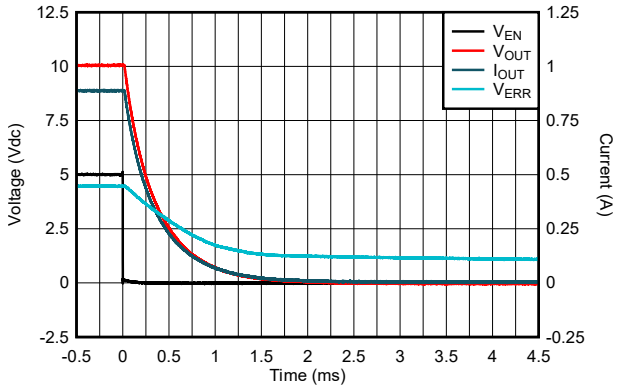
V_{IN} = 12V, I_{OUT} = 1.2A, 4 x LDO channels

Figure 3-28. Shutdown Into a 1.2A Load



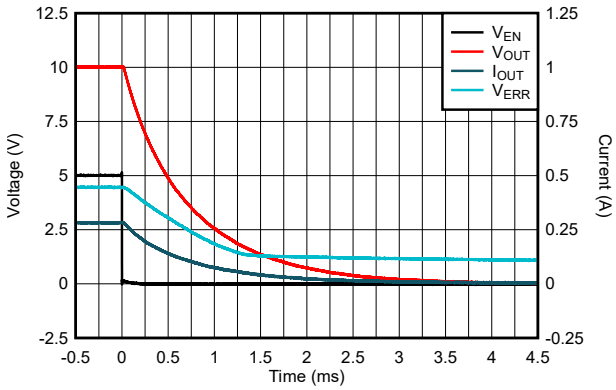
V_{IN} = 12V, I_{OUT} = 415mA, 3 x LDO channels

Figure 3-29. Shutdown Into a 415mA Load



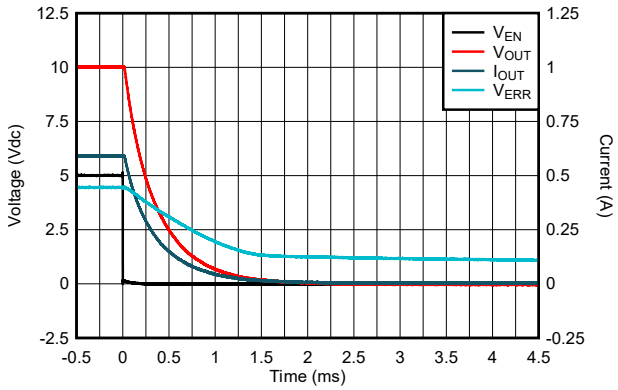
V_{IN} = 12V, I_{OUT} = 870mA, 3 x LDO channels

Figure 3-30. Shutdown Into a 870mA Load



V_{IN} = 12V, I_{OUT} = 275mA, V_{ERR} = V_{ERR1}, 2 x LDO channels

Figure 3-31. Shutdown Into a 275mA Load



V_{IN} = 12V, I_{OUT} = 580mA, V_{ERR} = V_{ERR1}, 2 x LDO channels

Figure 3-32. Shutdown Into a 580mA Load

3.3.6 Line Transient

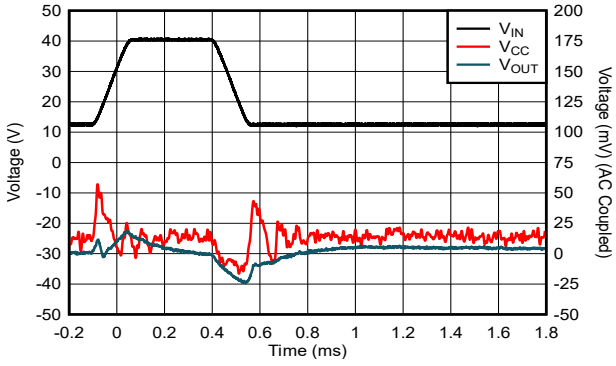


Figure 3-33. Op-Amp = LMV321A, 0.25V/µs, 2 x LDO Channels, 625mA Load

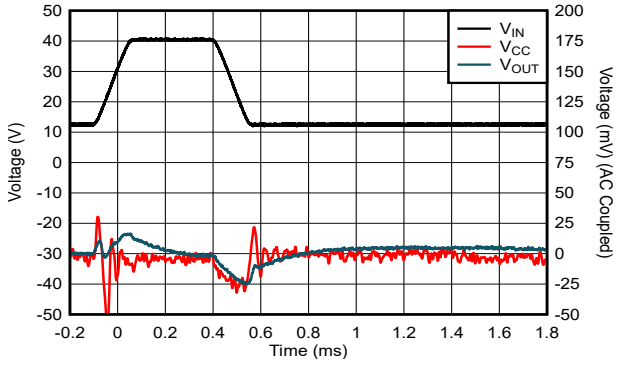


Figure 3-34. Op-Amp = OPA388, 0.25V/µs, 2 x LDO Channels, 625mA Load

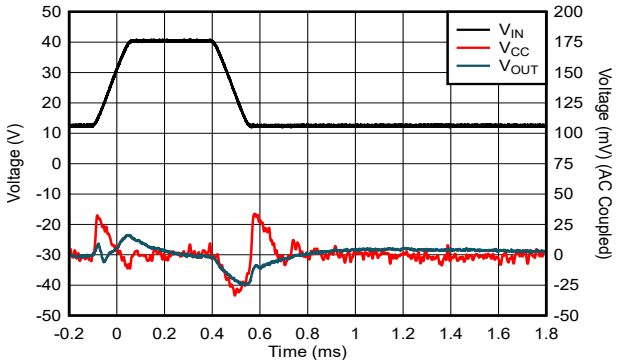


Figure 3-35. Op-Amp = LMV321A, 0.25V/µs, 3 x LDO Channels, 900mA Load

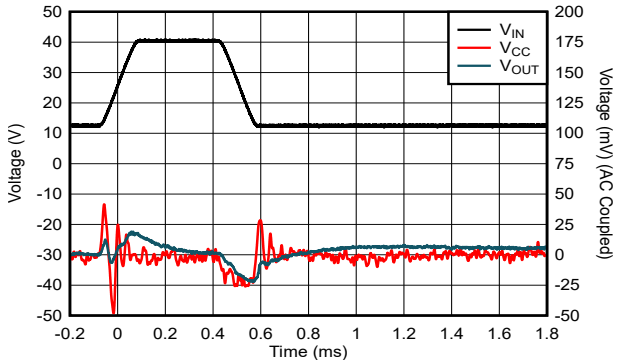


Figure 3-36. Op-Amp = OPA388, 0.25V/µs, 3 x LDO Channels, 900mA Load

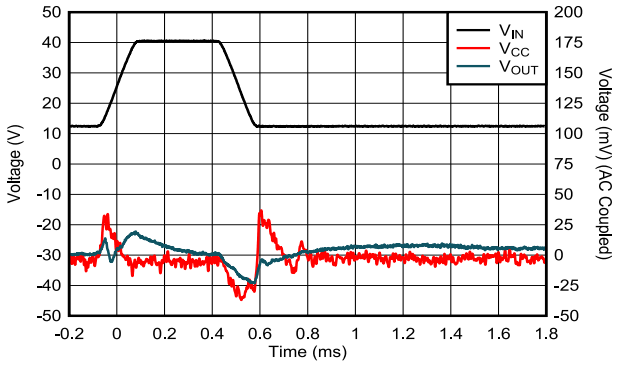


Figure 3-37. Op-Amp = LMV321A, 0.25V/µs, 4 x LDO Channels, 1.2A Load

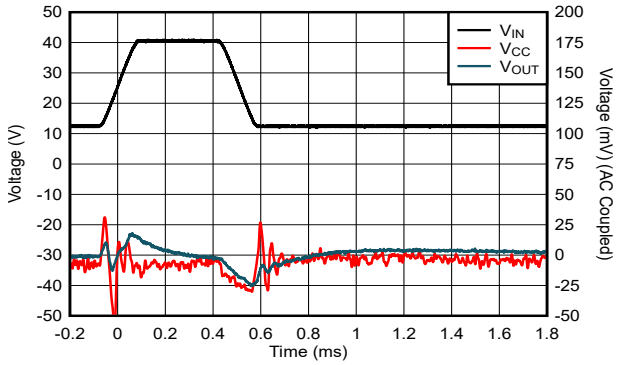
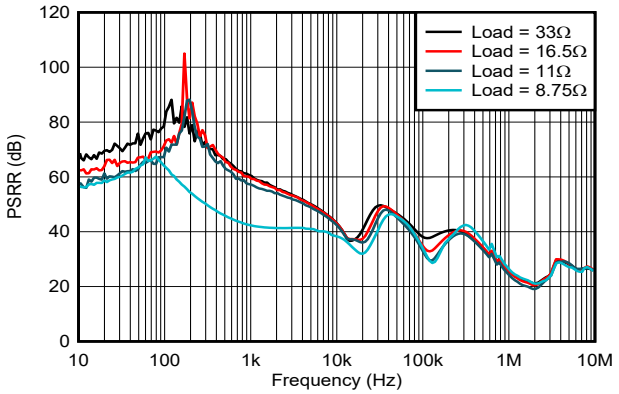


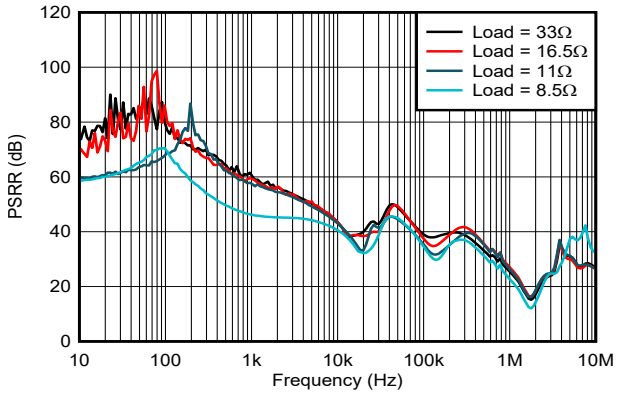
Figure 3-38. Op-Amp = OPA388, 0.25V/µs, 4 x LDO Channels, 1.2A Load

3.3.7 PSRR



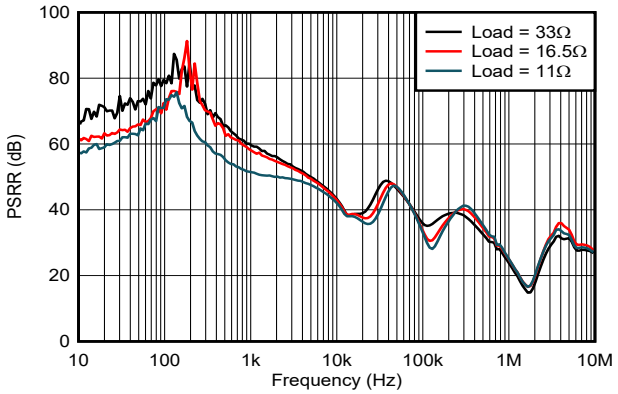
Op-Amp = LMV321A-Q1

Figure 3-39. 4 × LDO Channels: PSRR vs Frequency and I_{OUT}



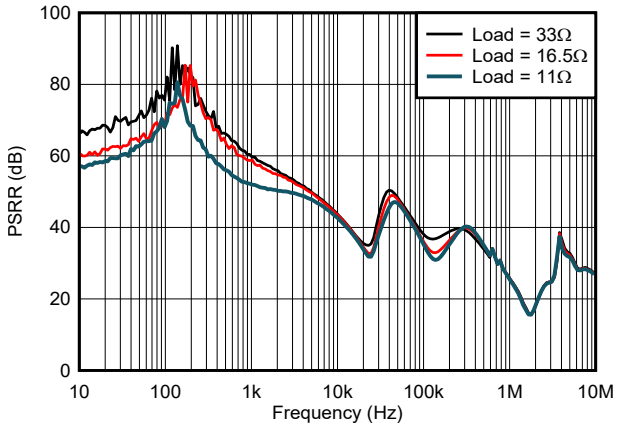
Op-Amp = OPA388-Q1

Figure 3-40. 4 × LDO Channels: PSRR vs Frequency and I_{OUT}



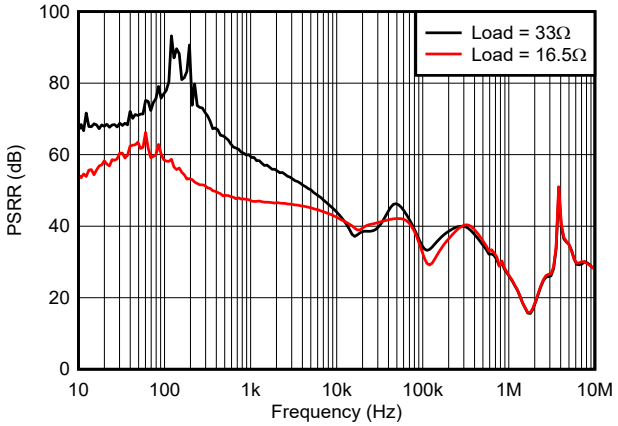
Op-Amp = LMV321A-Q1

Figure 3-41. 3 × LDO Channels: PSRR vs Frequency and I_{OUT}



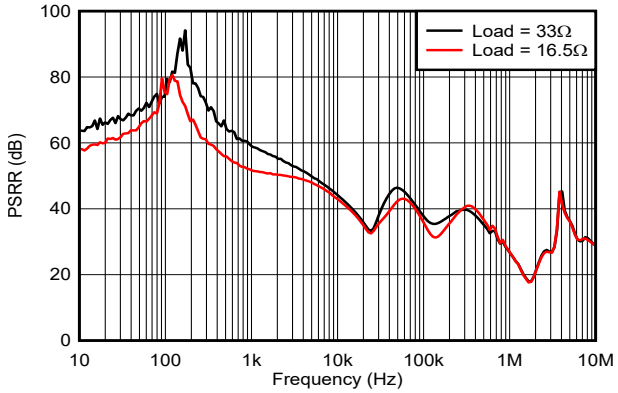
Op-Amp = OPA388-Q1

Figure 3-42. 3 × LDO Channels: PSRR vs Frequency and I_{OUT}



Op-Amp = LMV321A-Q1

Figure 3-43. 2 × LDO Channels: PSRR vs Frequency and I_{OUT}

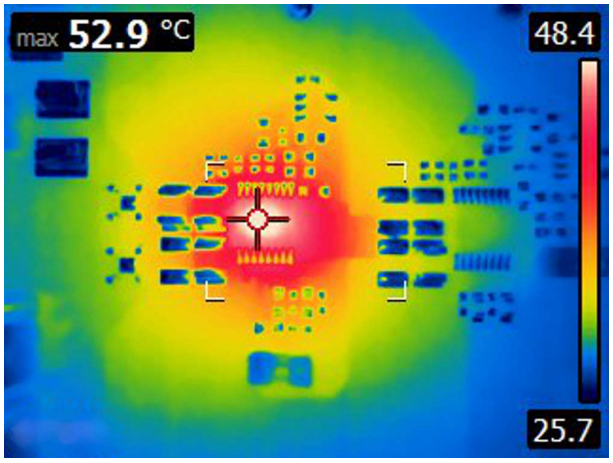


Op-Amp = OPA388-Q1

Figure 3-44. 2 × LDO Channels: PSRR vs Frequency and I_{OUT}

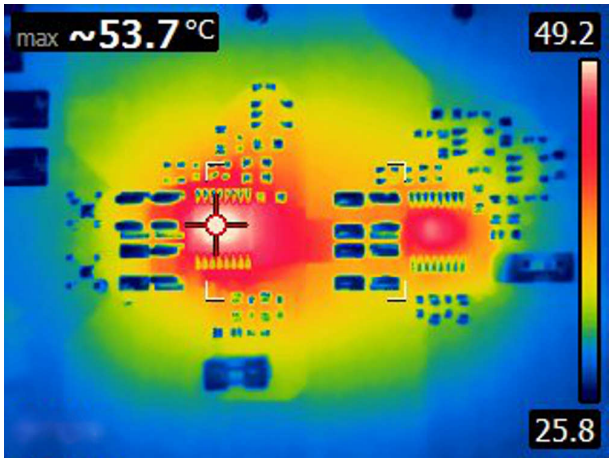
3.3.8 Thermal Performance

The load is applied for 30 minutes for each measurement. The measurements are captured with an ambient temperature of approximately 26°C.



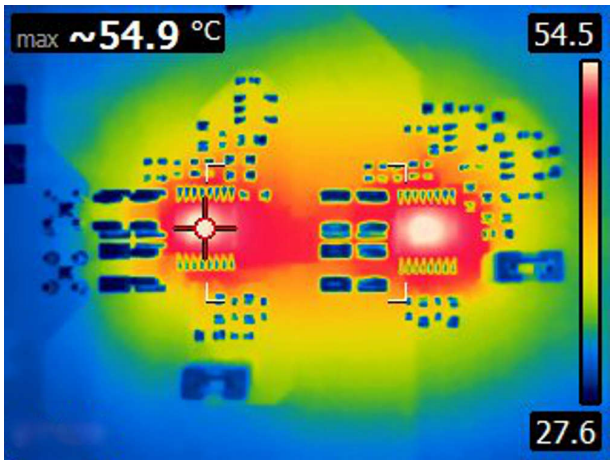
I_{LOAD} = 600mA, Op-Amp = OPA388-Q1

Figure 3-45. 2 x LDO Channels



I_{LOAD} = 900mA, Op-Amp = OPA388-Q1

Figure 3-46. 3 x LDO Channels

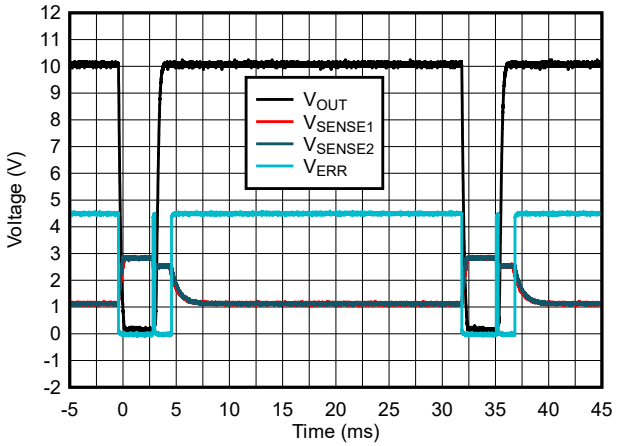


I_{LOAD} = 1.2A, Op-Amp = OPA388-Q1

Figure 3-47. 4 x LDO Channels

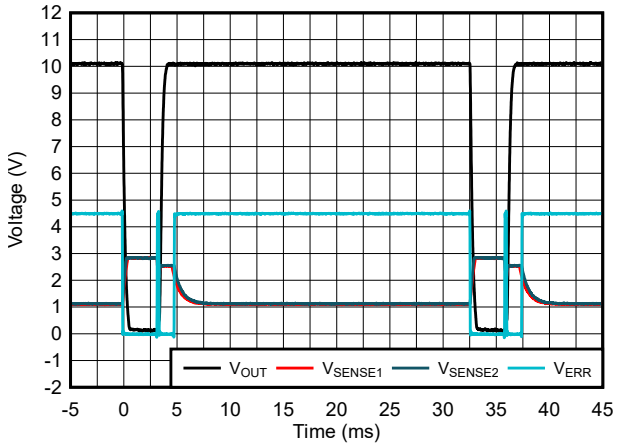
3.3.9 Thermal Limit Protection

The thermal protection performance of the parallel LDO channels exhibits a staircase effect on V_{LOAD} during turn off and turn on as each LDO enters and exits thermal shutdown. Thermal protection is repeatedly engaged until the power dissipation from the parallel LDO channels is removed. Figure 3-48 demonstrates the desired effect of the thermal protection circuitry in the presence of heavy power dissipation across the LDOs.



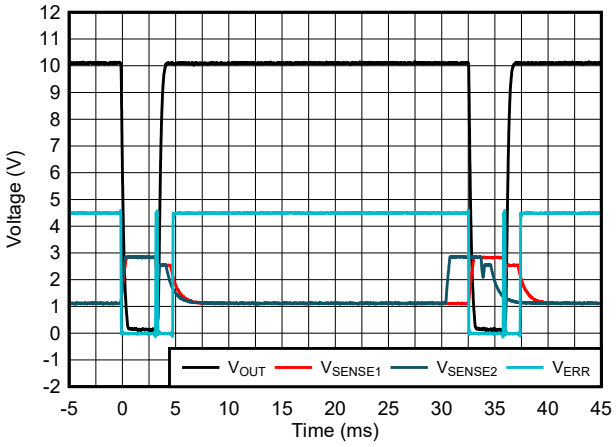
V_{ERR} = V_{ERR1}, V_{IN} = 21V, I_{OUT} = 1.2A

Figure 3-48. 2 × LDO Channels



V_{IN} = 21V, I_{OUT} = 900mA

Figure 3-49. 3 × LDO Channels



V_{IN} = 21V, I_{OUT} = 1.2A

Figure 3-50. 4 × LDO Channels

3.4 Test Results - Parallel LDOs Using Ballast Resistors

The test results in this section are taken under the following conditions:

V_{IN} = 12V, V_{OUT} = 10V, C_{INn} = 10µF, C_{OUTn} = 10µF, C_{FFn} = 22nF, R_B = 1.33Ω, C_{LOAD} = 10µF (unless otherwise noted).

3.4.1 Short to Battery

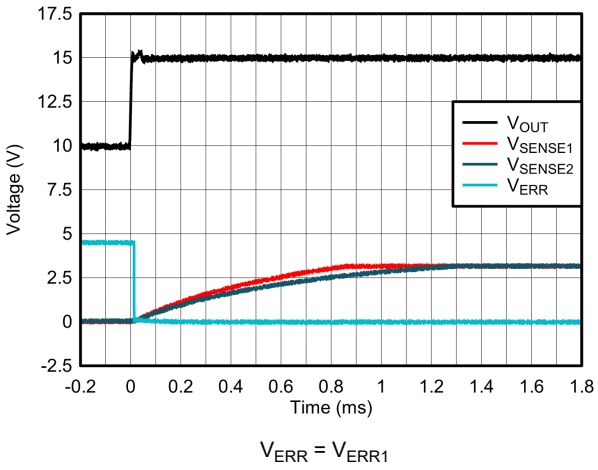
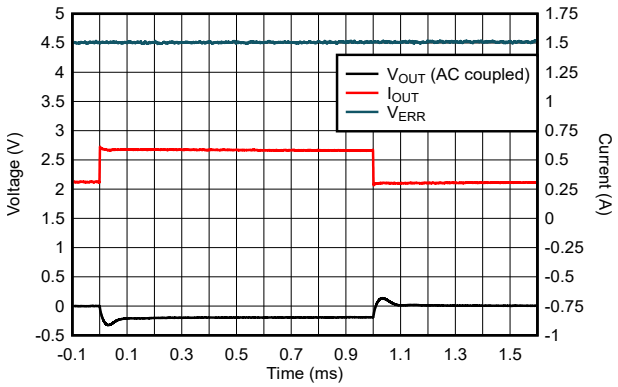


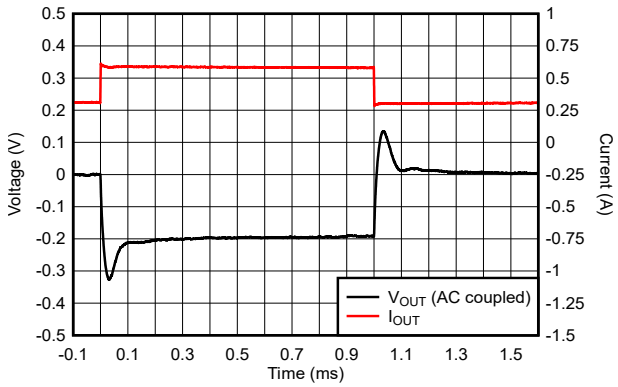
Figure 3-51. 2 × LDO Channels

3.4.2 Load Transient Response



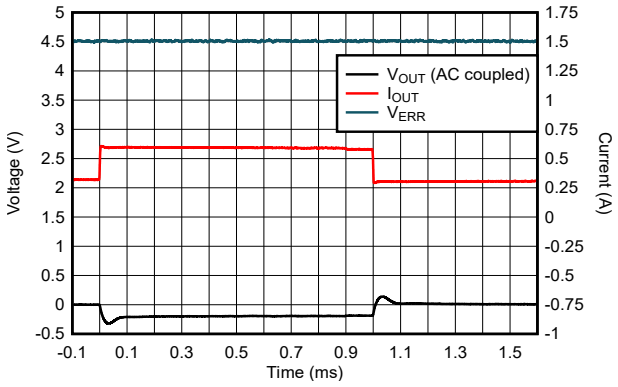
I_{OUT} = 300mA to 600mA to 300mA, SR = 1A/µs,
C_{FF} = Uninstalled

Figure 3-52. 2 × LDO Channels



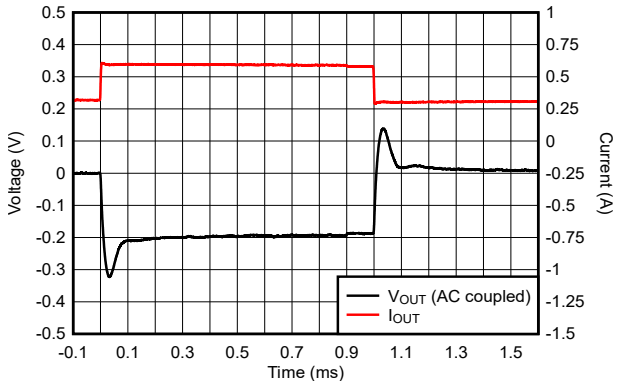
I_{OUT} = 300mA to 600mA to 300mA, SR = 1A/µs,
C_{FF} = Uninstalled

Figure 3-53. 2 × LDO Channels (Zoomed in)



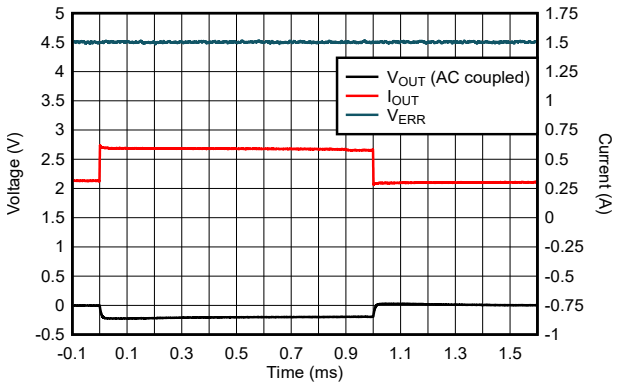
I_{OUT} = 300mA to 600mA to 300mA, SR = 0.1A/µs,
C_{FF} = Uninstalled

Figure 3-54. 2 × LDO Channels



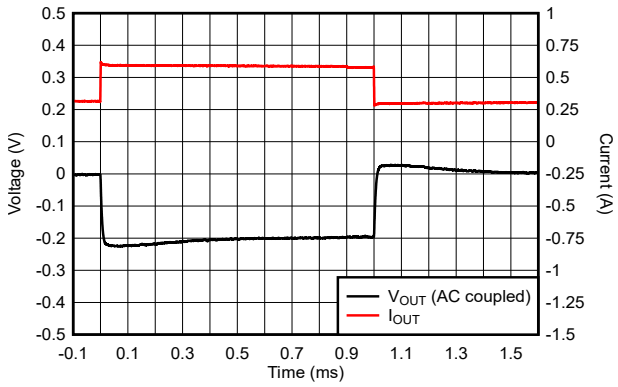
I_{OUT} = 300mA to 600mA to 300mA, SR = 0.1A/µs,
C_{FF} = Uninstalled

Figure 3-55. 2 × LDO Channels (Zoomed in)



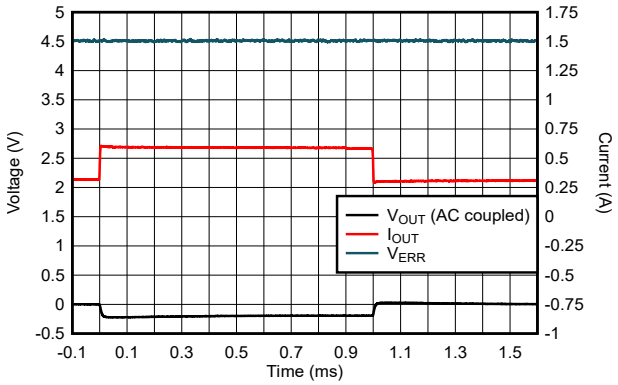
I_{OUT} = 300mA to 600mA to 300mA, SR = 1A/µs, C_{FF} = 22nF

Figure 3-56. 2 × LDO Channels



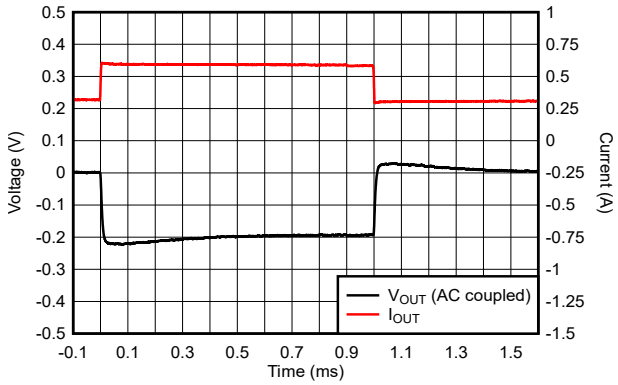
I_{OUT} = 300mA to 600mA to 300mA, SR = 1A/µs,
C_{FF} = 22nF

Figure 3-57. 2 × LDO Channels (Zoomed in)



I_{OUT} = 300mA to 600mA to 300mA, SR = 0.1A/µs, C_{FF} = 22nF

Figure 3-58. 2 × LDO Channels



I_{OUT} = 300mA to 600mA to 300mA, SR = 0.1A/µs, C_{FF} = 22nF

Figure 3-59. 2 × LDO Channels (Zoomed in)

3.4.3 Current Limit

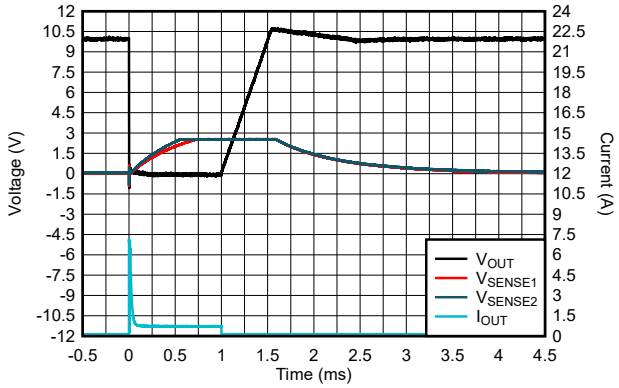
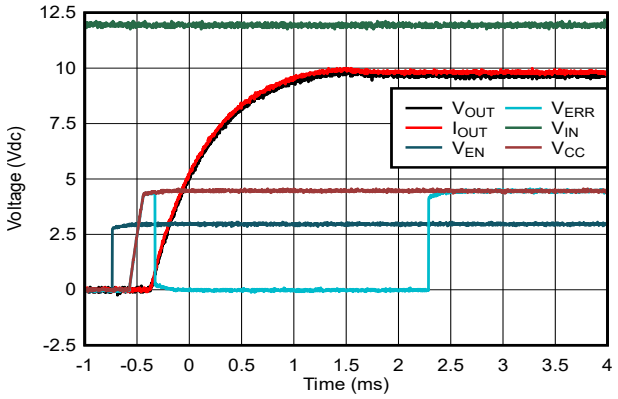


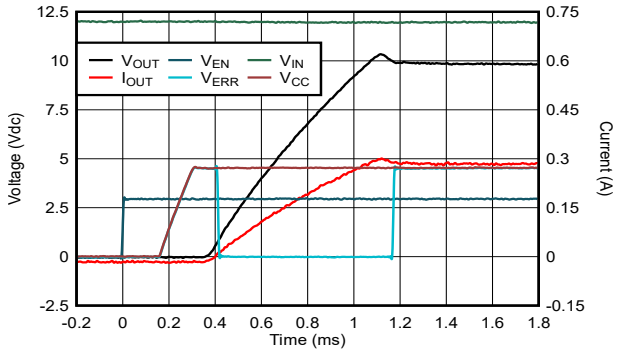
Figure 3-60. 2 × LDO Channels

3.4.4 Start-Up



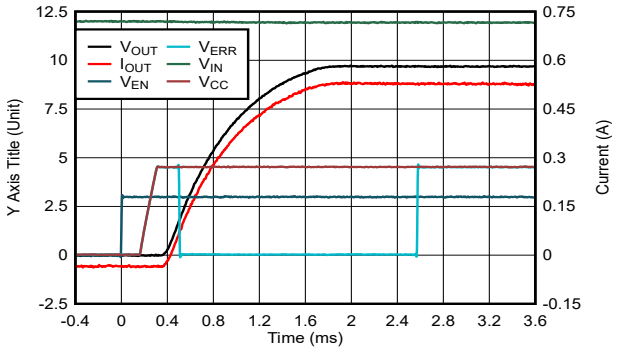
V_{IN} = 12V, I_{OUT} = 600mA, C_{FF} = uninstalled

Figure 3-61. Start-Up Into a 600mA Load



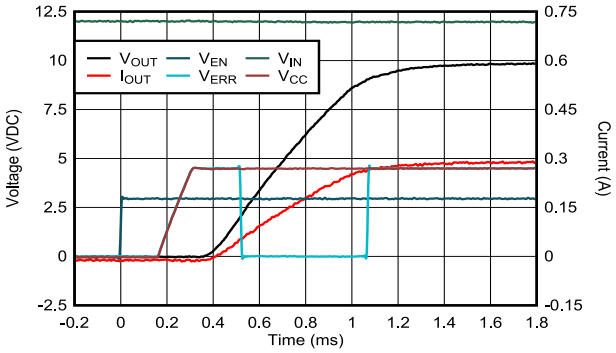
V_{IN} = 12V, I_{OUT} = 300mA, C_{FF} = uninstalled

Figure 3-62. Start-Up Into a 300mA Load



V_{IN} = 12V, I_{OUT} = 565mA, C_{FF} = 22nF

Figure 3-63. Start-Up Into a 565mA Load



V_{IN} = 12V, I_{OUT} = 300mA, C_{FF} = 22nF

Figure 3-64. Start-Up Into a 300mA Load

3.4.5 Line Transient

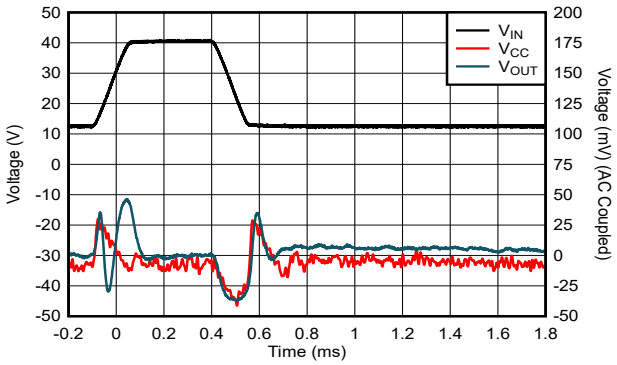
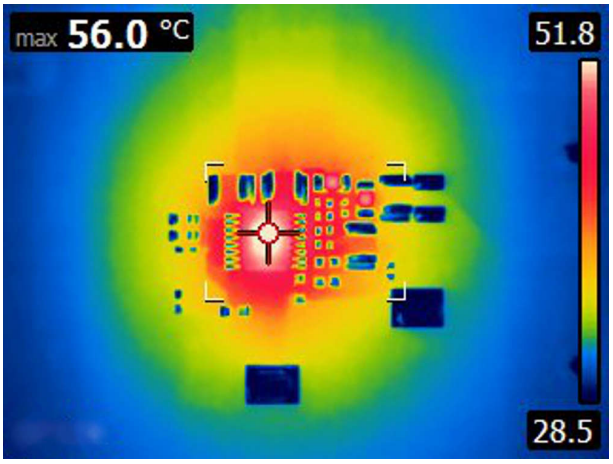


Figure 3-65. 0.25V/µs, 2 × LDO Channels, 598mA Load

3.4.6 Thermal Performance

The load is applied for 30 minutes for each measurement. The measurements are captured with an ambient temperature of approximately 26°C.

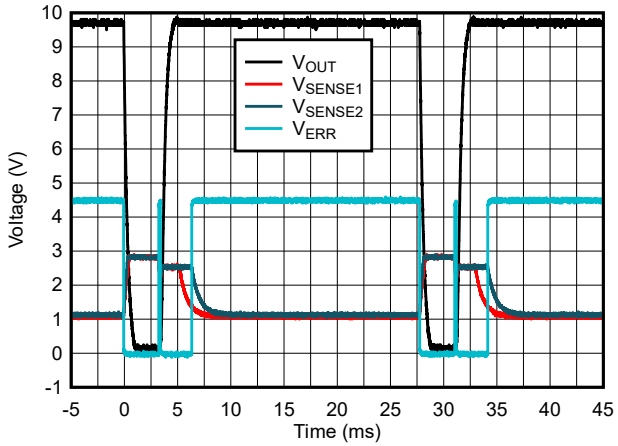


I_{LOAD} = 600mA

Figure 3-66. 2 × LDO Channels

3.4.7 Thermal Limit Protection

The thermal protection performance of the parallel LDO channels exhibits a staircase effect on V_{LOAD} during turn off and turn on as each LDO enters and exits thermal shutdown. Thermal protection is repeatedly engaged until the power dissipation from the parallel LDOs is removed. Figure 3-48 demonstrates the desired effect of the thermal protection circuitry in the presence of heavy power dissipation across the LDOs.



$V_{ERR} = V_{ERR1}$, V_{IN} = 21V, I_{OUT} = 600mA

Figure 3-67. 2 × LDO Channels (Ballast)

3.5 Comparison of Results Between Parallel LDO Techniques

The test results in this section are taken under the following conditions:

V_{IN} = 12V, V_{OUT} = 10V, C_{INn} = 10µF, C_{OUTn} = 10µF, C_{FFn} = 22nF, R_B = 1.33Ω, C_{LOAD} = 10µF, Op Amp = OPA388-Q1 (unless otherwise noted).

3.5.1 V_{LOAD} vs I_{LOAD}

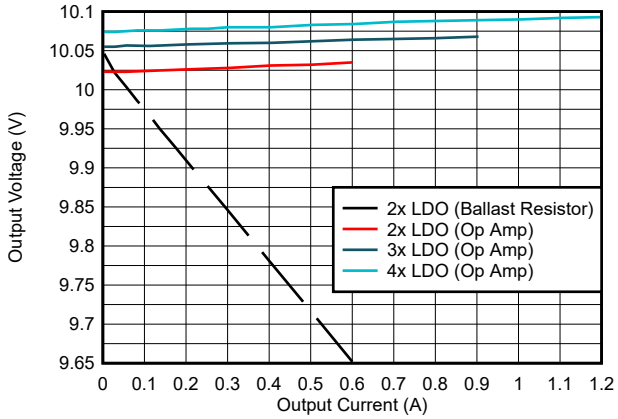


Figure 3-68. Load Voltage vs Total Load Current

3.5.2 PSRR

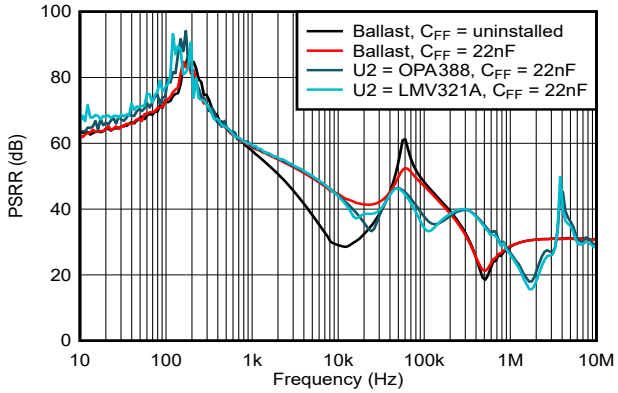


Figure 3-69. 2 × LDOs: PSRR vs Frequency

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-050096.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-050096.

4.1.3 Layout Prints

To download the layer plots, see the design files at TIDA-050096.

4.2 Tools

Parallel LDOs Using Ballast Resistors Calculator	Easily calculate the minimum number of parallel LDOs required to meet a set of system requirements (temperature, V_{IN}, V_{OUT}, I_{LOAD}, load regulation, and noise).

4.3 Documentation Support

1. IPC-2221B, Generic Standard on Printed Board Design
2. Texas Instruments, *TPS7B770x-Q1, Automotive, Single- and Dual-Channel Antenna LDO With Current Sense Data Sheet*
3. Texas Instruments, *LMV321A-Q1, LMV358A-Q1, LMV324A-Q1 Automotive Low-Voltage Rail-to-Rail Output Operational Amplifiers Data Sheet*
4. Texas Instruments, *Comprehensive Analysis and Universal Equations for Parallel LDOs Using Ballast Resistors Technical White Paper*
5. Texas Instruments, *Parallel Low-Dropout (LDO) Calculator*
6. Texas Instruments, *Parallel LDO Architecture Design Using Ballast Resistors Technical White Paper*
7. Texas Instruments, *Using New Thermal Metrics Application Note*
8. Texas Instruments, *Do-it-yourself: Three Ways to Stabilize Op Amp Capacitive Loads Technical Article*
9. Texas Instruments, *OPAx388 Precision, Zero-Drift, Zero-Crossover, True Rail-to-Rail, Input/Output Operational Amplifiers Data Sheet*

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

4.5 Trademarks

TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

5 About the Author

STEPHEN ZIEL is the Applications and Validation Manager for Low Voltage LDOs and became an elected Member, Group Technical Staff (MGTS) in 2023. Previous to working at TI, Stephen was a principal engineer at a large aerospace and defense company where he worked on all aspects of power electronics spanning 1mW to 1.5kW. Stephen holds over 18 years experience in power system requirements development and architecture design, power supply design, and engineering management leading large teams of power engineers. Stephen received a BSEE and MSEE from Michigan State University.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025