Technical Article

Tiny, but mighty: How small-size packaging and integration for MCUs help optimize space-constrained designs

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My first phone was a hot-pink flip phone. It could only make phone calls, but it was still an exciting piece of technology. Today, while the excitement is still there, I've come to expect a significantly larger feature set with each new phone: a higher-resolution screen, a longer battery life, faster processing speeds, and especially a smaller form factor.

And I'm not alone. Most consumers expect continuous advancements in size and functionality in their phones, headphones, smartwatches, even hair dryers. Without a cost, size or feature improvement, most consumers aren't likely to adopt the next generation of a product they already own.

The trend toward smaller, more capable electronics also affects embedded system designers, who are focused on increasing system functionality and performance while also reducing overall system size and cost.

To help embedded system designers, semiconductor manufacturers including TI are developing feature-rich microcontrollers (MCUs) and embedded processors with smaller footprints. These devices feature optimized packaging that requires less space on the printed circuit board (PCB), enabling more room for additional components and larger batteries for increased operational lifetimes. Inside the packaging, the design of these devices is also evolving, with the integration of numerous analog components to expand capabilities while reducing the need for discrete components.

In this article, I'll explore how packaging and analog component integration help reduce the size of embedded processors without compromising their capabilities, and the impact of optimized packaging on manufacturing processes.

Packaging

Packaging innovations are one of the few improvements in semiconductors that are visible to the human eye. To help reduce package size, semiconductor manufacturers are able to remove unnecessary plastic encasing and leads by shifting from traditional leaded options to advanced packaging options. The size of these packaging options directly relates to the size of the die and can reduce the area required to achieve the intended functionality.

TI offers several miniature packages in its embedded processing portfolio:

- Quad flat no-lead (QFN). Instead of traditional leads, a QFN package consists of flat contacts around the edges of the plastic encasing and an exposed thermal pad on the bottom for improved thermal performance. Figure 1 shows a package drawing of the MSPM0C1104, a 20-pin microcontroller that is only 9mm^2.

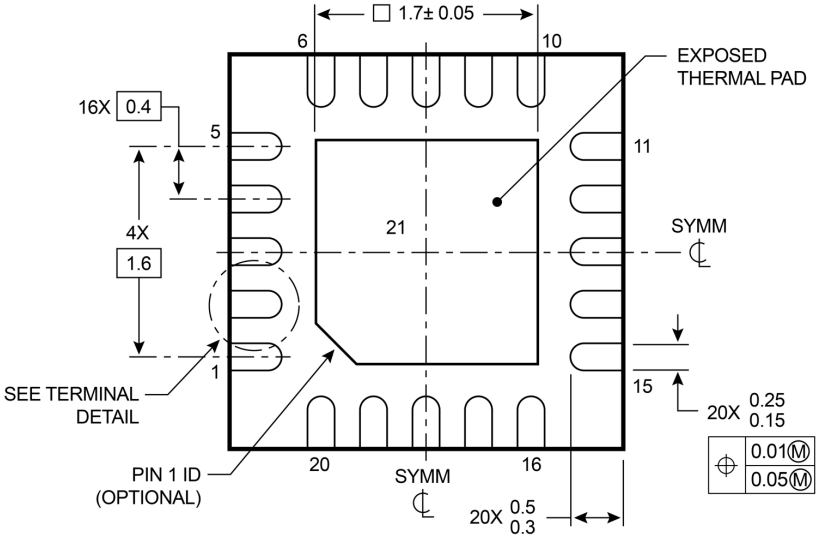

Figure 1. The MSPM0C1104 in a 20-pin 0.8mm QFN package drawing

- A wafer chip-scale package (WCSP). These packages offer the smallest form factor compared to other package types. An array of solder balls connects directly to the silicon, resulting in a package size equal to the silicon die (see Figure 2). Fitting eight solder balls in 1.38mm^2 enables the integration of more features per square millimeter. The MSPM0C1104 is also available in a WCSP that's 38% smaller than competing devices, making it the world's smallest MCU.

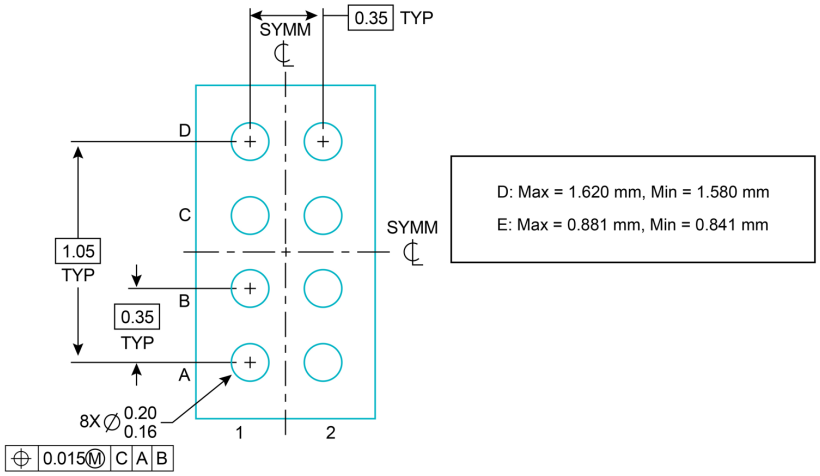

Figure 2. MSPM0C1104 eight-ball WCSP package drawing (nominally 1.50 x 0.86mm with a thickness of 0.35mm)

Integration

Another way to address limited board space is to optimize feature integration in the device. Components that each have their own plastic packaging, leads and required layout space can occupy significantly more board space than a single chip with integrated features.

In the push for miniaturization, MCUs and processors with integrated analog and digital peripherals can prove useful. Take a pulse oximeter, for example. In comparison to a discrete design approach, as shown in Figure 3, integrating the analog-to-digital converter (ADC), comparator and voltage reference into the MCU can reduce the number of required components and thus PCB size, as shown in Figure 4.

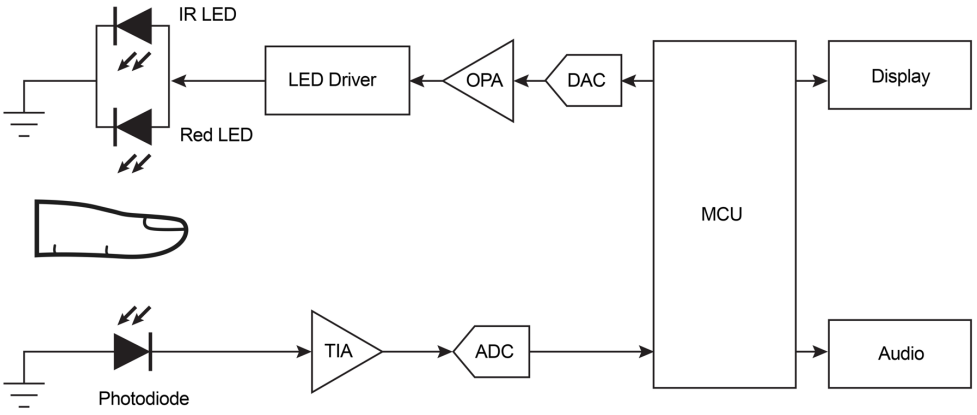

Figure 3. Pulse oximeter design with discrete analog components

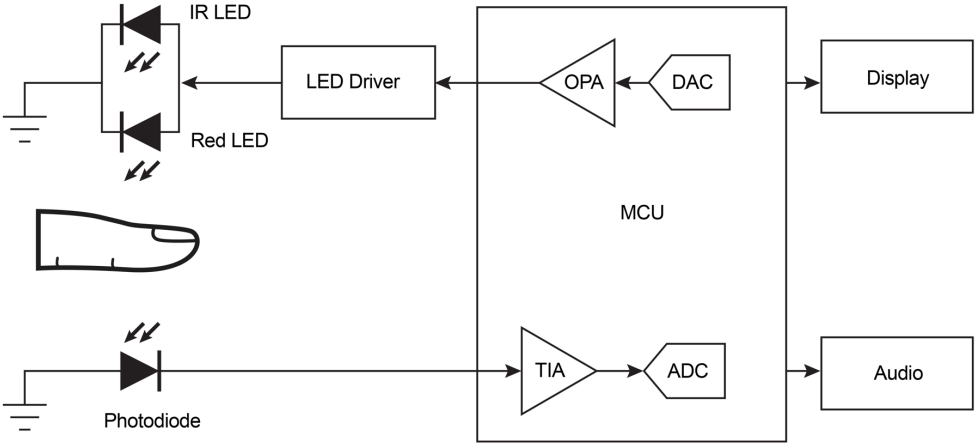

Figure 4. Pulse oximeter design with integrated components

Selecting which features to integrate in an MCU entails making some trade-offs. Feature integration can decrease the number of components in a design, but including unnecessary features can reverse the intent and increase the size of the single-chip solution.

That's why feature optimization is so crucial. Added peripherals are directly related to the size of the die and cost of the device. Unutilized features can be a waste of both space and money and reduce the efficiency of a space-constrained design. Understanding the true needs of the market can result in cost- and size-competitive embedded solutions. For example, the MSPM0C1104 8-ball WCSP is not only small, but features numerous integrated features and components. In a 1.38 mm^2 package it provides 16KB of flash memory, a 12-bit ADC with three channels, and three timers. Engineers have room to do more with their designs by using devices like the MSPM0C1104 to optimize the number of features per square millimeter.

Figure 5 shows a size comparison of a single MSPM0C1104 in a WCSP next to a wireless earbud.

Figure 5. Size comparison between an MSPM0C1104 and a wireless earbud

As the physical integrated circuit gets smaller, design and production methods have also evolved. While moving toward smaller electrical components can help minimize PCB size, there are also layout, handling and production flow considerations.

Two types of PCB land patterns are useful when designing with chip-scale packages: solder mask defined (SMD) and non-solder mask defined (NSMD), as shown in Figure 6. SMD types contain a larger copper pad that overlaps with the substrate, while NSMD types contain a smaller copper pad with tighter dimensions. NSMD-type pads offer improved uniform coverage, improved routing and reduced stress in chip-scale packages.

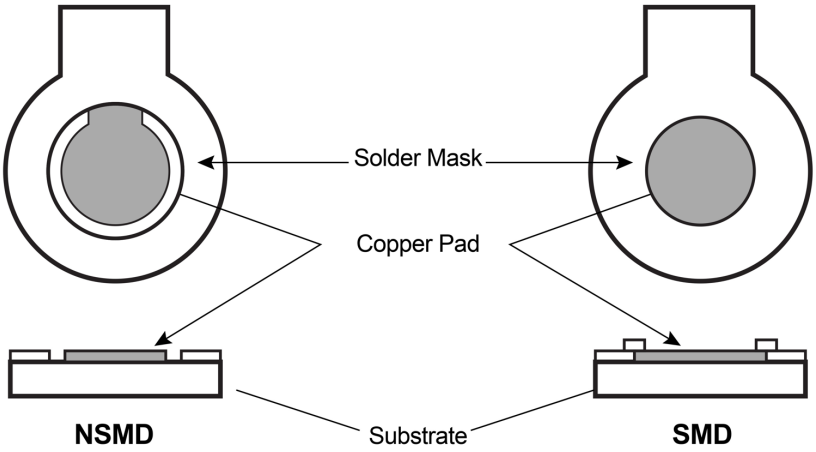

Figure 6. NSMD and SMD PCB land patterns

Component placement and handling can also prove difficult. For semiconductor and product manufacturers, pick-and-place machines and vacuum pens used in manufacturing minimize the risk of damaging the exposed die of WCSP and BGA packages. For improved placement accuracy, the vision system in a pick-and-place machine can locate the package outline or individual bumps. The solder-bump geometry enables self-centering and correction on the PCB pad. As electrical components have decreased in size, manufacturing machinery has evolved to compensate.

Conclusion

Innovation comes in cycles. Consumers are consistently anticipating lightweight, feature-dense products. Engineers are designing to balance conflicting interests. And the semiconductor industry is evolving to optimize package and feature options. Once the current generation of products hits the shelves, teams are already meeting to brainstorm the next best thing, and the cycle repeats.

TI’s semiconductor miniaturization efforts include selective feature integration, package optimization and manufacturing advancements, providing more options and possibilities for engineers designing products in a shrinking world.

Additional resources

- Learn more about TI’s Arm Cortex-M0+ MSPM0 MCU portfolio.
- Read the application brief, "TI's Smallest M0+ MCU Package Enables Room to do More in Your Design".

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