



Description

This technical user's guide describes the hardware architecture of the AM62x-Low Power SK EVM, a low cost starter kit built around the AM62x System-on-Chip (SoC). The AM62x processor comprises of a quad-core 64-bit Arm®-Cortex® A53 microprocessor, single-core Arm Cortex-R5F MCU and an Arm Cortex-M4F MCU.

The SK EVM allows the user to experience a great dual display feature through HDMI (over DPI) and LVDS, up to 2K resolution, as well as industrial communication solutions using serial, Ethernet, USB and other interfaces. Its powerful Arm performance, up to quad-core Cortex-A53 at 1.4GHz, with rich interfaces, offers good control and communication capabilities for a wide ranges of automotive applications such as automotive HMI and driver monitoring system, as well as industrial applications such as PLC, automation control, monitor/supervisor system. In addition, the SK EVM can communicate with other processors or systems, and act as a communication gateway. In addition, the SK EVM can directly operate as a standard remote I/O system or simple sensor connected to

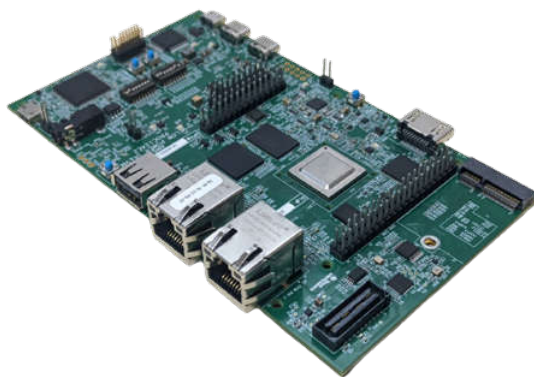
an industrial communication network. The embedded emulation logic allows for emulation and debugging using standard development tools such as Code Composer Studio™ from TI.

Note

This evaluation board is a pre-production release and has several known issues that should not be copied into a production system

Features

- 2x Gigabit Ethernet RJ45 connectors
- 2GB LPDDR4 memory
- 1Gb OSPI Flash memory
- 16GB eMMC Flash memory
- MicroSD card slot
- 1x USB 2.0 Type-C®
- 1x USB 2.0 Type-A
- 1x 3.5mm TRRS audio jack
- M.2 connector for Wi-Fi/BT module
- HDMI® connector for external display
- 3x GPIO expansion connector
- CSI Camera Header
- 1x LVDS Display connector



This design incorporates HDMI® technology.

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1 Evaluation Module Overview

1.1 Introduction

This technical user's guide describes the hardware architecture of the SK-AM62-LP EVM, a low-power starter kit evaluation module designed to accelerate development with the AM62x system-on-chip from Texas Instruments (TI™). This versatile platform features a powerful quad-core ARM® Cortex®-A53 processor and two integrated microcontrollers capable of running Embedded Linux and RTOS operating systems, making it ideal for a wide range of industrial automation and monitoring applications. Users can explore rich interface options, including dual-display capabilities (HDMI and LVDS) and robust industrial communication solutions using Ethernet, USB, and serial interfaces. The embedded emulation logic allows for emulation and debugging using standard development tools such as Code Composer Studio™ IDE from Texas Instruments (TI).

1.2 Kit Contents

- EVM
- Quick Start Guide

Note

The maximum length of the IO cables shall not exceed 3 meters.

1.3 Device Information

The SK-AM62-LP EVM is centered around the AM62x System-on-Chip (SoC) featuring a quad-core ARM Cortex-A53 processor and integrated microcontrollers. Key components include 2GB of LPDDR4 RAM, 512 Mbit OSPI flash, a TPS65219 Power Management IC (PMIC), and a SiI9022A HDMI transmitter. The board integrates an onboard XDS110 JTAG emulator. Furthermore, the SK-AM62-LP supports Linux® and Android development with a feature-rich software development kit (SDK). On-chip emulation logic allows for emulation and debugging using standard development tools such as the Code Composer Studio integrated development environment (IDE) (CCSTUDIO) as well as an intuitive out-of-box user's guide to quickly start design evaluation

1.4 EVM Revisions and Assembly Variants

The various SK-AM62-LP EVM PCB design revisions, and assembly variants are listed in [Table 1-1](#). The specific PCB revision is indicated in silkscreen on the PCB and the specific assembly variant is indicated with an additional sticker label

Table 1-1. SK EVM PCB design revisions and assembly variants

OPN	PCB Revision	Assembly Variant	Revision and Assembly Variant Description
SK-AM62-LP	PROC124E1	N/A	First prototype, early release revision of the AM62X Low-Power SK EVM. Implements the Sitara AM62X MPU with a PMIC power solution.
SK-AM62-LP	PROC124E2	N/A	Second prototype, early release revision of the AM62X Low-Power SK EVM. Implements a number of changes and bug fixes.
SK-AM62-LP	PROC124E2	PROC124E2A	Few components updated in assembly

1.5 Specification

The functional block diagram of the AM62x-Low Power SK EVM is shown in [Figure 1-1](#).



2 Hardware

2.1 Additional Images

This section shows the EVM pictures and location of various blocks on the board.

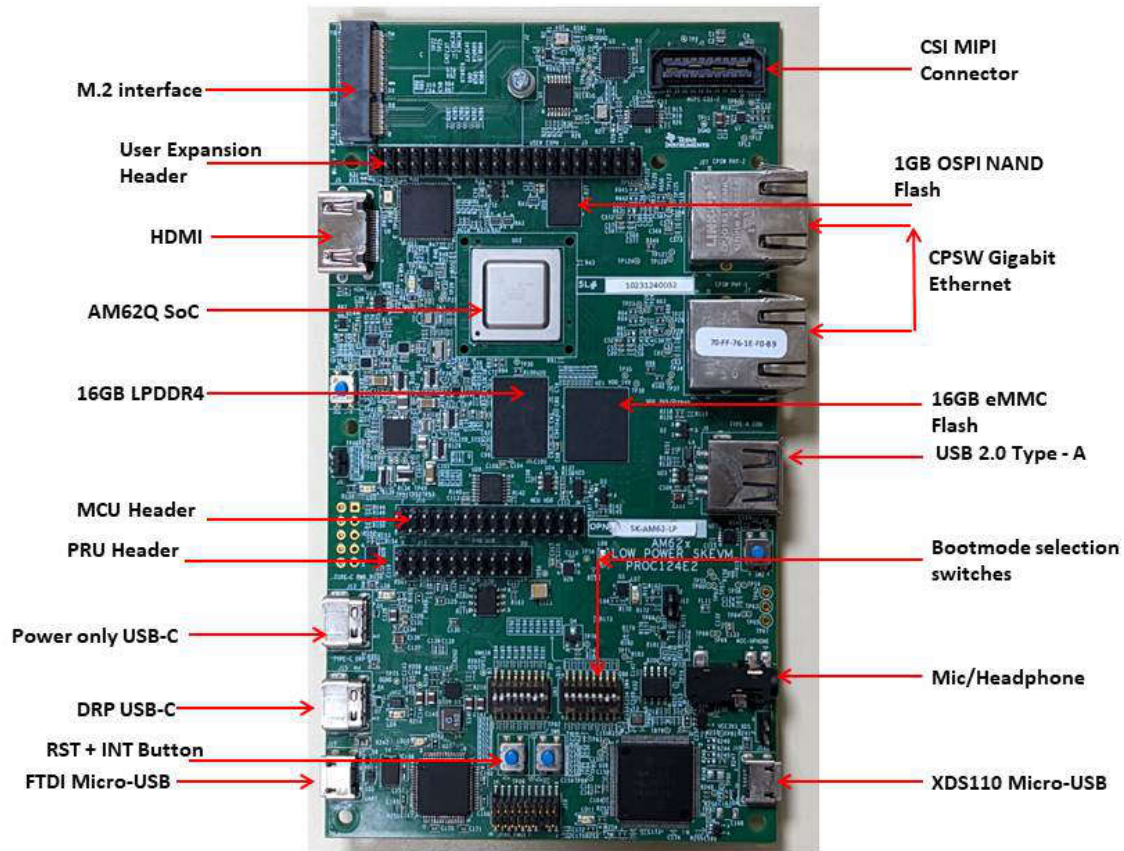


Figure 2-1. SK EVM Top

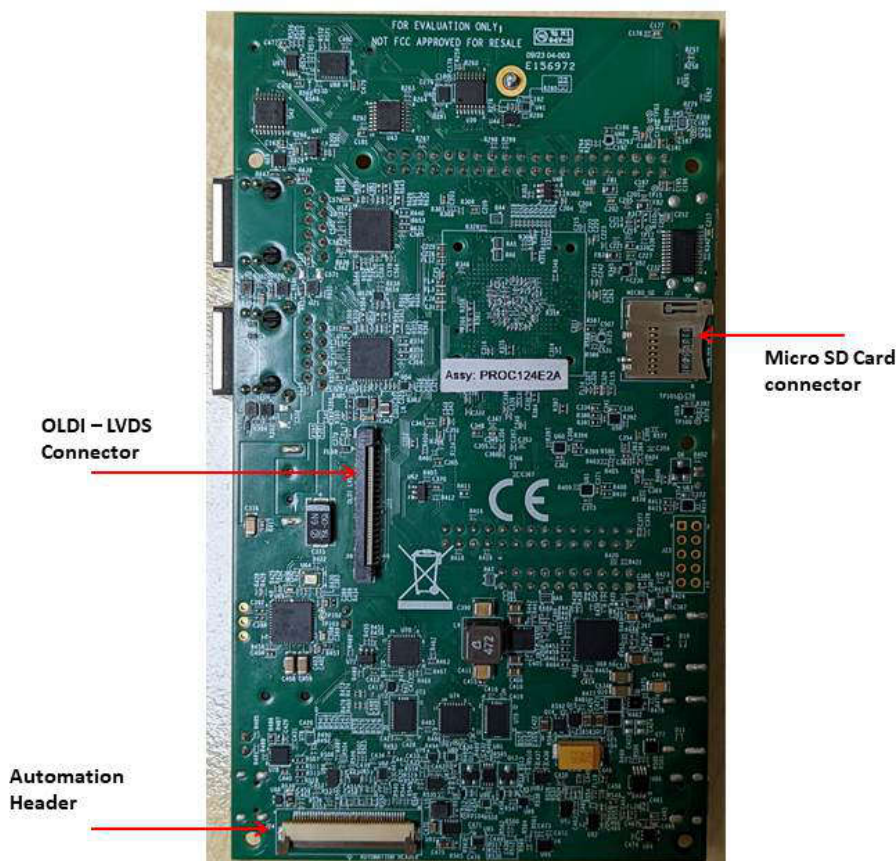


Figure 2-2. SK EVM Bottom

2.2 Key Features

The AM62x-Low Power SK EVM is a high performance, standalone development platform that enables users to evaluate and develop industrial applications for the Texas Instrument's AM62x System-on-Chip (SoC).

The following sections discuss the SK EVM's key features.

2.2.1 Processor

- AM62x SoC, 17.2mm x 17.2mm, 0.8mm pitch, 441-pin FCBGA.

2.2.2 Memory

- 2GB LPDDR4 supporting data rate up to 1600MT/s.
- Micro SD Card slot with UHS-1 support
- 1Gbit Octal SPI Flash memory
- 512 Kbit Inter-Integrated Circuit (I2C) board ID EEPROM
- 16GB eMMC Flash

2.2.3 JTAG Emulator

- XDS110 On-Board Emulator
- Supports 20-pin JTAG connection from external emulator

2.2.4 Supported Interfaces and Peripherals

- 1x USB2.0 Type C Interface supporting DFP and UFP modes (Data) and DRP mode (Power)
- 1x USB2.0 Host Interface - Type A

- 1x HDMI Interface
- Audio Line in and Mic + Headphone out
- M.2 Key E interface support for both Wi-Fi and Bluetooth modules
- 2x Gigabit Ethernet ports supporting 10/100/1000Mbps data rate on two connectors (RJ45, Un-populated Automotive).
- Quad port UART to USB circuit over microB USB connector
- INA devices for current monitoring
- 2x Temperature Sensors near SoC and LPDDR4 for thermal monitoring

2.2.5 Expansion Connectors Headers to Support Application Specific Add On Boards

- CSI Camera Header
- 1x LVDS Display connector
- User Expansion connector
- PRU Header
- MCU Header
- Test Automation Header

2.3 Power

2.3.1 Power Requirements

AM62x-Low Power SK EVM can be powered through either of the two USB Type C Connectors –

- Connector 1(J13) - Power role – SINK, No Data role
- Connector 2(J15) - Power role – DRP, Data role – USB2.0 DFP or UFP

The AM62x-Low Power SK EVM supports voltage input ranges of 5V - 15V and 3A of current. A USB PD controller Mfr. Part#TPS65988DHRSHR is used for PD negotiation upon cable detection to get necessary power required for the board. Connector 1 is configured to be an UFP Port and has no Data role. Connector 2 is configured as a DRP port, it can act as DFP only when the board is being powered by Connector 1. When both the connectors are connected to external power supply, the port with highest PD power contract will be selected to power the board.

Table 2-1. Type-C port Power roles

J13(UFP)	J15(DRP)	BoardPower	Remarks
Plugged in	NC	ON - J13	J13 will be UFP and will only sink power & J15 can act as DFP if a peripheral is connected
NC	Plugged in	ON - J15	J15 will be UFP and can only sink power
Plugged in	Plugged in	ON- J13 or J15	Board will be powered by the port with highest PD power contract

The PD IC uses a SPI EEPROM to load the necessary configuration on power up so it can negotiate a power contract with a compatible power source.

The configuration file is loaded to the EEPROM using header J23. Once the EEPROM is programmed the PD obtains the configuration files via SPI communication. Upon loading the configuration files the PD negotiates with the source to obtain the necessary power requirement.

Power indication LEDs are provided for both the Type-C connectors for the user to identify which connector is powering the SKEVM Board. An external power supply (Type-C output) can be used to power the EVM but is not included as part of the SKEVM kit.

Table 2-2. Recommended External Power Supplies

DigiKeyPart#	Manufacturer	Manufacturer Part #
1939-1794-ND	GlobTek, Inc.	TR9CZ3000USBCG2R6BF2(*)
Q1251-ND	Qualtek	QADC-65-20-08CB

Note

Minimum Voltage: 5VDC, Recommended Minimum Current: 3000mA, Maximum Voltage: 15VDC, Maximum current: 5000mA. Because SK-AM62-LP implements USB PD for power, the device is able to negotiate to the highest Voltage/Current combination supported by both the Device and Power Adapter, as such, if the power supply exceeds the maximum voltage and current requirements listed above is acceptable as long as the power adapter is compliant with the USB-C PD specification.

(*) This is the adapter part number used for compliance testing.

Note

TI recommends using an external power supply or power accessory which complies with applicable regional safety standards such as (by example) UL, CSA, VDE, CCC, PSE, etc.

2.3.2 Power Input

Both Type-C Connectors (VBUS and CC lines) are connected to a Dual PD controller Mfr Part# TPS65988. The TPS65988 is a stand-alone USB Type-C and Power Delivery (PD) controller providing cable plug and orientation detection for two USB Type-C Connectors. Upon cable detection, the TPS65988 communicates on the CC wire using the USB PD protocol. When cable detection and USB PD negotiation are complete, the TPS65988 enables the appropriate power path. The two internal power paths of TPS65988 are configured as sink paths for the two Type-C ports and an external FET path is provided for Type-C CONN 2 to source 5V when acting as DFP. The external FET path is controlled by GPIO17/PP_EXT2 of the PD controller. TPS65988 PD controller can provide an output of 3A (15V max) through CC negotiation. The VBUS pins from both the Type C connectors are connected to the VBUS pins of the PD controller. The output of the PD is VMAIN which is given to on board Buck-Boost and Buck regulators to generate fixed 5V and 3.3V supply for the SKEVM board.

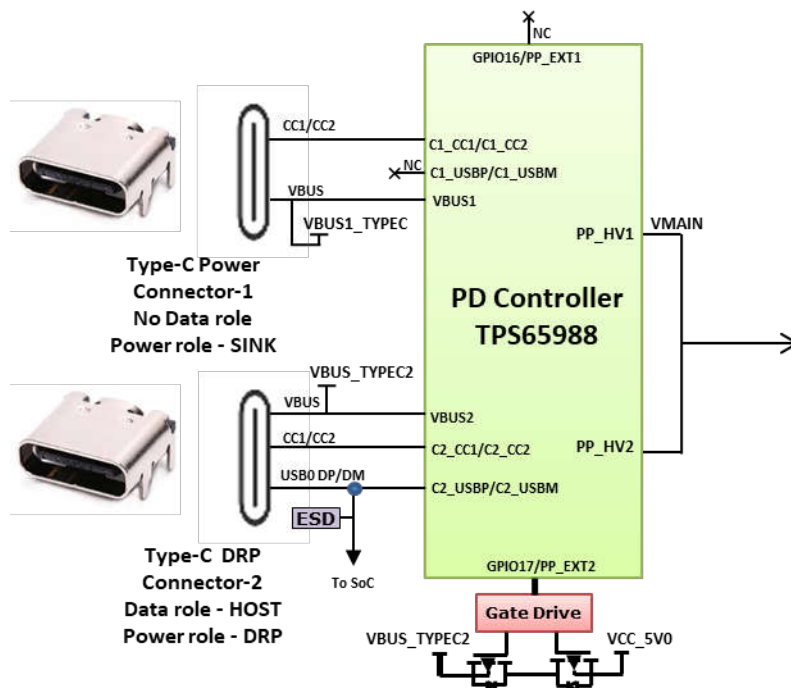


Figure 2-3. Power Input Block Diagram

2.3.3 Power Supply

AM62x-Low Power SK EVM utilizes an array of DC-DC converters to supply the various memories, clocks, SoC and other components on the board with the necessary voltage and the power required.

Figure 2-4 shows the various discrete regulators and LDOs used to generate power rails and the current consumption of each peripheral on AM62x-Low Power SK EVM board.



The AM62x-Low Power SK EVM board includes a power solution based on a PMIC as well as discrete power supply components. The initial stage of the power supply will be VBUS voltage from either of the two USB Type C connectors J13 and J15. USB Type-C Dual PD controller of Mfr. Part# TPS65988DHRSHR is used for negotiation of the required power to the system.

- TPS62824DMQR - To generate VDD_2V5 rail for PHY and DDR peripherals
- TLV75510PDQNR - To generate VDD_1V0 for Ethernet PHYs
- TPS65219 - To generate various SoC and peripheral supply's
- TPS62177DQCR - Powering the always-on circuits of Test Automation Section
- TLV75518LDO - e-Fuse programming of SoC
- TPS79601LDO - XDS110 On board emulator
- TPS73533LDO - FT4232 UART to USB Bridge
- TLV705075YFPT- To generate VDD_CANUART rail

Additionally, GPIO from the test automation header is also connected to the TPS630702RNMR Enable pin to control ON/OFF of the SKEVM via the test automation board. It only disables the VCC_5V0 output of TPS630702RNMR from which all other power supplies are derived. SoC has different IO groups.

2.3.4 Power ON OFF Procedures

Power to the EVM is provided through an external power supply providing PD voltage and current to the either of the two USB Type-C Ports.

2.3.4.1 Power-On Procedure

1. Place the SK EVM boot switch selectors (SW3, SW4) into selected boot mode. Example boot-modes for SD card is shown below.
2. Connect your boot media (if applicable).
3. Attach the PD capable USB Type-C cable to the SKEVM Type-C (J13 or J15) Connector.
4. Connect the other end of the Type-C cable to the source, either AC Power Adapter, or Type C source device (such as a Laptop computer).
5. Visually inspect that either LD8 or LD9 LED should be illuminated.
6. XDS110 JTAG and UART debug console output are routed to micro-USB ports J18 and J17, respectively.

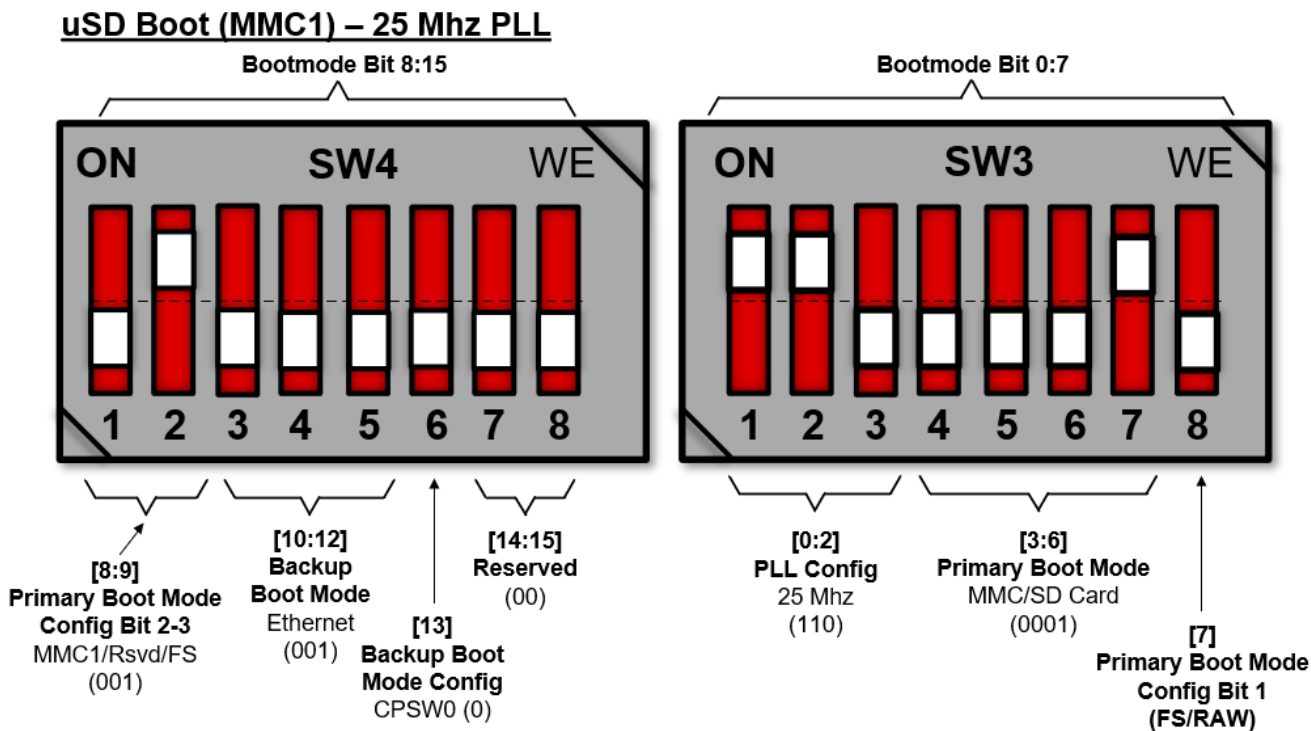


Figure 2-5. Example SD Boot Mode

2.3.4.2 Power-Off Procedure

1. Disconnect AC power from AC/DC converter.
2. Remove the USB Type-C cable from the SK EVM.

2.3.4.3 Power Test Points

Test points for each power output on the board are mentioned in [Table 2-3](#).

Table 2-3. Power Test Points

SI #	Power Supply	Test Point	Voltage
1	VBUS_TYPEC1	R165.1	5V-15V
2	VBUS_TYPEC2	R214.1	5V-15V

Table 2-3. Power Test Points (continued)

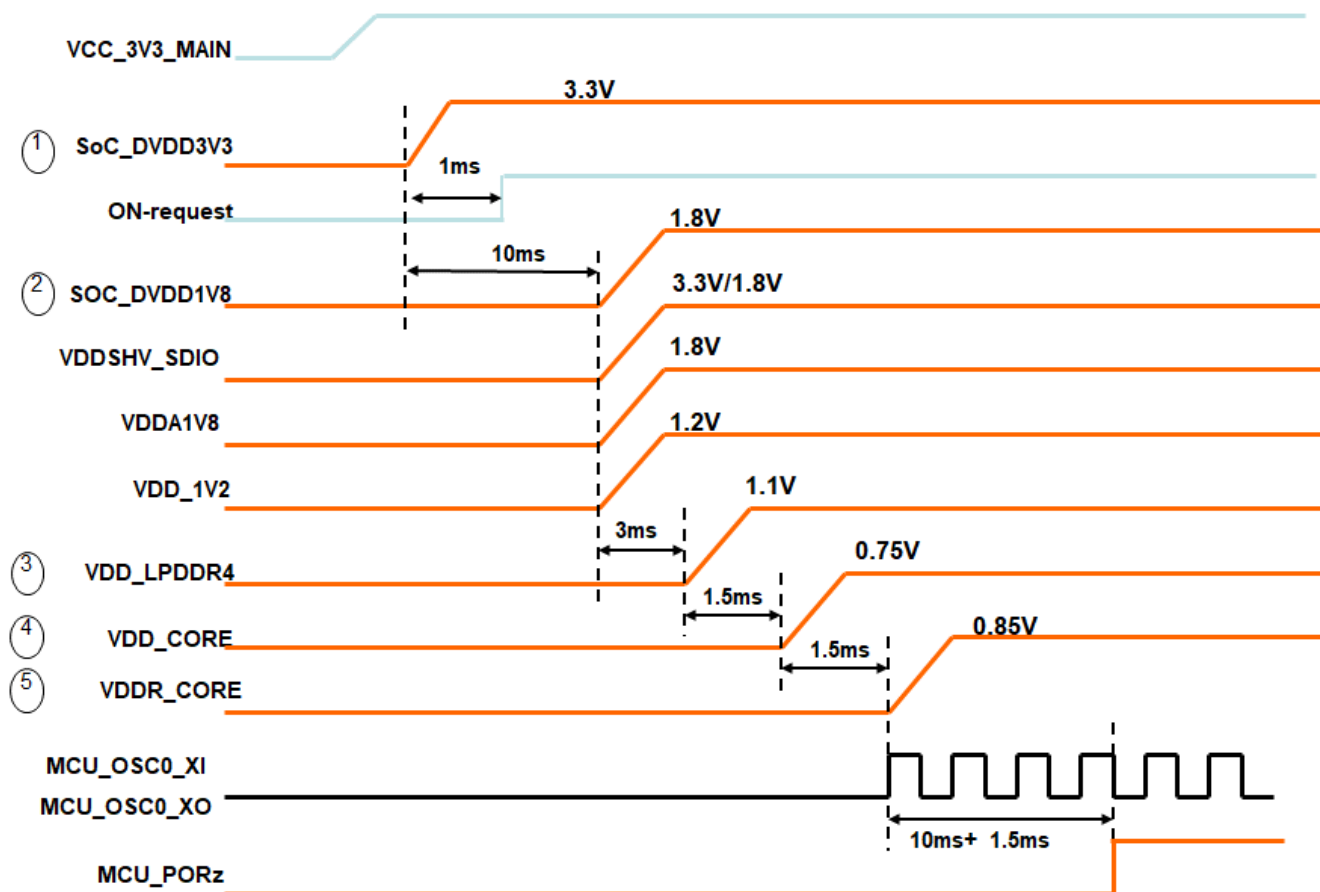
SI #	Power Supply	Test Point	Voltage
3	VMAIN	TP73	5V-15V
4	VCC_5V0	TP76	5V
5	VCC_3V3_MAIN	TP56	3.3V
6	VCC3V3_TA	TP91	3.3V
7	VCC_3V3_SYS	TP54	3.3V
8	VCC_CORE	TP39	0.75V
9	VCC1V8_SYS	TP44	1.8V
10	VCC1V1	TP49	1.1V
11	VDDSHV_SDIO	TP41	1.8V/3.3V
12	VCC_0V85	TP51	0.85V
13	VDDA1V8	TP52	1.8V
14	VDD_1V2	TP53	1.2V
15	VDD_2V5	TP40	2.5V
16	VPP_1V8	TP33	1.8V
17	VDD_1V0	TP35	1.0V
18	VCC_CSI_IO	C12.1	1.8V/3.3V
19	VCC3V3_EXP	C192.1/J3.1	3.3V
20	VCC5V0_EXP	C185.1/J3.2	5.0V
21	VCC3V3_PRU	C384.1/J11.1	3.3V
22	VDD_MMC1	C39.1/FL8.1	3.3V
23	VBUS_5V0_TYPEA1	C375.1/C110.1	5.0V
24	XDS_USB_VBUS ⁽¹⁾	TP90	5.0V
25	VCC3V3_XDS ⁽¹⁾	TP81	3.3V
26	FT4232_USB_VBUS ⁽²⁾	J17.1	5.0V
27	VCC_3V3_FT4232 ⁽²⁾	LD10.2	3.3V
28	VCC_1V8_FT4232 ⁽²⁾	C166.2	1.8V

(1) This voltage is available only when micro B to type A USB cable is connected between J18 and host PC.

(2) This voltage is available only when micro B to type A USB cable is connected between J17 and host PC.

2.3.5 Power Sequencing

The power sequencing of AM62x-Low Power EVM is given below.



2.3.6 AM62x 17x17 SoC Power

The core voltage of the AM62x 17x17 SoC can be 0.75V or 0.85V based on the PMIC configuration and on the power optimization requirement. By default, the PMIC, configured as **VDD_CORE = 0.75V**, can be changed to 0.85V by changing the PMIC configuration register. Current monitors are provided on all the SoC power rails.

The SoC has different IO groups. Each IO group is powered by specific power supplies as shown in the table below.

Table 2-4. SoC Power Rails

Sl. No	Power Supply	SoC Supply Rails	IO Power Group	Voltage
1	VDD_CORE	VDDA_CORE_USB	CANUART	0.75
		VDDA_CORE_CSI		
		VDD_CANUART		
		VDD_CORE		
2	VDDR_CORE	VDDR_CORE	CORE	0.85
3	VDDA_1V8	VDDA_1V8_CSIRX.	CSI	1.8
		VDDA_1V8_USB	USB	
		VDDA_1V8_MCU		
		VDDA_1V8_OLDI	OLDI	
		VDDA_1V8_OSCO	OSCO	
		VDDA_PLL0, VDDA_PLL1, VDDA_PLL2		
4	VDD_LPDDR4	VDDS_DDR	DDR0	1.1
		VDDS_DDR_C		
5	VPP_1V8	VPP_1V8		1.8

Table 2-4. SoC Power Rails (continued)

Sl. No	Power Supply	SoC Supply Rails	IO Power Group	Voltage
6	SoC_VDDSHV5_SDIO	VDDSHV5	MMC1	3.3
7	SOC_DVDD1V8	VDDSHV0	General	3.3
		VDDSHV1	OSPI	1.8
		VDDSHV4	MMC0	
		VDDSHV6	MMC2	
		VMON_1P8_SOC		
8	SOC_DVDD3V3	VDDSHV0	General	3.3
		VDDSHV2	RGMII	
		VDDSHV3	GPMC	
		VDDSHV_MCU	MCU General	
		VMON_3P3_SOC		
		VDDA_3P3_USB	USB	

2.3.7 Current Monitoring

INA231 power monitor devices are used to monitor current and voltage of various power rails of AM62x 17x17 SoC. The INA231 interfaces to the AM62x 17x17 SoC through I2C interface (SoC_I2C1). Four terminal, high precision shunt resistors are provided to measure load current.

Table 2-5. INA I2C Device Address

Source	Supply net	Device Address	Value of the Shunt Connected to the Supply Rail
VCC_CORE	VDD_CORE	0x40	10mΩ± 1%
VCC_0V85	VDDR_CORE	0x41	10mΩ± 1%
VCC_3V3_SYS	SoC_DVDD3V3	0x4C	10mΩ± 1%
VCC_1V8	SoC_DVDD1V8	0x45	10mΩ± 1%
VDDA1V8	VDDA_1V8	0x4E	10mΩ± 1%
VCC1V1	VDD_LPDDR4	0x46	10mΩ± 1%

2.4 AM62x-Low Power SK EVM Interface Mapping

Table 2-6. Interface Mapping

Interface Name	Port on SoC	DevicePart Number
Memory – LPDDR4	DDR0	MT53E1G16D1FW-046 WT:A
Memory –OSPI	OSPI0	W35N01JWTBAG
Memory –Micro SD Socket	MMC1	MEM2051-00-195-00-A
Memory –eMMC	MMC0	MTFC16GAPALBH-IT
Memory –Board ID EEPROM	SoC_I2C0	M24512-DFMC6TG
Ethernet 1– RGMII	SoC_RGMII1	DP83867IRRGZ
Ethernet 2– RGMII	SoC_RGMII2	DP83867IRRGZ
GPIO Port Expander1	SoC_I2C1	TCA6424ARGJR
PRU Header – 2x10 HDR	PR0_PRU0_GPOand SoC_I2C0	PREC010DAAN-RC
User Expansion Connector – 2x20 HDR	SPI0, SPI2, UART5, SoC_I2C0, SoC_I2C2 and GPIOs	PEC20DAAN
MCU Header – 2x14 HDR	MCU MCU_UART0, MCU_MCAN0, MCU_SPI0, MCU_I2C0 and MCU GPIOs	PREC014DAAN-RC
USB2.0 Type C	USB0	2012670005
USB2.0 Type A	USB1	629104151021
LVDS Display Connector	OLDI0	FFC2A32-40-T
CSI Interface	CSI0	QSH-020-01-L-D-DP-A-K

Table 2-6. Interface Mapping (continued)

Interface Name	Port on SoC	DevicePart Number
HDMI	VOUT0	SiI9022ACNU+ TPD12S016PWR + 10029449-001RLF
Audio Codec	McASP1 and SoC_I2C1	TLV320AIC3106IRGZT+ SJ-43514-SM
GPIO Port Expander 2	SoC_I2C1	TCA6424ARGJR
UART Terminal (UART-to-USB)	SoC_UART SoC_UART[1:0], WKUP_UART0 and MCU_UART0	FT4232HL + 629105150521
Test Automation Header	SoC_I2C1	FH12A-40S-0.5SH
Temperature Sensors	SoC_I2C1	TMP100NA/3K
Current Monitors	SoC_I2C1	INA231AIYFDR
Connectivity– M.2 Key E	MMC2, McASP1 and SoC_UART1	2199119-4

2.5 Clocking

The clocking architecture of the AM62x Low-Power SK EVM is shown below.

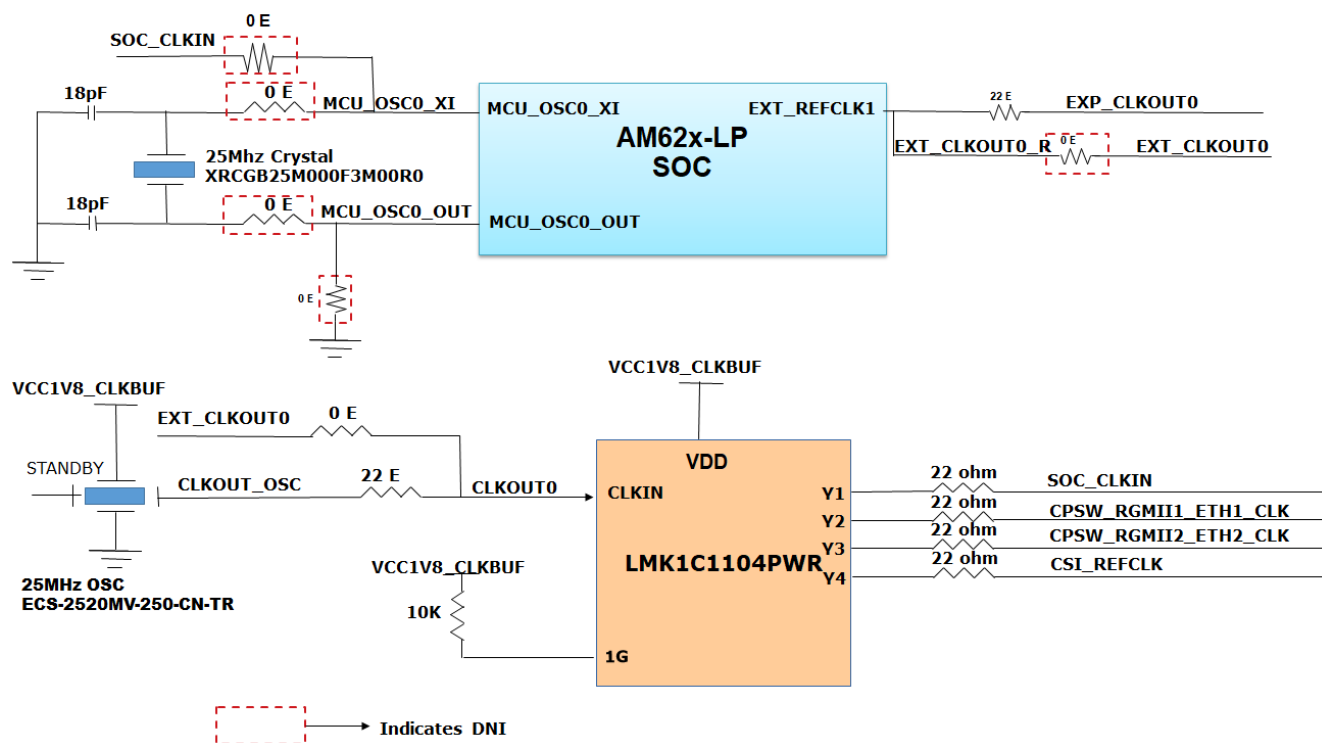


Figure 2-6. Clock architecture

A clock generator of part number LMK1C1104PWR is used to drive the 25MHz clock to the SOC and two Ethernet PHYs. LMK1C1104PWR is a 1:4 LVCMOS clock buffer, which takes the 25MHz crystal/LVCMOS reference input and provides four 25MHz LVCMOS clock outputs. The source for the clock buffer shall be either the `CLKOUT0` pin from the SOC or a 25MHz oscillator, the selection is made using a set of resistors. By default, an oscillator is used as input to the clock buffer on the AM62x Low Power SK EVM. Output Y2 and Y3 of the clock buffer are used as reference clock inputs for two Gigabit Ethernet PHYs. Output Y4 of the clock buffer are used as reference clock inputs for CSI Camera interface.

There is one external crystal attached to the AM62x SoC to provide clock to the WKUP domain of the SoC (32.768KHz).

SOC WKUP DOMAIN

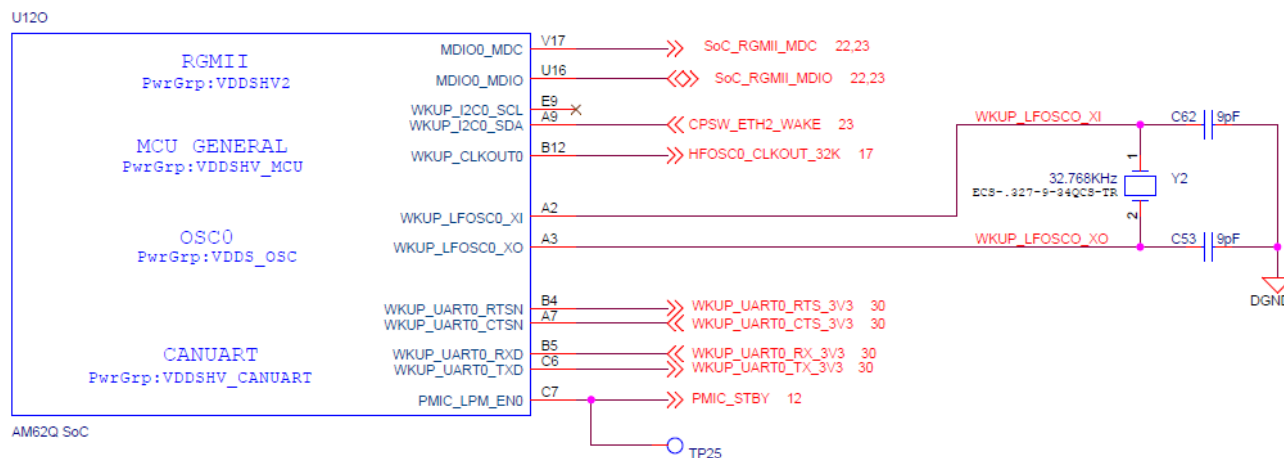


Figure 2-7. SoC Wakeup Domain Clock

Clock inputs required for peripherals such as XDS110, FT4232, HDMI transmitter and audio codec are generated locally using separate crystals or oscillators. Crystals or oscillators used to provide the reference clocks to the EVM peripherals are shown in [Table 2-7](#).

Table 2-7. Peripheral Clocking Table

Peripheral	Mfr.Part #	Description	Frequency
XDS110 emulator(Y3)	XRCGB16M000FXN01R0	CRY 16.000MHz 8pF SMD	16.000MHz
FT4232 Bridge(Y4)	445I23D12M00000	CRY 12.000MHz 18pF SMD	12.000MHz
Audio Codec(U64)	KC3225Z12.2880C1KX00	OSC 12.288MHz CMOS SMD	12.288MHz
HDMITransmitter(U9)	KC3225Z12.2880C1KX00	OSC 12.288MHz CMOS SMD	12.288MHz

The clock required by the HDMI transmitter can be provided by either the on board oscillator or the SoC's AUDIO_EXT_REFCLK1, which can be selected through a resistor mux. SoC's EXT_REFCLK1 is used to provide clock to the User Expansion Connector on the SK EVM. The 32KHz clock to the M.2 module is provided by WKUP_CLKOUT0 of AM62x SoC through a voltage translational buffer.

2.6 Reset

The Reset Architecture of AM62x-Low Power SK EVM is shown below. The SoC has the following resets:

- RESETSTATz is the Main domain warm reset status output
- PORz_OUT is the Main domain power ON reset status output
- RESET_REQz is the Main domain warm reset input
- MCU_PORz is the MCU domain power ON/ Cold Reset input
- MCU_RESETSTATz is the MCU domain warm reset status output

Upon Power on Reset, all peripheral devices connected to the main domain get reset by RESETSTATz.

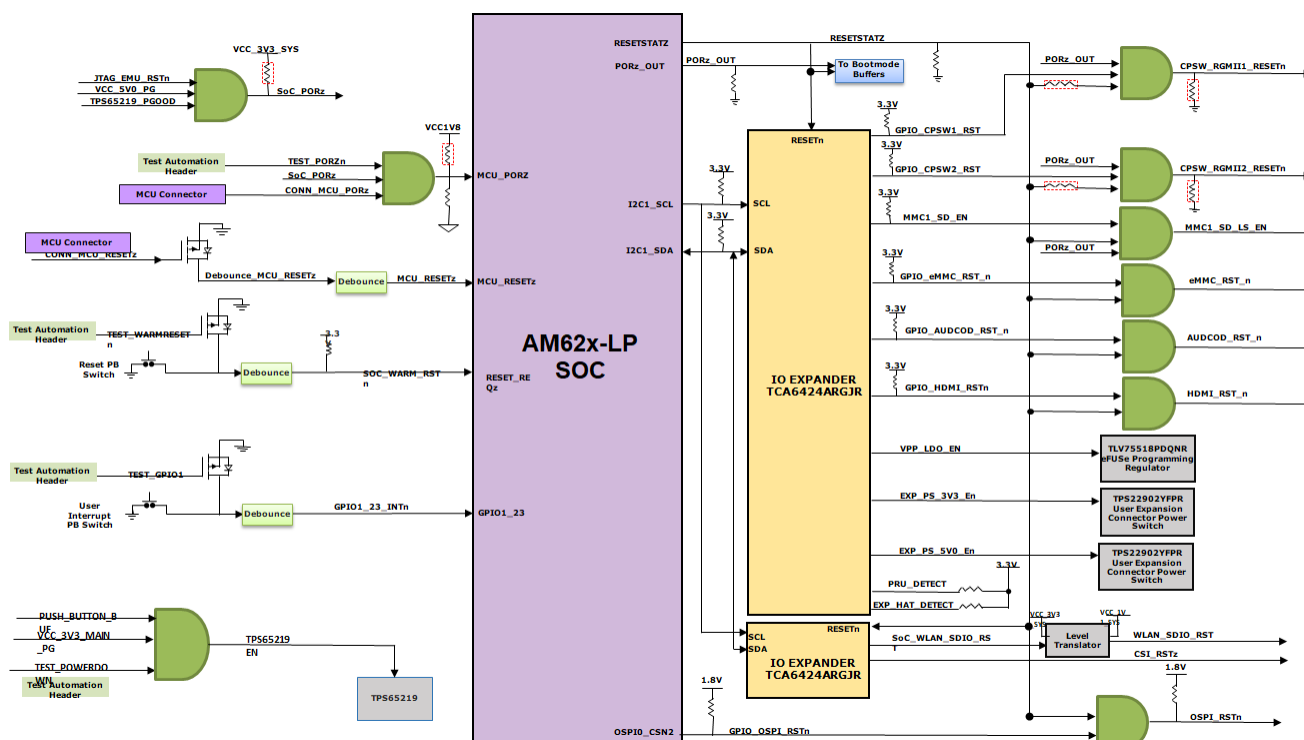


Figure 2-8. Reset Block Diagram

2.7 OLDI Display Interface

The OLDI0 Display interface of the AM62x 17x17 SoC is connected to 40 pin LVDS display connector (J22) Mfr Part # FFC2A32-40-T from GCT. The OLDI Interface supports dual channel 8 bit LVDS output. The Pin-out details of the Display connector/ are given in [Table 2-8](#).

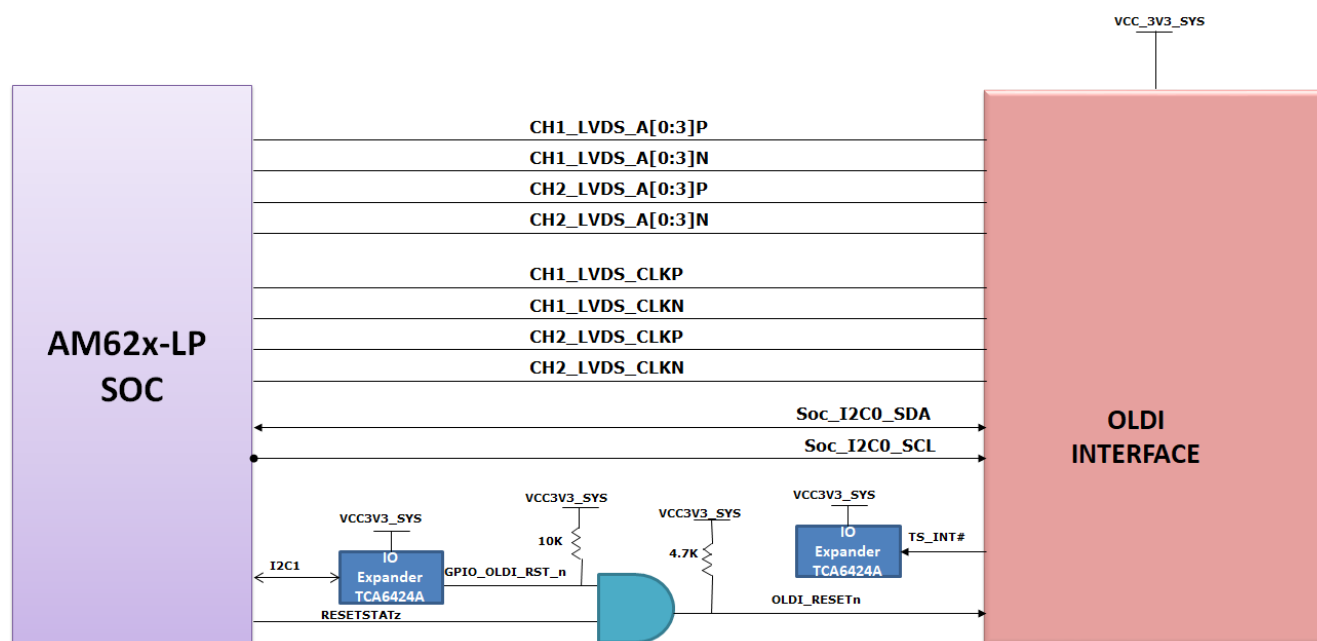


Figure 2-9. OLDI Interface Block Diagram

Table 2-8. Display Connector Pinout

Pin no.	Signal	Pin no.	Signal
1	VCC_3V3_SYS(EEPROM_VDD)	21	CH1_LVDS_A2P
2	SoC_I2C0_SCL	22	GND
3	SoC_I2C0_SDA	23	CH1_LVDS_A3N
4	NC	24	CH1_LVDS_A3P
5	NC	25	GND
6	GND	26	CH2_LVDS_A0N
7	GND	27	CH2_LVDS_A0P
8	OLDI_RESETh	28	GND
9	GPIO_OLDI_INT	29	CH2_LVDS_A1N
10	GND	30	CH2_LVDS_A1P
11	CH1_LVDS_A0N	31	GND
12	CH1_LVDS_A0P	32	CH2_LVDS_CLKN
13	GND	33	CH2_LVDS_CLKP
14	CH1_LVDS_A1N	34	GND
15	CH1_LVDS_A1P	35	CH2_LVDS_A2N
16	GND	36	CH2_LVDS_A2P
17	CH1_LVDS_CLKN	37	GND
18	CH1_LVDS_CLKP	38	CH2_LVDS_A3N
19	GND	39	CH2_LVDS_A3P
20	CH1_LVDS_A2N	40	GND

2.8 CSI Interface

The CSI-2 interface from the AM62x 17x17 SoC is terminated to a 40 pin Camera MIPI connector QSH-020-01-L-D-DP-A-K. The SoC supports 4 CSI RX Lanes, four are pinned out on the SKEVM. The table below contains 40 pin Camera MIPI connector pin-out. SoC I2C2 signals are also connected to the CSI Header. IO Expander GPIO signals are connected to the camera GPIO's.

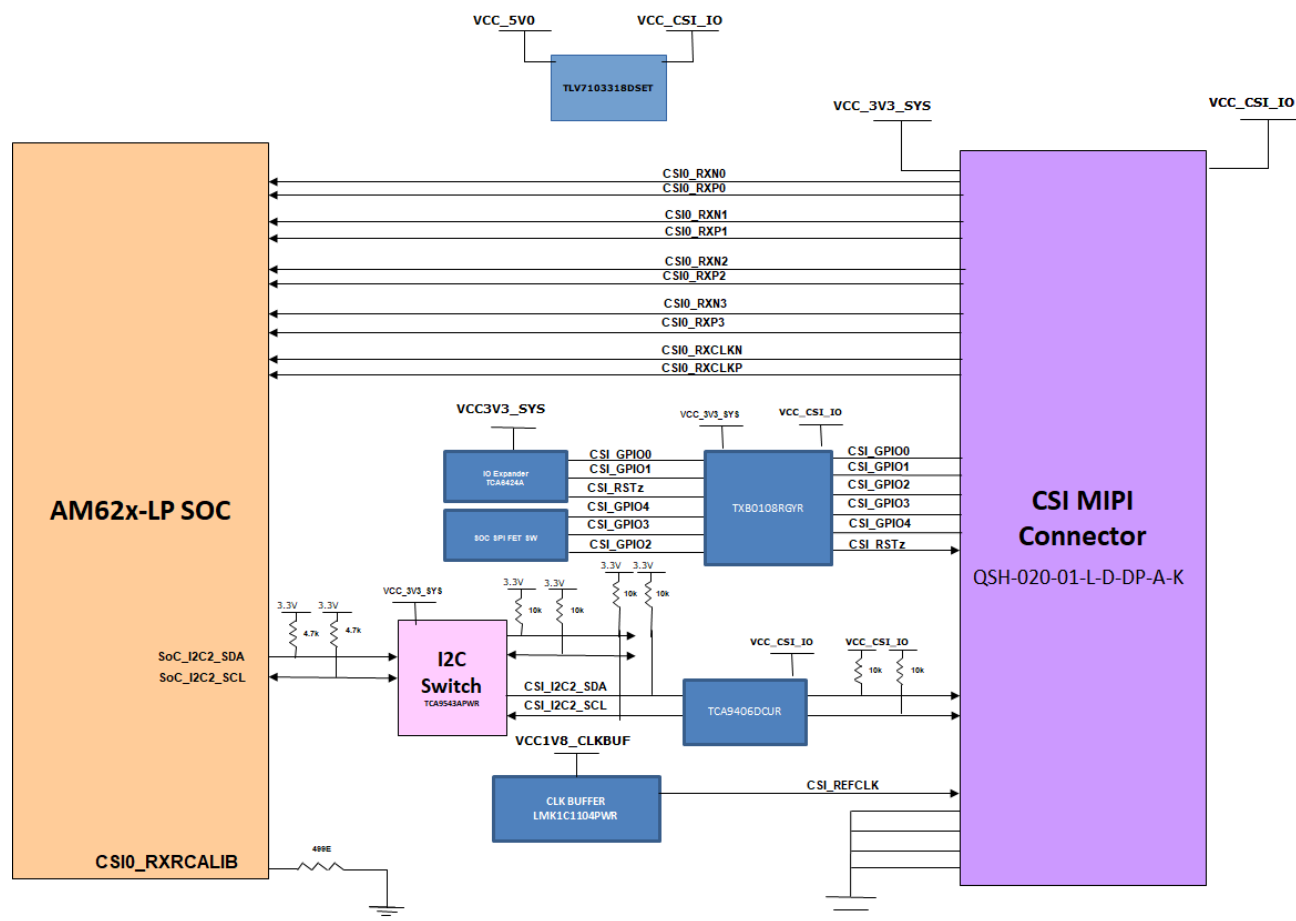


Figure 2-10. CSI Interface Block Diagram

Table 2-9. CSI Camera Connector J19 Pinout

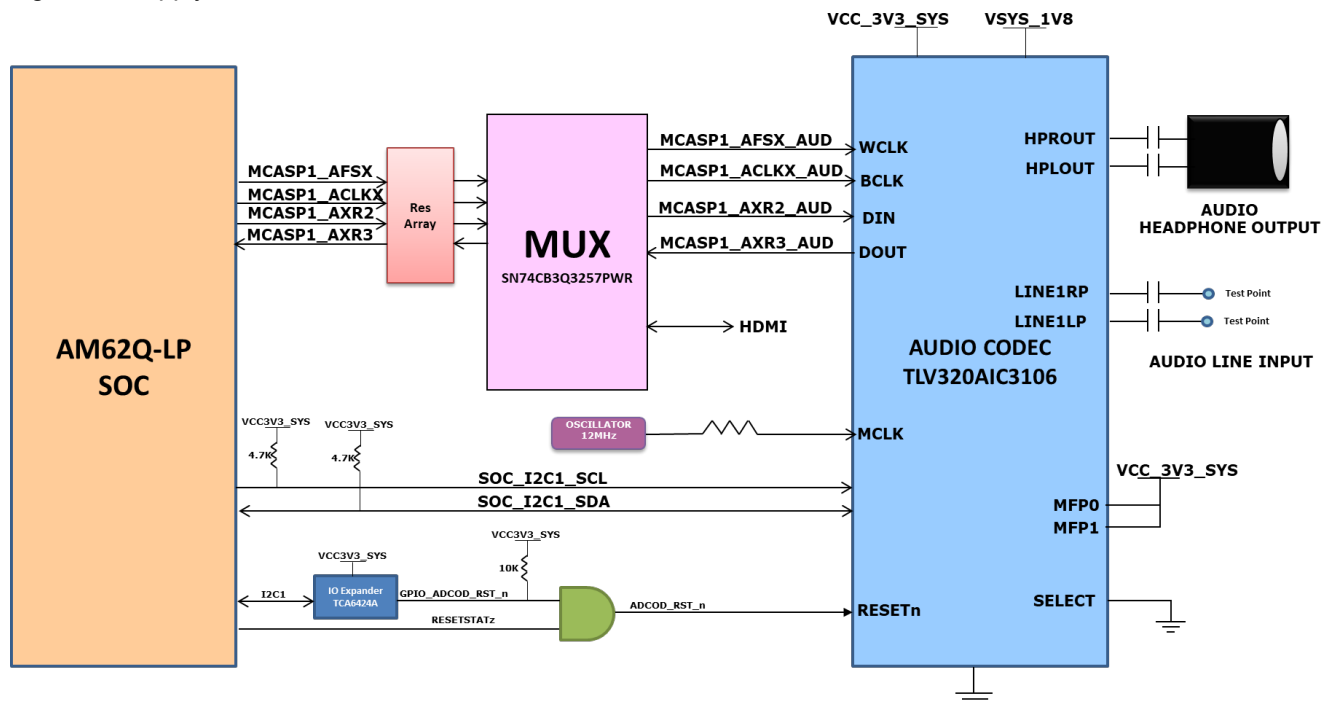
Pin No	Pin Description	Pin No	Pin Description
1	NC	21	CSI0_RXP3
2	CSI_I2C2_SCL_BUFF	22	CSI_GPIO4_buff
3	NC	23	CSI0_RXN3
4	CSI_I2C2_SDA_BUFF	24	Ground
5	CSI0_RXCLKP	25	NC
6	CSI_GPIO0_buff	26	NC
7	CSI0_RXCLKN	27	NC
8	CSI_GPIO1_buff	28	NC
9	CSI0_RXP0	29	NC
10	CSI_REFCLK	30	VCC_3V3_SYS
11	CSI0_RXN0	31	NC
12	Ground	32	VCC_3V3_SYS
13	CSI0_RXP1	33	NC
14	CSI_RSTz_buff	34	VCC_3V3_SYS
15	CSI0_RXN1	35	NC
16	Ground	36	VCC_3V3_SYS
17	CSI0_RXP2	37	NC
18	CSI_GPIO2_buff	38	VCC_CSI_IO
19	CSI0_RXN2	39	NC

Table 2-9. CSI Camera Connector J19 Pinout (continued)

Pin No	Pin Description	Pin No	Pin Description
20	CSI_GPIO3_buff	40	VCC_CSI_IO

2.9 Audio Codec Interface

AM62x-Low Power SK EVM uses TI's Low-Power TLV320AIC3106 Stereo Audio Codec to interface with AM62x via McASP. TLV320AIC3106 is a low-power stereo audio codec with stereo headphone amplifier, as well as multiple inputs and outputs programmable in single ended or fully differential configurations. The record path of the TLV320AIC3106 contains integrated microphone bias, digitally controlled stereo microphone preamplifier and Automatic gain control (AGC) with mix/Mux capability among the multiple analog inputs. The stereo audio DAC supports sampling rates from 8kHz to 96kHz. 1x Standard 3.5mm TRRS Audio Jack connector Mfr. Part# SJ-43514 shall be provided for MIC and Headphone output. Audio Codec's Line inputs are terminated to Test points. SELECT pin shall be held LOW to select I2C as control interface. Codec can be configured over I2C interface, where I2C address can be set by driving pins MFP0 and MFP1 pin either high or low. Both these pins are set to high, so the Device address is set to 0x1B. Unused inputs and outputs of the Audio Codec are connected to ground. The Controller Clock input, MCLK to the Audio Codec is provided through a 12.288MHz Oscillator. Audio serial data bus bit clock BCLK of the codec is driven by the AM62x SoC through a buffer. Audio serial data bus input and output DIN, DOUT are connected to SoC's MCASP1_AXR0 and MCASP1_AXR2 through buffers. An AND output of RESETSTATz and a GPIO sourced via IO expander are used to reset the Audio codec. The TLV320AIC3106 is powered by an analog supply of 3.3V, a digital core supply of 1.8V, and a digital I/O supply 3.3V.

**Figure 2-11. Audio Codec Interface Block Diagram**

2.10 HDMI Display Interface

The DSS (Display Sub system) interface from AM62X 17x17 SoC is used on the SK EVM to provide a HDMI Interface through a standard Type-A Connector. The SK EVM features a SiI9022A HDMI Transmitter from Lattice semiconductors to convert the 24bit Parallel RGB DSS output stream as well as a McASP to a HDMI-compliant digital audio and video signal. The Data mapping format used is RGB888. The data bus width is 24-bits. SoC_I2C1 is connected to the HDMI Transmitter accesses the compatible mode registers, the TPI registers, and the CPI registers. To use the SiI9022A, the SoC needs to setup the device. This is done via the I2C interface between the SoC and the SiI9022A. Audio Data is sent from SoC to HDMI transmitter through the McASP1 instance. HDMI_I2C Bus accesses the EDID and HDCP data on an attached sink device. TMDs

Differential data pairs along with the differential clock signals from the transmitter are connected to the HDMI connector through HDMI ESD device Mfr Part# TPD12S016PWR which also acts as a load switch to limit current supplied to the HDMI connector from board 5V supply. The HDMI Framer is powered using 3.3V Board IO Supply and 1.2V by a dedicated PMIC LDO.

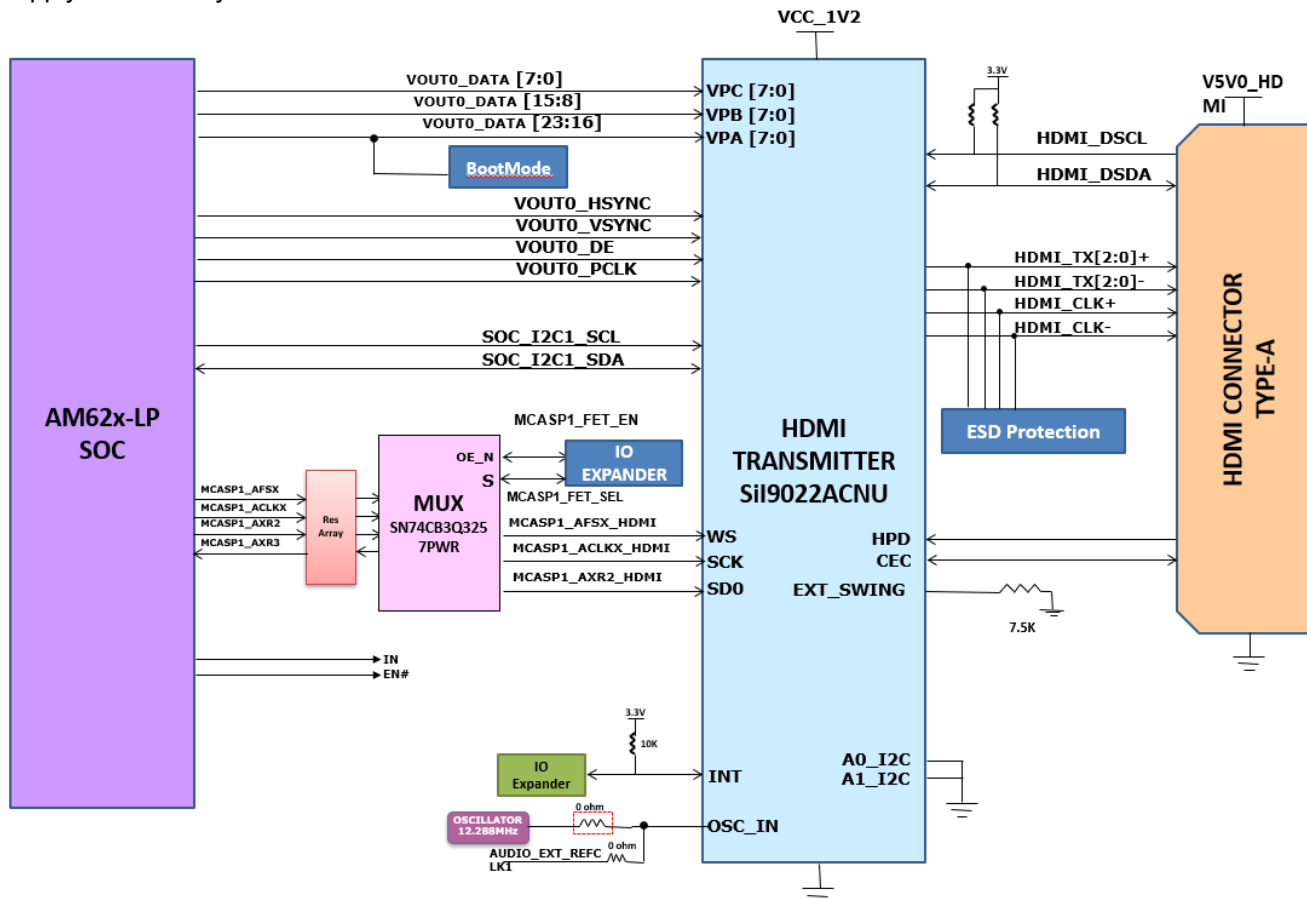


Figure 2-12. HDMI Interface Block Diagram

2.11 JTAG Interface

The AM62x Low-Power SK EVM board includes XDS110 class on board emulation. The connection for the emulator uses an USB 2.0 micro-B connector and the circuit acts as a Bus powered USB device. The VBUS power from the connector will be used to power the emulation circuit such that connection to the emulator is not lost when the power to the SKEVM is removed. Voltage translation buffers are used to isolate the XDS110 circuit from the rest of the SKEVM. Optionally, JTAG Interface on SKEVM is also provided through 20 Pin Standard JTAG cTI Header J19. This allows the user to connect an external JTAG Emulator Cable. Voltage translation buffers are used to isolate the JTAG signals from cTI header from the rest of the SKEVM. The output from the voltage translators from XDS110 Section and cTI Header Section are muxed and connected to AM62X JTAG Interface. If a connection to the cTI 20 Pin JTAG connector is sensed using a presence detect circuit, the mux will be set to route the 20 pin signals from the cTI connector to the AM62X SoC in place of the on-board emulation circuit.

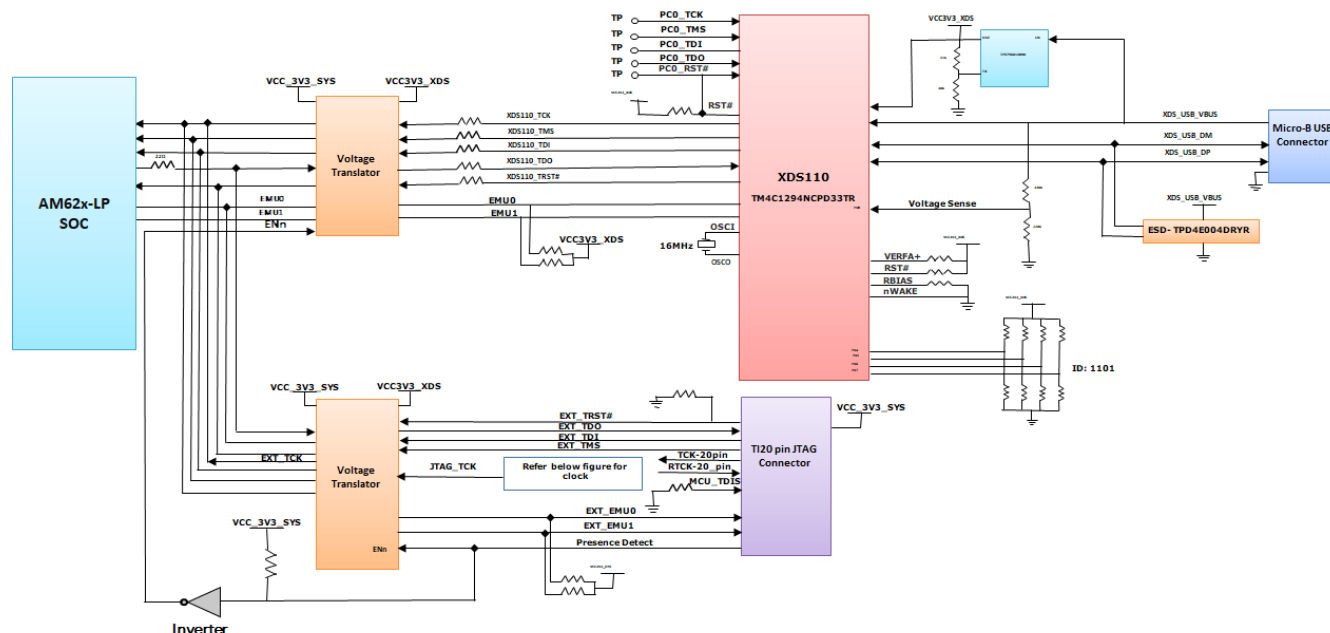


Figure 2-13. JTAG Interface Block Diagram

The pin-out of the cTI 20 pin JTAG connector are given in [Table 2-10](#). A ESD protection part number TPD4E004 is provided on USB signals to steer ESD current pulses to VCC or GND. TPD4E004 protects against ESD pulses up to ± 15 -kV Human-Body Model (HBM) as specified in IEC 61000-4-2 and provides ± 8 -kV contact discharge and ± 12 -kV air-gap discharge.

Table 2-10. JTAG Connector (J19) Pinout

Pin No.	Signal
1	JTAG_TMS
2	JTAG_TRST#
3	JTAG_TDI
4	JTAG_TDIS
5	VCC3V3_SYS
6	NC
7	JTAG_TDO
8	SEL_XDS110_INV
9	JTAG_cTI_RTCK
10	DGND
11	JTAG_cTI_TCK
12	DGND
13	JTAG_EMU0
14	JTAG_EMU1
15	JTAG_EMU_RSTn
16	DGND
17	NC
18	NC
19	NC
20	DGND

The pin-outs of the cTI 20 pin JTAG connector are given in [Table 2-10](#). A ESD protection part number TPD4E004 is provided on USB signals to steer ESD current pulses to VCC or GND. TPD4E004 protects against

ESD pulses up to $\pm 15\text{kV}$ Human-Body Model (HBM) as specified in IEC 61000-4-2 and provides $\pm 8\text{kV}$ contact discharge and $\pm 12\text{kV}$ air-gap discharge.

2.12 Test Automation Header

The AM62x-Low Power SK EVM has a 40 pin test automation header (FH12A-40S-0.5SH) to allow an external controller to manipulate some basic operations like Power Down, POR, Warm Reset, Boot Mode control etc.

The Test Automation Circuit is powered by the 3.3V supply generated by a dedicated regulator Mfr.Part# TPS62177DQCR. The SoC's I2C1 is connected to the test automation header. Another I2C instance (BOOTMODE_I2C) from the Test Automation Header is connected to the 24 bit I2C boot mode IO Expander of Mfr. Part# TCA6424ARGJR to allow control of the boot modes for the AM62X SoC.

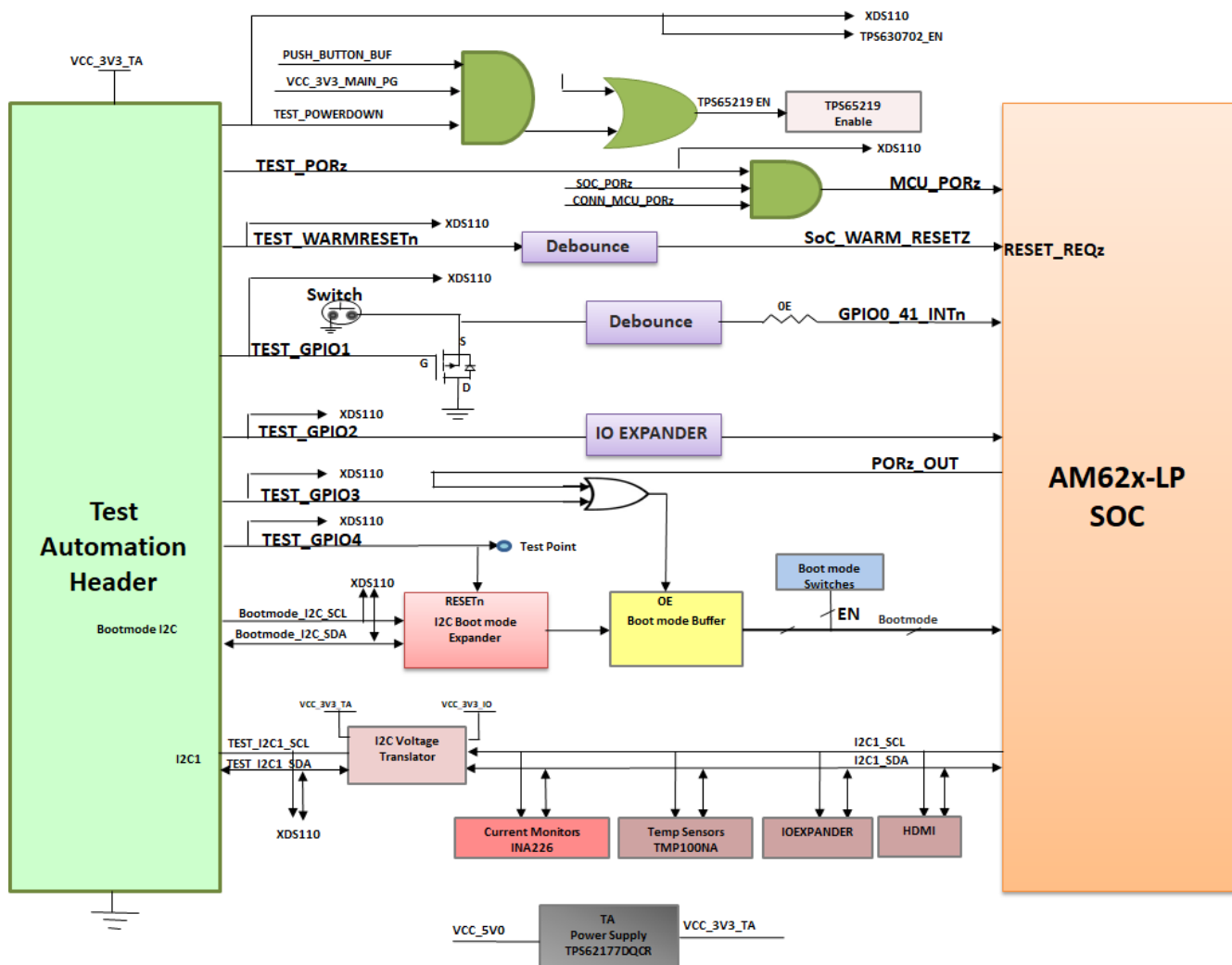


Figure 2-14. Test Automation Interface Block Diagram

The test automation circuit has voltage translation circuits so that the controller is isolated from the IO voltages used by the AM62x SoC. Boot mode for the AM62x SoC must be controlled by either the user using DIP Switches or the test automation header through the I2C IO Expander. Boot Mode Buffers are used to isolate the Boot Mode controls driven through DIP Switches or I2C IO Expander. The boot mode is controlled by the user using two 8-bit DIP switches on the board, which will connect a pull-up resistor to the output of a buffer when the switch is set to the ON position and to weaker pull-down resistor when set to the OFF position. The output of the buffer is connected to the boot mode pins on the AM62x SoC and the output is enabled when the boot mode is needed during a reset cycle.

When boot mode is set through Test Automation header, the required switch values are set at the I2C IO expander output, which overwrites the DIP switch values to give the desired boot values to the SoC. The pins used for boot mode also have other functions which will be isolated by disabling the boot mode buffer during normal operation.

The power down signal from the test automation header instructs the SK EVM to power down all the rails except for dedicated power supplies on the board. Similarly PORZn signal is also provided to give a hard reset to the SoC and WARM_RESETh for warm reset of the SoC.

Table 2-11. Test Automation Connector (J24) Pinout

Pin no.	Signal	IO Direction	Pin no.	Signal	IO Direction
1	VCC3V3_TA	Power	21	NC	NA
2	VCC3V3_TA	Power	22	NC	NA
3	VCC3V3_TA	Power	23	NC	NA
4	NC	NA	24	NC	NA
5	NC	NA	25	DGND	Power
6	NC	NA	26	TEST_POWERDOWN	Input
7	DGND	Power	27	TEST_PORZn	Input
8	NC	NA	28	TEST_WARMRESETh	Input
9	NC	NA	29	NC	NA
10	NC	NA	30	TEST_GPIO1	Bidirectional
11	NC	NA	31	TEST_GPIO2	Bidirectional
12	NC	NA	32	TEST_GPIO3	Input
13	NC	NA	33	TEST_GPIO4	Input
14	NC	NA	34	DGND	Power
15	NC	NA	35	NC	NA
16	DGND	Power	36	SoC_I2C1_TA_SCL	Bidirectional
17	NC	NA	37	BOOTMODE_I2C_SCL	Bidirectional
18	NC	NA	38	SoC_I2C1_TA_SDA	Bidirectional
19	NC	NA	39	BOOTMODE_I2C_SDA	Bidirectional
20	NC	NA	40	DGND	Power

2.13 UART Interface

The four UART ports of the AM62x SoC (MCU UART0, WKUP UART0, SOC UART0 and SOC UART1) are interfaced with an FTDI FT4232HL for UART-to-USB functionality and terminated on a USB micro-B connector (J17) on board. When the AM62x-Low Power SK EVM is connected to a Host using USB cable, the computer can establish a Virtual Com Port which can be used with any terminal emulation application. The FT4232HL is bus powered.

Since the circuit is powered through BUS power, the connection to the COM port will not be lost when the SK EVM power is removed.

Table 2-12. UART Port Interface

UART Port	USB to UART Bridge	USB Connector	COM Port
SOC_UART0	FT4232HL	J17	COM1
SOC_UART1			COM2
WKUP_UART0			COM3
MCU_UART0			COM4

The FT4232 chip is configured to operate in 'Single chip USB to four channel UART' mode and will take the configuration file from the external SPI EEPROM connected to it. The EEPROM (93LC46B) supports 1Mbit/s cloc krate. The EEPROM is programmable in-circuit over USB using a utility program called FT_PROG available

from FTDI's web site. The FT_PROG is also used for programming the board serial number for users to identify the connected COM port with board serial number when one or more boards are connected to the computer.

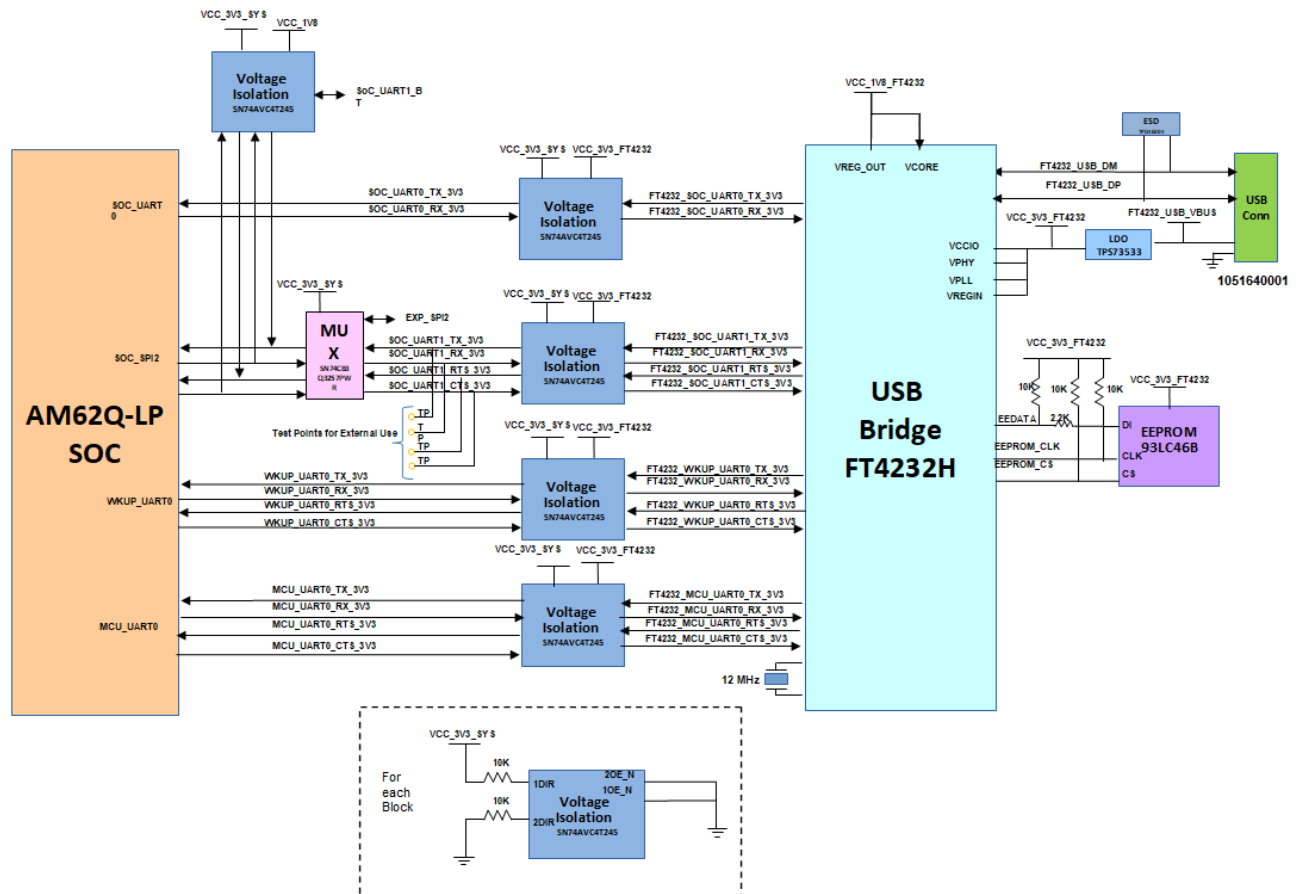


Figure 2-15. UART Interface Block Diagram

2.14 USB Interface

2.14.1 USB2.0 Type A Interface

USB2.0 data lines from Type A connector J9 are connected to the USB1 interface of the AM62x 17x17 SOC to provide USB high-speed/full-speed communication. USB1_VBUS to the SOC is provided through a resistor divider network to support (5V-30V) VBUS operation. USB1_DRVVBUS from SOC is connected to the enable pin of Load switch Mfr Part # TPD3S014DBVR to allow on board 5V supply to power the VBUS..

A common mode choke of Mfr Part# DLW21SZ900HQ2B is provided on USB Data lines to take care of EMI/ EMC.

USB Data lines from Type-A connectors are also connected to the Current Limit Load Switch and ESD Protection IC Mfr Part# TPD3S014DBVR. This switch limits the current to 500mA and dissipates the ESD strikes above the maximum level specified in the IEC 61000-4-2.

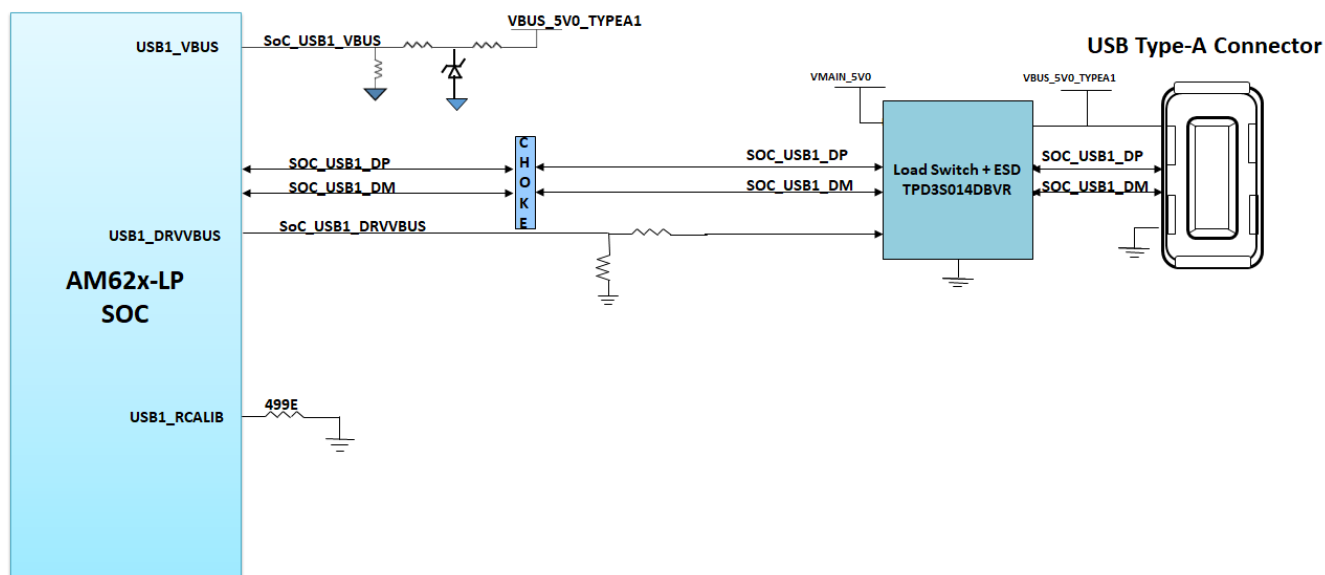


Figure 2-16. USB Type A Interface Block Diagram

2.14.2 USB2.0 Type C Interface

On AM62x-Low Power SK EVM, USB 2.0 Interface is offered through USB Type-C Connector J15 Mfr part# 2012670005 which supports data rate up to 480Mbps. J15 is used for Data communication and also as power connector. It is configured as a DRP port using PD controller TPS65988DHRSHR IC. So it can act as either Host or Device. Role of the port depends on the type of the device getting connected on the connector and its ability to either sink or source. When the port is acting as DFP, it can source up to 5V@500mA.

USB2.0 Data lines DP and DM from J15 are connected to the USB0 interface of AM62X LOW POWER SoC via choke and ESD protection device. USB0_VBUS to the SOC is provided through a resistor divider network.

A common mode choke of Mfr Part# DLW21SZ900HQ2B is provided on USB Data lines to take care of EMI/EMC. An ESD protection device of part number ESD122DMXR is included to dissipate ESD strikes on USB2.0 DP/DM Signals. An ESD protection device of part number TPD1E01B04DPLT is included on CC signals and TVS2200DRVR IC is included on VBUS rail of Type-C Connector J15 to dissipate ESD strikes.

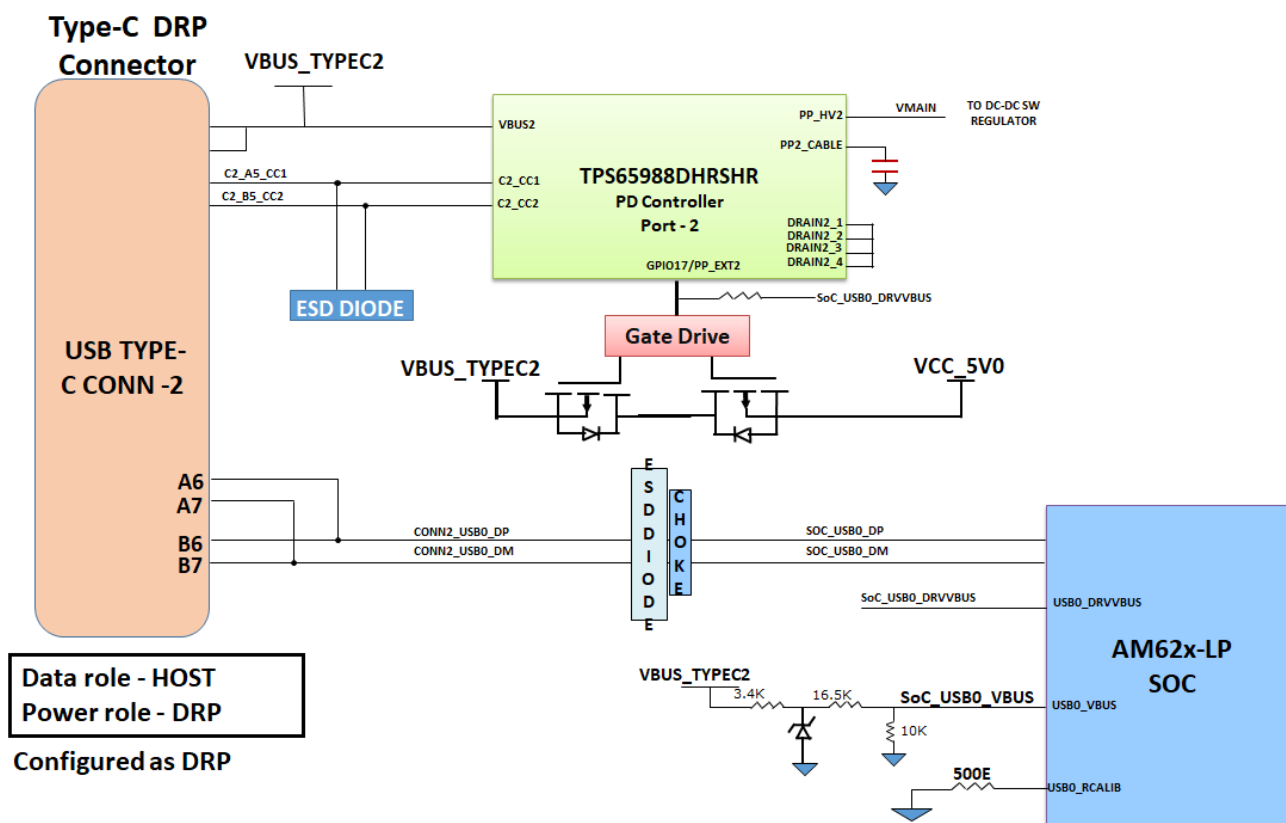


Figure 2-17. USB2.0 Type C Interface Block Diagram

2.15 Memory Interfaces

2.15.1 LPDDR4 Interface

AM62x-Low Power SK EVM has 2GB, 16bit wide LPDDR4 memory with operating speed of up to 2133MT/s. Micron's MT53E1G16D1FW-046 WT:A is used. This uses two x8 8Gb Micron dies to make one x16 interface. The LPDDR memory is mounted on-board (single chip). The Placement and routing of LPDDR4 device is point to point.

The LPDDR4 requires 1.8V and thus reduces power demand. The devices require I/O power of 1.1V. LPDDR4 reset is an active low signal, which is controlled by SoC and the signal is pulled down to set the default active state. A footprint for pull up is also provided.

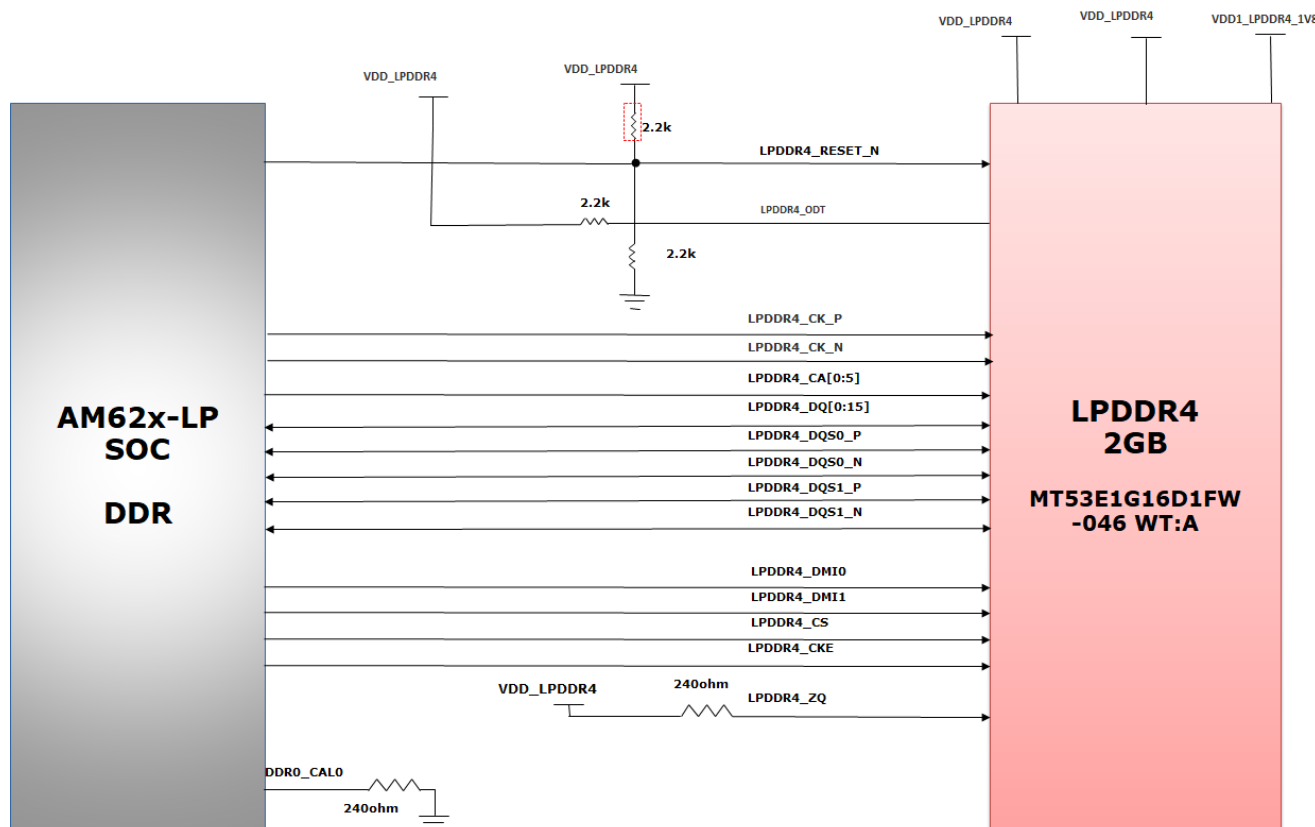


Figure 2-18. LPDDR4 Interface Block Diagram

2.15.2 OSPI

The AM62x Low-Power SK EVM board has a 1-Gbit OSPI memory device from Cypress Part# W35N01JWTBAG which is connected to OSPI0 of the AM62x 17x17 SoC. OSPI supports single and double data rates with clock speeds up to 166Mhz STR and 120Mhz DTR.

OSPI & QSPI implementation: 0 ohm resistors are provided for DATA[7:0], DQS, INT# and CLK signals. Footprints to mount external pull up resistors are provided on DATA[7:0] to prevent bus floating. The footprint for the OSPI memory also allows the installation of either a QSPI memory or an OSPI memory. The 0 ohm series resistors provided for pins OSPI_DATA[4:7] will be removed if QSPI flash is to be mounted.

The reset for the OSPI flash is connected to a circuit that ANDs the RESETSTATz from the SoC with the signal GPIO_OSPI_RSTn from the SoC GPIO. This will apply reset for warm and cold reset. A pull-up is provided on GPIO_OSPI_RSTn coming from SoC pin to set the default active state.

The OSPI flash is powered by 1.8V IO supply. The 1.8V supply is provided to both VCC and VCCQ pins of the OSPI flash memory. OSPI of the SOC is powered by VDDSHV1 Power group of SoC and is connected to 1.8V IO supply.

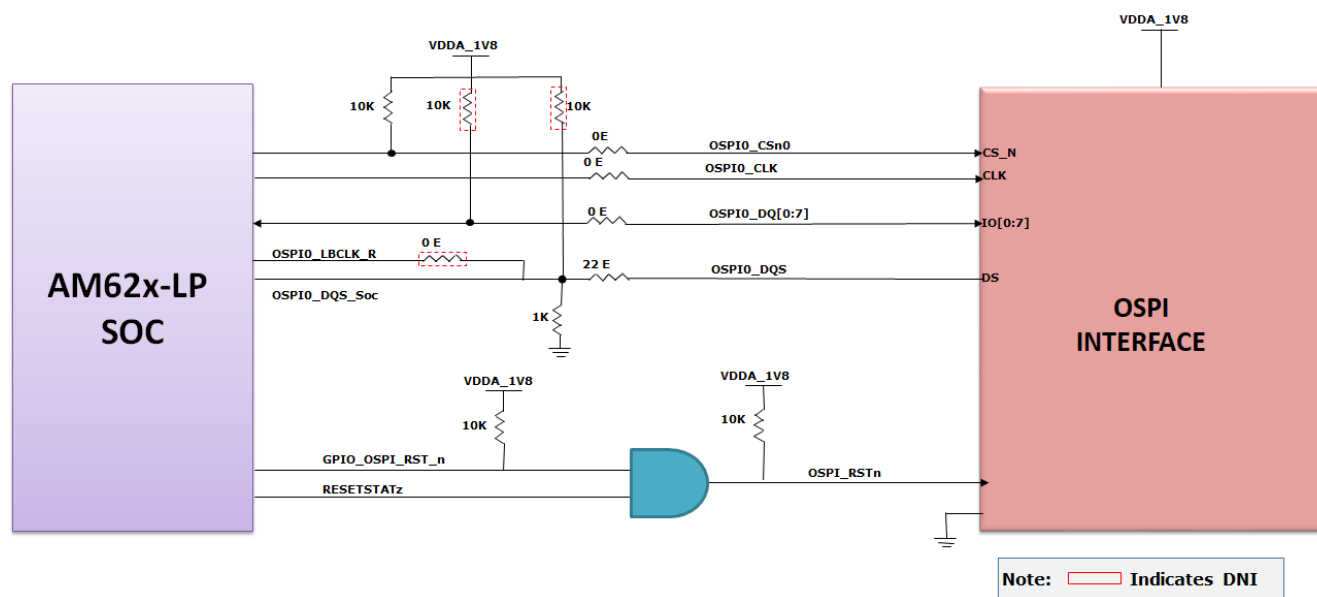


Figure 2-19. OSPI Block Diagram

2.15.3 MMC Interfaces

The AM62x 17x17 SoC has three MMC ports. MMC0 is connected to an eMMC flash, MMC1 is interfaced with Micro SD Socket on the board and MMC2 is connected to an optional M.2 module for WiFi and Bluetooth.

2.15.3.1 MMC0 - eMMC Interface

The AM62x-Low Power SK EVM board contains 16GB of eMMC flash memory from Micron Part# MTFC16GAPALBH-IT connected to MMC0 port of the AM62X 17x17 SoC. The flash is connected to 8 bits of the MMC0 interface supporting HS400 double data rates up to 200MHz.

The eMMC device requires two power supplies, 3.3V for NAND memory and 1.8V for the eMMC interface. The MMC0 interface of the SOC is powered by the VDDSHV4 power domain, which is connected to 1.8V IO supply.

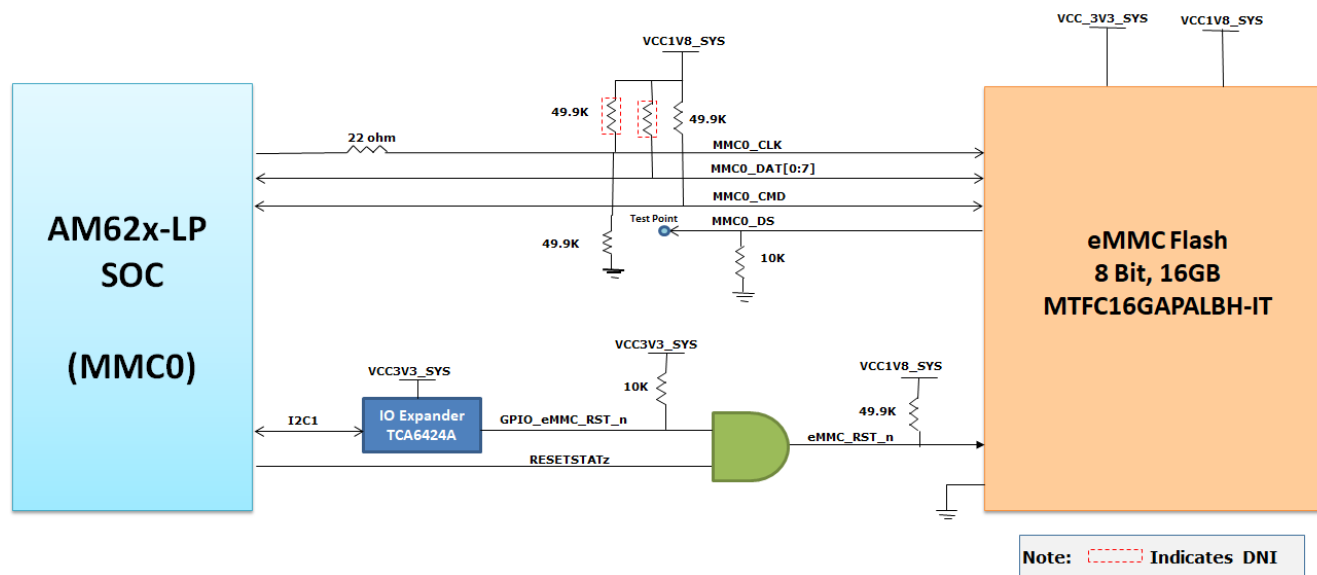


Figure 2-20. EMMC Interface Block Diagram

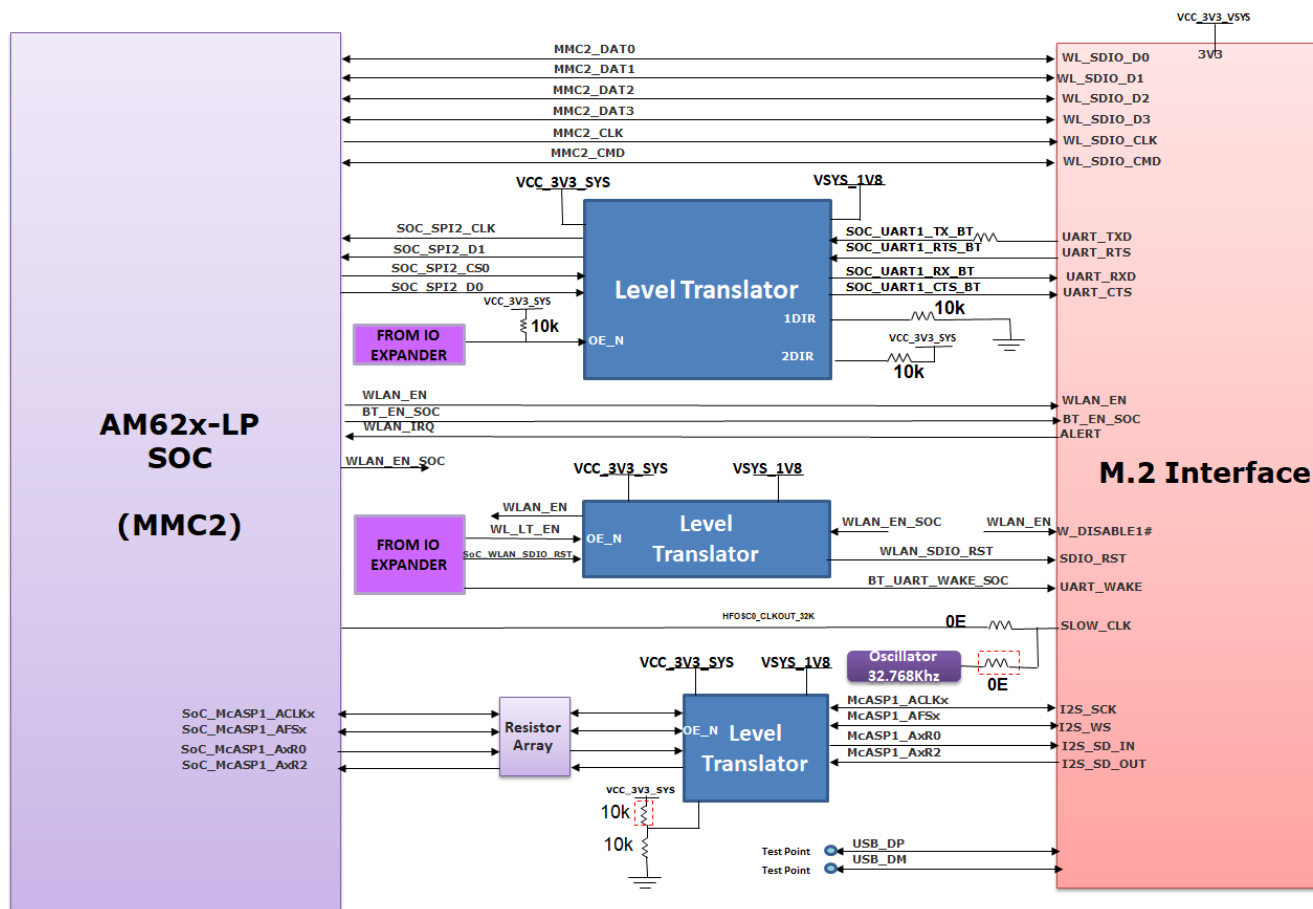


Figure 2-22. M.2 Interface Block Diagram

2.15.4 EEPROM

AM62x-Low Power SK EVM boards are identified by version and serial number, which are stored on the onboard EEPROM. The EEPROM is accessible from AM62x 17x17 SoC I2C0 port.

The Board ID EEPROM I2C address is set to 0x51. The AM62x-Low Power SK EVM includes an M24512-DFMC6TG 512kb EEPROM. The first 259 bytes of memory are preprogrammed with identification information for each board. The remaining 65277 bytes are available to the user for data or code storage.

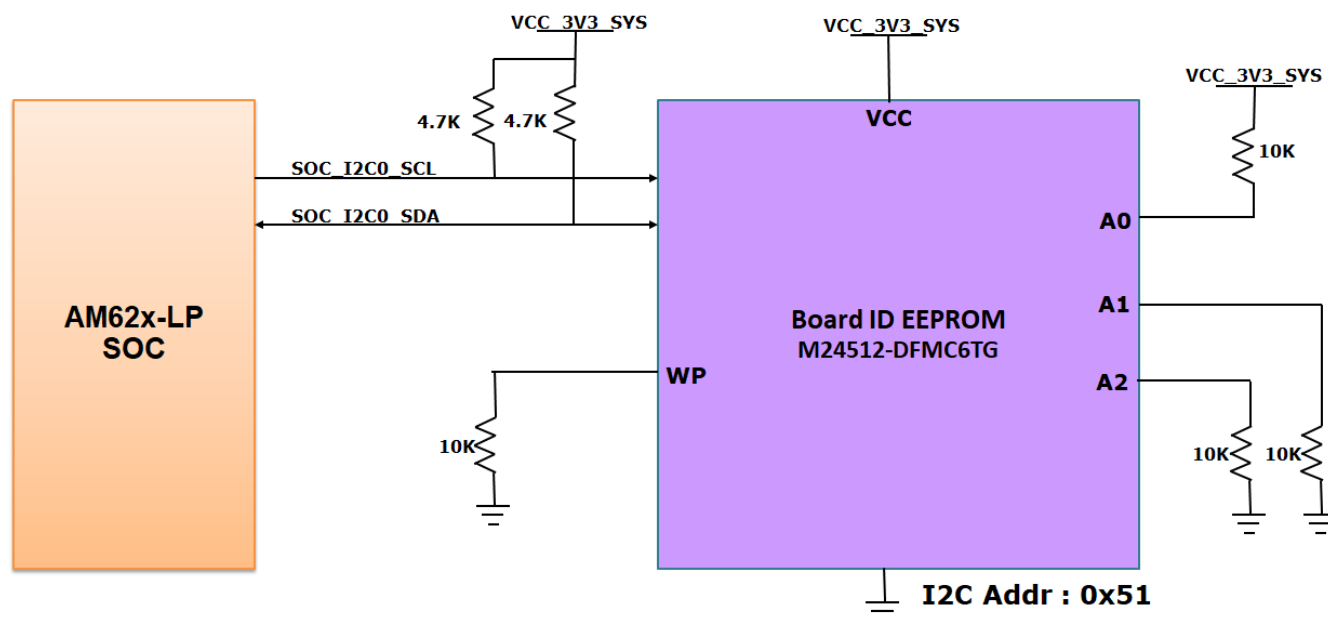


Figure 2-23. Board ID EEPROM Interface Block Diagram

2.16 Ethernet Interface

The AM62x-Low Power SK EVM offers two Ethernet Ports of 1 Gigabit Speed for external Communication. RGMII1 Gigabit Ethernet CPSW Port from AM62x 17x17 SOC is connected to the On-Board PHY Transceiver DP83867 while RGMII2 Gigabit Ethernet CPSW Port signals are terminated to a Board to Board connector providing flexibility of interfacing either to an optional daughter card. CPSW_RGMII1 and CPSW_RGMII2 Ports share a common MDIO Bus to communicate with the external PHY Transceiver.

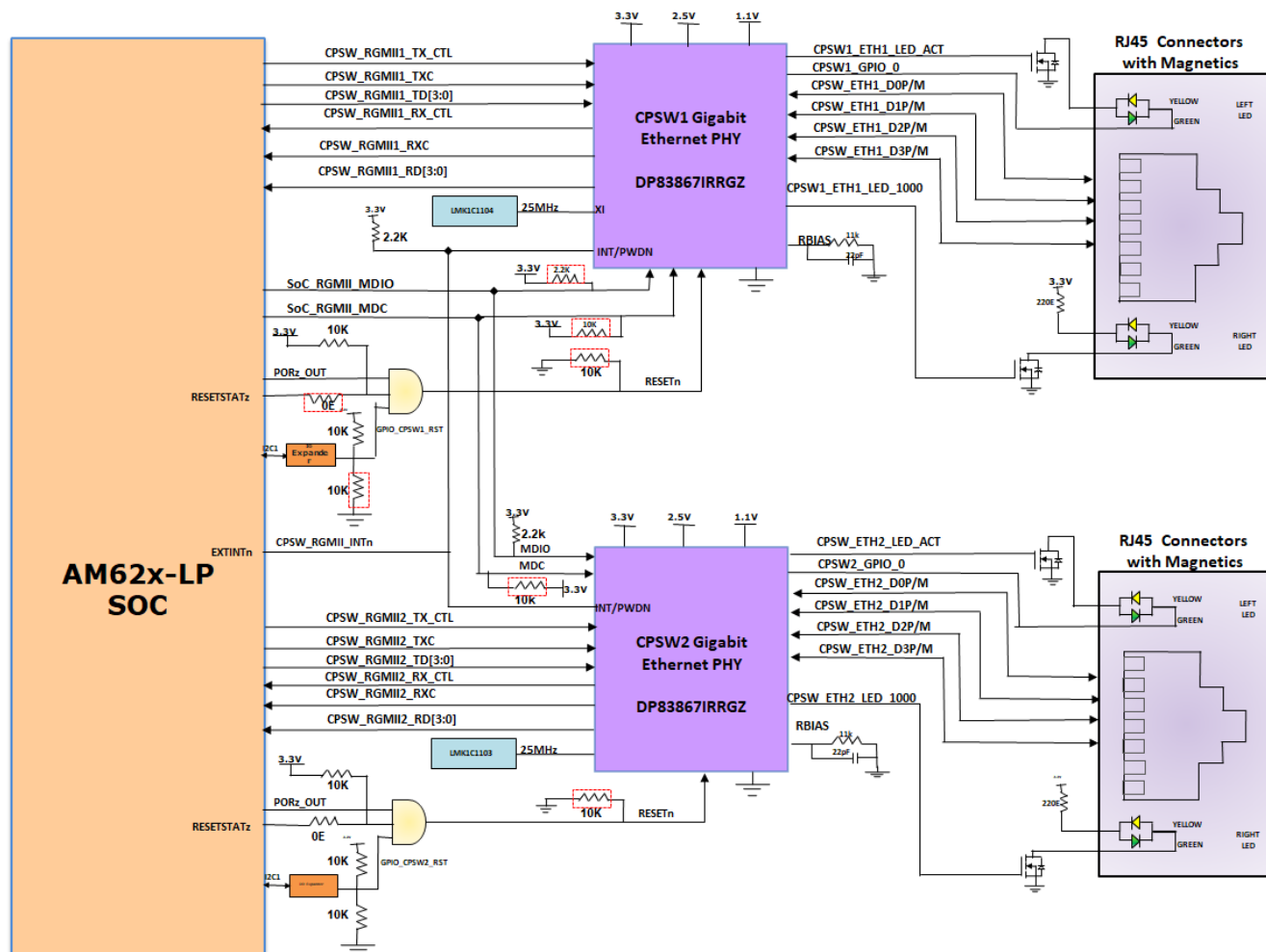


Figure 2-24. Ethernet Interface Block Diagram

2.16.1 CPSW Ethernet PHY1 Default Configuration

The default configuration of the DP83867 is determined using a number of resistor pull-up and pull-down values on specific pins of the PHY. Depending on the values installed, each of the configuration pins can be set to one of four modes by using the pull up and pull down options provided. The AM62x-Low Power SK EVM uses the 48-pin QFN package which supports the RGMII interface.

The DP83867 PHY uses four level configurations based on resistor strapping which generate four distinct voltage ranges. The resistors are connected to the RX data and control pins which are normally driven by the PHY and are inputs to the processor. The voltage range for each mode is shown below:

- Mode1 – 0V to 0.3V
- Mode 2 – 0.462V to 0.6303V
- Mode3 – 0.7425V to 0.9372V
- Mode4 – 2.2902V to 2.9304V

Footprints for both pull-up and pull-down is provided on all the strapping pins except LED_0. LED_0 is for Mirror Enable, which is set to mode 1 by default, Mode 4 is not applicable and Mode2, Mode3 option is not desired. CPSW_RGMII1 port of the AM62X 17x17 SoC is connected to DP83867 whose configuration is as given below:

- PHY ADDR: 00000
- Auto_neg: Disabled
- ANG_sel: 10/100/1000
- RGMII_Clk skew Tx: 0ns

- RGMIIclk skew Rx: 2ns

Table 2-13. CPSW Ethernet PHY–1 Strap values

Strap Setting	Pin Name	Strap Function	Mode	Value of Strap Function	Description
PHY Address	RX_D2	PHY_AD3	1	0	PHY Address: 0000
		PHY_AD2	1	0	
	RX_D0	PHY_AD1	1	0	
		PHY_AD0	1	0	
Auto Negotiation	RX_DV/ RX_CTRL	Auto- neg	3	0	Autoneg Disabled
Modes of Operation	LED2	RGMII Clock Skew TX[1]	5	0	RGMII TX Clock Skew is set to 0ns
		RGMII Clock Skew TX[0]	5	0	
	LED_1	RGMII Clock Skew TX[2]	5	1	
		ANEG_SEL	1	0	advertiseability of 10/100/1000
	LED_0	Mirror Enable	1	0	Mirror Enable Disabled
	GPIO_1	RGMII Clock Skew RX[2]	1	0	RGMII RX Clock Skew is set to 2ns
		RGMII Clock Skew RX[1]	1	0	
	GPIO_0	RGMII Clock Skew RX[0]	1	0	

2.16.2 CPSW Ethernet PHY2 Default Configuration

CPSW_RGMII2 port of the AM62x 17x17 SoC is connected to DP83867 whose configuration is as given below.

Table 2-14. CPSW Ethernet PHY–2 Strap values

Strap Setting	Pin Name	Strap Function	Mode	Value of Strap Function	Description
PHY Address	RX_D2	PHY_AD3	1	0	PHY Address: 0001
		PHY_AD2	1	0	
	RX_D0	PHY_AD1	2	0	
		PHY_AD0	2	1	
Auto Negotiation	RX_DV/ RX_CTRL	Auto- neg	3	0	Autoneg Disabled
Modes of Operation	LED2	RGMII Clock Skew TX[1]	5	0	RGMII TX Clock Skew is set to 0ns
		RGMII Clock Skew TX[0]	5	0	
	LED_1	RGMII Clock Skew TX[2]	5	1	
		ANEG_SEL	1	0	advertise ability of 10/100/1000
	LED_0	Mirror Enable	1	0	Mirror Enable Disabled
	GPIO_1	RGMII Clock Skew RX[2]	1	0	RGMII RX Clock Skew is set to 2ns
		RGMII Clock Skew RX[1]	1	0	
	GPIO_0	RGMII Clock Skew RX[0]	1	0	

The interrupts generated from two CPSW RGMII PHYs are tied together and is connected to EXTINTn pin of AM62x SoC.

LED_0is connected to RJ45 Right LED (Green) to indicate 1000MHz link (status).

LED_1is connected to RJ45 Left LED (Green) to indicate transmit/receive activity.

2.17 GPIO Port Expander

The I/O Expanders are used in the AM62x-Low Power SK EVM are a 24-Bit I2C based I/O Expander which is used for daughter card plug-in detection and for generating resets and enable signals to various peripheral devices connected to it. The SoC_I2C1 bus of the AM62X 17x17 SoC is used to interface with the I/O Expanders. The I2C device address of the I/O Expander is 0x21 and 0x23. See the tables below for the list of signals being controlled by the Expanders.

Table 2-15. IO Expander 1 Signal Details

IO EXPANDER - 01			
Pin no	SIGNAL	DIRECTION	DEVICE
P11	GPIO_EMMC_RSTN	OUTPUT	eMMC Reset control GPIO
P01	GPIO_CPSW1_RST	OUTPUT	CPSW Ethernet PHY-1 Reset Control GPIO
P00	GPIO_CPSW2_RST	OUTPUT	CPSW Ethernet PHY-2 Reset Control GPIO
P03	MMC1_SD_EN	OUTPUT	SD Card Load Switch Enable
P04	VPP_LDO_EN	OUTPUT	SOC eFuse Voltage(VPP=1.8V) Regulator Enable
P05	EXP_PS_3V3_EN	OUTPUT	EXP CONN 3.3V Power Switch Enable
P06	EXP_PS_5V0_EN	OUTPUT	EXP CONN 5V Power Switch Enable
P10	GPIO_AUD_RSTN	OUTPUT	Audio Codec Reset Control GPIO
P07	EXP_HAT_DETECT	INPUT	EXP CONN HAT Board Detection
P02	PRU_DETECT	INPUT	PRU Board Detection
P12	UART1_FET_BUF_EN	OUTPUT	SOC UART1 Mux Select
P13	BT_UART_WAKE_SOC	INPUT	BT UART WKUP Signal
P14	GPIO_HDMI_RSTN	OUTPUT	HDMI Transmitter Reset Control GPIO
P15	CSI_GPIO0	NA	Raspberry Pi Camera CSI0 GPIO1
P16	CSI_GPIO1	NA	Raspberry Pi Camera CSI0 GPIO2
P17	GPIO_OLDI_INT	INPUT	OLDI Interrupt
P20	HDMI_INTN	INPUT	HDMI Interrupt
P21	TEST_GPIO2	INPUT	TEST GPIO2 from Test Automation Connector
P22	MCASP1_FET_EN	OUTPUT	MCASP1 Enable and Direction Control
P23	MCASP1_BUF_BT_EN	OUTPUT	
P24	MCASP1_FET_SEL	OUTPUT	
P25	UART1_FET_SEL	OUTPUT	
P27	IO_EXP_TEST_LED	OUTPUT	User Test LED 2

Table 2-16. IO Expander 2 Signal Details

IO EXPANDER - 02			
Pin no	SIGNAL	DIRECTION	DEVICE
P20	SPI0_FET_SEL	OUTPUT	SoC SPI0 MUX Selection
P21	SPI0_FET_OE	OUTPUT	SoC SPI0 MUX Enable

Table 2-16. IO Expander 2 Signal Details (continued)

IO EXPANDER - 02			
Pin no	SIGNAL	DIRECTION	DEVICE
P22	GPIO_OLDI_RSTn	OUTPUT	OLDI Reset
P23	PRU_3V3_EN	OUTPUT	PRU Power Switch Enable
P26	CSI_VLDO_SEL	OUTPUT	CSI Regulator Enable (VCC_CSI_IO)
P27	SOC_WLAN_SDIO_RST	OUTPUT	WLAN Reset control GPIO
P10	WL_LT_EN	OUTPUT	Wilink Enable
P11	CSI_RSTZ	OUTPUT	CSI Reset control GPIO

2.18 GPIO Mapping

The table below describes the detailed GPIO mapping of AM62x 17x17 SoC with AM62x-Low Power SK EVM peripherals

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	FUNCTIONALITY	GPIO USED	PACKAGE SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE CONNECTED ON SKEVM
1	Enable for WLAN Interface	WLAN_EN	ENABLE	GPIO0_71	MMC2_SD0P	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	WLAN_IRQ	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	Enable for BT Interface	BT_EN_SOC	ENABLE	MCU_GPIO0_0	MCU_SPI0_C50	OUTPUT	LOW	HIGH	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn/PRU_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_C5n1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	MCU Header GPIO0_16	MCU_GPIO0_16	GPIO	MCU_GPIO0_16	MCU_MCAN1_RX	NA	NA	NA	VDDSHV_CANUART	SoC_DVDD3V3
7	MCU Header GPIO0_15	MCU_GPIO0_15	GPIO	MCU_GPIO0_15	MCU_MCAN1_TX	NA	NA	NA	VDDSHV_CANUART	SoC_DVDD3V3
8	PMIC Interrupt	PMIC_INT_B	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV3	SoC_DVDD3V3
9	IO Expander Interrupt									
10	TEST GPIO2 from Test Automation Connector/ User Interrupt Push Button		INTERRUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	SoC_DVDD3V3
11	User Test LED 1	SOC_GPIO1_49	GPIO	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
12	CAN_FD_WKUP_SW signal from switch	ETH_CAN_INH_SOC	INTERRUPT	MCU_GPIO0_19	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_MCU	SoC_DVDD3V3
13	CAN_FD_WKUP_HDR_INH signal from header	EXP_GPIO1_22	GPIO	GPIO1_22	UART0_CTSn	NA	NA	NA	VDDSHV0	SoC_DVDD3V3
14	User EXP Conn GPIO									
15	IO Expander Interrupt	GPIO1_23_INTn	INTERRUPT	GPIO1_23	UART0_RTSn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
16	User Interrupt									
17	User EXP Conn GPIO	EXP_GPIO0_14_LT	GPIO	GPIO0_14	OSPI0_C5n1	NA	NA	NA	VDDSHV1	SoC_DVDD1V8
18	PMIC Standby Enable	PMIC_STBY	ENABLE	MCU_GPIO0_22	PMIC_LPM_END	OUTPUT	HIGH	HIGH	VDDSHV_CANUART	SoC_DVDD3V3
19	User EXP Conn GPIO	EXP_EHRPWM1_B	GPIO	GPIO1_10	MCASP0_AXR0	NA	NA	NA	VDDSHV0	SoC_DVDD3V3
IO EXPANDER - 01										
1	eMMC Reset control GPIO	GPIO_EMMC_RSTN	RESET	IO EXPANDER-P11		OUTPUT	HIGH	LOW		VCC_3V3_SYS
2	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER-P01		OUTPUT	HIGH	LOW		VCC_3V3_SYS
3	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER-P00		OUTPUT	HIGH	LOW		VCC_3V3_SYS
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER-P03		OUTPUT	HIGH	LOW		VCC_3V3_SYS
5	SOC eFuse Voltage(VP=1.8V) Regulator Enable	VPP_LDO_EN	ENABLE	IO EXPANDER-P04		OUTPUT	LOW	HIGH		VCC_3V3_SYS
6	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER-P05		OUTPUT	LOW	HIGH		VCC_3V3_SYS
7	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER-P06		OUTPUT	LOW	HIGH		VCC_3V3_SYS
8	Audio Codec Reset Control GPIO	GPIO_AUD_RSTN	RESET	IO EXPANDER-P10		OUTPUT	HIGH	LOW		VCC_3V3_SYS
9	EXP CONN HAT Board Detection	EXP_HAT_DETECT	DETECTION	IO EXPANDER-P07		INPUT	HIGH	LOW		VCC_3V3_SYS
10	PRU Board Detection	PRU_DETECT	DETECTION	IO EXPANDER-P02		INPUT	HIGH	LOW		VCC_3V3_SYS
11	SOC UART1 Mux Select	UART1_FET_BUF_EN	SELECT	IO EXPANDER-P12		OUTPUT	HIGH	LOW		VCC_3V3_SYS
12	BT UART WKUP Signal	BT_UART_WAKE_SOC	INTERRUPT	IO EXPANDER-P13		INPUT	HIGH	LOW		VCC_3V3_SYS
13	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTN	RESET	IO EXPANDER-P14		OUTPUT	HIGH	LOW		VCC_3V3_SYS
14	Raspberry Pi Camera CSIO GPIO1	CSI_GPIO0	INPUT/OUTPUT	IO EXPANDER-P15		NA	NA	NA		VCC_3V3_SYS
15	Raspberry Pi Camera CSIO GPIO2	CSI_GPIO1	INPUT/OUTPUT	IO EXPANDER-P16		NA	NA	NA		VCC_3V3_SYS
16	OLDI Interrupt	GPIO_OLDI_INT	INTERRUPT	IO EXPANDER-P17		INPUT	HIGH	LOW		VCC_3V3_SYS
17	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER-P20		INPUT	HIGH	LOW		VCC_3V3_SYS
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO	IO EXPANDER-P21		INPUT	HIGH	LOW		VCC_3V3_SYS
19	MCASP1 Enable and Direction Control	MCASP1_FET_EN	ENABLE	IO EXPANDER-P22		OUTPUT	LOW	LOW		VCC_3V3_SYS
20		MCASP1_BUF_BT_EN	ENABLE	IO EXPANDER-P23		OUTPUT	LOW	HIGH		VCC_3V3_SYS
21		MCASP1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P24		OUTPUT	HIGH	LOW		VCC_3V3_SYS
22		UART1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P25		OUTPUT	HIGH	LOW		VCC_3V3_SYS
23	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER-P27		OUTPUT	LOW	HIGH		VCC_3V3_SYS
IO EXPANDER - 02										
1	SoC SPI0 MUX Selection	SPI0_FET_SEL	ENABLE	IO EXPANDER-P20		OUTPUT	LOW	HIGH		VCC_3V3_SYS
2	SoC SPI0 MUX Enable	SPI0_FET_OE	CONTROL	IO EXPANDER-P21		OUTPUT	LOW	LOW		VCC_3V3_SYS
3	OLDI Reset	GPIO_OLDI_RSTn	RESET	IO EXPANDER-P22		OUTPUT	HIGH	LOW		VCC_3V3_SYS
4	PRU Power Switch Enable	PRU_3V3_EN	ENABLE	IO EXPANDER-P23		OUTPUT	LOW	HIGH		VCC_3V3_SYS
5	CSI Regulator Enable (VCC_CSI_IO)	CSI_VLDO_SEL	ENABLE	IO EXPANDER-P26		OUTPUT	LOW	HIGH		VCC_3V3_SYS
6	WLAN Reset control GPIO	SOC_WLAN_SDIO_RST	RESET	IO EXPANDER-P27		OUTPUT	HIGH	LOW		VCC_3V3_SYS
7	Wilink Enable	WL_LT_EN	ENABLE	IO EXPANDER-P10		OUTPUT	LOW	HIGH		VCC_3V3_SYS
8	CSI Reset control GPIO	CSI_RSTZ	RESET	IO EXPANDER-P11		OUTPUT	LOW	HIGH		VCC_3V3_SYS

2.19 AM62x-Low Power SK EVM User Setup and Configuration

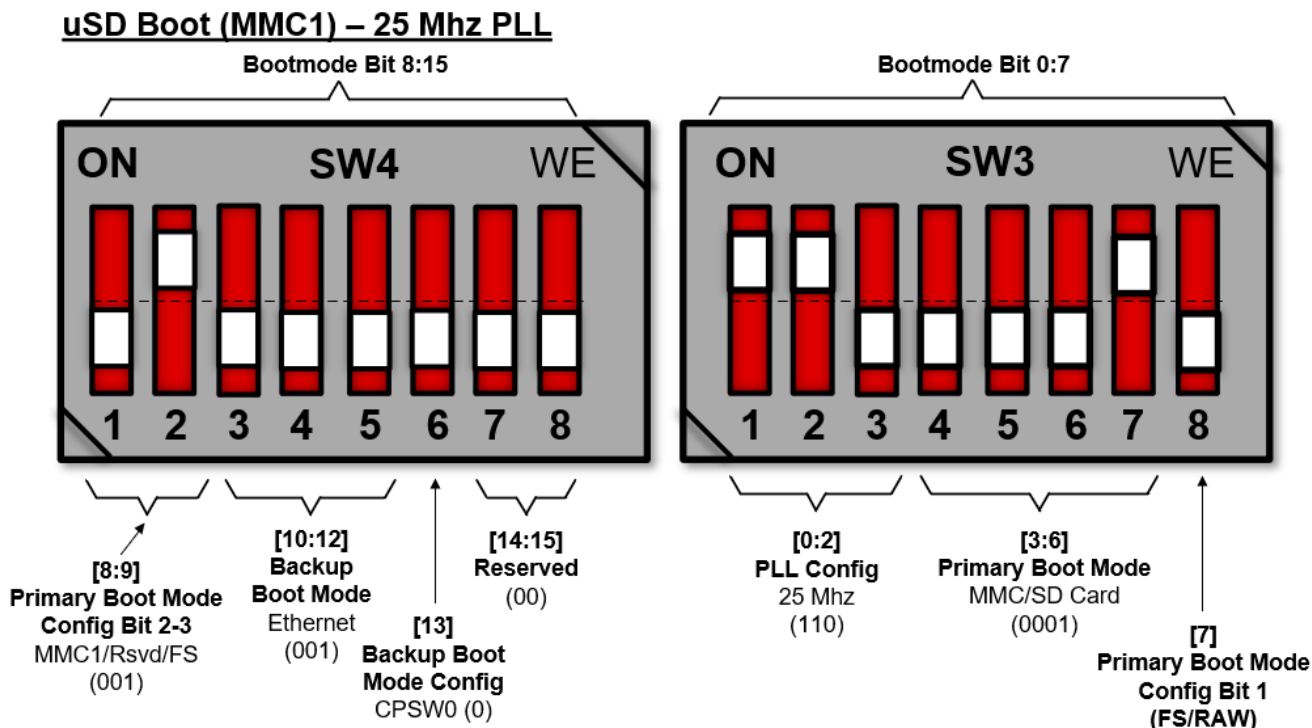
2.19.1 EVM DIP Switches

AM62x-Low Power SK EVM has two 8 - position DIP Switch to set the SoC Boot mode and related parameters.

2.19.2 Boot Modes

The boot mode for the AM62x-Low power SK EVM board is defined by two banks of switches SW3 and SW4 or by the I2C buffer connected to the Test automation connector. This allows for AM62x SoC Boot mode control by either the user (DIP Switch Control) or by the Test Automation connector.

All the bits of switch (SW3 & SW4) have weak pull down resistor and a strong pull up resistor as shown in below picture. Note that OFF setting provides a low logic level ('0') and an ON setting provides a high logic level ('1').



The boot mode pins of the SoC have associated alternate functions during normal operation. Hence isolation is provided using Buffer IC's to cater for alternate pin functionality. The output of the buffer is connected to the bootmode pins on the AM62x Low Power SK EVM. The output is enabled when the bootmode is needed during a reset cycle.

The input to the buffer is connected to the DIP switch circuit and to the output of an I2C buffer set by the test automation circuit. If the test automation circuit is going to control the bootmode, all the switches will manually be set to the OFF position. The bootmode buffer should be powered by an always ON power supply to ensure that the bootmode remains present even if the SoC power is cycled.

Switch SW1 and SW2 bits [15:0] are used to set the SoC Boot mode.

The switch map to the boot mode functions is provided in the tables below.

Figure 2-25. Boot Mode Switch Example

Table 2-17. Boot Mode Pin Mapping

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Backup Boot Mode Configuration	Backup Boot Mode			Primary Boot Mode Configuration			Primary Boot Mode			PLL Configuration			

BOOT-MODE[0:2] – Denote system clock frequency for PLL configuration. By default this bits are set for 25MHz.

Table 2-18. PLL Reference Clock Selection

SW3.3	SW3.2	SW3.1	PLL REF CLK (MHz)
OFF	OFF	OFF	RSVD
OFF	OFF	ON	RSVD
OFF	ON	OFF	24
OFF	ON	ON	25

Table 2-18. PLL Reference Clock Selection (continued)

SW3.3	SW3.2	SW3.1	PLL REF CLK (MHz)
ON	OFF	OFF	26
ON	OFF	ON	RSVD
ON	ON	OFF	RSVD
ON	ON	ON	RSVD

BOOT-MODE [3:6] – This provides primary boot mode configuration to select the requested boot mode after POR, that is, the peripheral/memory to boot from primary boot device selection details.

Table 2-19. Boot Device Selection BOOT-MODE [6:3]

SW3.7	SW3.6	SW3.5	SW3.4	Primary Boot Device Selected
OFF	OFF	OFF	OFF	Serial NAND
OFF	OFF	OFF	ON	OSPI
OFF	OFF	ON	OFF	QSPI
OFF	OFF	ON	ON	SPI
OFF	ON	OFF	OFF	Ethernet RGMII1
OFF	ON	OFF	ON	Ethernet RMII1
OFF	ON	ON	OFF	I2C
OFF	ON	ON	ON	UART
ON	OFF	OFF	OFF	MMC/SD card
ON	OFF	OFF	ON	eMMC
ON	OFF	ON	OFF	USB0
ON	OFF	ON	ON	GPMC NAND
ON	ON	OFF	OFF	GPMC NOR
ON	ON	OFF	ON	Rsvd
ON	ON	ON	OFF	xSPI
ON	ON	ON	ON	No boot/Dev Boot

- BOOT-MODE [10:12] – Select the backup boot mode, used when the primary boot mode is not available.

Table 2-20. Backup Boot Mode Selection BOOT-MODE [12:10]

SW4.5	SW4.4	SW4.3	Backup Boot Device Selected
OFF	OFF	OFF	None (No backup mode)
OFF	OFF	ON	USB
OFF	ON	OFF	Reserved
OFF	ON	ON	UART
ON	OFF	OFF	Ethernet
ON	OFF	ON	MMC/SD
ON	ON	OFF	SPI
ON	ON	ON	I2C

BOOT-MODE [9:7] – These pins provide optional settings and are used in conjunction with the primary boot device selected.

Table 2-21. Primary Boot Media Configuration BOOT-MODE[9:7]

SW4.2	SW4.1	SW3.8	Boot Device
Reserved	Read Mode 2	Read Mode 1	Serial NAND
Reserved	Iclk	Csel	QSPI
Speed	Iclk	Csel	OSPI
Reserved	Mode	Csel	SPI

Table 2-21. Primary Boot Media Configuration BOOT-MODE[9:7] (continued)

SW4.2	SW4.1	SW3.8	Boot Device
Clkout	0	Link stat	Ethernet RGMII
Clkout	Clk src	0	Ethernet RMII
Bus Reset	Reserved	Addr	I2C
Reserved	Reserved	Reserved	UART
Port	Reserved	Fs/raw	MMC/ SD card
Reserved	Reserved	Reserved	eMMC
Core Volt	Mode	Lane swap	USB0
Reserved	Reserved	Reserved	GPMC NAND
Reserved	Reserved	Reserved	GPMC NOR
Reserved	Reserved	Reserved	Reserved
SFDP	Read Cmd	Mode	xSPI
Reserved	ARM/Thumb	No/Dev	No boot/Dev Boot

BOOT-MODE[13] – These pins provide optional settings and are used in conjunction with the backup boot device devices. Switch SW4.6 when ON sets 1 and sets 0 if OFF, see the device-specific TRM.

BOOT-MODE [14:15] – Reserved. Provides backup boot media configuration options.

Table 2-22. Backup Boot Media Configuration BOOT-MODE[13]

SW4.6	Boot Device
Reserved	None
Mode	USB
Reserved	Reserved
Reserved	UART
IF	Ethernet
Port	MMC/SD
Reserved	SPI
Reserved	I2C

Table 2-23. Serial NAND Configuration Fields

BOOTMODE Pins	Field	Value	Description
8 [SW5.1]	Read Mode 2	0	Reserved (Read mode is taken from Read Mode 1)
		1	SPI/ 1-1-1 mode (Read mode is taken from Read Mode 2 and Read Mode 1 is ignored)
7 [SW3.8]	Read Mode 1	0	OSPI/ 1-1-8 Mode (valid only when Read Mode 2 is 0)
		1	OSPI/ 1-1-4 Mode (valid only when Read Mode 2 is 0)

Table 2-24. OSPI Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
8 [SW5.1]	Iclk	0	Iclock source external
		1	Iclock source internal (pad loopback)
7 [SW3.8]	Csel	0	Boot Flash is on CS 0
		1	Boot Flash is on CS 1

Table 2-25. QSPI Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
8 [SW5.1]	Iclk	0	Iclock source external
		1	Iclock source internal (pad loopback)
7 [SW3.8]	Csel	0	Boot Flash is on CS 0
		1	Boot Flash is on CS 1

Table 2-26. SPI Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
8 [SW4.1]	Mode	0	SPI Mode 0
		1	SPI Mode 3
7 [SW3.8]	Csel	0	Boot Flash is on CS 0
		1	Boot Flash is on CS 1

Table 2-27. Ethernet RGMII Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9 [SW4.2]	Clkout	0	25MHz clock not generated on CLKOUT0
		1	25MHz clock generated on CLKOUT0
8 [SW4.1]	Delay	0	Must be set to 0 for RGMII with internal Tx delay
		1	Reserved
7 [SW3.8]	Link info	0	MDIO PHY scan used for link parameters
		1	Link parameters programmed by the ROM

Table 2-28. Ethernet RMII Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9 [SW4.2]	Clkout	0	50MHz clock not generated on CLKOUT0
		1	50MHz clock generated on CLKOUT0
8 [SW4.1]	Clk src	0	External clock source for RMII1_REF_CLK
		1	Internal clock source for RMII1_REF_CLK
7 [SW3.8]	RMII	0	This bit must be set to 0
		1	Reserved

Table 2-29. Ethernet RMII Clocking

BOOTMODE Pin 9 (Clk out)	BOOTMODE Pin 8 (Clk src)	Description
0	0	50MHz external source to RMII_REF_CLK and to external Ethernet PHY input clock (CLKOUT0 is unused) These are the recommended settings
0	1	Not a valid configuration
1	0	CLKOUT0 is configured to 50MHz and connect to both RMII1_REF_CLK and to external Ethernet PHY input clock
1	1	Not a valid configuration

Table 2-30. Ethernet Backup Boot Configuration Field

BOOTMODE Pins	Field	Value	Description
13 [SW4.2]	Interface	0	RGMII with internal TX delay
		1	RMII with external clock source

Table 2-31. I2C Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9 [SW4.2]	Bus reset	0	Hung bus reset attempt after 1ms
		1	No hung bus reset attempted
7 [SW3.8]	Address	0	EEPROM's address is 0x50
		1	EEPROM's address is 0x51

Table 2-32. SD Card Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9 [SW4.2]	Port	0	Reserved
13 ⁽¹⁾ [SW4.2]		1	MMC Port 1 (4 bit width). This bit must be set to 1

Table 2-32. SD Card Boot Configuration Fields (continued)

BOOTMODE Pins	Field	Value	Description
7 [SW3.8]	FS/Raw	0	Filesystem mode
		1	Raw Mode

(1) When MMCSD is the backup mode

Table 2-33. eMMC Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9 [SW4.2]	Port	0	MMCSD Port 0 (8 bit width). This bit must be set to 0
13 ⁽¹⁾ [SW4.2]		1	Reserved
7 [SW3.8]	FS/Raw	0	Filesystem mode
		1	Raw Mode

(1) When MMCSD is the backup mode

Table 2-34. USB Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9 [SW4.2]	Core Voltage	0	0.85V core voltage
		1	0.75V core voltage
8 [SW4.1]	Mode	0	DFU (USB device firmware upgrade)
13 ⁽¹⁾ [SW4.2]		1	Host (MSC boot)
7 [SW3.8]	Lane Swap	0	D+/D- lines are not swapped
		1	D+/D- lines are swapped

(1) When USB is the backup mode.

Table 2-35. xSPI Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9 [SW4.2]	SFDP	0	SFDP disabled
		1	SFDP enabled
8 [SW4.1]	Read cmd	0	0x0B Read Command
		1	0xEE Read Command
7 [SW3.8]	Mode	0	1S-1S-1S mode @ 50MHz
		1	8D-8D-8D mode @ 25MHz

2.19.3 User Test LEDs

The AM62x-Low Power SK EVM contains two LEDs for user defined functions.

The table below indicates the User test LEDs and the associated GPIOs used to control it.

Table 2-36. User Test LEDs

SI #	LED	GPIO used	SCH Net Names
1	LD3	GPIO1_49	SOC_GPIO1_49
2	LD7	U70.24(P27)	IO_EXP_TEST_LED

2.20 Expansion Headers

The AM62x-Low Power SK EVM features three expansion headers: the 40 pin User expansion connector, 20 pin PRU Header and the 28 pin MCU Header.

2.20.1 User Expansion Connector

The AM62x-Low Power SK EVM supports RPi expansion interface using a 40-pin User expansion connector Mfr. Part# PEC20DAAN. Four mounting holes must be oriented with the connector to allow for connection of these boards.

The following interfaces and IOs are included on to the 40 pin User Expansion connector.

- 2x SPI : SPI0 with 2 CS and SPI2 with 3 CS
- 2x I2C: SoC_I2C0 and SoC_I2C2
- 1x UART: UART5
- 2x PWM: EHRPWM0_A, EHRPWM1_B1xCLK: CLKOUT0
- 10x GPIO: GPIOs from main domain
- 5V and 3.3V supply (current limited to 155mA and 500mA)

Each of the power supplies 5V and 3.3V are current limited to 155mA and 500mA respectively. This is achieved by using two individual load switches TPS22902YFPR and TPS22946YZPR. The Enable signals for the load switches is driven via I2C based GPIO Port expander.

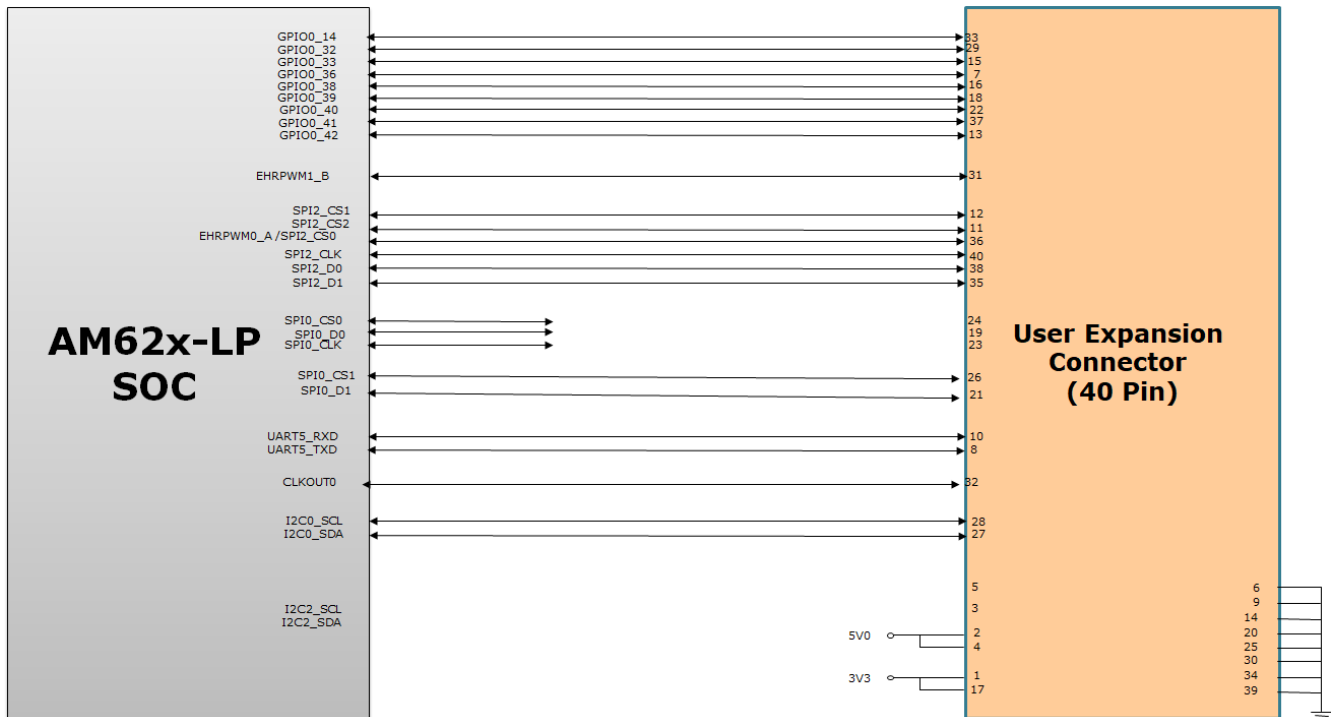


Table 2-37. 40 Pin User Expansion Connector (J3)

Pin No.	SoC Ball	Net name	Comments
1	-	VCC3V3_EXP	
2	-	VCC5V0_EXP	
3	H19	EXP_I2C2_SDA	I2C SW
4	-	VCC5V0_EXP	
5	H18	EXP_I2C2_SCL	I2C SW
6	-	DGND	
7	C14	EXP_CLKOUT0	
8	A15	EXP_UART5_TXD	
9	-	DGND	
10	B13	EXP_UART5_RXD	
11	C17	EXP_SPI2_CS1	
12	D15	EXP_SPI2_CS0/EHRPWM0_A	MUX
13	H17	EXP_GPIO0_42	
14	-	DGND	
15	-	EXP_GPIO0_22	
16	P17	EXP_GPIO0_38	
17	-	VCC3V3_EXP	

Table 2-37. 40 Pin User Expansion Connector (J3) (continued)

Pin No.	SoC Ball	Net name	Comments
18	J20	EXP_GPIO0_39	
19	C12	EXP_SPI0_D0	
20	-	DGND	
21	A14	EXP_SPI0_D1	
22	E18	EXP_GPIO0_14	
23	D12	EXP_SPI0_CLK	
24	C11	EXP_SPI0_CS0	
25	-	DGND	
26	D13	EXP_SPI0_CS1	
27	D14	SoC_I2C0_SDA	
28	E12	SoC_I2C0_SCL	
29	K18	EXP_GPIO0_36	
30	K20	EXP_GPIO0_32	
31	K21	EXP_GPIO0_33	
32	J19	EXP_GPIO0_40/ PR0_ECAPH0_IN_APWM_OUT	
33	D18	EXP_EHRPWM1_B	
34	-	DGND	
35	B17	EXP_SPI2_D1/ ECAP2_IN_APWM_OUT	MUX
36	A18	EXP_SPI2_CS2	
37	J18	EXP_GPIO0_41	
38	B18	EXP_SPI2_D0	MUX
39	-	EXP_HAT_DETECT	
40	D16	EXP_SPI2_CLK	MUX

2.20.2 MCU Connector

The AM62x-Low Power SK EVM has a 14x2 standard 0.1 spaced MCU connector which includes signals connected to the MCU Domain of SoC. 13 Signals include MCU_I2C0, MCU_UART0 (with flow control), MCU_SPI0 and MCU_MCAN0 signals are connected to the MCU Header. Additional control signals provided on the Header include CONN_MCU_RESETz, CONN_MCU_PORz, MCU_RESETSTATz, MCU_SAFETY_ERRORn, 3.3V IO and GND. MCU_UART0 signals from AM62x SoC are connected to both MCU Header and FT4232 Bridge through MUX Mfr Part # SN74CB3Q3257PWR. The MCU Header does not include the Board ID memory interface. Allowed current limit is 100mA on 3.3V rail.

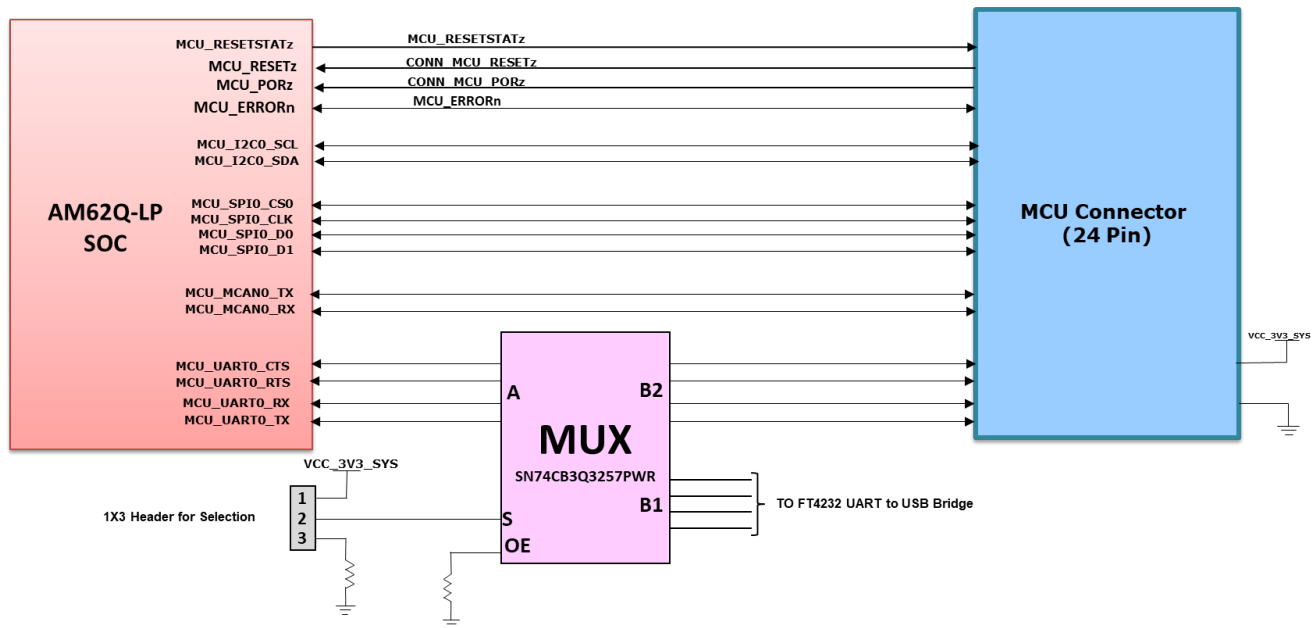


Figure 2-26. MCU Connector Interface

Table 2-38. MCU Connector (J10) Pinout

Pin No.	SoCBall No.	Netname
1	-	VCC_3V3_SYS
2	-	DGND
3	-	DGND
4	D8	MCU_SPI0_D1
5	-	CAN_FD_WKUP_HDR_INH
6	E8	MCU_SPI0_D0
7	-	DGND
8	C8	MCU_SPI0_CS1
9	-	DGND
10	D5	MCU_GPIO0_15
11	D6	MCU_GPIO0_16
12	B8	MCU_UART0_CTS_CONN
13	A8	MCU_UART0_RXD_CONN
14	-	DGND
15	-	DGND
16	C5	MCU_MCAN0_TX
17	D7	MCU_UART0_RTS_CONN
18	B7	MCU_SPI0_CLK
19	B6	MCU_UART0_TXD_CONN
20	-	DGND
21	A10	MCU_I2C0_SDA
22	C4	MCU_MCAN0_RX
23	A12	MCU_RESETSTATz
24	B9	MCU_I2C0_SCL
25	-	CONN_MCU_RESETh
26	-	MCU_SAFETY_ERRORz_3V3
27	-	DGND

Table 2-38. MCU Connector (J10) Pinout (continued)

Pin No.	SoC Ball No.	Netname
28	-	CONN_MCU_PORz

2.20.3 PRU Connector

The AM62x-Low Power SK EVM has a 20 pin PRU Header which offers a low speed connection to the PRG0 Interface using a connector Mfr Part # PREC010DAAN-RC. The connector features PR0_PRU0_GPO [0: 7], SoC_I2C0, +3.3V PRU_ICSSG signals from PRG0 Port (PRG0_PRU0) are connected to a 10x2 standard 0.1" spaced Receptacle PWR and Ground reference. INTn signal from PRU Header is wired along with the CPSW PHY interrupts and connected to the EXTINTn pin of the SoC.

The 3.3V supply is current limited to 500mA. This is achieved by using load switch TPS22902YFPR. Enable for the load switch is controlled by IO expander. Signals routed from the PRU Connector are listed in [Table 2-39](#).

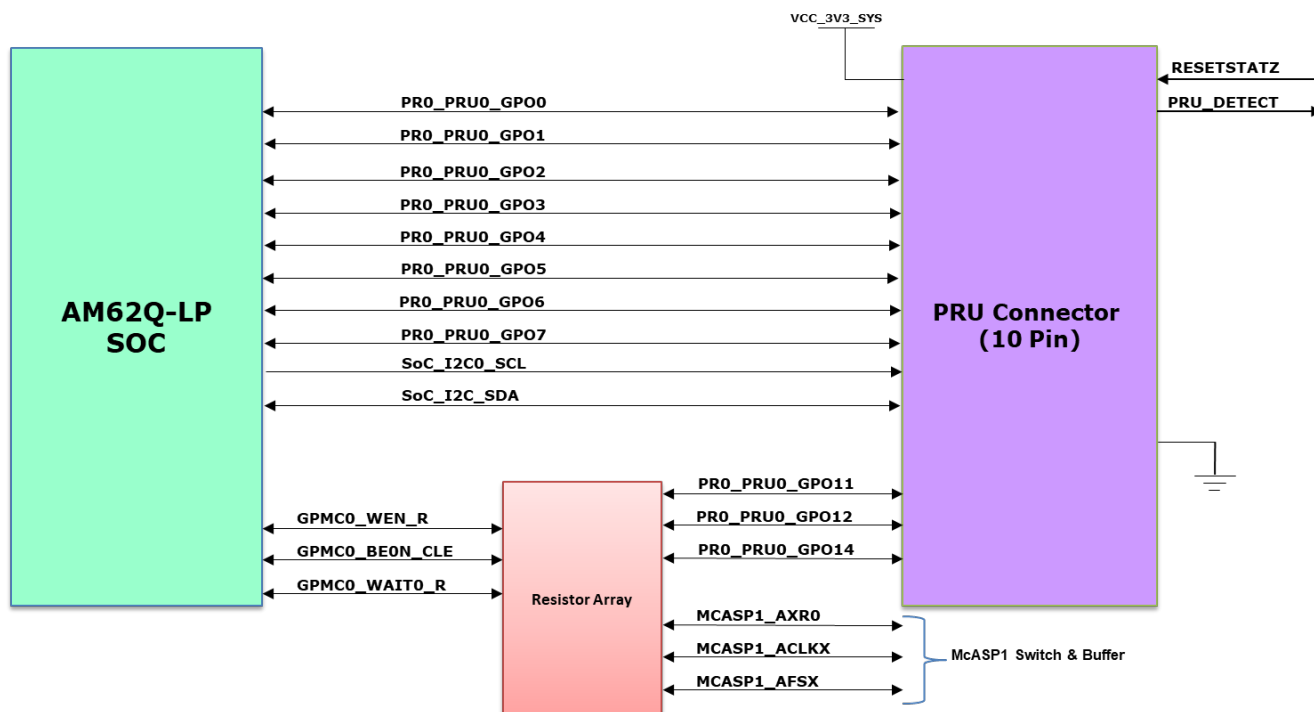


Figure 2-27. PRU Connector Interface

Table 2-39. PRU Header (J11) Pinout

Pin No.	SoC Ball No.	Net name
1	-	VCC3V3_PRU
2	-	DGND
3	-	PRU_DETECT
4	-	PRU_RESETz
5	B16	PRU_INTn
6	E12	SoC_I2C0_SCL
7	J17	PR0_PRU0_GPO11
8	D14	SoC_I2C0_SDA
9	P21	PR0_PRU0_GPO12
10	-	NC
11	K17	PR0_PRU0_GPO14
12	-	NC
13	K19	PR0_PRU0_GPO0

Table 2-39. PRU Header (J11) Pinout (continued)

Pin No.	SoC Ball No.	Net name
14	L19	PR0_PRU0_GPO1
15	L20	PR0_PRU0_GPO2
16	L21	PR0_PRU0_GPO3
17	M21	PR0_PRU0_GPO4
18	L17	PR0_PRU0_GPO5
19	L18	PR0_PRU0_GPO6
20	M20	PR0_PRU0_GPO7

2.21 Push Buttons

AM62x-Low Power SK EVM supports two interrupts for providing Reset input and User Interrupt to the processor. The interrupts are push buttons placed on the Top side of the Board and are listed in the table below.

Table 2-40. EVM Push Buttons

SI #	Push Buttons	Signal	Function
1	SW5	SoC_WARM_RESETZ	Main domain Warm Reset input
2	SW6	GPIO_MCU	Generates interrupt on MCU_GPIO0_15

2.22 I2C Address Mapping

There are three I2C interfaces used in AM62x-Low Power SK EVM board.

- SoC_I2C0 Interface: SoC I2C [0] is connected to Board ID EEPROM, User Expansion Connector Header, USB PD controller, PRU header, PMIC and OLDI Display Touch interface.
- SOC I2C1 Interface: SoC I2C [1] is connected to Test Automation Header, Current Monitors, Temperature Sensors, Audio Codec, HDMI Transmitter, , GPIO Port Expander.
- SOC I2C2 Interface: Soc I2C [2] is Connected to the User Expansion Connector Header and CSI Camera Connector.
- MCU I2C0 Interface: MCU I2C [0] is Connected to MCU Header.

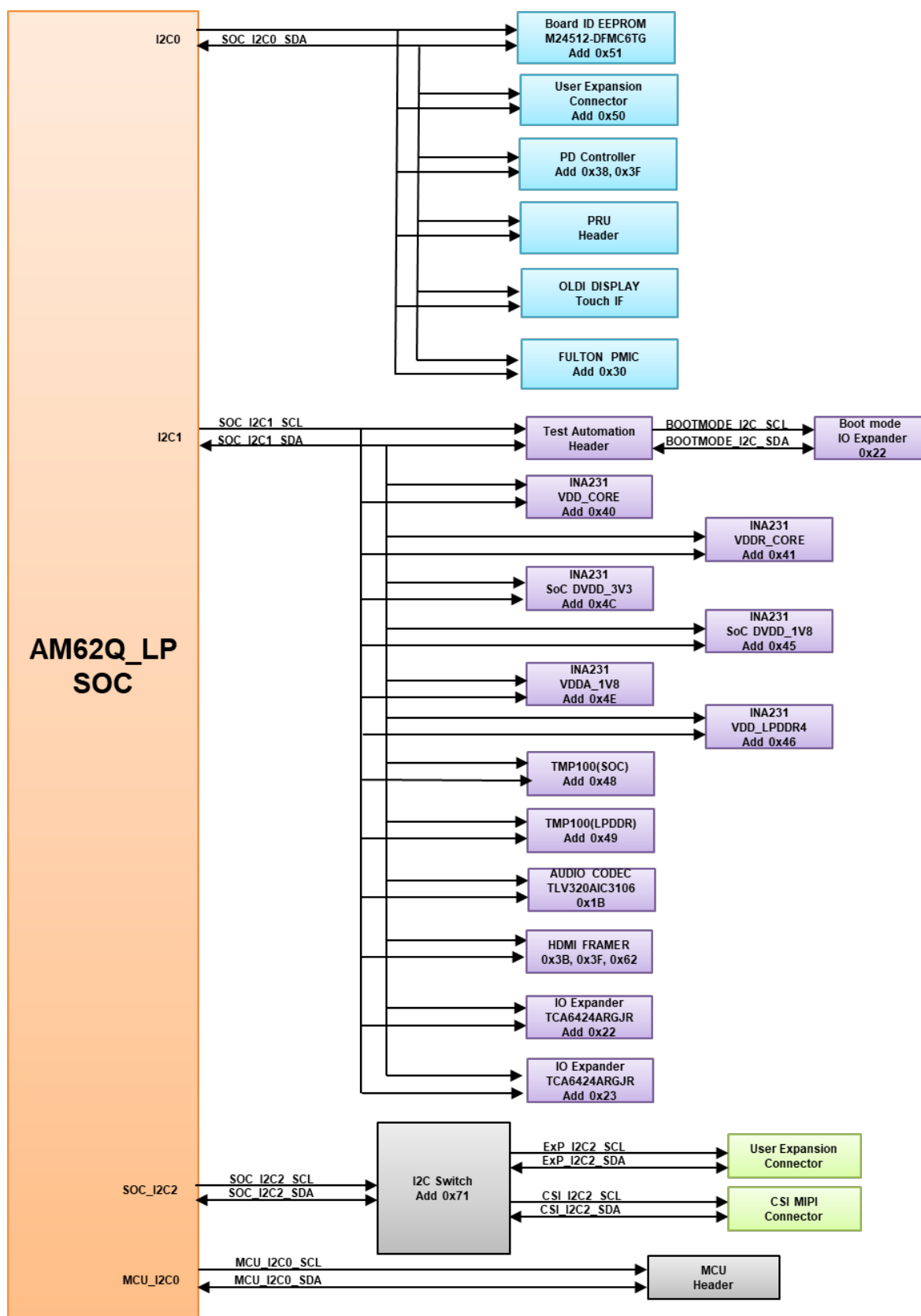


Figure 2-28. I2C Interface Block Diagram

Table 2-41. I2C Mapping Table

I2C Port	Device/Function	Part#	I2C Address
SoC_I2C0	Board ID EEPROM	M24512-DFMC6TG	0x51
SoC_I2C0	User Expansion Connector	<connector interface>	
SoC_I2C0	USB PD Controller	TPS65988DHRSHR	0x38, 0x3F
SoC_I2C0	PRU Header	<connector interface>	
SoC_I2C0	OLDI Display Touch Interface	<connector interface>	
SoC_I2C1	PMIC	TPS65219	0x30
SoC_I2C1	Test Automation Header	<connector interface>	
SoC_I2C1	Current Monitors	INA231AIYFDR	0x40, 0x41, 0x4C, 0x45, 0x4E & 0x46
SoC_I2C1	Temperature Sensors	TMP100NA/3K	0x48, 0x49
SoC_I2C1	Audio Codec	TLV320AIC3106IRGZT	0x1B
SoC_I2C1	HDMI Transmitter	SiI9022ACNU	0x3B, 0x3F, 0x62
SoC_I2C1	GPIO Port Expander	TCA6424ARGJR	0x22, 0x23
SoC_I2C2	CSI Camera Connector	<connector interface>	
SoC_I2C2	User Expansion Connector	<connector interface>	
MCU_I2C0	MCU Header	<connector interface>	
Others			
BOOTMODE_I2C	I2C Bootmode Buffer	TCA6424ARGJR	0x22
BOOTMODE_I2C	Test Automation Header	<connector interface>	

3 Hardware Design Files

The hardware design files such as schematics, BOM, PCB Layout, Assembly Files and Gerber files are available in the link below.

[Design Files](#)

4 Compliance Information

4.1 EMC, EMI and ESD Compliance

Components installed on the product are sensitive to Electric Static Discharge (ESD). It is recommended this product be used in an ESD controlled environment. This can include a temperature and/or humidity controlled environment to limit the buildup of ESD. It is also recommended to use ESD protection such as wrist straps and ESD mats when interfacing with the product.

The product is used in the basic electromagnetic environment as in laboratory conditions, and the applied standard is as per EN IEC 61326-1:2021.

5 Additional Information

5.1 Known Issues and Modifications

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6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from June 30, 2023 to November 30, 2025 (from Revision * (June 2023) to Revision A (November 2025))

Page

- | | |
|--|---|
| • Updated to new Evaluation Model User Guide standard..... | 1 |
| • Added HDMI Compliance and Trademark disclaimers..... | 1 |

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CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

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This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

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Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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<https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html>

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