*Application Note*

# *DP83TD510E Troubleshooting Guide*

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**ABSTRACT**

This guide provides a systematic approach to troubleshooting DP83TD510E with a focus on identifying and resolving issues commonly not countered during development, validation and deployment. The document covers key areas such as schematic and layout best practices, component selection and verification, and signal integrity on both the MDI and MAC interfaces. By combining practical measurements, test mode usage, and several diagnostic techniques, the guide helps engineers gain a deeper understanding of the DP83TD510E and accelerates root cause analysis.

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# 1 Introduction

DP83TD510E is a physical-layer transceiver compliant to IEEE 802.3cg 10Base-T1L specification. The PHY uses low noise coupled signal processing receiver architecture to offer longer cable reach along with ultra-low power consumption. The device supports both 2.4V p2p and 1V p2p voltage modes as defined by IEEE 802.3cg 10Base-T1L specifications. DP83TD510E supports direct connection to several Media Access Controller (MAC) interfaces (MII, RMII, RGMII, and low power RMII). The device also supports back-to-back RMII mode and RGMII in non-managed mode to provide range extension and repeater functionality.

Figure 1-1 shows a high-level overview of a typical media conversion application (SPE ↔ RJ-45) with DP83TD510E:

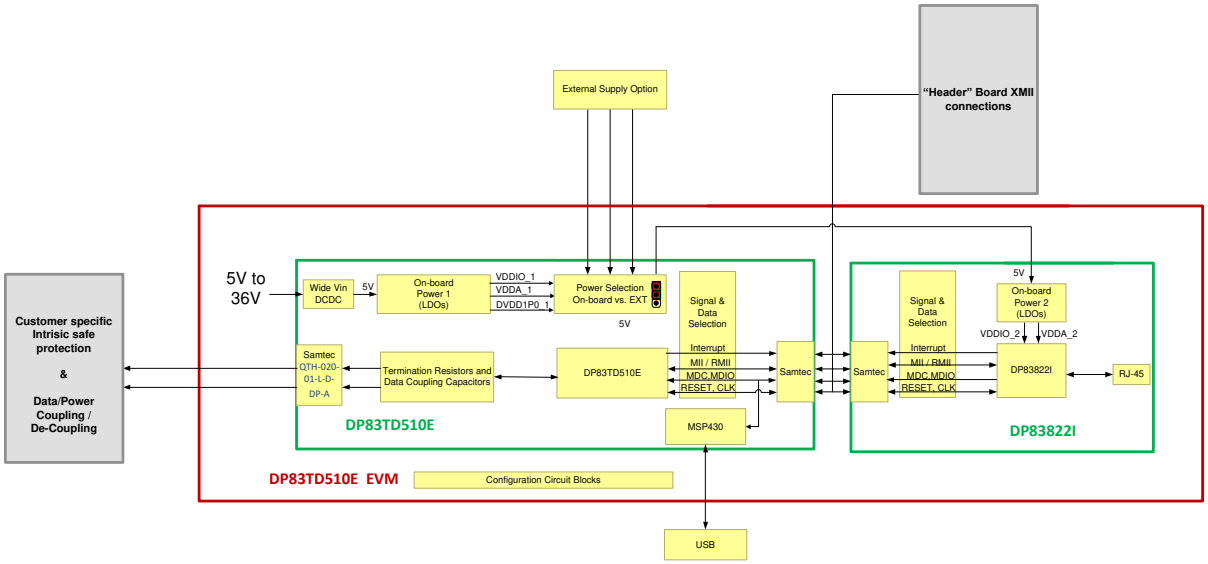


**Figure 1-1. DP83TD510E-EVM Block Diagram**



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# 2 Troubleshooting the Application

The following sections approach debugging the application from a high level, starting with application characteristics that have a broad impact before zeroing in on more focused aspects of the design.

This application note is laid out in three major sections:

- Device Health Checks
- MDI Health Checks
- MII Health Checks

Depending on the particular behavior observed, all three of these sections are possibly not needed. Because of this, certain sections can be skipped if the correct behavior is observed. The comment is mentioned at the start of each section, as well as given in the following.

Device Health Checks section can be skipped if the device

- Linking up (Status read through register 0x0010) when connected to link partner OR showing NLP signals when Ethernet cable is unconnected
- Responding as expected to register access

MDI Health Checks section can be skipped if the device

- Linked up AND reporting no packet errors via register 0x0015 when sending traffic through the device

There are several register settings discussed in this app note. For ease of access, we have included some debug scripts in this application note. These can be used with the tool USB-2-MDIO to reprogram the DP83TD510E into different modes. A collection of all the scripts mentioned here, and more, can also be found on the product page.

## 2.1 Schematic and Layout Checklist

When reviewing the schematic and layout, make sure that the design follows the recommended reference guidelines listed in the Schematic and Layout Checklists respectively. This is important to verify various design choices that, if not adhering to the listed requirements, can result in unusual PHY Behavior. This careful review can help in identifying potential design issues early reducing the likelihood of performance problems down the line. Reference and verify all of the noted schematic and layout recommendations in the following checklists:

Industrial PHY Layout Checklist

DP83TD510E Schematic Checklist

The following sections can present expected behaviors if the PHY is powered and initialized correctly. Any deviations from expected behaviors can point to errors due to incorrect peripheral circuitry.

## 2.2 Component Checklist

Make sure that the components such as the CMC and the Crystal/Oscillator meet the requirements listed in the data sheet (also linked in the following).

CMC Requirements (Section 7.2.1.4)

25MHz Crystal Requirements (Section 7.2.2.1.2)

Oscillator Requirements (Section 5.6)

## 2.3 Device Health Checks

This section dives into device health checks which makes sure that a device has been powered and initialized adequately. This section can be skipped if DP83TD510 is:

- Linking up (Status read through register 0x0010) when connected to link partner OR showing NLP signals when Ethernet cable is unconnected
- Responding as expected to register access



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### 2.3.1 Check Voltage Supply Pins

Before delving onto more complex diagnostics, this is essential to establish that the PHY is correctly powered. The DP83TD510E supports both single and dual supply operations. For single supply operation, DVDD must be shorted to C_EXT, measure the voltages at pins VDDA and VDDIO is needed. However, in dual supply operation, check all three voltage pins, VDDA, VDDIO, and DVDD to make sure that the voltages are stable and within the tolerance listed in Table 2-1. Also make sure that the correct decoupling capacitors (1uF, 100nF, 10nF) are used for both single and dual supply configurations.

These voltages are designed to be measured on the PHY voltage input pins, or as close to the input pins as possible

**Table 2-1. Expected Voltage Level for Power Pins**

| Pin Name | Pin Number | Description | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| DVDD 1.0 | 1 | Digital Supply | 0.90 | 1.0 | 1.1 | V |
| VDDA 1.8 | 3 | Analog Supply | 1.62 | 1.8 | 1.98 | V |
| VDDA 3.3 | | Analog Supply | 3.0 | 3.3 | 3.6 | V |
| VDDIO | 17 | Digital Supply Voltage, 1.8V operation | 1.62 | 1.8 | 1.98 | V |
| | | Digital Supply Voltage, 2.5V operation | 2.25 | 2.5 | 2.75 | |
| | | Digital Supply Voltage, 3.3V operation | 3.0 | 3.3 | 3.6 | |

### 2.3.2 Probe the RST_N Pin

The RST_N pin is an active low input to the PHY. Confirm that the controller is not driving the RST_N signal low, otherwise, the device can be held in reset and can appear non-functional. In this case, the device cannot link up, or even have register access. Make sure that the voltage on this pin corresponds to the chosen VDDIO voltage.

### 2.3.3 Probe the CLKOUT Pin

The CLKOUT/LED_1 Pin (Pin 30) is an Input/Output GPIO pin which defaults to output a reference clock signal, which can be used to supply a clock to any other devices on the board. This reference clock is of the utmost importance to maintain proper operation of the PHY. Failure to meet the requirements in the data sheet can lead to bit errors, read or write issues, and in some cases, total non-operation of the PHY.

Verify that the input clock, crystal or oscillator, is available at power-up.

This clock signal is a buffered representation of the input clock crystal or oscillator. If a crystal is being used, do not probe the crystal directly, since the change in capacitance due to the probe can change the behavior of the crystal.

Make sure that this CLKOUT signal is within the ppm requirement.

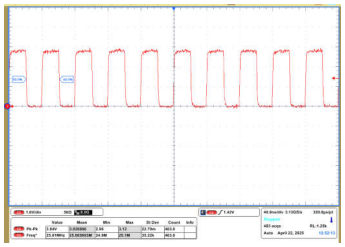

**Figure 2-1. CLKOUT Signal**

### 2.3.4 Probe the SMI Pins

If register reads or writes are successful, this section can be skipped.

If register reads or writes are unsuccessful, probe the MDC pin (pin 12) to verify that there is a ≤1.75MHz clock signal being sourced from the Host Controller. Since this is a lower speed device, at 10Mbps, the supported MDC Clock rate is also lower. Also make sure that the MDIO pin has a external pull-up resistor 2.2kΩ - 4.0kΩ. Additionally, the MDIO signal (pin 11) can be decoded using a Logic Analyzer.



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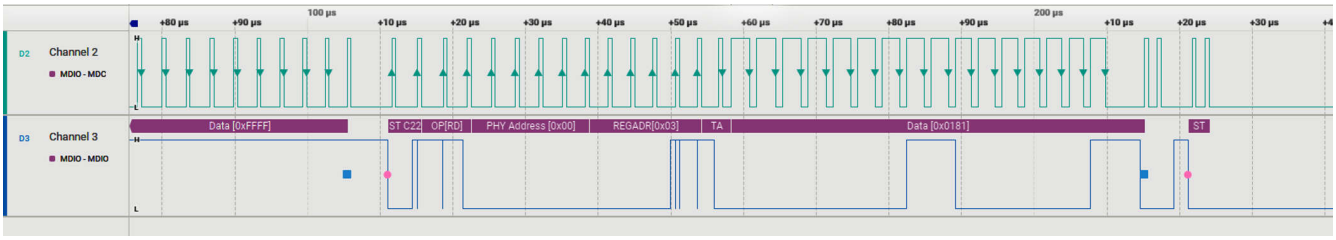


**Figure 2-2. MDC/MDIO Signaling**

The signal ib Figure 2-2 shows a simple read command for register 0x3, which contains the device model number, and must always read as 0x0181 for the DP83TD510.

Note, to access registers beyond 0x1F, the extended register access procedure must be followed, which is given in section 6.3.10 of the data sheet..

## 2.4 Read and Check Register Values

Read the registers and verify the returned values match with the defaults values in the data sheet. Note that the initial values of some registers vary based on strap options.

With the PHY linked, use these values as a reference to identify any variance from the expected operation. It's recommended to check the following key registers to confirm the device configuration:

**Table 2-2. DP83TD510E Key Registers**

| Register Address | Reset Value | Key Bits/Information |
|---|---|---|
| 0x0000 | 0x0000 | [15] - Digital Reset<br>[14] - MII Loopback |
| 0x0003 | 0x0181 | Device Model and Revision Number |
| 0x0010 | 0x0000 | [0] - Link Status |
| 0x0012/0x0013 | 0x0000 | Interrupts |
| 0x0015 | 0x0000 | MII RX Error count |
| 0x0016 | 0x0100 | [8] - Power Mode (Sleep)<br>[6-0] - Loopbacks |
| 0x0017<br>(Mac Configuration) | 0x4001 | [12:11] - RGMII shift/align mode<br>[9] - RGMII enable<br>[7] - XI is {25, 50} MHz<br>[5] - RMII or MII mode |
| 0x012A | 0x0000 | [1-0] - TX/RX CRC Error Indication |
| 0x012D | 0x0000 | TX CRC Error Counter |
| 0x0130 | 0x0000 | RX CRC Error Counter |
| 0x0200 | 0x1000 | [15] - AN Reset<br>[12] - AN Enable/Disable |
| 0x20E (Autonegotiation Configuration) | 0xA000 | [15] - T1L capability<br>[14] - EEE capability<br>[13] - Increased transmit/receive level advertisement<br>[12] - Increased transmit level request |
| 0x020F | 0x0000 | Link Partner Advertisements |
| 0x18F6 | 0x0000 | [12] - Transmit Level Selection<br>[10] - EEE Enable |

## 2.5 Verifying Strap Configuration

Incorrect strap configurations are one of the most common issues leading to lack of data throughput. For example, if the incorrect MII interface is chosen, or an incorrect PHY address is strapped, data transmission cannot be successful.


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Make sure that the MAC is not driving any pins connected to the PHY during power-up or reset pin de-assertion. This can cause an incorrect voltage to be sampled during this time, and cause the strap value to change, because of which the device can perform stochastically. All MAC pins connected to the PHY must be placed in a High-Z state while the PHY is powering up or being coming out of reset.

Strap values sampled at power-up can be read from the register 0x467 (CHIP_SOR_1) using Extended Register Access. More information about strapping is given in section 6.4.1 of the data sheet.

## 2.6 Loopbacks

The DP83TD510E has several loopback options that enable verification of various functional blocks within the PHY. A block diagram of the different loopback modes offered by the PHY is shown in Figure 2-3.

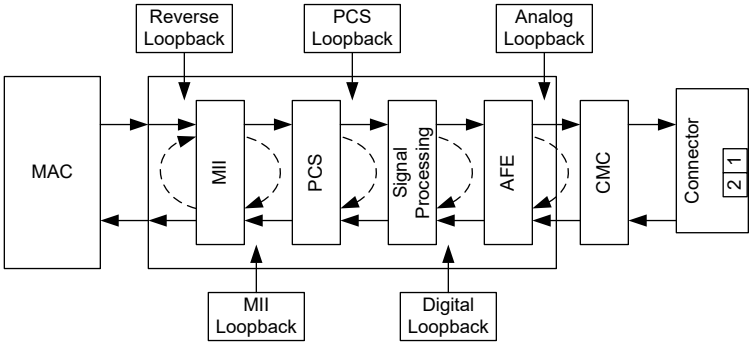


**Figure 2-3. Loopback Block Diagram**

MII Loopback can be configured through the Control Register (BMCR, address 0x0000). All other loopback modes are enabled using the BIST Control Register (BISCR, address 0x0016). These loopback modes can be used to validate both the MII, MDI, and the internal blocks within the PHY. This can be crucial in narrowing down the part of the data path responsible for behavior such as packet loss/errors.

Table 2-3 shows the register writes to enable each loopback mode, assuming the other register configurations are left as default.

**Table 2-3. Register Writes for Loopbacks**

| Loopback Mode | Register | Write Value |
|---|---|---|
| MII Loopback | 0x0000 | 0x4000 |
| PCS Loopback | 0x0016 | 0x0102 |
| Digital Loopback | 0x0016 | 0x0104 |
| Analog Loopback | 0x0016 | 0x0108 |
| Reverse Loopback | 0x0016 | 0x0110 |

There are a few built in counters, for both TX and RX, that can aid in debugging with loopbacks. The counters can be used to validate the number of packets being received or transmitted in different loopback modes. Note that the counters are reset if 0x12B, 0x12C, and 0x12D for TX counters, and 0x12E, 0x12F, and 0x130 for RX counters. These counters can be found in the set of registers given in Table 2-4.

**Table 2-4. TX/RX Packet Counter Registers**

| Register | Function |
|---|---|
| 0x012A | [1] RX CRC Indication<br>[0] TX CRC Indication |
| 0x012B | Lower 16 bits TX Packet Counter |
| 0x012C | Upper 16 bits TX Packet Counter |
| 0x012D | TX Packets with CRC Errors |
| 0x012E | Lower 16 bits RX Packet Counter |
| 0x012F | Upper 16 bits RX Packet Counter |



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**Table 2-4. TX/RX Packet Counter Registers (continued)**

| Register | Function |
|---|---|
| 0x0130 | RX Packets with CRC Errors |

## 2.7 MDI Health Checks

MDI issues usually include packet loss, Auto-Negotiation issues, and link drop. There are a few different tests used to narrow down the root cause of the unexpected behaviors encountered.

This section can be skipped if DP83TD510 if:

- Linked up AND reporting no packet errors via register 0x0015 when sending traffic through the device

### *2.7.1 Link Up Common Issues*

If the DP83TD510E is having trouble linking up with a link partner, check for the following common reasons.

Make sure that the device is sending Normal Link Pulses (NLPs) on the MDI lines when connected to an non-powered link partner, or properly terminated with 50Ω. These signals act as an exchange of information between the 2 PHYs sharing the link, so that the signals are able to link up in a configuration designed for both devices. The following waveforms show the expected signal.

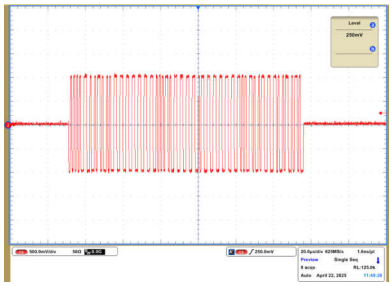

**Figure 2-4. Normal Link Pulse (Zoomed In)**

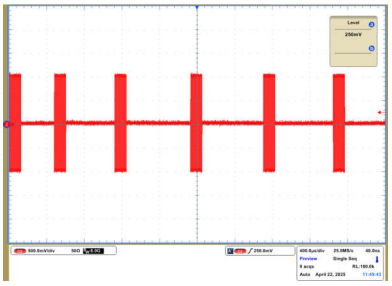

**Figure 2-5. Normal Link Pulses**

The DP83TD510 can also bypass this auto-negotiation stage and force a link by manually disabling auto-negotiation and configuring each device, one to host, and the other to client. The scripts for these functions are given in the following. The transmit level selected is the same as what the device has been strapped to and is reflected in register 0x18F6[12].

```
begin

000D 0007
000E 0200
000D 4007
000E 0000 // Disable AN

000D 0001
000E 08F6
000D 4001
000E 1000 // Force transmit level to 2.4V, write 0000 for 1V

000D 0001
000E 0834
000D 4001
000E 4002 // Configure Device as Master, write 0002 for Slave

end
```

### *2.7.2 Transmit Level*

10Base-T1L Devices have the ability to switch between 2 transmit levels, 2.4Vpp and 1Vpp. Usually, Auto-negotiation takes care of choosing the transmit level based on the advertisements received from the link partner, but this is important to make sure that both PHYs being linked are configured to have the desired transmit levels advertised. The advertized transmit level can be checked in bit 12 of register 0x20E


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An excellent process is that the transmit levels must be selected through strapping into the desired transmit level, but these levels can also be changed through register configuration after power-up.

Also important is to make sure that proper 100Ω termination is being used when measuring the voltage output level.

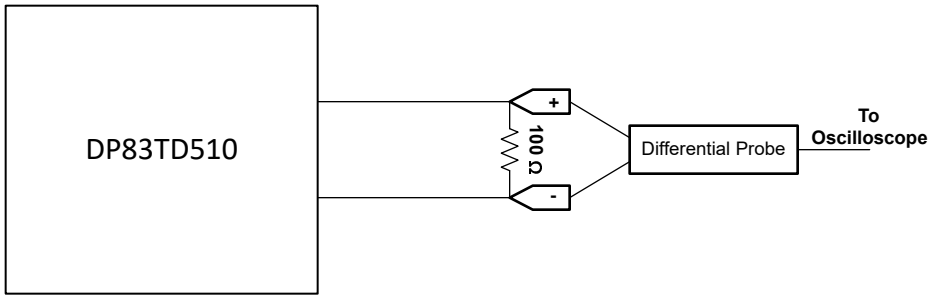


**Figure 2-6. MDI Measurement**

#### 2.7.2.1 Change Transmit Level

Broadly speaking, there are two methods for switching transmit levels. The first is when there is no established link, and the second with an established link between 2 PHYs.

Without an established link, change the register 0x20E to only advertise the desired voltage. To test this, enable the 3-level output signal by forcing link up by enabling digital loopback. This starts idle waveforms on the MDI signal which can be probed to verify the voltage swing level.

```
begin

000D 0001
000E 08F6
000D 4001
000E 1000 // Force transmit level to 2.4V, write 0000 for 1V

000D 001F
000E 0016
000D 401F
000E 0104 // Enable digital loopback to force link up to have three level signal

end
```

In the second situation, we need to change the transmit level on both PHYs, which is why it's a 3-step process. First, we need to disable auto-negotiation, force the desired voltage, change transmit level advertisement, and perform a soft reset on PHY 1. Secondly, we need to perform the same operations on PHY 2 and re-enable auto-negotiation at the very end. Lastly, we can go back to PHY 1 and re-enable auto-negotiation. The scripts for these 3 steps are given in the following.

Step 1 (DP83TD510 PHY 1)

```
begin

000D 0007
000E 0200
000D 4007
000E 0000 // Disable AN

000D 0001
000E 08F6
000D 4001
000E 1000 // Force transmit level to 2.4V, write 0000 for 1V

000D 0007
000E 020E
000D 4007
000E B000 // Increase the transmit level advertisment, write 8000 for 1V

000D 001F
```



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```
000E 0010
000D 401F
000E 4000 // Soft reset

end
```

Step 2 (DP83TD510 PHY 2)

```
begin

000D 0007
000E 0200
000D 4007
000E 0000 // Disable AN

000D 0001
000E 08F6
000D 4001
000E 1000 // Force transmit level to 2.4V, write 0000 for 1V

000D 0007
000E 020E
000D 4007
000E B000 // Increase the transmit level advertisment, write 8000 for 1V

000D 001F
000E 0010
000D 401F
000E 4000 // Soft reset

000D 0007
000E 0200
000D 4007
000E 1000 // Re-enable AN

end
```

Step 3 (DP83TD510 PHY 1)

```
begin

000D 0007
000E 0200
000D 4007
000E 1000 // Re-enable AN

end
```

### *2.7.3 Time-Domain Reflectometry*

Time-Domain reflectometry is used to determine the quality of the cables, connectors, and terminations, in addition to estimating the cable length. This determines faults such as opens, shorts, cable impedance mismatches, bad connectors, termination mismatches, cross faults, cross shorts, and any other discontinuities along the cable.

This process involves sending a test pulse of a known amplitude of 1V through each of the wires in the pair, and measuring the return time and amplitude of the signal reflections caused by any imperfections, and the end of the cable.

For more information about the cable diagnostic toolkit of the DP83TD510, please refer to the application note linked below.

Cable Diagnostic Toolkit

### *2.7.4 Signal Quality Check*

After confirming the link up by reading register 0x0010, the signal quality of the link can be verifying by using the built in Signal Quality Indicator (SQI) Function. Poor link quality can be caused by layout or cable imperfections, and can also lead to packet loss or errors, or even link drops.



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While TDR can provide information about the existence and location of cable faults, this real-time monitoring of the signal quality can provide valuable information before a fault occurs by measuring the Signal to Noise Ratio (SNR) at periodic intervals after link is achieved.

This MSE value is stored in the memory register 0x0A85. These values can be compared to Table 2-5 to evaluate the health of the link.

**Table 2-5. SQI Link Health**

| SQI Link Health | MSE | SNR (dB) |
|---|---|---|
| Poor | MSE > 0660h | SNR < 17.29 |
| Marginal | 0660h ≥ MSE > 0320h | 17.29 < SNR < 20.38 |
| Good | MSE ≤ 0320h | SNR > 20.38 |

For more information about the cable diagnostic toolkit of the DP83TD510, please refer to the Cable Diagnostic Toolkit, application note

### *2.7.5 MDI Test Modes*

There are three built in test modes to validate the MDI output to be within expected specifications. These test modes can be activated through register 0x18F8. These test modes are useful in performing PMA compliance tests, and to verify the correct output voltage. Some captured waveforms of test mode 1 are shown in the following images.

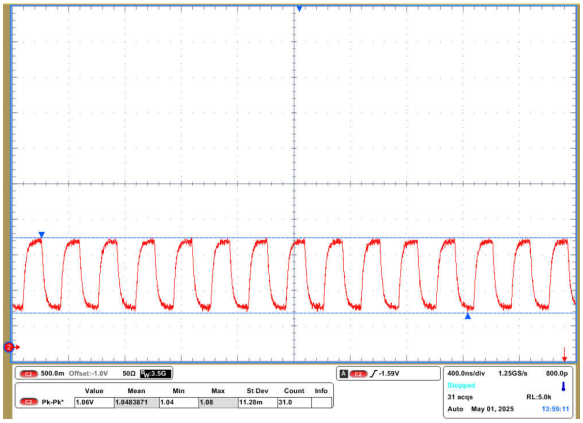

**Figure 2-7. Test Mode 1 (1Vpp)**

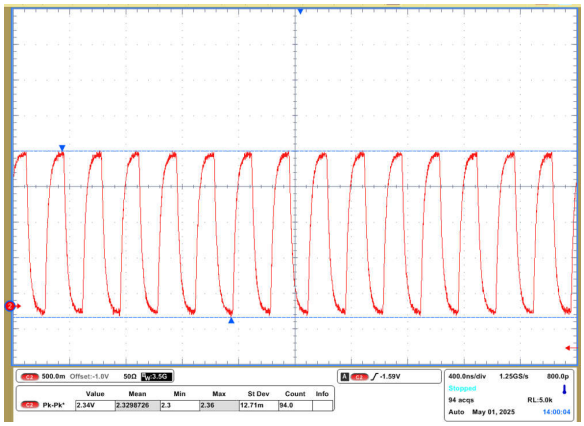

**Figure 2-8. Test Mode 1 (2.4Vpp)**

## 2.8 MII Health Checks

MII issues usually include MII mode mismatches, Master or Slave configuration, Clocking and Timing discrepancies. The DP83TD510 supports MII, RMII (Master and Slave) and RGMII modes. Before investigating further, make sure that the correct MII interface is being selected on both the PHY and the MAC. This can be checked through bits 5 and 9 of register 0x17 (MAC_CFG_1).

### *2.8.1 RGMII*

The RGMII interface can be chosen via straps or by using register 0x17. Failing to meet the timing requirements listed in the data sheet for RGMII is a common issue. While the RGMII interface has the strictest timing requirements amoung the interface options, these requirements are not as strict for 10Mbps speeds as compared to gigabit RGMII. Regardless, it's crucial to verify that the timing requirements are being met. These requirements are listed in section 5.6 of the data sheet.

Also verify that the required signals for RGMII shown below are all routed properly between the PHY and the MAC.



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If a MAC bus is suspected to be problematic, probe the lines at the receiver side of the trace making sure that the receiver's setup an hold times are met, along with VIH/VIL. Typical symptoms of violating these specifications is packet errors at the MAC while the PHY is indicating clean traffic (Register 0x15)

RGMII clock shift can be toggled using register 0x0017 bits [12:11] to meet these requirements

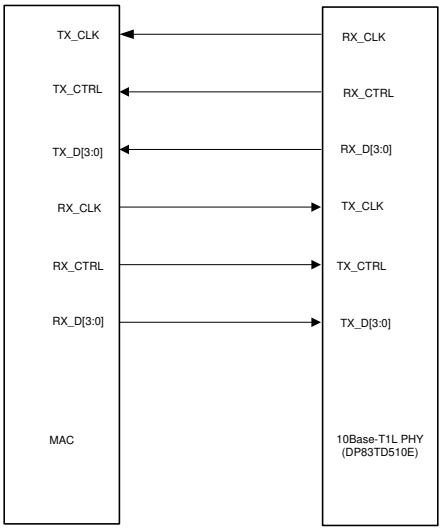


**Figure 2-9. RGMII Signaling**

### *2.8.2 RMII*

The RMII interface can be chosen via straps or by using register 0x17. Similarly to RGMII and MII, RMII also has certain timing requirements that must be met for proper function of the PHY. These requirements are listed in section 5.6 of the data sheet.

Unlike RGMII and MII, RMII has master and slave modes. These modes can be strapped to on power-up and cannot be changed through registers.

If a MAC bus is suspected to be problematic, probe the lines at the receiver side of the trace making sure that the receiver's setup an hold times are met, along with VIH/VIL. Typical symptoms of violating these specifications is packet errors at the MAC while the PHY is indicating clean traffic (Register 0x15)

RMII clock shift can be toggled using register 0x0017 bit [8] to meet these requirements

In RMII Master mode, the DP83TD510 operates off of the 25MHz input clock (crystal or oscillator) and supplies the MAC with a referenced 50MHz clock to synchronize the data. This clock can be shifted to make sure that the setup and hold times for the receiver (MAC) is met by using register 0x17 [9]. Enabling this delay adds approximately 4ns Delay on the 50MHz output clock. The setup and hold times are an important timing requirement and must be met to make sure that no packet loss or errors occur during transmission.


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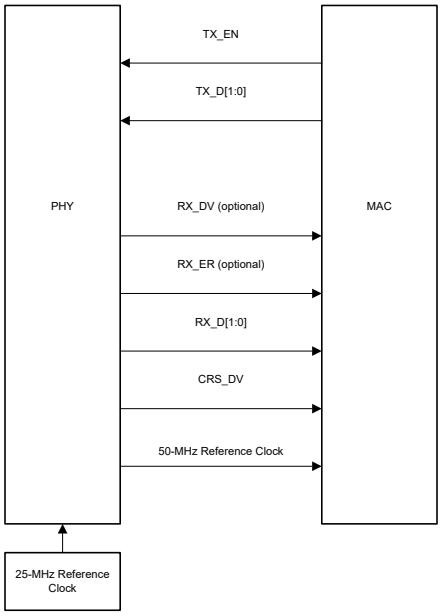


**Figure 2-10. RMII Master Signaling**

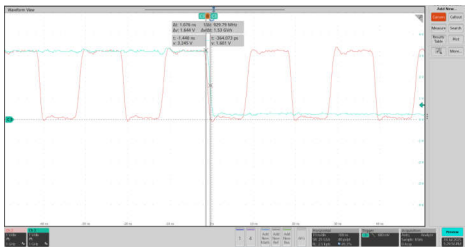

**Figure 2-11. RMII Clock Shift Disabled**

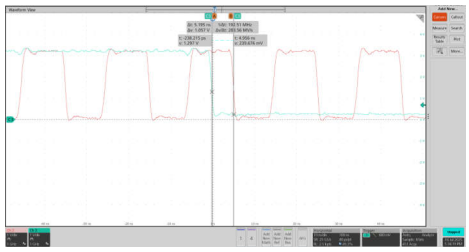

**Figure 2-12. RMII Clock Shift Enabled**

In RMII Slave mode, the DP83TD510 operates off a 50MHz input clock which is shared by both the PHY and the MAC. Alternatively, the PHY can operate off a 50MHz reference clock provided by the MAC. Make sure that this clock being supplied to the PHY in RMII Slave mode meets the requirement for ± 100ppm for proper functioning of the PHY.

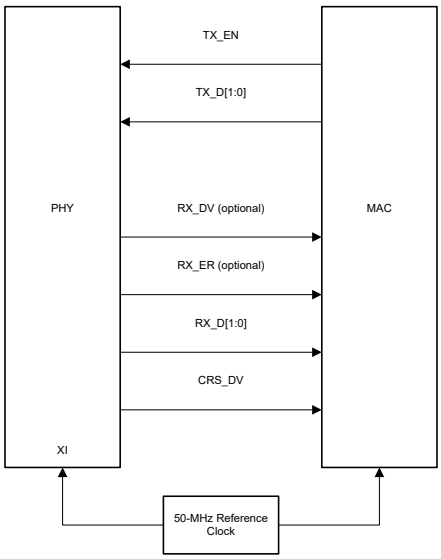


**Figure 2-13. RMII Slave Signaling**



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Since each mode requires a different input clock signal, make sure that the correct or expected RMII mode is being strapped during power-up for the device to boot up and perform properly.

### *2.8.3 MII*

The MII interface can be chosen via straps or by using register 0x17. Similarly to RGMII, MII also has certain timing requirements that must be met for proper function of the PHY. These requirements are listed in section 5.6 of the data sheet.

Also verify that the required signals for MII shown below are all routed properly between the PHY and the MAC.

If a MAC bus is suspected to be problematic, probe the lines at the receiver side of the trace making sure that the receiver's setup an hold times are met, along with VIH/VIL. Typical symptoms of violating these specifications is packet errors at the MAC while the PHY is indicating clean traffic (Register 0x15)

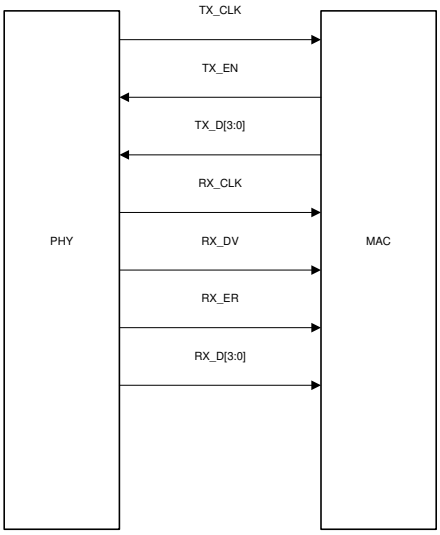


**Figure 2-14. MII Signaling**


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# 3 Summary

This application note provides a suggested flow for evaluating a new application and confirming the expected functionality. The step-by-step recommendations can help ease board bring up and initial evaluation of DP83TD510 designs.



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# 4 References


- Texas Instruments, *DP83TD510E Ultra Low Power 802.3cg 10Base-T1L 10M Single Pair Ethernet PHY*, data sheet
- Texas Instruments, *DP83TD510E Cable Diagnostics Toolkit*, application note.
- Texas Instruments, *DP83TD510E-USB-2-MDIO-SCRIPTS*, supporting software




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