



ABSTRACT

This programming guide lists the device registers of the LMK5C22212A.

Trademarks

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1 Device Registers

[Table 1-1](#) lists the memory-mapped registers for the Device registers. All register offset addresses not listed in [Table 1-1](#) should be considered as reserved locations and the register contents should not be modified.

Table 1-1. DEVICE Registers

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x0	R0	VNDRID_15:8								
0x1	R1	VNDRID								
0x2	R2	PRODID								
0x3	R3	REVID								
0x4	R4	PRTID_47:40								
0x5	R5	PRTID_39:32								
0x6	R6	PRTID_31:24								
0x7	R7	PRTID_23:16								
0x8	R8	PRTID_15:8								
0x9	R9	PRTID								
0x10	R16	NVMCNT								
0x12	R18	RESERVED				TARGET_ADR_MSB				
0x13	R19	EEREV								
0x14	R20	ROM_PLUS_EE	EE_ROM_PAGE_SEL					RESERVED		
0x15	R21	SPI_3WIRE_DIS	SYNC_SW	RESERVED						
0x16	R22	RESERVED		DPLL1_EN	APLL1_EN	DPLL2_EN	APLL2_EN	RESERVED		
0x17	R23	RESERVED	SWRST	RESERVED	DPLL2_SWRST	DPLL1_SWRST	RESERVED	APLL2_SWRST	APLL1_SWRST	
0x18	R24	RESERVED		APLL1_STRT_PRTY		APLL2_STRT_PRTY		RESERVED		
0x19	R25	RESERVED								SYNC_EN
0x1A	R26	RESERVED		SYSREF_REQ_MODE		SYSREF_REQ_SEL			SYSREF_REQ_SW	
0x1B	R27	TEC_CNTR_39:32								
0x1C	R28	TEC_CNTR_31:24								
0x1D	R29	TEC_CNTR_23:16								
0x1E	R30	TEC_CNTR_15:8								
0x1F	R31	TEC_CNTR								
0x20	R32	RESERVED						TEC_CNTR_TRIG_SEL	TEC_CNTR_EN	
0x21	R33	RESERVED					LOL_PLL2	RESERVED	LOS_FDET_XC	
0x23	R35	LOPL_DPLL2	LOFL_DPLL2	RESERVED	HLDOVR2	RESERVED				

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x25	R37	RESERVED					LOL_PLL2_MAS K	RESERVED	LOS_FDET_XO_ MASK	
0x27	R39	LOPL_DPLL2_M ASK	LOFL_DPLL2_M ASK	HIST2_MASK	HLDOVR2_MAS K	REFSWITCH2_M ASK	LOR_MISSCLK2 _MASK	LOR_FREQ2_M ASK	LOR_PH2_MAS K	
0x28	R40	LOPL_DPLL1_M ASK	LOFL_DPLL1_M ASK	HIST1_MASK	HLDOVR1_MAS K	REFSWITCH1_M ASK	LOR_MISSCLK1 _MASK	LOR_FREQ1_M ASK	LOR_PH1_MAS K	
0x29	R41	RESERVED					LOL_PLL2_POL	RESERVED	LOS_FDET_XO_ POL	
0x2B	R43	LOPL_DPLL2_P OL	LOFL_DPLL2_P OL	HIST2_POL	HLDOVR2_POL	REFSWITCH2_P OL	LOR_MISSCLK2 _POL	LOR_FREQ2_P OL	LOR_PH2_POL	
0x2C	R44	LOPL_DPLL1_P OL	LOFL_DPLL1_P OL	HIST1_POL	HLDOVR1_POL	REFSWITCH1_P OL	LOR_MISSCLK1 _POL	LOR_FREQ1_P OL	LOR_PH1_POL	
0x2D	R45	RESERVED					LOL_PLL2_INTR	RESERVED	LOS_FDET_XO_ INTR	
0x2F	R47	LOPL_DPLL2_IN TR	LOFL_DPLL2_IN TR	HIST2_INTR	HLDOVR2_INTR	REFSWITCH2_I NTR	LOR_MISSCLK2 _INTR	LOR_FREQ2_IN TR	LOR_PH2_INTR	
0x30	R48	LOPL_DPLL1_IN TR	LOFL_DPLL1_IN TR	HIST1_INTR	HLDOVR1_INTR	REFSWITCH1_I NTR	LOR_MISSCLK1 _INTR	LOR_FREQ1_IN TR	LOR_PH1_INTR	
0x31	R49	RESERVED				INT_LATCH_OR _LIVE	INT_AND_OR	INT_EN	INT_CLR	
0x32	R50	RESERVED						REF1_VALID_ST ATUS	REF0_VALID_ST ATUS	
0x34	R52	RESERVED		REF1_PH_STAT US	RESERVED	REF1_FDET_ST ATUS	REF0_PH_STAT US	RESERVED	REF0_FDET_ST ATUS	
0x35	R53	RESERVED			TEC_CNTR_HEL D	RESERVED				
0x36	R54	RESERVED	GPIO0_IN_FLT_ EN	GPIO0_MODE						
0x37	R55	RESERVED	GPIO1_IN_FLT_ EN	GPIO1_MODE						
0x38	R56	RESERVED	GPIO2_IN_FLT_ EN	GPIO2_MODE						
0x39	R57	RESERVED	GPIO0_SEL							
0x3A	R58	RESERVED	GPIO1_SEL							
0x3B	R59	RESERVED	GPIO2_SEL							
0x3C	R60	RESERVED		GPIO0_OPEND	GPIO1_OPEND	GPIO2_OPEND	GPIO0_POL	GPIO1_POL	GPIO2_POL	
0x3D	R61	RESERVED			GPIO_SYSREF_SEL				MUTE_DPLL1_P HLOCK	MUTE_DPLL1_F RLOCK

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x3E	R62	RESERVED		MUTE_DPLL2_P HLOCK	MUTE_DPLL2_F RLOCK	MUTE_APLL2_L OCK	RESERVED		
0x3F	R63	RESERVED			XO_FDET_BYP	XO_ITYPE			
0x40	R64	RESERVED			XO_OUT_BUF_EN				
0x43	R67	RESERVED		REF1_ITYPE					
0x44	R68	RESERVED		REF0_ITYPE					
0x46	R70	RESERVED							STATUS_MUX_D IV2_EN
0x4B	R75	RESERVED	TDC1_ZDM_BYP ASS_FB_DIV	TDC1_ZDM_FB_ PRE_BYP	TDC1_IN_SEL		TDC1_IN_DRV_SEL		
0x4C	R76	RESERVED	TDC2_ZDM_BYP ASS_FB_DIV	TDC2_ZDM_FB_ PRE_BYP	TDC2_IN_SEL		TDC2_IN_DRV_SEL		
0x4D	R77	RESERVED							RESERVED
0x4E	R78	RESERVED		REF_OUT01_EN	REF_OUT01_SEL				
0x4F	R79	RESERVED		REF0_EARLY_D ET_EN	REF0_PH_VALID _EN	REF0_VALTMR_ EN	REF0_PPM_EN	REF0_MISSCLK _EN	RESERVED
0x50	R80	RESERVED		REF1_EARLY_D ET_EN	REF1_PH_VALID _EN	REF1_VALTMR_ EN	REF1_PPM_EN	REF1_MISSCLK _EN	RESERVED
0x53	R83	RESERVED				REF1_DET_CLK_DIV		REF0_DET_CLK_DIV	
0x54	R84	RESERVED		REF0_MISSCLK_DIV_21:16					
0x55	R85	REF0_MISSCLK_DIV_15:8							
0x56	R86	REF0_MISSCLK_DIV							
0x57	R87	RESERVED		REF1_MISSCLK_DIV_21:16					
0x58	R88	REF1_MISSCLK_DIV_15:8							
0x59	R89	REF1_MISSCLK_DIV							
0x60	R96	RESERVED							REF0_MISSCLK _VCOSEL
0x61	R97	RESERVED		REF0_EARLY_CLK_DIV_21:16					
0x62	R98	REF0_EARLY_CLK_DIV_15:8							
0x63	R99	REF0_EARLY_CLK_DIV							
0x64	R100	RESERVED		REF1_EARLY_CLK_DIV_21:16					
0x65	R101	REF1_EARLY_CLK_DIV_15:8							
0x66	R102	REF1_EARLY_CLK_DIV							
0x6D	R109	RESERVED	REF0_PPM_MIN_14:8						
0x6E	R110	REF0_PPM_MIN							
0x6F	R111	RESERVED	REF0_PPM_MAX_14:8						

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x70	R112	REF0_PPM_MAX							
0x71	R113	RESERVED	REF1_PPM_MIN_14:8						
0x72	R114	REF1_PPM_MIN							
0x73	R115	RESERVED	REF1_PPM_MAX_14:8						
0x74	R116	REF1_PPM_MAX							
0x7D	R125	RESERVED				REF0_CNTSTRT_27:24			
0x7E	R126	REF0_CNTSTRT_23:16							
0x7F	R127	REF0_CNTSTRT_15:8							
0x80	R128	REF0_CNTSTRT							
0x81	R129	RESERVED				REF0_HOLD_CNTSTRT_27:24			
0x82	R130	REF0_HOLD_CNTSTRT_23:16							
0x83	R131	REF0_HOLD_CNTSTRT_15:8							
0x84	R132	REF0_HOLD_CNTSTRT							
0x85	R133	RESERVED				REF1_CNTSTRT_27:24			
0x86	R134	REF1_CNTSTRT_23:16							
0x87	R135	REF1_CNTSTRT_15:8							
0x88	R136	REF1_CNTSTRT							
0x89	R137	RESERVED				REF1_HOLD_CNTSTRT_27:24			
0x8A	R138	REF1_HOLD_CNTSTRT_23:16							
0x8B	R139	REF1_HOLD_CNTSTRT_15:8							
0x8C	R140	REF1_HOLD_CNTSTRT							
0x9D	R157	RESERVED			REF0VLDTMR				
0x9E	R158	RESERVED			REF1VLDTMR				
0xA1	R161	RESERVED		REF0_PH_VALID_THR_13:8					
0xA2	R162	REF0_PH_VALID_THR							
0xA3	R163	RESERVED		REF1_PH_VALID_THR_13:8					
0xA4	R164	REF1_PH_VALID_THR							
0xAA	R170	NVMSCRC							
0xAB	R171	RESERVED	REGCOMMIT	NVMCRCERR	RESERVED		NVMBUSY	NVMERASE	NVMPROG
0xAC	R172	NVMLCRC							
0xAD	R173	RESERVED			MEMADR_12:8				
0xAE	R174	MEMADR							
0xAF	R175	NVMDAT							
0xB0	R176	RAMDAT							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xB4	R180	NVMUNLK							
0x175	R373	RESERVED		DPLL2_REF0_AUTO_PRTY			DPLL2_REF1_AUTO_PRTY		
0x177	R375	RESERVED		DPLL2_REF4_AUTO_PRTY			DPLL2_REF5_AUTO_PRTY		
0x178	R376	RESERVED		DPLL2_MAN_REFSEL			DPLL2_MAN_SWITCH_PIN_MODE	DPLL2_SWITCH_MODE	
0x179	R377	RESERVED		DPLL2_REFSEL_STAT					
0x17A	R378	DPLL2_LOCKDET_PPM_EN	DPLL2_LOCKDET_PPM_MAX_14:8						
0x17B	R379	DPLL2_LOCKDET_PPM_MAX							
0x17C	R380	RESERVED	DPLL2_UNLOCKDET_PPM_MAX_14:8						
0x17D	R381	DPLL2_UNLOCKDET_PPM_MAX							
0x17E	R382	RESERVED		DPLL2_LOCKDET2_PPM_CNTSTRT_29:24					
0x17F	R383	DPLL2_LOCKDET2_PPM_CNTSTRT_23:16							
0x180	R384	DPLL2_LOCKDET2_PPM_CNTSTRT_15:8							
0x181	R385	DPLL2_LOCKDET2_PPM_CNTSTRT							
0x182	R386	RESERVED		DPLL2_LOCKDET_PPM_CNTSTRT_29:24					
0x183	R387	DPLL2_LOCKDET_PPM_CNTSTRT_23:16							
0x184	R388	DPLL2_LOCKDET_PPM_CNTSTRT_15:8							
0x185	R389	DPLL2_LOCKDET_PPM_CNTSTRT							
0x186	R390	RESERVED		DPLL2_LOCKDET_VCO_PPM_CNTSTRT_29:24					
0x187	R391	DPLL2_LOCKDET_VCO_PPM_CNTSTRT_23:16							
0x188	R392	DPLL2_LOCKDET_VCO_PPM_CNTSTRT_15:8							
0x189	R393	DPLL2_LOCKDET_VCO_PPM_CNTSTRT							
0x18A	R394	RESERVED							DPLL2_STATUS_PPM_LOCK
0x18D	R397	DPLL2_LOOP_EN	DPLL2_PHASE_CANCEL_EN	DPLL2_FASTLOCK_ALWAYS	DPLL2_PHS1_EN	DPLL2_ZDM_EN	DPLL2_HIST_EN	DPLL2_PHASE_CANCEL_ALWAYS	RESERVED
0x18E	R398	DPLL2_HOLD_SLEW_LIM_EN	RESERVED						
0x190	R400	RESERVED			DPLL2_PH_OFFSET_44:40				
0x191	R401	DPLL2_PH_OFFSET_39:32							
0x192	R402	DPLL2_PH_OFFSET_31:24							
0x193	R403	DPLL2_PH_OFFSET_23:16							
0x194	R404	DPLL2_PH_OFFSET_15:8							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x195	R405	DPLL2_PH_OFFSET							
0x196	R406	DPLL2_FREE_RUN_39:32							
0x197	R407	DPLL2_FREE_RUN_31:24							
0x198	R408	DPLL2_FREE_RUN_23:16							
0x199	R409	DPLL2_FREE_RUN_15:8							
0x19A	R410	DPLL2_FREE_RUN							
0x19B	R411	RESERVED	DPLL2_1PPS_M ODE	DPLL2_1PPS_E N	RESERVED				
0x1B8	R440	RESERVED							DPLL2_LCK_TIMER_9:8
0x1B9	R441	DPLL2_LCK_TIMER							
0x1BA	R442	RESERVED							DPLL2_HIST_TIMER_9:8
0x1BB	R443	DPLL2_HIST_TIMER							
0x1BC	R444	RESERVED							DPLL2_HOLD_TIMER_9:8
0x1BD	R445	DPLL2_HOLD_TIMER							
0x1BE	R446	RESERVED							DPLL2_PHS1_TIMER_9:8
0x1BF	R447	DPLL2_PHS1_TIMER							
0x1C4	R452	RESERVED				DPLL2_HIST_GAIN			
0x1C5	R453	RESERVED			DPLL2_PL_THRESH				
0x1C6	R454	RESERVED			DPLL2_PL_UNLK_THRESH				
0x1C7	R455	RESERVED			DPLL2_PHS1_THRESH				
0x1CA	R458	RESERVED			DPLL2_HOLD_SLEW_STEP				
0x1CC	R460	RESERVED			DPLL2_STATUS _PL	RESERVED			
0x1CD	R461	RESERVED				DPLL2_DCO_SL EW_ACTIVE	RESERVED		
0x1D0	R464	RESERVED							DPLL2_FB_DIV_ 32:32
0x1D1	R465	DPLL2_FB_DIV_31:24							
0x1D2	R466	DPLL2_FB_DIV_23:16							
0x1D3	R467	DPLL2_FB_DIV_15:8							
0x1D4	R468	DPLL2_FB_DIV							
0x1D5	R469	DPLL2_FB_NUM_39:32							
0x1D6	R470	DPLL2_FB_NUM_31:24							
0x1D7	R471	DPLL2_FB_NUM_23:16							
0x1D8	R472	DPLL2_FB_NUM_15:8							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1D9	R473	DPLL2_FB_NUM							
0x1DA	R474	DPLL2_FB_DEN_39:32							
0x1DB	R475	DPLL2_FB_DEN_31:24							
0x1DC	R476	DPLL2_FB_DEN_23:16							
0x1DD	R477	DPLL2_FB_DEN_15:8							
0x1DE	R478	DPLL2_FB_DEN							
0x1DF	R479	RESERVED							DPLL2_FB2_DIV_32:32
0x1E0	R480	DPLL2_FB2_DIV_31:24							
0x1E1	R481	DPLL2_FB2_DIV_23:16							
0x1E2	R482	DPLL2_FB2_DIV_15:8							
0x1E3	R483	DPLL2_FB2_DIV							
0x1E4	R484	DPLL2_FB2_NUM_39:32							
0x1E5	R485	DPLL2_FB2_NUM_31:24							
0x1E6	R486	DPLL2_FB2_NUM_23:16							
0x1E7	R487	DPLL2_FB2_NUM_15:8							
0x1E8	R488	DPLL2_FB2_NUM							
0x1E9	R489	DPLL2_FB2_DEN_39:32							
0x1EA	R490	DPLL2_FB2_DEN_31:24							
0x1EB	R491	DPLL2_FB2_DEN_23:16							
0x1EC	R492	DPLL2_FB2_DEN_15:8							
0x1ED	R493	DPLL2_FB2_DEN							
0x1EE	R494	RESERVED		DPLL2_REF5_F_B_SEL	DPLL2_REF4_F_B_SEL	RESERVED		DPLL2_REF1_F_B_SEL	DPLL2_REF0_F_B_SEL
0x1EF	R495	RESERVED					DPLL2_FB_MASH_ORDER		
0x1F0	R496	RESERVED		DPLL2_FB_FDEV_37:32					
0x1F1	R497	DPLL2_FB_FDEV_31:24							
0x1F2	R498	DPLL2_FB_FDEV_23:16							
0x1F3	R499	DPLL2_FB_FDEV_15:8							
0x1F4	R500	DPLL2_FB_FDEV							
0x1F5	R501	RESERVED							DPLL2_FB_FDEV_UPDATE
0x1F6	R502	RESERVED							DPLL2_FB_FDEV_EN
0x1F7	R503	DPLL2_FB_NUM_STAT_39:32							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1F8	R504	DPLL2_FB_NUM_STAT_31:24							
0x1F9	R505	DPLL2_FB_NUM_STAT_23:16							
0x1FA	R506	DPLL2_FB_NUM_STAT_15:8							
0x1FB	R507	DPLL2_FB_NUM_STAT							
0x1FC	R508	RESERVED				DPLL2_REF0_D BLR_EN	DPLL2_REF1_D BLR_EN	RESERVED	
0x1FD	R509	DPLL2_REF0_RDIV_15:8							
0x1FE	R510	DPLL2_REF0_RDIV							
0x1FF	R511	DPLL2_REF1_RDIV_15:8							
0x200	R512	DPLL2_REF1_RDIV							
0x205	R517	DPLL2_REF4_RDIV_15:8							
0x206	R518	DPLL2_REF4_RDIV							
0x207	R519	DPLL2_REF5_RDIV_15:8							
0x208	R520	DPLL2_REF5_RDIV							
0x20B	R523	RESERVED		DPLL1_REF0_AUTO_PRTY			DPLL1_REF1_AUTO_PRTY		
0x20D	R525	RESERVED					DPLL1_REF5_AUTO_PRTY		
0x20E	R526	RESERVED		DPLL1_MAN_REFSEL			DPLL1_MAN_S WITCH_PIN_MO DE	DPLL1_SWITCH_MODE	
0x20F	R527	RESERVED		DPLL1_REFSEL_STAT					
0x210	R528	DPLL1_LOCKDE T_PPM_EN	DPLL1_LOCKDET_PPM_MAX_14:8						
0x211	R529	DPLL1_LOCKDET_PPM_MAX							
0x212	R530	RESERVED	DPLL1_UNLOCKDET_PPM_MAX_14:8						
0x213	R531	DPLL1_UNLOCKDET_PPM_MAX							
0x214	R532	RESERVED		DPLL1_LOCKDET2_PPM_CNTSTRT_29:24					
0x215	R533	DPLL1_LOCKDET2_PPM_CNTSTRT_23:16							
0x216	R534	DPLL1_LOCKDET2_PPM_CNTSTRT_15:8							
0x217	R535	DPLL1_LOCKDET2_PPM_CNTSTRT							
0x218	R536	RESERVED		DPLL1_LOCKDET_PPM_CNTSTRT_29:24					
0x219	R537	DPLL1_LOCKDET_PPM_CNTSTRT_23:16							
0x21A	R538	DPLL1_LOCKDET_PPM_CNTSTRT_15:8							
0x21B	R539	DPLL1_LOCKDET_PPM_CNTSTRT							
0x21C	R540	RESERVED		DPLL1_LOCKDET_VCO_PPM_CNTSTRT_29:24					
0x21D	R541	DPLL1_LOCKDET_VCO_PPM_CNTSTRT_23:16							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x21E	R542	DPLL1_LOCKDET_VCO_PPM_CNTSTRT_15:8							
0x21F	R543	DPLL1_LOCKDET_VCO_PPM_CNTSTRT							
0x220	R544	RESERVED							DPLL1_STATUS_PPM_LOCK
0x223	R547	DPLL1_LOOP_EN	DPLL1_PHASE_CANCEL_EN	DPLL1_FASTLOCK_ALWAYS	DPLL1_PHS1_EN	DPLL1_ZDM_EN	DPLL1_HIST_EN	DPLL1_PHASE_CANCEL_ALWAYS	RESERVED
0x224	R548	DPLL1_HOLD_SLEW_LIM_EN	RESERVED						
0x226	R550	RESERVED			DPLL1_PH_OFFSET_44:40				
0x227	R551	DPLL1_PH_OFFSET_39:32							
0x228	R552	DPLL1_PH_OFFSET_31:24							
0x229	R553	DPLL1_PH_OFFSET_23:16							
0x22A	R554	DPLL1_PH_OFFSET_15:8							
0x22B	R555	DPLL1_PH_OFFSET							
0x22C	R556	DPLL1_FREE_RUN_39:32							
0x22D	R557	DPLL1_FREE_RUN_31:24							
0x22E	R558	DPLL1_FREE_RUN_23:16							
0x22F	R559	DPLL1_FREE_RUN_15:8							
0x230	R560	DPLL1_FREE_RUN							
0x231	R561	DPLL1_PPM_REF_SEL	DPLL1_1PPS_MODE	DPLL1_1PPS_EN	RESERVED				
0x24E	R590	RESERVED						DPLL1_LCK_TIMER_9:8	
0x24F	R591	DPLL1_LCK_TIMER							
0x250	R592	RESERVED						DPLL1_HIST_TIMER_9:8	
0x251	R593	DPLL1_HIST_TIMER							
0x252	R594	RESERVED						DPLL1_HOLD_TIMER_9:8	
0x253	R595	DPLL1_HOLD_TIMER							
0x254	R596	RESERVED						DPLL1_PHS1_TIMER_9:8	
0x255	R597	DPLL1_PHS1_TIMER							
0x25A	R602	RESERVED			DPLL1_HIST_GAIN				
0x25B	R603	RESERVED		DPLL1_PL_THRESH					
0x25C	R604	RESERVED		DPLL1_PL_UNLK_THRESH					
0x25D	R605	RESERVED		DPLL1_PHS1_THRESH					
0x262	R610	RESERVED		DPLL1_STATUS_PL	RESERVED				

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x263	R611	RESERVED			DPLL1_DCO_SL EW_ACTIVE	RESERVED			
0x266	R614	RESERVED							DPLL1_FB_DIV_ 32:32
0x267	R615	DPLL1_FB_DIV_31:24							
0x268	R616	DPLL1_FB_DIV_23:16							
0x269	R617	DPLL1_FB_DIV_15:8							
0x26A	R618	DPLL1_FB_DIV							
0x26B	R619	DPLL1_FB_NUM_39:32							
0x26C	R620	DPLL1_FB_NUM_31:24							
0x26D	R621	DPLL1_FB_NUM_23:16							
0x26E	R622	DPLL1_FB_NUM_15:8							
0x26F	R623	DPLL1_FB_NUM							
0x270	R624	DPLL1_FB_DEN_39:32							
0x271	R625	DPLL1_FB_DEN_31:24							
0x272	R626	DPLL1_FB_DEN_23:16							
0x273	R627	DPLL1_FB_DEN_15:8							
0x274	R628	DPLL1_FB_DEN							
0x275	R629	RESERVED							DPLL1_FB2_DIV_ 32:32
0x276	R630	DPLL1_FB2_DIV_31:24							
0x277	R631	DPLL1_FB2_DIV_23:16							
0x278	R632	DPLL1_FB2_DIV_15:8							
0x279	R633	DPLL1_FB2_DIV							
0x27A	R634	DPLL1_FB2_NUM_39:32							
0x27B	R635	DPLL1_FB2_NUM_31:24							
0x27C	R636	DPLL1_FB2_NUM_23:16							
0x27D	R637	DPLL1_FB2_NUM_15:8							
0x27E	R638	DPLL1_FB2_NUM							
0x27F	R639	DPLL1_FB2_DEN_39:32							
0x280	R640	DPLL1_FB2_DEN_31:24							
0x281	R641	DPLL1_FB2_DEN_23:16							
0x282	R642	DPLL1_FB2_DEN_15:8							
0x283	R643	DPLL1_FB2_DEN							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x284	R644	RESERVED		DPLL1_REF5_F B_SEL	DPLL1_REF4_F B_SEL	RESERVED		DPLL1_REF1_F B_SEL	DPLL1_REF0_F B_SEL
0x285	R645	RESERVED						DPLL1_FB_MASH_ORDER	
0x286	R646	RESERVED		DPLL1_FB_FDEV_37:32					
0x287	R647	DPLL1_FB_FDEV_31:24							
0x288	R648	DPLL1_FB_FDEV_23:16							
0x289	R649	DPLL1_FB_FDEV_15:8							
0x28A	R650	DPLL1_FB_FDEV							
0x28B	R651	RESERVED							DPLL1_FB_FDE V_UPDATE
0x28C	R652	RESERVED							DPLL1_FB_FDE V_EN
0x28D	R653	DPLL1_FB_NUM_STAT_39:32							
0x28E	R654	DPLL1_FB_NUM_STAT_31:24							
0x28F	R655	DPLL1_FB_NUM_STAT_23:16							
0x290	R656	DPLL1_FB_NUM_STAT_15:8							
0x291	R657	DPLL1_FB_NUM_STAT							
0x292	R658	RESERVED				DPLL1_REF0_D BLR_EN	DPLL1_REF1_D BLR_EN	RESERVED	
0x293	R659	DPLL1_REF0_RDIV_15:8							
0x294	R660	DPLL1_REF0_RDIV							
0x295	R661	DPLL1_REF1_RDIV_15:8							
0x296	R662	DPLL1_REF1_RDIV							
0x29D	R669	DPLL1_REF5_RDIV_15:8							
0x29E	R670	DPLL1_REF5_RDIV							
0x2E9	R745	RESERVED		PLL3_NDIV_OU TPUT_EN	RESERVED				
0x305	R773	RESERVED							
0x309	R777	PLL2_CP_PU_R							
0x30A	R778	RESERVED			PLL2_CP_PU_DI S	PLL2_CPG			
0x30B	R779	PLL2_LF_R2							
0x30C	R780	RESERVED		PLL2_LF_R3					
0x30D	R781	RESERVED		PLL2_LF_R4					
0x30E	R782	PLL2_DISABLE_3RD4TH		PLL2_LF_C3			PLL2_LF_C4		
0x30F	R783	RESERVED							PLL2_RDIV_8:8

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x310	R784	PLL2_RDIV							
0x311	R785	RESERVED			PLL2_RDIV_XO_EN	PLL2_RDIV_XO_DBLR_EN	PLL2_RDIV_BYPASS_EN	PLL2_RDIV_MUX_SEL	
0x312	R786	RESERVED							PLL2_NDIV_8:8
0x313	R787	PLL2_NDIV							
0x314	R788	PLL2_NUM_MSB							
0x315	R789	PLL2_NUM_39:32							
0x316	R790	PLL2_NUM_31:24							
0x317	R791	PLL2_NUM_23:16							
0x318	R792	PLL2_NUM_15:8							
0x319	R793	PLL2_NUM							
0x31A	R794	RESERVED	PLL2_DTHRMODE			PLL2_ORDER			PLL2_MODE
0x31B	R795	APLL2_NUM_STAT_39:32							
0x31C	R796	APLL2_NUM_STAT_31:24							
0x31D	R797	APLL2_NUM_STAT_23:16							
0x31E	R798	APLL2_NUM_STAT_15:8							
0x31F	R799	APLL2_NUM_STAT							
0x323	R803	RESERVED			PLL2_VCO_BUF_EN	PLL2_VCO_BUF_2REF_EN		PLL2_VCO_BUF_2DPLL_EN	PLL2_VCO_BUF_2WNDDDET_EN
0x324	R804	RESERVED		PLL2_VCO_DIV_SYNC_EN	PLL2_VCO_DIV_EN	PLL2_VCO_DIV			
0x325	R805	RESERVED	PLL2_VCO_BUF_FB_TDC_EN		PLL2_P1_OUT14_15_EN	PLL2_P1_OUT8_13_EN	PLL2_P1_OUT4_7_EN	PLL2_P1_OUT2_3_EN	PLL2_P1_OUT0_1_EN
0x328	R808	RESERVED				PLL2_RDIV_OUTPUT_EN	RESERVED		
0x32D	R813	RESERVED		PLL2_VM_INSIDE	PLL2_VM_HI	RESERVED			
0x332	R818	RESERVED		PLL2_NDIV_OUTPUT_EN	RESERVED				
0x333	R819	RESERVED							PLL2_VCO_PREBUF_EN
0x348	R840	PLL1_CPBAW_BLEED							
0x349	R841	RESERVED			PLL1_CP_PU_DISS	PLL1_CPG			
0x34A	R842	RESERVED		PLL1_LF_R2					
0x34B	R843	RESERVED		PLL1_LF_R3					

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x34C	R844	RESERVED		PLL1_LF_R4					
0x34D	R845	RESERVED		PLL1_LF_C3			PLL1_LF_C4		
0x34E	R846	RESERVED							PLL1_RDIV_8:8
0x34F	R847	PLL1_RDIV							
0x350	R848	RESERVED			PLL1_RDIV_XO_EN	PLL1_RDIV_XO_DBLR_EN	PLL1_RDIV_BYPASS_EN	PLL1_RDIV_MUX_SEL	
0x351	R849	RESERVED							PLL1_NDIV_8:8
0x352	R850	PLL1_NDIV							
0x353	R851	PLL1_NUM_MSB							
0x354	R852	PLL1_NUM_39:32							
0x355	R853	PLL1_NUM_31:24							
0x356	R854	PLL1_NUM_23:16							
0x357	R855	PLL1_NUM_15:8							
0x358	R856	PLL1_NUM							
0x359	R857	RESERVED		PLL1_DTHRMODE		PLL1_ORDER			PLL1_MODE
0x35A	R858	APLL1_NUM_STAT_39:32							
0x35B	R859	APLL1_NUM_STAT_31:24							
0x35C	R860	APLL1_NUM_STAT_23:16							
0x35D	R861	APLL1_NUM_STAT_15:8							
0x35E	R862	APLL1_NUM_STAT							
0x360	R864	PLL1_VCO_BUF_OUT_EN				PLL1_VCO_DIV_SYNC_EN	PLL1_PRI_DIV		
0x361	R865	PLL1_VCO_DIV_SEL		PLL1_VCO_CHA_N_DRVR_IN_EN	PLL1_P1_OUT14_15_EN	PLL1_P1_OUT8_13_EN	PLL1_P1_OUT4_7_EN	PLL1_P1_OUT2_3_EN	PLL1_P1_OUT0_1_EN
0x362	R866	RESERVED			PLL1_VCO_BUF_2REF_EN		PLL1_WIN_DET_DRVR_EN	PLL1_VCO_BUF_FB_TDC_EN	
0x368	R872	RESERVED				PLL1_RDIV_OUTPUT_EN	RESERVED		
0x372	R882	RESERVED		PLL1_NDIV_OUTPUT_EN	RESERVED				
0x3C1	R961	RESERVED	OUT_0_EN	OUT_0_FMT					
0x3C2	R962	OUT_0_CAP_EN	OUT_0_STATIC_LOW	OUT_0_P_CMOS_EN	OUT_0_N_CMOS_EN	OUT_0_P_INVERT_POLARITY	OUT_0_N_INVERT_POLARITY	OUT_0_P_FORCE_LOW	OUT_0_N_FORCE_LOW
0x3C3	R963	OUT_0_CONFIGURATION							
0x3C4	R964	RESERVED	OUT_1_EN	OUT_1_FMT					

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x3C5	R965	OUT_1_CAP_EN	OUT_1_STATIC_LOW	OUT_1_P_CMO S_EN	OUT_1_N_CMO S_EN	OUT_1_P_INVE RT_POLARITY	OUT_1_N_INVE RT_POLARITY	OUT_1_P_FORC ELOW	OUT_1_N_FORC ELOW
0x3C6	R966	OUT_1_CONFIGURATION							
0x3C7	R967	RESERVED						OUT_0_1_CMOS _OUT_VOLTAGE _SEL	OUT_0_1_CMOS _OUT_LDO_EN
0x3C8	R968	RESERVED				OUT_0_1_ZDM_TDC_SEL			OUT_0_1_ZDM _EN
0x3C9	R969	RESERVED	OUT_0_1_DIV MUTE_EN	OUT_0_1_DIV_S YNC_EN	OUT_0_1_SR DI V_SYNC_EN	OUT_0_1_CH0 CHAN_POL_SEL	OUT_0_1_CH1 CHAN_POL_SEL	OUT_0_1_CH0 DIV_EN	OUT_0_1_CH1 DIV_EN
0x3CB	R971	OUT_0_1_CLK_IN_SEL							
0x3CC	R972	RESERVED						OUT_0_1_CH0 CH_DIV_SR MU X_CLK_SEL	RESERVED
0x3CD	R973	OUT_0_1_CLK_IN_FANOUT						OUT_0_1_CLK_IN_SEL_9:8	
0x3CE	R974	RESERVED				OUT_0_1_CH0_CH_STATIC_OFFSET_11:8			
0x3CF	R975	OUT_0_1_CH0_CH_STATIC_OFFSET							
0x3D0	R976	RESERVED				OUT_0_1_CH1_CH_STATIC_OFFSET_11:8			
0x3D1	R977	OUT_0_1_CH1_CH_STATIC_OFFSET							
0x3D2	R978	RESERVED				OUT_0_1_CH0_CH_DIV_11:8			
0x3D3	R979	OUT_0_1_CH0_CH_DIV							
0x3D4	R980	RESERVED				OUT_0_1_CH1_CH_DIV_11:8			
0x3D5	R981	OUT_0_1_CH1_CH_DIV							
0x3D6	R982	RESERVED			OUT_0_1_SR_ANA_DELAY				
0x3D7	R983	RESERVED		OUT_0_1_SR_A NA_DELAY_DIV2 _SEL	OUT_0_1_SR_A NA_DELAY_EN	OUT_0_1_SR_A NA_DELAY_SMA LL_STEP_EN	OUT_0_1_SR_ANA_DELAY_RANGE		
0x3D8	R984	RESERVED			OUT_0_1_SR_DDLY				
0x3D9	R985	RESERVED				OUT_0_1_SR_DIV_19:16			
0x3DA	R986	OUT_0_1_SR_DIV_15:8							
0x3DB	R987	OUT_0_1_SR_DIV							
0x3DC	R988	RESERVED	OUT_0_1_SR_DIV_STATIC_OFFSET_14:8						
0x3DD	R989	OUT_0_1_SR_DIV_STATIC_OFFSET							
0x3DE	R990	OUT_0_1_SR_R EQ_MODE	OUT_0_1_SR_G PIO_EN	RESERVED	OUT_0_1_PULSE_COUNT			OUT_0_1_SR_MODE	

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x3DF	R991	RESERVED		OUT_0_1_SR_C H0_DIV_BYPAS S	RESERVED				
0x400	R1024	RESERVED	OUT_2_EN	OUT_2_FMT					
0x401	R1025	RESERVED				OUT_2_CAP_EN	OUT_2_CONFIGURATION		
0x402	R1026	OUT_2_CHAN_P OL_SEL	OUT_2_CLK_MUX		RESERVED	OUT_2_DIV_EN	OUT_2_CH_MUX_SEL		
0x403	R1027	RESERVED			OUT_2_MUTE_E N	OUT_2_SYNC_E N	RESERVED		
0x404	R1028	RESERVED				OUT_2_CH_STATIC_OFFSET_11:8			
0x405	R1029	OUT_2_CH_STATIC_OFFSET							
0x406	R1030	RESERVED				OUT_2_CH_DIV_11:8			
0x407	R1031	OUT_2_CH_DIV							
0x420	R1056	RESERVED	OUT_3_EN	OUT_3_FMT					
0x421	R1057	RESERVED				OUT_3_CAP_EN	OUT_3_CONFIGURATION		
0x422	R1058	OUT_3_CHAN_P OL_SEL	OUT_3_CLK_MUX		RESERVED	OUT_3_DIV_EN	OUT_3_CH_MUX_SEL		
0x423	R1059	RESERVED			OUT_3_MUTE_E N	OUT_3_SYNC_E N	RESERVED		
0x424	R1060	RESERVED				OUT_3_CH_STATIC_OFFSET_11:8			
0x425	R1061	OUT_3_CH_STATIC_OFFSET							
0x426	R1062	RESERVED				OUT_3_CH_DIV_11:8			
0x427	R1063	OUT_3_CH_DIV							
0x440	R1088	RESERVED					OUT_4_5_SR_ANA_DLY_BIASTRIM		
0x441	R1089	RESERVED	OUT_4_EN	OUT_4_FMT					
0x442	R1090	RESERVED	OUT_4_CAP_EN	RESERVED	OUT_4_CONFIGURATION				
0x443	R1091	RESERVED	OUT_5_EN	OUT_5_FMT					
0x444	R1092	RESERVED	OUT_5_CAP_EN	RESERVED	OUT_5_CONFIGURATION				
0x445	R1093	RESERVED		OUT_4_5_DIV_S YNC_EN	OUT_4_5_SR_DI V_SYNC_EN	RESERVED		OUT_4_5_CHAN _POL_SEL	OUT_4_5_DIV_E N
0x446	R1094	OUT_4_5_MUTE _EN	OUT_4_5_ZDM _EN	OUT_4_5_CLK_I N_SEL	OUT_4_5_CH_DI V_SR_MUX_CLK _SEL	OUT_4_5_CH_MUX_SEL			
0x447	R1095	RESERVED				OUT_4_5_CH_STATIC_OFFSET_11:8			
0x448	R1096	OUT_4_5_CH_STATIC_OFFSET							
0x449	R1097	RESERVED				OUT_4_5_CH_DIV_11:8			

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x44A	R1098	OUT_4_5_CH_DIV							
0x44B	R1099	RESERVED			OUT_4_5_SR_ANA_DELAY				
0x44C	R1100	RESERVED		OUT_4_5_SR_A NA_DELAY_DIV2 _SEL	OUT_4_5_SR_A NA_DELAY_EN	OUT_4_5_SR_A NA_DELAY_SMA LL_STEP_EN	OUT_4_5_SR_ANA_DELAY_RANGE		
0x44D	R1101	RESERVED			OUT_4_5_SR_DDLY				
0x44E	R1102	RESERVED				OUT_4_5_SR_DIV_19:16			
0x44F	R1103	OUT_4_5_SR_DIV_15:8							
0x450	R1104	OUT_4_5_SR_DIV							
0x451	R1105	RESERVED	OUT_4_5_SR_DIV_STATIC_OFFSET_14:8						
0x452	R1106	OUT_4_5_SR_DIV_STATIC_OFFSET							
0x453	R1107	RESERVED	OUT_4_5_SR_R EQ_MODE	OUT_4_5_PULSE_COUNT			OUT_4_5_SR_G PIO_EN	OUT_4_5_SR_MODE	
0x454	R1108	RESERVED			OUT_4_5_SR_C H_DIV_BYPASS	RESERVED			
0x461	R1121	RESERVED	OUT_6_EN	OUT_6_FMT					
0x462	R1122	RESERVED	OUT_6_CAP_EN	RESERVED	OUT_6_CONFIGURATION				
0x463	R1123	RESERVED	OUT_7_EN	OUT_7_FMT					
0x464	R1124	RESERVED	OUT_7_CAP_EN	RESERVED	OUT_7_CONFIGURATION				
0x465	R1125	RESERVED		OUT_6_7_DIV_S YNC_EN	OUT_6_7_SR_DI V_SYNC_EN	RESERVED		OUT_6_7_CHAN _POL_SEL	OUT_6_7_DIV_E N
0x466	R1126	OUT_6_7_MUTE _EN	RESERVED	OUT_6_7_CLK_I N_SEL	OUT_6_7_CH_DI V_SR_MUX_CLK _SEL	OUT_6_7_CH_MUX_SEL			
0x467	R1127	RESERVED				OUT_6_7_CH_STATIC_OFFSET_11:8			
0x468	R1128	OUT_6_7_CH_STATIC_OFFSET							
0x469	R1129	RESERVED				OUT_6_7_CH_DIV_11:8			
0x46A	R1130	OUT_6_7_CH_DIV							
0x46B	R1131	RESERVED			OUT_6_7_SR_ANA_DELAY				
0x46C	R1132	RESERVED		OUT_6_7_SR_A NA_DELAY_DIV2 _SEL	OUT_6_7_SR_A NA_DELAY_EN	OUT_6_7_SR_A NA_DELAY_SMA LL_STEP_EN	OUT_6_7_SR_ANA_DELAY_RANGE		
0x46D	R1133	RESERVED			OUT_6_7_SR_DDLY				
0x46E	R1134	RESERVED				OUT_6_7_SR_DIV_19:16			
0x46F	R1135	OUT_6_7_SR_DIV_15:8							
0x470	R1136	OUT_6_7_SR_DIV							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x471	R1137	RESERVED	OUT_6_7_SR_DIV_STATIC_OFFSET_14:8						
0x472	R1138	OUT_6_7_SR_DIV_STATIC_OFFSET							
0x473	R1139	RESERVED	OUT_6_7_SR_R EQ_MODE	OUT_6_7_PULSE_COUNT			OUT_6_7_SR_G PIO_EN	OUT_6_7_SR_MODE	
0x474	R1140	RESERVED			OUT_6_7_SR_C H_DIV_BYPASS	RESERVED			
0x481	R1153	RESERVED	OUT_8_EN	OUT_8_FMT					
0x482	R1154	RESERVED	OUT_8_CAP_EN	RESERVED	OUT_8_CONFIGURATION				
0x483	R1155	RESERVED	OUT_9_EN	OUT_9_FMT					
0x484	R1156	RESERVED	OUT_9_CAP_EN	RESERVED	OUT_9_CONFIGURATION				
0x485	R1157	RESERVED		OUT_8_9_DIV_S YNC_EN	OUT_8_9_SR_DI V_SYNC_EN	RESERVED		OUT_8_9_CHAN _POL_SEL	OUT_8_9_DIV_E N
0x486	R1158	OUT_8_9_MUTE _EN	RESERVED	OUT_8_9_CLK_I N_SEL	OUT_8_9_CH_DI V_SR_MUX_CLK _SEL	OUT_8_9_CH_MUX_SEL			
0x487	R1159	RESERVED				OUT_8_9_CH_STATIC_OFFSET_11:8			
0x488	R1160	OUT_8_9_CH_STATIC_OFFSET							
0x489	R1161	RESERVED				OUT_8_9_CH_DIV_11:8			
0x48A	R1162	OUT_8_9_CH_DIV							
0x48B	R1163	RESERVED			OUT_8_9_SR_ANA_DELAY				
0x48C	R1164	RESERVED		OUT_8_9_SR_A NA_DELAY_DIV2 _SEL	OUT_8_9_SR_A NA_DELAY_EN	OUT_8_9_SR_A NA_DELAY_SMA LL_STEP_EN	OUT_8_9_SR_ANA_DELAY_RANGE		
0x48D	R1165	RESERVED			OUT_8_9_SR_DDLY				
0x48E	R1166	RESERVED				OUT_8_9_SR_DIV_19:16			
0x48F	R1167	OUT_8_9_SR_DIV_15:8							
0x490	R1168	OUT_8_9_SR_DIV							
0x491	R1169	RESERVED	OUT_8_9_SR_DIV_STATIC_OFFSET_14:8						
0x492	R1170	OUT_8_9_SR_DIV_STATIC_OFFSET							
0x493	R1171	RESERVED	OUT_8_9_SR_R EQ_MODE	OUT_8_9_PULSE_COUNT			OUT_8_9_SR_G PIO_EN	OUT_8_9_SR_MODE	
0x4A1	R1185	RESERVED	OUT_10_EN	OUT_10_FMT					
0x4A2	R1186	RESERVED	OUT_10_CAP_E N	RESERVED	OUT_10_CONFIGURATION				
0x4A3	R1187	RESERVED	OUT_11_EN	OUT_11_FMT					
0x4A4	R1188	RESERVED	OUT_11_CAP_E N	RESERVED	OUT_11_CONFIGURATION				

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x4A5	R1189	RESERVED		OUT_10_11_DIV_SYNC_EN	OUT_10_11_SR_DIV_SYNC_EN	RESERVED		OUT_10_11_CH_AN_POL_SEL	OUT_10_11_DIV_EN
0x4A6	R1190	OUT_10_11_MUTE_EN	OUT_10_11_ZDM_EN	OUT_10_11_CLK_IN_SEL	OUT_10_11_CH_DIV_SR_MUX_CLK_SEL	OUT_10_11_CH_MUX_SEL			
0x4A7	R1191	RESERVED				OUT_10_11_CH_STATIC_OFFSET_11:8			
0x4A8	R1192	OUT_10_11_CH_STATIC_OFFSET							
0x4A9	R1193	RESERVED				OUT_10_11_CH_DIV_11:8			
0x4AA	R1194	OUT_10_11_CH_DIV							
0x4AB	R1195	RESERVED			OUT_10_11_SR_ANA_DELAY				
0x4AC	R1196	RESERVED		OUT_10_11_SR_ANA_DELAY_DIV2_SEL	OUT_10_11_SR_ANA_DELAY_EN	OUT_10_11_SR_ANA_DELAY_SMA_ALL_STEP_EN	OUT_10_11_SR_ANA_DELAY_RANGE		
0x4AD	R1197	RESERVED			OUT_10_11_SR_DDLY				
0x4AE	R1198	RESERVED				OUT_10_11_SR_DIV_19:16			
0x4AF	R1199	OUT_10_11_SR_DIV_15:8							
0x4B0	R1200	OUT_10_11_SR_DIV							
0x4B1	R1201	RESERVED	OUT_10_11_SR_DIV_STATIC_OFFSET_14:8						
0x4B2	R1202	OUT_10_11_SR_DIV_STATIC_OFFSET							
0x4B3	R1203	RESERVED	OUT_10_11_SR_REQ_MODE	OUT_10_11_PULSE_COUNT			OUT_10_11_SR_GPIO_EN	OUT_10_11_SR_MODE	
0x4B4	R1204	RESERVED			OUT_10_11_SR_CH_DIV_BYPASS	RESERVED			
0x4C1	R1217	RESERVED	OPTIMIZE_R1217_b6	OUT_12_FMT					
0x4C2	R1218	RESERVED	OUT_12_CAP_EN	RESERVED	OPTIMIZE_R1218_b4to0				
0x4C3	R1219	RESERVED	OPTIMIZE_R1219_b6	OUT_13_FMT					
0x4C4	R1220	RESERVED	OUT_13_CAP_EN	RESERVED	OPTIMIZE_R1220_b4to0				
0x4C5	R1221	RESERVED		OUT_12_13_DIV_SYNC_EN	OUT_12_13_SR_DIV_SYNC_EN	RESERVED		OUT_12_13_CH_AN_POL_SEL	OUT_12_13_DIV_EN
0x4C6	R1222	OUT_12_13_MUTE_EN	RESERVED	OPTIMIZE_R1222_b5	OUT_12_13_CH_DIV_SR_MUX_CLK_SEL	OUT_12_13_CH_MUX_SEL			
0x4C7	R1223	RESERVED				OUT_12_13_CH_STATIC_OFFSET_11:8			

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x4C8	R1224	OUT_12_13_CH_STATIC_OFFSET							
0x4C9	R1225	RESERVED				OUT_12_13_CH_DIV_11:8			
0x4CA	R1226	OUT_12_13_CH_DIV							
0x4CB	R1227	RESERVED			OUT_12_13_SR_ANA_DELAY				
0x4CC	R1228	RESERVED		OUT_12_13_SR_ANA_DELAY_DIV2_SEL	OUT_12_13_SR_ANA_DELAY_EN	OUT_12_13_SR_ANA_DELAY_SMALL_STEP_EN	OUT_12_13_SR_ANA_DELAY_RANGE		
0x4CD	R1229	RESERVED			OUT_12_13_SR_DDLY				
0x4CE	R1230	RESERVED				OUT_12_13_SR_DIV_19:16			
0x4CF	R1231	OUT_12_13_SR_DIV_15:8							
0x4D0	R1232	OUT_12_13_SR_DIV							
0x4D1	R1233	RESERVED	OUT_12_13_SR_DIV_STATIC_OFFSET_14:8						
0x4D2	R1234	OUT_12_13_SR_DIV_STATIC_OFFSET							
0x4D3	R1235	RESERVED	OUT_12_13_SR_REQ_MODE	OUT_12_13_PULSE_COUNT			OUT_12_13_SR_GPIO_EN	OUT_12_13_SR_MODE	
0x4D4	R1236	RESERVED			OUT_12_13_SR_CH_DIV_BYPASS	RESERVED			
0x4E0	R1248	RESERVED	OPTIMIZE_R1248_b6	OUT_14_FMT					
0x4E1	R1249	RESERVED				OUT_14_CAP_EN	OUT_14_CONFIGURATION		
0x4E2	R1250	OUT_14_CHAN_POL_SEL	OUT_14_CLK_MUX		RESERVED	OUT_14_DIV_EN	OUT_14_CH_MUX_SEL		
0x4E3	R1251	RESERVED			OUT_14_MUTE_EN	OUT_14_SYNC_EN	RESERVED		
0x4E4	R1252	RESERVED				OUT_14_CH_STATIC_OFFSET_11:8			
0x4E5	R1253	OUT_14_CH_STATIC_OFFSET							
0x4E6	R1254	RESERVED				OUT_14_CH_DIV_11:8			
0x4E7	R1255	OUT_14_CH_DIV							
0x500	R1280	RESERVED	OPTIMIZE_R1280_b6	OUT_15_FMT					
0x501	R1281	RESERVED				OUT_15_CAP_EN	OUT_15_CONFIGURATION		
0x502	R1282	OUT_15_CHAN_POL_SEL	OUT_15_CLK_MUX		RESERVED	OUT_15_DIV_EN	OUT_15_CH_MUX_SEL		
0x503	R1283	RESERVED			OUT_15_MUTE_EN	OUT_15_SYNC_EN	RESERVED		

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x504	R1284	RESERVED				OUT_15_CH_STATIC_OFFSET_11:8			
0x505	R1285	OUT_15_CH_STATIC_OFFSET							
0x506	R1286	RESERVED				OUT_15_CH_DIV_11:8			
0x507	R1287	OUT_15_CH_DIV							

Complex bit access types are encoded to fit into small table cells. [Table 1-2](#) shows the codes that are used for access types in this section.

Table 1-2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W1S	W 1S	Write 1 to set
WSC	W	Write
Reset or Default Value		
-n		Value after reset or the default value

1.1 R0 (Offset = 0x0)

Return to the [Summary Table](#).

Table 1-3. R0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VNDRID_15:8	R	0x10	See Register 1

1.2 R1 (Offset = 0x1)

Return to the [Summary Table](#).

Table 1-4. R1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VNDRID	R	0xB	Vendor Identification Number. The Vendor Identification Number is a unique 16-bit identification number assigned to I2C/SMBus vendors. ROM=N, EEPROM=N

1.3 R2 (Offset = 0x2)

Return to the [Summary Table](#).

Table 1-5. R2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRODID	R	0x42	Product ID. ROM=N, EEPROM=N

1.4 R3 (Offset = 0x3)

Return to the [Summary Table](#).

Table 1-6. R3 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REVID	R	0x4	Revision ID. ROM=N, EEPROM=N

1.5 R4 (Offset = 0x4)

Return to the [Summary Table](#).

Table 1-7. R4 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRTID_47:40	R	0x0	Part ID. Used for manufacturing ROM=N, EEPROM=Y

1.6 R5 (Offset = 0x5)

Return to the [Summary Table](#).

Table 1-8. R5 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRTID_39:32	R	0x0	Part ID. Used for manufacturing ROM=N, EEPROM=Y

1.7 R6 (Offset = 0x6)

Return to the [Summary Table](#).

Table 1-9. R6 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRTID_31:24	R	0x0	Part ID. Used for manufacturing ROM=N, EEPROM=Y

1.8 R7 (Offset = 0x7)

Return to the [Summary Table](#).

Table 1-10. R7 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRTID_23:16	R	0x0	Part ID. Used for manufacturing ROM=N, EEPROM=Y

1.9 R8 (Offset = 0x8)

Return to the [Summary Table](#).

Table 1-11. R8 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRTID_15:8	R	0x0	Part ID. Used for manufacturing ROM=N, EEPROM=Y

1.10 R9 (Offset = 0x9)

Return to the [Summary Table](#).

Table 1-12. R9 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRTID	R	0x0	Part ID. Used for manufacturing ROM=N, EEPROM=Y

1.11 R16 (Offset = 0x10)

Return to the [Summary Table](#).

Table 1-13. R16 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMCNT	R	0x12	NVM Program Count. The NVMCNT increments automatically after every EEPROM Erase/Program Cycle. The NVMCNT value is retrieved automatically after reset, after a NVM Commit operation, or after a Erase/Program cycle. The NVMCNT register will increment until it reaches it's maximum value of 255 after which no further increments will take place. ROM=N, EEPROM=Y

1.12 R18 (Offset = 0x12)

Return to the [Summary Table](#).

Table 1-14. R18 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	TARGET_ADR_MSB	R	0x19	I2C/SMBus Target Address. This field holds the 5 MSB bits of the Target Address used to identify this device during I2C/SMBus transactions. The two least significant bits of the Target Address are defined by CSC/ADD/TEC pin upon power-up. This is user-writable to EEPROM only through SRAM register at address 12. ROM=N, EEPROM=Y

1.13 R19 (Offset = 0x13)

Return to the [Summary Table](#).

Table 1-15. R19 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	EEREV	R/W	0x0	EEPROM Image Revision ID. EEPROM Image Revision is automatically retrieved from EEPROM and stored in the EEREV register after a reset or after a NVM commit operation. This is user-writable to EEPROM only through SRAM register address 13. ROM=N, EEPROM=Y

1.14 R20 (Offset = 0x14)

Return to the [Summary Table](#).

Table 1-16. R20 Field Descriptions

Bit	Field	Type	Reset	Description
7	ROM_PLUS_EE	R/W	0x0	When set, the thin EEPROM settings are loaded. This is user-writable to EEPROM only through SRAM register address 14. ROM=N, EEPROM=Y
6:3	EE_ROM_PAGE_SEL	R/W	0x0	EE_ROM_PAGE_SEL value is added to the GPIO pin value for selecting the start-up ROM. ROM=N, EEPROM=Y
2:0	RESERVED	R	0x0	Reserved

1.15 R21 (Offset = 0x15)

Return to the [Summary Table](#).

Table 1-17. R21 Field Descriptions

Bit	Field	Type	Reset	Description
7	SPI_3WIRE_DIS	R/W	0x1	Disable SPI 3 wire readback. The SDIO pin will remain input at all times. ROM=Y, EEPROM=N 0x0 = 3-wire SPI readback enabled 0x1 = 3-wire SPI readback disabled
6	SYNC_SW	R/W	0x0	Software SYNC Assertion. Writing a '1' to this bit is equivalent to asserting the SYNC pin. SYNC_EN must also be set to 1. ROM=Y, EEPROM=Y
5:0	RESERVED	R	0x0	Reserved

1.16 R22 (Offset = 0x16)

Return to the [Summary Table](#).

Table 1-18. R22 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	DP1L1_EN	R/W	0x1	Enable DP1L1. ROM=Y, EEPROM=N
4	AP1L1_EN	R/W	0x1	Enable AP1L1. ROM=Y, EEPROM=Y
3	DP1L2_EN	R/W	0x0	Enable DP1L2. ROM=Y, EEPROM=N
2	AP1L2_EN	R/W	0x1	Enable AP1L2. ROM=Y, EEPROM=Y
1:0	RESERVED	R	0x0	Reserved

1.17 R23 (Offset = 0x17)

Return to the [Summary Table](#).

Table 1-19. R23 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	SWRST	R/W	0x0	Software Reset ALL functions (active low). Writing a '0' will cause the device to return to its power-up state apart from the programmed registers and the configuration controller. The configuration controller is excluded to prevent an re-transfer of EEPROM data to on-chip registers. Not a self clearing field. ROM=N, EEPROM=N
5	RESERVED	R	0x0	
4	DPLL2_SWRST	R-0/W1S	0x0	Software Reset DPLL2. Setting to '1' resets the DPLL loop filter. This bit is automatically cleared to '0'. ROM=N, EEPROM=N
3	DPLL1_SWRST	R-0/W1S	0x0	Software Reset DPLL1. Setting to '1' resets the DPLL loop filter. This bit is automatically cleared to '0'. ROM=N, EEPROM=N Software Reset DPLL1.. Setting to '1' resets the DPLL loop filter.This bit is automatically cleared to '0'. ROM=N, EEPROM=N
2	RESERVED	R	0x0	
1	APLL2_SWRST	R-0/W1S	0x0	Software Reset PLL2. Setting to '1' resets the PLL Calibrator, the PLL N Divider, R Divider and VCO Divider. The PLL Calibrator then takes control of the N Divider reset. This bit is automatically cleared to '0'. It does not reset the divider driving the CMOS Outputs. ROM=N, EEPROM=N
0	APLL1_SWRST	R-0/W1S	0x0	Software Reset PLL1. Setting to '1' resets the PLL Calibrator, the PLL N Divider, R Divider and VCO Divider. The PLL Calibrator then takes control of the N Divider reset. This bit is automatically cleared to '0'. It does not reset the divider driving the CMOS Outputs. ROM=N, EEPROM=N

1.18 R24 (Offset = 0x18)

Return to the [Summary Table](#).

Table 1-20. R24 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:4	APLL1_STRT_PRTY	R/W	0x0	APLL1 Start-up Priority. 0 is highest priority. APLLs with the same priority will start simultaneously. ROM=Y, EEPROM=Y
3:2	APLL2_STRT_PRTY	R/W	0x2	APLL2 Start-up Priority. 0 is highest priority. APLLs with the same priority will start simultaneously. ROM=Y, EEPROM=Y

Table 1-20. R24 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	RESERVED	R	0x0	Reserved

1.19 R25 (Offset = 0x19)

Return to the [Summary Table](#).

Table 1-21. R25 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:1	RESERVED	R	0x0	Reserved
0	SYNC_EN	R/W	0x1	Allows SYNC from SYNC_SW and GPIO pin. For GPIO sync, must be set together with SYNC input for GPIOx_MODE. ROM=Y, EEPROM=Y

1.20 R26 (Offset = 0x1A)

Return to the [Summary Table](#).

Table 1-22. R26 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:4	SYSREF_REQ_MODE	R/W	0x3	SYSREF Request Mode. Determines how a GPIO input is synchronized to generate a SYSREF request. ROM=Y, EEPROM=N 0x0 = Direct SYSREF request 0x1 = Reserved 0x2 = Reserved 0x3 = Resampled SYSREF request
3:1	SYSREF_REQ_SEL	R/W	0x3	SYSREF Request Select. Choses which output drives the SYSREF feedback clock. ROM=Y, EEPROM=N 0x0 = SYSREF0_1_CLK 0x1 = SYSREF4_5_CLK 0x2 = SYSREF6_7_CLK 0x3 = SYSREF8_9_CLK 0x4 = SYSREF10_11_CLK 0x5 = Reserved 0x6 = Reserved
0	SYSREF_REQ_SW	R/WSC	0x0	Software SYSREF request trigger ROM=N, EEPROM=N

1.21 R27 (Offset = 0x1B)

Return to the [Summary Table](#).

Table 1-23. R27 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEC_CNTR_39:32	R	0x0	Time Elapsed Counter Readback ROM=N, EEPROM=N

1.22 R28 (Offset = 0x1C)

Return to the [Summary Table](#).

Table 1-24. R28 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEC_CNTR_31:24	R	0x0	Time Elapsed Counter Readback ROM=N, EEPROM=N

1.23 R29 (Offset = 0x1D)

Return to the [Summary Table](#).

Table 1-25. R29 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEC_CNTR_23:16	R	0x0	Time Elapsed Counter Readback ROM=N, EEPROM=N

1.24 R30 (Offset = 0x1E)

Return to the [Summary Table](#).

Table 1-26. R30 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEC_CNTR_15:8	R	0x0	Time Elapsed Counter Readback ROM=N, EEPROM=N

1.25 R31 (Offset = 0x1F)

Return to the [Summary Table](#).

Table 1-27. R31 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEC_CNTR	R	0x0	Time Elapsed Counter Readback ROM=N, EEPROM=N

1.26 R32 (Offset = 0x20)

Return to the [Summary Table](#).

Table 1-28. R32 Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	TEC_CNTR_TRIG_SEL	R/W	0x0	Time Elapsed Counter trigger select. If using GPIO, must also set GPIOx_MODE to provide TEC trigger. ROM=Y, EEPROM=N 0x0 = SPI 0x1 = GPIO
0	TEC_CNTR_EN	R/W	0x0	Time Elapsed Counter counter enable. When transitioning from 0 --> 1, the TEC counter will start from 0. ROM=Y, EEPROM=N

1.27 R33 (Offset = 0x21)

Return to the [Summary Table](#).

Table 1-29. R33 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	LOL_PLL2	R	0x0	Loss of Lock - APLL2 ROM=N, EEPROM=N
1	RESERVED	R	0x0	Reserved
0	LOS_FDET_XO	R	0x0	Loss of Source Freq Detection - XO ROM=N, EEPROM=N

1.28 R35 (Offset = 0x23)

Return to the [Summary Table](#).

Table 1-30. R35 Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL2	R	0x0	Loss of Phase Lock - DPLL2 ROM=N, EEPROM=N
6	LOFL_DPLL2	R	0x0	Loss of Frequency Lock - DPLL2 ROM=N, EEPROM=N
5	RESERVED	R	0x0	Reserved
4	HLDOVR2	R	0x0	Holdover event - DPLL2 ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.29 R37 (Offset = 0x25)

Return to the [Summary Table](#).

Table 1-31. R37 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	LOL_PLL2_MASK	R/W	0x0	Masks Loss of Lock - APLL2. When LOL_PLL2_MASK is 1 then the LOL_PLL2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
1	RESERVED	R	0x0	Reserved
0	LOS_FDET_XO_MASK	R/W	0x0	Masks Loss of Source Freq Detection - XO. When LOS_FDET_XO_MASK is 1 then the LOS_FDET_XO interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N

1.30 R39 (Offset = 0x27)

Return to the [Summary Table](#).

Table 1-32. R39 Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL2_MASK	R/W	0x1	Masks Loss of Phase Lock - DPLL2. When LOPL_DPLL2_MASK is 1 then the LOPL_DPLL2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
6	LOFL_DPLL2_MASK	R/W	0x1	Masks Loss of Freq Lock - DPLL2. When LOFL_DPLL2_MASK is 1 then the LOFL_DPLL2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N

Table 1-32. R39 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	HIST2_MASK	R/W	0x1	Masks Tuning word history update - DPLL2. When HIST2_MASK is 1 then the HIST2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
4	HLDOVR2_MASK	R/W	0x1	Masks Holdover event - DPLL2. When HLDOVR2_MASK is 1 then the HLDOVR2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
3	REFSWITCH2_MASK	R/W	0x1	Masks Reference Switchover - DPLL2. When REFSWITCH2_MASK is 1 then the REFSWITCH2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
2	LOR_MISSCLK2_MASK	R/W	0x1	Masks Loss of Active Reference - Missing Clock - DPLL2. When LOR_MISSCLK2_MASK is 1 then the LOR_MISSCLK2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
1	LOR_FREQ2_MASK	R/W	0x1	Masks Loss of Active Reference - Frequency - DPLL2. When LOR_FREQ2_MASK is 1 then the LOR_FREQ2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
0	LOR_PH2_MASK	R/W	0x1	Masks Loss of Active Reference - Phase - DPLL2. When LOR_PH2_MASK is 1 then the LOR_PH2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N

1.31 R40 (Offset = 0x28)

Return to the [Summary Table](#).

Table 1-33. R40 Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL1_MASK	R/W	0x0	Masks Loss of Phase Lock - DPLL1. When LOPL_DPLL1_MASK is 1 then the LOPL_DPLL1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
6	LOFL_DPLL1_MASK	R/W	0x0	Masks Loss of Freq Lock - DPLL1. When LOFL_DPLL1_MASK is 1 then the LOFL_DPLL1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
5	HIST1_MASK	R/W	0x1	Masks Tuning word history update - DPLL1. When HIST1_MASK is 1 then the HIST1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
4	HLDOVR1_MASK	R/W	0x0	Masks Holdover event - DPLL1. When HLDOVR1_MASK is 1 then the HLDOVR3 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N

Table 1-33. R40 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	REFSWITCH1_MASK	R/W	0x0	Masks Reference Switchover - DPLL1. When REFSWITCH1_MASK is 1 then the REFSWITCH1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
2	LOR_MISSCLK1_MASK	R/W	0x0	Masks Loss of Active Reference - Missing Clock - DPLL1. When LOR_MISSCLK1_MASK is 1 then the LOR_MISSCLK1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
1	LOR_FREQ1_MASK	R/W	0x0	Masks Loss of Active Reference - Frequency - DPLL1. When LOR_FREQ1_MASK is 1 then the LOR_FREQ1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
0	LOR_PH1_MASK	R/W	0x0	Masks Loss of Active Reference - Phase - DPLL1. When LOR_PH1_MASK is 1 then the LOR_PH1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N

1.32 R41 (Offset = 0x29)

Return to the [Summary Table](#).

Table 1-34. R41 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	LOL_PLL2_POL	R/W	0x0	LOL_PLL2 Flag Polarity. When LOL_PLL2_POL = 1, LOL_PLL2 = 0 results in LOL_PLL2_INTR = 1. When LOL_PLL2_POL = 0, LOL_PLL2 = 1 results in LOL_PLL2_INTR = 1. ROM=Y, EEPROM=N
1	RESERVED	R	0x0	Reserved
0	LOS_FDET_XO_POL	R/W	0x0	LOS_FDET_XO Flag Polarity. When LOS_FDET_XO_POL = 1, LOS_FDET_XO = 0 results in LOS_FDET_XO_INTR = 1. When LOS_FDET_XO_POL = 0, LOS_FDET_XO = 1 results in LOS_FDET_XO_INTR = 1. ROM=Y, EEPROM=N

1.33 R43 (Offset = 0x2B)

Return to the [Summary Table](#).

Table 1-35. R43 Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL2_POL	R/W	0x0	LOPL_DPLL2 Flag Polarity. When LOPL_DPLL2_POL = 1, LOPL_DPLL2 = 0 results in LOPL_DPLL2_INTR = 1. When LOPL_DPLL2_POL = 0, LOPL_DPLL2 = 1 results in LOPL_DPLL2_INTR = 1. ROM=Y, EEPROM=N
6	LOFL_DPLL2_POL	R/W	0x0	LOFL_DPLL2 Flag Polarity. When LOFL_DPLL2_POL = 1, LOFL_DPLL2 = 0 results in LOFL_DPLL2_INTR = 1. When LOFL_DPLL2_POL = 0, LOFL_DPLL2 = 1 results in LOFL_DPLL2_INTR = 1. ROM=Y, EEPROM=N
5	HIST2_POL	R/W	0x0	HIST2 Flag Polarity. When HIST2_POL = 1, HIST2 = 0 results in HIST2_INTR = 1. When HIST2_POL = 0, HIST2 = 1 results in HIST2_INTR = 1. ROM=Y, EEPROM=N
4	HLDOVR2_POL	R/W	0x0	HLDOVR2 Flag Polarity. When HLDOVR2_POL = 1, HLDOVR2 = 0 results in HLDOVR2_INTR = 1. When HLDOVR2_POL = 0, HLDOVR2 = 1 results in HLDOVR2_INTR = 1. ROM=Y, EEPROM=N
3	REFSWITCH2_POL	R/W	0x0	REFSWITCH2 Flag Polarity. When REFSWITCH2_POL = 1, REFSWITCH2 = 0 results in REFSWITCH2_INTR = 1. When REFSWITCH2_POL = 0, REFSWITCH2 = 1 results in REFSWITCH2_INTR = 1. ROM=Y, EEPROM=N
2	LOR_MISSCLK2_POL	R/W	0x0	LOR_MISSCLK2 Flag Polarity. When LOR_MISSCLK2_POL = 1, LOR_MISSCLK2 = 0 results in LOR_MISSCLK2_INTR = 1. When LOR_MISSCLK2_POL = 0, LOR_MISSCLK2 = 1 results in LOR_MISSCLK2_INTR = 1. ROM=Y, EEPROM=N
1	LOR_FREQ2_POL	R/W	0x0	LOR_FREQ2 Flag Polarity. When LOR_FREQ2_POL = 1, LOR_FREQ2 = 0 results in LOR_FREQ2_INTR = 1. When LOR_FREQ2_POL = 0, LOR_FREQ2 = 1 results in LOR_FREQ2_INTR = 1. ROM=Y, EEPROM=N
0	LOR_PH2_POL	R/W	0x0	LOR_PH2 Flag Polarity. When LOR_PH2_POL = 1, LOR_PH2 = 0 results in LOR_PH2_INTR = 1. When LOR_PH2_POL = 0, LOR_PH2 = 1 results in LOR_PH2_INTR = 1. ROM=Y, EEPROM=N

1.34 R44 (Offset = 0x2C)

Return to the [Summary Table](#).

Table 1-36. R44 Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL1_POL	R/W	0x0	LOPL_DPLL1 Flag Polarity. When LOPL_DPLL1_POL = 1, LOPL_DPLL1 = 0 results in LOPL_DPLL1_INTR = 1. When LOPL_DPLL1_POL = 0, LOPL_DPLL1 = 1 results in LOPL_DPLL1_INTR = 1. ROM=Y, EEPROM=N

Table 1-36. R44 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	LOFL_DPLL1_POL	R/W	0x0	LOFL_DPLL1 Flag Polarity. When LOFL_DPLL1_POL = 1, LOFL_DPLL1 = 0 results in LOFL_DPLL1_INTR = 1. When LOFL_DPLL1_POL = 0, LOFL_DPLL1 = 1 results in LOFL_DPLL1_INTR = 1. ROM=Y, EEPROM=N
5	HIST1_POL	R/W	0x0	HIST1 Flag Polarity. When HIST1_POL = 1, HIST1 = 0 results in HIST1_INTR = 1. When HIST1_POL = 0, HIST1 = 1 results in HIST1_INTR = 1 ROM=Y, EEPROM=N
4	HLDOVR1_POL	R/W	0x0	HLDOVR1 Flag Polarity. When HLDOVR1_POL = 1, HLDOVR1 = 0 results in HLDOVR1_INTR = 1. When HLDOVR1_POL = 0, HLDOVR1 = 1 results in HLDOVR1_INTR = 1. ROM=Y, EEPROM=N
3	REFSWITCH1_POL	R/W	0x0	REFSWITCH1 Flag Polarity. When REFSWITCH1_POL = 1, REFSWITCH1 = 0 results in REFSWITCH1_INTR = 1. When REFSWITCH1_POL = 0, REFSWITCH1 = 1 results in REFSWITCH1_INTR = 1. ROM=Y, EEPROM=N
2	LOR_MISSCLK1_POL	R/W	0x0	LOR_MISSCLK1 Flag Polarity. When LOR_MISSCLK1_POL = 1, LOR_MISSCLK1 = 0 results in LOR_MISSCLK1_INTR = 1. When LOR_MISSCLK1_POL = 0, LOR_MISSCLK1 = 1 results in LOR_MISSCLK1_INTR = 1. ROM=Y, EEPROM=N
1	LOR_FREQ1_POL	R/W	0x0	LOR_FREQ1 Flag Polarity. When LOR_FREQ1_POL = 1, LOR_FREQ1 = 0 results in LOR_FREQ1_INTR = 1. When LOR_FREQ1_POL = 0, LOR_FREQ1 = 1 results in LOR_FREQ1_INTR = 1. ROM=Y, EEPROM=N
0	LOR_PH1_POL	R/W	0x0	LOR_PH1 Flag Polarity. When LOR_PH1_POL = 1, LOR_PH1 = 0 results in LOR_PH1_INTR = 1. When LOR_PH1_POL = 0, LOR_PH1 = 1 results in LOR_PH1_INTR = 1. ROM=Y, EEPROM=N

1.35 R45 (Offset = 0x2D)

Return to the [Summary Table](#).

Table 1-37. R45 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	LOL_PLL2_INTR	R	0x1	LOL_PLL2 Interrupt. The LOL_PLL2_INTR bit is set when a level of the correct polarity is detected on the LOL_PLL2 interrupt source. The LOL_PLL2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
1	RESERVED	R	0x0	Reserved

Table 1-37. R45 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LOS_FDET_XO_INTR	R	0x1	LOL_FDET_XO Interrupt. The LOL_FDET_XO_INTR bit is set when a level of the correct polarity is detected on the LOL_FDET_XO interrupt source. The LOL_FDET_XO_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N

1.36 R47 (Offset = 0x2F)

Return to the [Summary Table](#).

Table 1-38. R47 Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL2_INTR	R	0x1	LOPL_DPLL2 Interrupt. The LOPL_DPLL2_INTR bit is set when a level of the correct polarity is detected on the LOPL_DPLL2 interrupt source. The LOPL_DPLL2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
6	LOFL_DPLL2_INTR	R	0x1	LOFL_DPLL2 Interrupt. The LOFL_DPLL2_INTR bit is set when a level of the correct polarity is detected on the LOFL_DPLL2 interrupt source. The LOFL_DPLL2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
5	HIST2_INTR	R	0x1	HIST2 Interrupt. The HIST2_INTR bit is set when a level of the correct polarity is detected on the HIST2 interrupt source. The HIST2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
4	HLDOVR2_INTR	R	0x1	HLDOVR2 Interrupt. The HLDOVR2_INTR bit is set when a level of the correct polarity is detected on the HLDOVR2 interrupt source. The HLDOVR2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
3	REFSWITCH2_INTR	R	0x1	REFSWITCH2 Interrupt. The REFSWITCH2_INTR bit is set when a level of the correct polarity is detected on the REFSWITCH2 interrupt source. The REFSWITCH2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
2	LOR_MISSCLK2_INTR	R	0x0	LOR_MISSCLK2 Interrupt. The LOR_MISSCLK2_INTR bit is set when a level of the correct polarity is detected on the LOR_MISSCLK2 interrupt source. The LOR_MISSCLK2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
1	LOR_FREQ2_INTR	R	0x0	LOR_FREQ2 Interrupt. The LOR_FREQ2_INTR bit is set when a level of the correct polarity is detected on the LOR_FREQ2 interrupt source. The LOR_FREQ2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
0	LOR_PH2_INTR	R	0x0	LOR_PH2 Interrupt. The LOR_PH2_INTR bit is set when a level of the correct polarity is detected on the LOR_PH2 interrupt source. The LOR_PH2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N

1.37 R48 (Offset = 0x30)

Return to the [Summary Table](#).

Table 1-39. R48 Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL1_INTR	R	0x1	LOPL_DPLL1 Interrupt. The LOPL_DPLL1_INTR bit is set when a level of the correct polarity is detected on the LOPL_DPLL1 interrupt source. The LOPL_DPLL1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
6	LOFL_DPLL1_INTR	R	0x1	LOFL_DPLL1 Interrupt. The LOFL_DPLL1_INTR bit is set when a level of the correct polarity is detected on the LOFL_DPLL1 interrupt source. The LOFL_DPLL1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
5	HIST1_INTR	R	0x0	HIST1 Interrupt. The HIST1_INTR bit is set when a level of the correct polarity is detected on the HIST1 interrupt source. The HIST1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
4	HLDOVR1_INTR	R	0x1	HLDOVR1 Interrupt. The HLDOVR1_INTR bit is set when a level of the correct polarity is detected on the HLDOVR1 interrupt source. The HLDOVR1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
3	REFSWITCH1_INTR	R	0x1	REFSWITCH1 Interrupt. The REFSWITCH1_INTR bit is set when a level of the correct polarity is detected on the REFSWITCH1 interrupt source. The REFSWITCH1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
2	LOR_MISSCLK1_INTR	R	0x0	LOR_MISSCLK1 Interrupt. The LOR_MISSCLK1_INTR bit is set when a level of the correct polarity is detected on the LOR_MISSCLK1 interrupt source. The LOR_MISSCLK1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
1	LOR_FREQ1_INTR	R	0x0	LOR_FREQ1 Interrupt. The LOR_FREQ1_INTR bit is set when a level of the correct polarity is detected on the LOR_FREQ1 interrupt source. The LOR_FREQ1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
0	LOR_PH1_INTR	R	0x0	LOR_PH1 Interrupt. The LOR_PH1_INTR bit is set when a level of the correct polarity is detected on the LOR_PH1 interrupt source. The LOR_PH1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N

1.38 R49 (Offset = 0x31)

Return to the [Summary Table](#).

Table 1-40. R49 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved

Table 1-40. R49 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	INT_LATCH_OR_LIVE	R/W	0x0	ROM=Y, EEPROM=N 0x0 = Latch Mode 0x1 = Live Mode
2	INT_AND_OR	R/W	0x0	Interrupt AND/OR Combination. If INT_AND_OR is 1, then the interrupts are combined in an AND structure, in which case ALL un-masked interrupt flags must be active in order to generate the interrupt. If INT_AND_OR is 0, then the interrupts are combined in an OR structure, in which case ANY un-masked interrupt flags can generate the interrupt. ROM=Y, EEPROM=N 0x0 = OR 0x1 = AND
1	INT_EN	R/W	0x1	Interrupt Enable. If INT_EN is 1 then the interrupt circuit is enabled. If INT_EN is 0 the interrupt circuit is disabled. When INT_EN is 0, interrupts cannot be signaled on the GPIOx pins, and the flag registers (*_INTR) will not be updated; however, the live status registers will still reflect the current state of the internal interrupt source signals. To provide an interrupt on a pin, a GPIOx pin must also be configured as interrupt output. Interrupts may be enabled without providing a GPIOx output to allow sticky bits to be set. ROM=Y, EEPROM=N
0	INT_CLR	R/WSC	0x0	Clears all interrupt flag (*_INTR) registers ROM=N, EEPROM=N

1.39 R50 (Offset = 0x32)

Return to the [Summary Table](#).

Table 1-41. R50 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:2	RESERVED	R	0x0	Reserved
1	REF1_VALID_STATUS	R	0x0	Status of Reference Input Validation for IN1 ROM=N, EEPROM=N
0	REF0_VALID_STATUS	R	0x0	Status of Reference Input Validation for IN0 ROM=N, EEPROM=N

1.40 R52 (Offset = 0x34)

Return to the [Summary Table](#).

Table 1-42. R52 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-42. R52 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	REF1_PH_STATUS	R	0x0	Status of Reference 1 Phase Validation ROM=N, EEPROM=N
4	RESERVED	R	0x0	Reserved
3	REF1_FDET_STATUS	R	0x0	Status of Reference 1 Frequency Validation ROM=N, EEPROM=N
2	REF0_PH_STATUS	R	0x0	Status of Reference 0 Phase Validation ROM=N, EEPROM=N
1	RESERVED	R	0x0	Reserved
0	REF0_FDET_STATUS	R	0x0	Status of Reference 0 Frequency Validation ROM=N, EEPROM=N

1.41 R53 (Offset = 0x35)Return to the [Summary Table](#).**Table 1-43. R53 Field Descriptions**

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	TEC_CNTR_HELD	R	0x0	TEC Held. Reading back a 1 indicates GPIO or SPI event has latched a holdover value. Will clear to 0 after TEC CNTR LSB is read. ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.42 R54 (Offset = 0x36)Return to the [Summary Table](#).**Table 1-44. R54 Field Descriptions**

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	GPIO0_IN_FLT_EN	R/W	0x0	Enable GPIO0 Input Pin Deglitch Filter ROM=Y, EEPROM=N

Table 1-44. R54 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	GPIO0_MODE	R/W	0x0	Select GPIO0 Pin Operating Mode. ROM=Y, EEPROM=N 0x0 = STATUS or INT, Acts as status or interrupt outputs (See section on STATUS/ INTERRUPT) 0x1 = Reserved 0x2 = INSEL01_DPLL2, Selects input 0 or input 1 for DPLL2 0x3 = INSEL01_DPLL1, Selects input 0 or input 1 for DPLL1 0x4 = Reserved 0x5 = Reserved 0x6 = Reserved 0x7 = Reserved 0x8 = Reserved 0x9 = Reserved 0xA = Reserved 0xB = Reserved 0xC = Reserved 0xD = Reserved 0xE = Reserved 0xF = Reserved 0x10 = Reserved 0x11 = Reserved 0x12 = Reserved 0x13 = Reserved 0x14 = Reserved 0x15 = Reserved 0x16 = Reserved 0x17 = Reserved 0x18 = Reserved 0x19 = Reserved 0x1A = Reserved 0x1B = Reserved 0x1C = Reserved 0x1D = Reserved 0x1E = Reserved 0x1F = SYNC, Synchronizes selected outputs on a low-to-high pulse. "1" is normal state for outputs. "0" sets outputs in SYNC. 0x20 = SYSREF_REQ, Can request SYSREF pulses on appropriate output channels via low-to-high pulse. 0x21 = Reserved 0x22 = FDEV_TRIG_DPLL2, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL2 0x23 = FDEV_TRIG_DPLL1, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL1 0x24 = Reserved 0x25 = FDEV_DIR_DPLL2, FDEV_DIR_DPLL2 will determine the direction of the FDEV trigger. 0 = Negative and 1 = Positive 0x26 = FDEV_DIR_DPLL1, FDEV_DIR_DPLL1 will determine the direction of the FDEV trigger. 0 = Negative and 1 = Positive

Table 1-44. R54 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x27 = TEC_TRIG_SEL

1.43 R55 (Offset = 0x37)

Return to the [Summary Table](#).

Table 1-45. R55 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	GPIO1_IN_FLT_EN	R/W	0x0	Enable GPIO1 Input Pin Deglitch Filter ROM=Y, EEPROM=N

Table 1-45. R55 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	GPIO1_MODE	R/W	0x0	Select GPIO1 Pin Operating Mode. ROM=Y, EEPROM=N 0x0 = STATUS or INT, Acts as status or interrupt outputs (See section on STATUS/ INTERRUPT) 0x1 = Reserved 0x2 = INSEL01_DPLL2, Selects input 0 or input 1 for DPLL2 0x3 = INSEL01_DPLL1, Selects input 0 or input 1 for DPLL1 0x4 = Reserved 0x5 = Reserved 0x6 = Reserved 0x7 = Reserved 0x8 = Reserved 0x9 = Reserved 0xA = Reserved 0xB = Reserved 0xC = Reserved 0xD = Reserved 0xE = Reserved 0xF = Reserved 0x10 = Reserved 0x11 = Reserved 0x12 = Reserved 0x13 = Reserved 0x14 = Reserved 0x15 = Reserved 0x16 = Reserved 0x17 = Reserved 0x18 = Reserved 0x19 = Reserved 0x1A = Reserved 0x1B = Reserved 0x1C = Reserved 0x1D = Reserved 0x1E = Reserved 0x1F = SYNC, Synchronizes selected outputs on a low-to-high pulse. "1" is normal state for outputs. "0" sets outputs in SYNC. 0x20 = SYSREF_REQ, Can request SYSREF pulses on appropriate output channels via low-to-high pulse. 0x21 = Reserved 0x22 = FDEV_TRIG_DPLL2, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL2 0x23 = FDEV_TRIG_DPLL1, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL1 0x24 = Reserved 0x25 = FDEV_DIR_DPLL2, FDEV_DIR_DPLL2 will determine the direction of the FDEV trigger. 0 = Negative and 1 = Positive 0x26 = FDEV_DIR_DPLL1, FDEV_DIR_DPLL1 will determine the direction of the FDEV trigger. 0 = Negative and 1 = Positive

Table 1-45. R55 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x27 = TEC_TRIG_SEL

1.44 R56 (Offset = 0x38)

Return to the [Summary Table](#).

Table 1-46. R56 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	GPIO2_IN_FLT_EN	R/W	0x0	Enable GPIO2 Input Pin Deglitch Filter ROM=Y, EEPROM=N

Table 1-46. R56 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	GPIO2_MODE	R/W	0x0	Select GPIO2 Pin Operating Mode. ROM=Y, EEPROM=N 0x0 = STATUS or INT, Acts as status or interrupt outputs (See section on STATUS/ INTERRUPT) 0x1 = Reserved 0x2 = INSEL01_DPLL2, Selects input 0 or input 1 for DPLL2 0x3 = INSEL01_DPLL1, Selects input 0 or input 1 for DPLL1 0x4 = Reserved 0x5 = Reserved 0x6 = Reserved 0x7 = Reserved 0x8 = Reserved 0x9 = Reserved 0xA = Reserved 0xB = Reserved 0xC = Reserved 0xD = Reserved 0xE = Reserved 0xF = Reserved 0x10 = Reserved 0x11 = Reserved 0x12 = Reserved 0x13 = Reserved 0x14 = Reserved 0x15 = Reserved 0x16 = Reserved 0x17 = Reserved 0x18 = Reserved 0x19 = Reserved 0x1A = Reserved 0x1B = Reserved 0x1C = Reserved 0x1D = Reserved 0x1E = Reserved 0x1F = SYNC, Synchronizes selected outputs on a low-to-high pulse. "1" is normal state for outputs. "0" sets outputs in SYNC. 0x20 = SYSREF_REQ, Can request SYSREF pulses on appropriate output channels via low-to-high pulse. 0x21 = Reserved 0x22 = FDEV_TRIG_DPLL2, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL2 0x23 = FDEV_TRIG_DPLL1, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL1 0x24 = Reserved 0x25 = FDEV_DIR_DPLL2, FDEV_DIR_DPLL2 will determine the direction of the FDEV trigger. 0 = Negative and 1 = Positive 0x26 = FDEV_DIR_DPLL1, FDEV_DIR_DPLL1 will determine the direction of the FDEV trigger. 0 = Negative and 1 = Positive

Table 1-46. R56 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x27 = TEC_TRIG_SEL

1.45 R57 (Offset = 0x39)

Return to the [Summary Table](#).

Table 1-47. R57 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-47. R57 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	GPIO0_SEL	R/W	0x2	GPIO0 Status Signal Select. ROM=Y, EEPROM=N 0x0 = XO Loss of Signal (LOS) 0x1 = Reserved 0x2 = APLL2 Loss of Lock (LOL) 0x3 = APLL1 Loss of Lock (LOL) 0x4 = Reserved 0x5 = Reserved 0x6 = Reserved 0x7 = DPLL2 Loss of Phase Lock (LOPL) 0x8 = DPLL2 Loss of Frequency Lock (LOFL) 0x9 = PLL2 LOL DPLL2 LOPL DPLL2 LOFL 0xA = DPLL1 Loss of Phase Lock (LOPL) 0xB = DPLL1 Loss of Frequency Lock (LOFL) 0xC = PLL1 LOL DPLL1 LOPL DPLL1 LOFL 0xD = DPLL1 DPLL2 LOL 0xE = Interrupt (INTR). Derived from INT_FLAG register bits. 0xF = SPI Readback Data (SDO) 0x10 = Reserved 0x11 = Reserved 0x12 = Reserved 0x13 = Reserved 0x14 = Reserved 0x15 = Reserved 0x16 = Reserved 0x17 = Reserved 0x18 = Reserved 0x19 = Reserved 0x1A = Reserved 0x1B = DPLL2 REF0 Selected 0x1C = DPLL2 REF1 Selected 0x1D = Reserved 0x1E = Reserved 0x1F = Reserved 0x20 = DPLL2 Holdover Active 0x21 = DPLL1 REF0 Selected 0x22 = DPLL1 REF1 Selected 0x23 = Reserved 0x24 = Reserved 0x25 = Reserved 0x26 = DPLL1 Holdover Active 0x27 = REF0 Frequency Monitor 0x28 = REF1 Frequency Monitor 0x29 = Reserved 0x2A = Reserved 0x2B = Reserved 0x2C = REF0 Missing Clock Monitor 0x2D = REF1 Missing Clock Monitor 0x2E = Reserved

Table 1-47. R57 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = Reserved 0x30 = Reserved 0x31 = Reserved 0x32 = Reserved 0x33 = Reserved 0x34 = Reserved 0x35 = Reserved 0x36 = Reserved 0x37 = Reserved 0x38 = Reserved 0x39 = Reserved 0x3A = Reserved 0x3B = REF0 Phase Validation Monitor 0x3C = REF1 Phase Validation Monitor 0x3D = Reserved 0x3E = Reserved 0x3F = Reserved 0x40 = Reserved 0x41 = Reserved 0x42 = Reserved 0x43 = Reserved 0x44 = Reserved 0x45 = Reserved 0x46 = Reserved 0x47 = Reserved 0x48 = Reserved 0x49 = Reserved 0x4A = Reserved 0x4B = Reserved 0x4C = Reserved 0x4D = Reserved 0x4E = Reserved 0x4F = Reserved 0x50 = Reserved 0x51 = PLL2 N-Divider Divided By 2 0x52 = PLL1 N-Divider Divided By 2 0x53 = Reserved 0x54 = PLL2 R-Divider Divided By 2 0x55 = PLL1 R-Divider Divided By 2 0x56 = Reserved 0x57 = Reserved 0x58 = Reserved 0x59 = REF0 Monitor Divider Output Divided By 2 / REF _x _DET_CLK_DIV 0x5A = REF1 Monitor Divider Output Divided By 2 / REF _x _DET_CLK_DIV 0x5B = Reserved 0x5C = Reserved 0x5D = Reserved 0x5E = Reserved 0x5F = Reserved

Table 1-47. R57 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x60 = Reserved 0x61 = TDC2 R-Divider Divided By 2 0x62 = Reserved 0x63 = TDC2 FB-Divider Divided By 2 0x64 = TDC1 R-Divider Divided By 2 0x65 = Reserved 0x66 = TDC1 FB-Divider Divided By 2 0x67 = Reserved 0x68 = Reserved 0x69 = Reserved 0x6A = Reserved 0x6B = Reserved 0x6C = Reserved 0x6D = Reserved 0x6E = Reserved 0x6F = Reserved 0x70 = Reserved 0x71 = Reserved 0x72 = Reserved

1.46 R58 (Offset = 0x3A)

Return to the [Summary Table](#).

Table 1-48. R58 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-48. R58 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	GPIO1_SEL	R/W	0xF	GPIO1 Status Signal Select. ROM=Y, EEPROM=N 0x0 = XO Loss of Signal (LOS) 0x1 = Reserved 0x2 = APLL2 Loss of Lock (LOL) 0x3 = APLL1 Loss of Lock (LOL) 0x4 = Reserved 0x5 = Reserved 0x6 = Reserved 0x7 = DPLL2 Loss of Phase Lock (LOPL) 0x8 = DPLL2 Loss of Frequency Lock (LOFL) 0x9 = PLL2 LOL DPLL2 LOPL DPLL2 LOFL 0xA = DPLL1 Loss of Phase Lock (LOPL) 0xB = DPLL1 Loss of Frequency Lock (LOFL) 0xC = PLL1 LOL DPLL1 LOPL DPLL1 LOFL 0xD = DPLL1 DPLL2 LOL 0xE = Interrupt (INTR). Derived from INT_FLAG register bits. 0xF = SPI Readback Data (SDO) 0x10 = Reserved 0x11 = Reserved 0x12 = Reserved 0x13 = Reserved 0x14 = Reserved 0x15 = Reserved 0x16 = Reserved 0x17 = Reserved 0x18 = Reserved 0x19 = Reserved 0x1A = Reserved 0x1B = DPLL2 REF0 Selected 0x1C = DPLL2 REF1 Selected 0x1D = Reserved 0x1E = Reserved 0x1F = Reserved 0x20 = DPLL2 Holdover Active 0x21 = DPLL1 REF0 Selected 0x22 = DPLL1 REF1 Selected 0x23 = Reserved 0x24 = Reserved 0x25 = Reserved 0x26 = DPLL1 Holdover Active 0x27 = REF0 Frequency Monitor 0x28 = REF1 Frequency Monitor 0x29 = Reserved 0x2A = Reserved 0x2B = Reserved 0x2C = REF0 Missing Clock Monitor 0x2D = REF1 Missing Clock Monitor 0x2E = Reserved

Table 1-48. R58 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = Reserved 0x30 = Reserved 0x31 = Reserved 0x32 = Reserved 0x33 = Reserved 0x34 = Reserved 0x35 = Reserved 0x36 = Reserved 0x37 = Reserved 0x38 = Reserved 0x39 = Reserved 0x3A = Reserved 0x3B = REF0 Phase Validation Monitor 0x3C = REF1 Phase Validation Monitor 0x3D = Reserved 0x3E = Reserved 0x3F = Reserved 0x40 = Reserved 0x41 = Reserved 0x42 = Reserved 0x43 = Reserved 0x44 = Reserved 0x45 = Reserved 0x46 = Reserved 0x47 = Reserved 0x48 = Reserved 0x49 = Reserved 0x4A = Reserved 0x4B = Reserved 0x4C = Reserved 0x4D = Reserved 0x4E = Reserved 0x4F = Reserved 0x50 = Reserved 0x51 = PLL2 N-Divider Divided By 2 0x52 = PLL1 N-Divider Divided By 2 0x53 = Reserved 0x54 = PLL2 R-Divider Divided By 2 0x55 = PLL1 R-Divider Divided By 2 0x56 = Reserved 0x57 = Reserved 0x58 = Reserved 0x59 = REF0 Monitor Divider Output Divided By 2 / REF _x _DET_CLK_DIV 0x5A = REF1 Monitor Divider Output Divided By 2 / REF _x _DET_CLK_DIV 0x5B = Reserved 0x5C = Reserved 0x5D = Reserved 0x5E = Reserved 0x5F = Reserved

Table 1-48. R58 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x60 = Reserved 0x61 = TDC2 R-Divider Divided By 2 0x62 = Reserved 0x63 = TDC2 FB-Divider Divided By 2 0x64 = TDC1 R-Divider Divided By 2 0x65 = Reserved 0x66 = TDC1 FB-Divider Divided By 2 0x67 = Reserved 0x68 = Reserved 0x69 = Reserved 0x6A = Reserved 0x6B = Reserved 0x6C = Reserved 0x6D = Reserved 0x6E = Reserved 0x6F = Reserved 0x70 = Reserved 0x71 = Reserved 0x72 = Reserved 0x73 = Continuous SYSREF / 1-PPS from selected SYSREF DIV

1.47 R59 (Offset = 0x3B)

Return to the [Summary Table](#).

Table 1-49. R59 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-49. R59 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	GPIO2_SEL	R/W	0xE	GPIO2 Status Signal Select. ROM=Y, EEPROM=N 0x0 = XO Loss of Signal (LOS) 0x1 = Reserved 0x2 = APLL2 Loss of Lock (LOL) 0x3 = APLL1 Loss of Lock (LOL) 0x4 = Reserved 0x5 = Reserved 0x6 = Reserved 0x7 = DPLL2 Loss of Phase Lock (LOPL) 0x8 = DPLL2 Loss of Frequency Lock (LOFL) 0x9 = PLL2 LOL DPLL2 LOPL DPLL2 LOFL 0xA = DPLL1 Loss of Phase Lock (LOPL) 0xB = DPLL1 Loss of Frequency Lock (LOFL) 0xC = PLL1 LOL DPLL1 LOPL DPLL1 LOFL 0xD = DPLL1 DPLL2 LOL 0xE = Interrupt (INTR). Derived from INT_FLAG register bits. 0xF = SPI Readback Data (SDO) 0x10 = Reserved 0x11 = Reserved 0x12 = Reserved 0x13 = Reserved 0x14 = Reserved 0x15 = Reserved 0x16 = Reserved 0x17 = Reserved 0x18 = Reserved 0x19 = Reserved 0x1A = Reserved 0x1B = DPLL2 REF0 Selected 0x1C = DPLL2 REF1 Selected 0x1D = Reserved 0x1E = Reserved 0x1F = Reserved 0x20 = DPLL2 Holdover Active 0x21 = DPLL1 REF0 Selected 0x22 = DPLL1 REF1 Selected 0x23 = Reserved 0x24 = Reserved 0x25 = Reserved 0x26 = DPLL1 Holdover Active 0x27 = REF0 Frequency Monitor 0x28 = REF1 Frequency Monitor 0x29 = Reserved 0x2A = Reserved 0x2B = Reserved 0x2C = REF0 Missing Clock Monitor 0x2D = REF1 Missing Clock Monitor 0x2E = Reserved

Table 1-49. R59 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = Reserved 0x30 = Reserved 0x31 = Reserved 0x32 = Reserved 0x33 = Reserved 0x34 = Reserved 0x35 = Reserved 0x36 = Reserved 0x37 = Reserved 0x38 = Reserved 0x39 = Reserved 0x3A = Reserved 0x3B = REF0 Phase Validation Monitor 0x3C = REF1 Phase Validation Monitor 0x3D = Reserved 0x3E = Reserved 0x3F = Reserved 0x40 = Reserved 0x41 = Reserved 0x42 = Reserved 0x43 = Reserved 0x44 = Reserved 0x45 = Reserved 0x46 = Reserved 0x47 = Reserved 0x48 = Reserved 0x49 = Reserved 0x4A = Reserved 0x4B = Reserved 0x4C = Reserved 0x4D = Reserved 0x4E = Reserved 0x4F = Reserved 0x50 = Reserved 0x51 = PLL2 N-Divider Divided By 2 0x52 = PLL1 N-Divider Divided By 2 0x53 = Reserved 0x54 = PLL2 R-Divider Divided By 2 0x55 = PLL1 R-Divider Divided By 2 0x56 = Reserved 0x57 = Reserved 0x58 = Reserved 0x59 = REF0 Monitor Divider Output Divided By 2 / REF _x _DET_CLK_DIV 0x5A = REF1 Monitor Divider Output Divided By 2 / REF _x _DET_CLK_DIV 0x5B = Reserved 0x5C = Reserved 0x5D = Reserved 0x5E = Reserved 0x5F = Reserved

Table 1-49. R59 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x60 = Reserved 0x61 = TDC2 R-Divider Divided By 2 0x62 = Reserved 0x63 = TDC2 FB-Divider Divided By 2 0x64 = TDC1 R-Divider Divided By 2 0x65 = Reserved 0x66 = TDC1 FB-Divider Divided By 2 0x67 = Reserved 0x68 = Reserved 0x69 = Reserved 0x6A = Reserved 0x6B = Reserved 0x6C = Reserved 0x6D = Reserved 0x6E = Reserved 0x6F = Reserved 0x70 = Reserved 0x71 = Reserved 0x72 = Reserved 0x73 = Continuous SYSREF / 1-PPS from selected SYSREF DIV

1.48 R60 (Offset = 0x3C)

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Table 1-50. R60 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	GPIO0_OPEND	R/W	0x0	GPIO0 Open Drain Enable ROM=Y, EEPROM=N 0x0 = CMOS 0x1 = NMOS open drain. External pull-up from 1.8 V to 5.5 V supply rail required.
4	GPIO1_OPEND	R/W	0x1	GPIO1 Open Drain Enable ROM=Y, EEPROM=N 0x0 = CMOS 0x1 = NMOS open drain. External pull-up from 1.8 V to 5.5 V supply rail required.
3	GPIO2_OPEND	R/W	0x0	GPIO2 Open Drain Enable ROM=Y, EEPROM=N 0x0 = CMOS 0x1 = NMOS open drain. External pull-up from 1.8 V to 5.5 V supply rail required.

Table 1-50. R60 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	GPIO0_POL	R/W	0x1	GPIO0 Status Output Polarity. The GPIO0_STAT_POL bit defines the polarity of information presented on the GPIO0 output. If GPIO0_STAT_POL is set to 1, then GPIO0 is active high. If GPIO0_STAT_POL is 0, then GPIO0 is active low. ROM=Y, EEPROM=N 0x0 = Active High 0x1 = Active Low
1	GPIO1_POL	R/W	0x0	GPIO1 Status Output Polarity. The GPIO1_STAT_POL bit defines the polarity of information presented on the GPIO1 output. If GPIO1_STAT_POL is set to 1, then GPIO1 is active high. If GPIO1_STAT_POL is 0, then GPIO1 is active low. ROM=Y, EEPROM=N 0x0 = Active High 0x1 = Active Low
0	GPIO2_POL	R/W	0x0	GPIO2 Status Output Polarity. The GPIO2_STAT_POL bit defines the polarity of information presented on the GPIO2 output. If GPIO2_STAT_POL is set to 1, then GPIO2 is active high. If GPIO2_STAT_POL is 0, then GPIO2 is active low. ROM=Y, EEPROM=N 0x0 = Active High 0x1 = Active Low

1.49 R61 (Offset = 0x3D)

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Table 1-51. R61 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:2	GPIO_SYSREF_SEL	R/W	0x0	Select SYSREF divider output for GPIO output. When GPIOx_SEL chooses SYSREF divider, this is the SYSREF divider output on the GPIO. This signal is continuous. This could be used for low frequency outputs such as 1-PPS or 8 kHz as a 3.3-V LVCMOS signal. Select SYSREF divider output after static digital delay but before the analog and digital delay and pulser. ROM=Y, EEPROM=N 0x0 = OUT_0_1 0x1 = OUT_4_5 0x2 = OUT_6_7 0x3 = OUT_8_9 0x4 = OUT_10_11
1	MUTE_DPLL1_PHLOCK	R/W	0x0	DPLL1 mute enabled during phase lock. Muted outputs will start clocking glitch free once achieving lock status. PLL1 outputs will be muted even if DPLL1_EN = 0. ROM=Y, EEPROM=Y
0	MUTE_DPLL1_FRLOCK	R/W	0x0	DPLL1 mute enabled during dpll lock. Muted outputs will start clocking glitch free once achieving lock status. PLL1 outputs will be muted even if DPLL1_EN = 0. ROM=Y, EEPROM=Y

1.50 R62 (Offset = 0x3E)

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Table 1-52. R62 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	MUTE_DPLL2_PHLOCK	R/W	0x0	DPLL2 mute enabled during phase lock. Muted outputs will start clocking glitch free once achieving lock status. PLL2 outputs will be muted even if DPLL2_EN = 0. ROM=Y, EEPROM=Y
4	MUTE_DPLL2_FRLOCK	R/W	0x0	DPLL2 mute enabled during dpll lock. Muted outputs will start clocking glitch free once achieving lock status. PLL2 outputs will be muted even if DPLL2_EN = 0. ROM=Y, EEPROM=Y
3	MUTE_APLL2_LOCK	R/W	0x0	APLL2 mute enabled during PLL lock. Muted outputs will start clocking glitch free once achieving lock status. ROM=Y, EEPROM=Y
2:0	RESERVED	R	0x0	Reserved

1.51 R63 (Offset = 0x3F)

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Table 1-53. R63 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	XO_FDET_BYP	R/W	0x0	Frequency Detector Bypass. When XO_FDET_BYP is set to 1, the output of the XO frequency detector is ignored. ROM=Y, EEPROM=N
3:0	XO_ITYPE	R/W	0x0	XO interface type control. ROM=Y, EEPROM=Y 0x0 = DC (ext term) 0x1 = AC (ext term) 0x3 = AC (int 100 Ω to GND) 0x4 = DC (int 50 Ω to GND) 0x5 = AC (int 50 Ω to GND) 0x8 = LVCMOS 0xC = LVCMOS (int 50 Ω)

1.52 R64 (Offset = 0x40)

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Table 1-54. R64 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	XO_OUT_BUF_EN	R/W	0x9	Bit position enables XO Output Buffer path to: [0] The XO Freq Detector [1] Reserved [2] APLL2 REF [3] APLL1 REF, and [4] OUT0_1 ROM=Y, EEPROM=Y

1.53 R67 (Offset = 0x43)

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Table 1-55. R67 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF1_ITYPE	R/W	0x0	REF1 interface type control. ROM=Y, EEPROM=N 0x0 = DIFFin, ext DC, ext term 0x1 = DIFFin, ext AC, ext term 0x2 = DIFFin, ext DC, int 100 Ω diff 0x3 = DIFFin, ext AC, int 100 Ω diff 0x4 = DIFFin, ext DC, int 50 Ω to GND 0x5 = DIFFin, ext AC, int 50 Ω to GND 0x8 = CMOS, ext DC, int AC couple, 70 mV margin 0xC = S-E, ext DC, int AC couple, 70 mV margin, int 50 Ω to GND 0x18 = CMOS, ext DC, int DC couple, 150 mV hysteresis 0x23 = DIFFin, ext AC/DC, int 100 Ω diff, 210 mV margin 0x28 = CMOS, ext DC, int AC couple, 210 mV margin 0x38 = CMOS, ext DC, int DC couple, 0 mV hysteresis

1.54 R68 (Offset = 0x44)

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Table 1-56. R68 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-56. R68 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	REF0_ITYPE	R/W	0x0	REF0 interface type control. ROM=Y, EEPROM=N 0x0 = DIFFin, ext DC, ext term 0x1 = DIFFin, ext AC, ext term 0x2 = DIFFin, ext DC, int 100 Ω diff 0x3 = DIFFin, ext AC, int 100 Ω diff 0x4 = DIFFin, ext DC, int 50 Ω to GND 0x5 = DIFFin, ext AC, int 50 Ω to GND 0x8 = CMOS, ext DC, int AC couple, 70 mV margin 0xC = S-E, ext DC, int AC couple, 70 mV margin, int 50 Ω to GND 0x18 = CMOS, ext DC, int DC couple, 150 mV hysteresis 0x23 = DIFFin, ext AC/DC, int 100 Ω diff, 210 mV margin 0x28 = CMOS, ext DC, int AC couple, 210 mV margin 0x38 = CMOS, ext DC, int DC couple, 0 mV hysteresis

1.55 R70 (Offset = 0x46)

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Table 1-57. R70 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	STATUS_MUX_DIV2_EN	R/W	0x0	Enable all DivideBy2 clocks for Status MUX debug signals ROM=N, EEPROM=N

1.56 R75 (Offset = 0x4B)

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Table 1-58. R75 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	TDC1_ZDM_BYPASS_FB_DIV	R/W	0x0	Selects TDC1 feedback input source. 0 = FB_DIV (Normal or ZDM) 1 = bypass FB DIV (ZDM) ROM=Y, EEPROM=N 0x0 = Select FB Divider 0x1 = Bypass FB Divider
5	TDC1_ZDM_FB_PRE_BYP	R/W	0x0	Bypasses TDC1 feedback divider when using ZDM with DPLL1. ROM=Y, EEPROM=N 0x0 = Select FB Prescaler 0x1 = Bypass FB Prescaler

Table 1-58. R75 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:3	TDC1_IN_SEL	R/W	0x3	Selects TDC1 zero delay input ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = OUT_10_11_ZD_FB 0x2 = OUT_0_1_ZD_FB 0x3 = VCO1 direct (ZDM disabled)
2:0	TDC1_IN_DRV_SEL	R/W	0x2	Enables zero delay input mux output ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = ZDM disabled 0x3 = Reserved 0x4 = Reserved 0x5 = ZDM enabled 0x6 = Reserved 0x7 = Reserved

1.57 R76 (Offset = 0x4C)

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Table 1-59. R76 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	TDC2_ZDM_BYPASS_FB_DIV	R/W	0x0	Selects TDC2 feedback input source. 0 = FB_DIV (Normal or ZDM) 1 = bypass FBDIV (ZDM) ROM=Y, EEPROM=N 0x0 = Select FB Divider 0x1 = Bypass FB Divider
5	TDC2_ZDM_FB_PRE_BYP	R/W	0x0	Bypasses TDC2 feedback divider when using ZDM with DPLL2. ROM=Y, EEPROM=N 0x0 = Select FB Prescaler 0x1 = Bypass FB Prescaler
4:3	TDC2_IN_SEL	R/W	0x3	Selects zero delay input ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = OUT_4_5_ZD_FB 0x2 = OUT_0_1_ZD_FB 0x3 = VCO2 direct (ZDM disabled)

Table 1-59. R76 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	TDC2_IN_DRV_SEL	R/W	0x2	Enables zero delay input mux output ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = ZDM disabled 0x3 = Reserved 0x4 = Reserved 0x5 = ZDM enabled 0x6 = Reserved 0x7 = Reserved

1.58 R77 (Offset = 0x4D)

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Table 1-60. R77 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RESERVED	R	0x0	Reserved

1.59 R78 (Offset = 0x4E)

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Table 1-61. R78 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	REF_OUT01_EN	R/W	0x0	Ref to OUT0_1 Enable. Enables the path for a reference clock (selected by REF_2OUT01_SEL) to be available for selection at OUT0_1. ROM=Y, EEPROM=N
4:0	REF_OUT01_SEL	R/W	0x0	Ref to OUT0_1 Select. Selects one reference clock which will be fed to the input of OUT0_1 (if path enabled by REF_2OUT01_EN). ROM=Y, EEPROM=N 0x0 = OFF 0x1 = REF0 0x2 = REF1

1.60 R79 (Offset = 0x4F)

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Table 1-62. R79 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	REF0_EARLY_DET_EN	R/W	0x1	REF0 Early Clock Detect Enable ROM=Y, EEPROM=N
4	REF0_PH_VALID_EN	R/W	0x0	REF0 Phase Validation Enable ROM=Y, EEPROM=N
3	REF0_VALTMR_EN	R/W	0x1	REF0 Validation Timer Enable ROM=Y, EEPROM=N
2	REF0_PPM_EN	R/W	0x1	REF0 Freq ppm Enable ROM=Y, EEPROM=N
1	REF0_MISSCLK_EN	R/W	0x1	REF0 Missing Clock Detect Enable ROM=Y, EEPROM=N
0	RESERVED	R	0x0	Reserved

1.61 R80 (Offset = 0x50)

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Table 1-63. R80 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	REF1_EARLY_DET_EN	R/W	0x1	REF1 Early Clock Detect Enable ROM=Y, EEPROM=N
4	REF1_PH_VALID_EN	R/W	0x0	REF1 Phase Validation Enable ROM=Y, EEPROM=N
3	REF1_VALTMR_EN	R/W	0x1	REF1 Validation Timer Enable ROM=Y, EEPROM=N
2	REF1_PPM_EN	R/W	0x1	REF1 Freq ppm Enable ROM=Y, EEPROM=N
1	REF1_MISSCLK_EN	R/W	0x1	REF1 Missing Clock Detect Enable ROM=Y, EEPROM=N
0	RESERVED	R	0x0	Reserved

1.62 R83 (Offset = 0x53)

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Table 1-64. R83 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:2	REF1_DET_CLK_DIV	R/W	0x2	REF1 Clock Detector Divider. Bit 0 controls the divide value (0=Div4, 1=Div16). Bit 1, if set, causes the divider to be bypassed. ROM=Y, EEPROM=N 0x0 = Div By 4 0x1 = Div By 16 0x2 = Bypass 0x3 = Bypass (Reserved)
1:0	REF0_DET_CLK_DIV	R/W	0x0	REF0 Clock Detector Divider. Bit 0 controls the divide value (0=Div4, 1=Div16). Bit 1, if set, causes the divider to be bypassed. ROM=Y, EEPROM=N 0x0 = Div By 4 0x1 = Div By 16 0x2 = Bypass 0x3 = Bypass (Reserved)

1.63 R84 (Offset = 0x54)

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Table 1-65. R84 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF0_MISCLK_DIV_21:16	R/W	0x0	See Register 86

1.64 R85 (Offset = 0x55)

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Table 1-66. R85 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_MISCLK_DIV_15:8	R/W	0x0	See Register 86

1.65 R86 (Offset = 0x56)

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Table 1-67. R86 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_MISSCLK_DIV	R/W	0xB	REF0 Missing Clock Detector Divider. 21-bit divide value. Should be equal to the ratio of either VCO1/2 to REF0 or VCO2/5 to REF0 (determined by REF0_MISSCLK_VCOSEL selection) with some offset added for upper bound. ROM=Y, EEPROM=N

1.66 R87 (Offset = 0x57)

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Table 1-68. R87 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF1_MISSCLK_DIV_21:16	R/W	0x0	See Register 89

1.67 R88 (Offset = 0x58)

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Table 1-69. R88 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_MISSCLK_DIV_15:8	R/W	0x0	See Register 89

1.68 R89 (Offset = 0x59)

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Table 1-70. R89 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_MISSCLK_DIV	R/W	0x7E	REF1 Missing Clock Detector Divider. 21-bit divide value. Should be equal to the ratio of either VCO1/2 to REF1 or VCO2/5 to REF0 (determined by REF1_MISSCLK_VCOSEL selection) with some offset added for upper bound. ROM=Y, EEPROM=N

1.69 R96 (Offset = 0x60)

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Table 1-71. R96 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:1	RESERVED	R	0x0	Reserved
0	REF0_MISSCLK_VCOSEL	R/W	0x0	Missing/Early Clock Detector VCO selection for all references. Also selects TEC clock source. ROM=Y, EEPROM=N 0x0 = VCO1 0x1 = VCO2

1.70 R97 (Offset = 0x61)

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Table 1-72. R97 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF0_EARLY_CLK_DIV_21:16	R/W	0x0	See Register 99

1.71 R98 (Offset = 0x62)

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Table 1-73. R98 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_EARLY_CLK_DIV_15:8	R/W	0x0	See Register 99

1.72 R99 (Offset = 0x63)

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Table 1-74. R99 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_EARLY_CLK_DIV	R/W	0x3	REF0 Early Clock Detector Divider. 21-bit divide value. Should be equal to the ratio of either VCO1/2 to REF0 or VCO2/5 to REF0 (determined by REF0_MISSCLK_VCOSEL selection) with some offset subtracted for lower bound. ROM=Y, EEPROM=N

1.73 R100 (Offset = 0x64)

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Table 1-75. R100 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF1_EARLY_CLK_DIV_21:16	R/W	0x0	See Register 102

1.74 R101 (Offset = 0x65)

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Table 1-76. R101 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_EARLY_CLK_DIV_15:8	R/W	0x0	See Register 102

1.75 R102 (Offset = 0x66)

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Table 1-77. R102 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_EARLY_CLK_DIV	R/W	0x76	REF1 Early Clock Detector Divider. 21-bit divide value. Should be equal to the ratio of either VCO1/2 to REF1 or VCO2/5 to REF1 (determined by REF0_MISSCLK_VCOSEL selection) with some offset subtracted for lower bound. ROM=Y, EEPROM=N

1.76 R109 (Offset = 0x6D)

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Table 1-78. R109 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	REF0_PPM_MIN_14:8	R/W	0x0	See Register 110

1.77 R110 (Offset = 0x6E)

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Table 1-79. R110 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_PPM_MIN	R/W	0x6F	REF0 Frequency PPM Lower Limit ROM=Y, EEPROM=N

1.78 R111 (Offset = 0x6F)

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Table 1-80. R111 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	REF0_PPM_MAX_14:8	R/W	0x0	See Register 112

1.79 R112 (Offset = 0x70)

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Table 1-81. R112 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_PPM_MAX	R/W	0x77	REF0 Frequency PPM Upper Limit ROM=Y, EEPROM=N

1.80 R113 (Offset = 0x71)

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Table 1-82. R113 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	REF1_PPM_MIN_14:8	R/W	0x0	See Register 114

1.81 R114 (Offset = 0x72)

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Table 1-83. R114 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_PPM_MIN	R/W	0x6F	REF1 Frequency PPM Lower Limit ROM=Y, EEPROM=N

1.82 R115 (Offset = 0x73)

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Table 1-84. R115 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	REF1_PPM_MAX_14:8	R/W	0x0	See Register 116

1.83 R116 (Offset = 0x74)

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Table 1-85. R116 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_PPM_MAX	R/W	0x77	REF1 Frequency PPM Upper Limit ROM=Y, EEPROM=N

1.84 R125 (Offset = 0x7D)

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Table 1-86. R125 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:4	RESERVED	R	0x0	Reserved
3:0	REF0_CNTSTRT_27:24	R/W	0x0	See Register 128

1.85 R126 (Offset = 0x7E)

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Table 1-87. R126 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_CNTSTRT_23:16	R/W	0x18	See Register 128

1.86 R127 (Offset = 0x7F)

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Table 1-88. R127 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_CNTSTRT_15:8	R/W	0xD5	See Register 128

1.87 R128 (Offset = 0x80)

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Table 1-89. R128 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_CNTSTRT	R/W	0xD5	28-bit REF0 PPM detect counter. REF0 decreases a counter reset by REF0_CNTSTRT value. When this becomes 0, then counter reset by REF0_HOLD_CNTSTRT is the error and used to know frequency accuracy. ROM=Y, EEPROM=N

1.88 R129 (Offset = 0x81)

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Table 1-90. R129 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	REF0_HOLD_CNTSTRT_27:24	R/W	0x0	See Register 132

1.89 R130 (Offset = 0x82)

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Table 1-91. R130 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_HOLD_CNTSTRT_23:16	R/W	0x1E	See Register 132

1.90 R131 (Offset = 0x83)

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Table 1-92. R131 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_HOLD_CNTSTRT_15:8	R/W	0x84	See Register 132

1.91 R132 (Offset = 0x84)

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Table 1-93. R132 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_HOLD_CNTSTRT	R/W	0x81	28-bit REF0 PPM detect counter. XO decreases a counter reset by REF0_HOLD_CNTSTRT. When counter reset by REF0_CNTSTRT becomes 0, this counter reset by REF0_HOLD_CNTSTRT contains the time error from which PPM error may be determined. ROM=Y, EEPROM=N

1.92 R133 (Offset = 0x85)

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Table 1-94. R133 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:4	RESERVED	R	0x0	Reserved
3:0	REF1_CNTSTRT_27:24	R/W	0x0	See Register 136

1.93 R134 (Offset = 0x86)

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Table 1-95. R134 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_CNTSTRT_23:16	R/W	0x6	See Register 136

1.94 R135 (Offset = 0x87)

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Table 1-96. R135 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_CNTSTRT_15:8	R/W	0x5B	See Register 136

1.95 R136 (Offset = 0x88)

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Table 1-97. R136 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_CNTSTRT	R/W	0x9B	28-bit REF1 PPM detect counter. REF1 decreases a counter reset by REF1_CNTSTRT value. When this becomes 0, then counter reset by REF1_HOLD_CNTSTRT is the error and used to know frequency accuracy. ROM=Y, EEPROM=N

1.96 R137 (Offset = 0x89)

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Table 1-98. R137 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	REF1_HOLD_CNTSTRT_27:24	R/W	0x0	See Register 140

1.97 R138 (Offset = 0x8A)

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Table 1-99. R138 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_HOLD_CNTSTRT_23:16	R/W	0x1E	See Register 140

1.98 R139 (Offset = 0x8B)

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Table 1-100. R139 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_HOLD_CNTSTRT_15:8	R/W	0x84	See Register 140

1.99 R140 (Offset = 0x8C)

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Table 1-101. R140 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_HOLD_CNTSTRT	R/W	0x82	28-bit REF1 PPM detect counter. XO decreases a counter reset by REF1_HOLD_CNTSTRT. When counter reset by REF1_CNTSTRT becomes 0, this counter reset by REF1_HOLD_CNTSTRT contains the time error from which PPM error may be determined. ROM=Y, EEPROM=N

1.100 R157 (Offset = 0x9D)

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Table 1-102. R157 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved

Table 1-102. R157 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	REF0VLDTMR	R/W	0xA	REF0 Validation Timer. All selected validations must be valid for selected amount of time before the IN0/REF0 is considered valid. ROM=Y, EEPROM=N 0x0 = 0.1 ms 0x1 = 0.2 ms 0x2 = 0.4 ms 0x3 = 0.8 ms 0x4 = 1.6 ms 0x5 = 3.2 ms 0x6 = 6.4 ms 0x7 = 12.8 ms 0x8 = 25.6 ms 0x9 = 51.2 ms 0xA = 102.4 ms 0xB = 204.8 ms 0xC = 409.6 ms 0xD = 819.2 ms 0xE = 1.6 s 0xF = 3.3 s 0x10 = 6.6 s 0x11 = 13.1 s 0x12 = 26.2 s 0x13 = 52.4 s 0x14 = 1.7 min 0x15 = 3.5 min 0x16 = 7.0 min 0x17 = 14.0 min 0x18 = 28.0 min 0x19 = 55.9 min 0x1A = 1.9 hr 0x1B = 3.7 hr 0x1C = 7.5 hr 0x1D = 14.9 hr 0x1E = 29.8 hr 0x1F = 59.7 hr

1.101 R158 (Offset = 0x9E)

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Table 1-103. R158 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved

Table 1-103. R158 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	REF1VLDTMR	R/W	0xA	REF1 Validation Timer. All selected validations must be valid for selected amount of time before the IN1/REF1 is considered valid. ROM=Y, EEPROM=N 0x0 = 0.1 ms 0x1 = 0.2 ms 0x2 = 0.4 ms 0x3 = 0.8 ms 0x4 = 1.6 ms 0x5 = 3.2 ms 0x6 = 6.4 ms 0x7 = 12.8 ms 0x8 = 25.6 ms 0x9 = 51.2 ms 0xA = 102.4 ms 0xB = 204.8 ms 0xC = 409.6 ms 0xD = 819.2 ms 0xE = 1.6 s 0xF = 3.3 s 0x10 = 6.6 s 0x11 = 13.1 s 0x12 = 26.2 s 0x13 = 52.4 s 0x14 = 1.7 min 0x15 = 3.5 min 0x16 = 7.0 min 0x17 = 14.0 min 0x18 = 28.0 min 0x19 = 55.9 min 0x1A = 1.9 hr 0x1B = 3.7 hr 0x1C = 7.5 hr 0x1D = 14.9 hr 0x1E = 29.8 hr 0x1F = 59.7 hr

1.102 R161 (Offset = 0xA1)

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Table 1-104. R161 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF0_PH_VALID_THR_13:8	R/W	0x0	REF0 Phase Validation Threshold ROM=Y, EEPROM=N

1.103 R162 (Offset = 0xA2)

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Table 1-105. R162 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_PH_VALID_THR	R/W	0x0	REF0 Phase Validation Threshold ROM=Y, EEPROM=N

1.104 R163 (Offset = 0xA3)

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Table 1-106. R163 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF1_PH_VALID_THR_13:8	R/W	0x0	REF1 Phase Validation Threshold ROM=Y, EEPROM=N

1.105 R164 (Offset = 0xA4)

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Table 1-107. R164 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_PH_VALID_THR	R/W	0x0	REF1 Phase Validation Threshold ROM=Y, EEPROM=N

1.106 R170 (Offset = 0xAA)

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Table 1-108. R170 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMSCRC	R	0x0	NVM Stored CRC ROM=N, EEPROM=N

1.107 R171 (Offset = 0xAB)

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Table 1-109. R171 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	REGCOMMIT	R/WSC	0x0	Copy fields which also exist in SRAM to SRAM memory. The REGCOMMIT bit is automatically cleared to 0 when the transfer is complete. Next an EEPROM programming operation may be performed to update NVM EEPROM. When programming to alter an NVM profile, it is suggested to toggle PD# to assure default conditions, change the desired fields, then assert the REGCOMMIT bit. ROM=N, EEPROM=N
5	NVMCRCERR	R	0x0	NVM CRC Error Indication. The NVMCRCERR bit is set to 1 if a CRC Error has been detected when reading back from on-chip EEPROM during device configuration. ROM=N, EEPROM=N
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	NVMBUSY	R	0x0	NVM Program Busy Indication. The NVMBUSY bit is 1 during an on-chip EEPROM Erase/Program cycle. While NVMBUSY is 1 the on-chip EEPROM cannot be accessed. Toggling PD# or removing power while NVMBUSY is asserted will corrupt the EEPROM. ROM=N, EEPROM=N
1	NVMERASE	R/WSC	0x0	NVM Erase Start. The NVMERASE bit is used to begin an on-chip EEPROM Erase cycle. The Erase cycle is only initiated if the immediately preceding I2C/SMBus transaction was a write to the NVMUNLK register with the appropriate code. The NVMERASE bit is automatically cleared to 0.
0	NVMPROG	R/WSC	0x0	NVM Program Start. The NVMPROG bit is used to begin an on-chip EEPROM Program cycle. The Program cycle is only initiated if the immediately preceding I2C/SMBus transaction was a write to the NVMUNLK register with the appropriate code. The NVMPROG bit is automatically cleared to 0.

1.108 R172 (Offset = 0xAC)

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Table 1-110. R172 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMLCRC	R	0x0	NVM Live CRC ROM=N, EEPROM=N

1.109 R173 (Offset = 0xAD)

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Table 1-111. R173 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved

Table 1-111. R173 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	MEMADR_12:8	R/W	0x0	See Register 174

1.110 R174 (Offset = 0xAE)

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Table 1-112. R174 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	MEMADR	R/W	0x0	Memory Address. The MEMADR value determines the starting address for access to the on-chip memories. This same MEMADR value is used for EEPROM and SRAM access which share the same memory map and also ROM access. The NVMDAT field is used to read and write from EEPROM. The RAMDAT field is used to read and write from SRAM. The ROMDAT field is used to read and write from ROM.

1.111 R175 (Offset = 0xAF)

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Table 1-113. R175 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMDAT	R/W	0x0	EEPROM Read Data. The first time an I2C/SMBus read transaction accesses the NVMDAT register address, either because it was explicitly targeted or because the address was auto-incremented, the read transaction will return the EEPROM data located at the address specified by the MEMADR register. Any additional read's which are part of the same transaction will cause the EEPROM address to be incremented and the next EEPROM data byte will be returned. The I2C/SMBus address will no longer be auto-incremented, i.e the I2C/SMBus address will be locked to the NVMDAT register after the first access. Access to the NVMDAT register will terminate at the end of the current I2C/SMBus transaction. ROM=N, EEPROM=N

1.112 R176 (Offset = 0xB0)

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Table 1-114. R176 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RAMDAT	R/W	0x0	RAM Read/Write Data. The first time an I2C/SMBus read or write transaction accesses the RAMDAT register address, either because it was explicitly targeted or because the address was auto-incremented, a read transaction will return the RAM data located at the address specified by the MEMADR register and a write transaction will cause the current I2C/SMBus data to be written to the address specified by the MEMADR register. Any additional accesses which are part of the same transaction will cause the RAM address to be incremented and a read or write access will take place to the next SRAM address. The I2C/SMBus address will no longer be auto-incremented (that is, the I2C/SMBus address will be locked to the RAMDAT register after the first access). Access to the RAMDAT register will terminate at the end of the current I2C/SMBus transaction. ROM=N, EEPROM=N

1.113 R180 (Offset = 0xB4)

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Table 1-115. R180 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMUNLK	R/W	0x0	NVM Prog Unlock. The NVMUNLK register must be written immediately prior to setting the NVMERASE and NVMPROG bit, otherwise the Erase/Program cycle will not be triggered. NVMUNLK must be written with a value of 0xEA. ROM=N, EEPROM=N

1.114 R373 (Offset = 0x175)

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Table 1-116. R373 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	DPLL2_REF0_AUTO_PRTY	R/W	0x0	REF0 Priority for Automatic Switchover. Sets the priority for REF0 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

Table 1-116. R373 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	DPLL2_REF1_AUTO_PRTY	R/W	0x0	REF1 Priority for Automatic Switchover. Sets the priority for REF1 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.115 R375 (Offset = 0x177)

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Table 1-117. R375 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	DPLL2_REF4_AUTO_PRTY	R/W	0x0	REF4 Priority for Automatic Switchover. Sets the priority for REF4 feedback from APLL1 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th
2:0	DPLL2_REF5_AUTO_PRTY	R/W	0x0	REF5 Priority for Automatic Switchover. Sets the priority for REF5 feedback from APLL1 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.116 R376 (Offset = 0x178)

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Table 1-118. R376 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5:3	DPLL2_MAN_REFSEL	R/W	0x0	DPLL2 Manual Reference Selection ROM=Y, EEPROM=N 0x0 = REF0 0x1 = REF1 0x2 = Reserved 0x3 = Reserved 0x4 = Reserved 0x5 = PLL1
2	DPLL2_MAN_SWITCH_PIN_MODE	R/W	0x0	DPLL2 Manual Reference Selection Mode. Determines how the manually selected reference is chosen. If this is set to a '1', the manually selected reference is taken from a GPIO input pin. If it is set to a '0', the manually selected reference is taken from a register. ROM=Y, EEPROM=N 0x0 = Register 0x1 = Pin
1:0	DPLL2_SWITCH_MODE	R/W	0x1	DPLL2 Reference Switchover Mode. Selects between Automatic Non-revertive, Automatic Revertive, Manual Selection with Automatic Fallback, and Manual Selection with Automatic Holdover. ROM=Y, EEPROM=N 0x0 = Auto non-revertive 0x1 = Auto revertive 0x2 = Manual with fallback 0x3 = Manual with holdover

1.117 R377 (Offset = 0x179)

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Table 1-119. R377 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-119. R377 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	DPLL2_REFSEL_STAT	R	0x2	Reads the DPLL2 selected reference ROM=N, EEPROM=N 0x0 = Holdover 0x1 = REF0 0x2 = REF1 0x4 = Reserved 0x8 = Reserved 0x10 = Reserved 0x20 = APLL1

1.118 R378 (Offset = 0x17A)

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Table 1-120. R378 Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL2_LOCKDET_PPM_EN	R/W	0x0	DPLL frequency lock detect enable ROM=Y, EEPROM=N
6:0	DPLL2_LOCKDET_PPM_MAX_14:8	R/W	0x0	See Register 379

1.119 R379 (Offset = 0x17B)

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Table 1-121. R379 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_PPM_MAX	R/W	0xA	DPLL frequency lock detect in-lock threshold ROM=Y, EEPROM=N

1.120 R380 (Offset = 0x17C)

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Table 1-122. R380 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	DPLL2_UNLOCKDET_PPM_MAX_14:8	R/W	0x0	See Register 381

1.121 R381 (Offset = 0x17D)

Return to the [Summary Table](#).

Table 1-123. R381 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_UNLOCKDET_PPM_MAX	R/W	0x64	DPLL frequency lock detect out-of-lock threshold ROM=Y, EEPROM=N

1.122 R382 (Offset = 0x17E)

Return to the [Summary Table](#).

Table 1-124. R382 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_LOCKDET2_PPM_CNTSTR T_29:24	R/W	0x0	See Register 385

1.123 R383 (Offset = 0x17F)

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Table 1-125. R383 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET2_PPM_CNTSTR T_23:16	R/W	0x0	See Register 385

1.124 R384 (Offset = 0x180)

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Table 1-126. R384 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET2_PPM_CNTSTR T_15:8	R/W	0x9	See Register 385

1.125 R385 (Offset = 0x181)

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Table 1-127. R385 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET2_PPM_CNTSTR T	R/W	0xC5	DPLL frequency lock detect reference count value used with DPLL2 feedback configuration 2 ROM=Y, EEPROM=N

1.126 R386 (Offset = 0x182)

Return to the [Summary Table](#).

Table 1-128. R386 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_LOCKDET_PPM_CNTSTR T_29:24	R/W	0x0	See Register 389

1.127 R387 (Offset = 0x183)

Return to the [Summary Table](#).

Table 1-129. R387 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_PPM_CNTSTR T_23:16	R/W	0x2	See Register 389

1.128 R388 (Offset = 0x184)

Return to the [Summary Table](#).

Table 1-130. R388 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_PPM_CNTSTR T_15:8	R/W	0x8	See Register 389

1.129 R389 (Offset = 0x185)

Return to the [Summary Table](#).

Table 1-131. R389 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_PPM_CNTSTRT	R/W	0xD6	DPLL frequency lock detect reference count value used with DPLL2 feedback configuration 1 ROM=Y, EEPROM=N

1.130 R390 (Offset = 0x186)

Return to the [Summary Table](#).

Table 1-132. R390 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_LOCKDET_VCO_PPM_CNT STRT_29:24	R/W	0x0	See Register 393

1.131 R391 (Offset = 0x187)

Return to the [Summary Table](#).

Table 1-133. R391 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_VCO_PPM_CNT STRT_23:16	R/W	0x98	See Register 393

1.132 R392 (Offset = 0x188)

Return to the [Summary Table](#).

Table 1-134. R392 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_VCO_PPM_CNT STRT_15:8	R/W	0x96	See Register 393

1.133 R393 (Offset = 0x189)

Return to the [Summary Table](#).

Table 1-135. R393 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_VCO_PPM_CNT STRT	R/W	0xB2	DPLL frequency lock detect VCO count value ROM=Y, EEPROM=N

1.134 R394 (Offset = 0x18A)

Return to the [Summary Table](#).

Table 1-136. R394 Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:1	RESERVED	R	0x0	Reserved
0	DPLL2_STATUS_PPM_LOCK	R	0x1	Readback lock indicator from DPLL PPM Checker ROM=N, EEPROM=N

1.135 R397 (Offset = 0x18D)

Return to the [Summary Table](#).

Table 1-137. R397 Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL2_LOOP_EN	R/W	0x0	Enable DPLL2 loop filter and R-Div mash engine ROM=Y, EEPROM=N
6	DPLL2_PHASE_CANCEL_EN	R/W	0x1	Enable Phase Cancellation ROM=Y, EEPROM=N
5	DPLL2_FASTLOCK_ALWAYS	R/W	0x0	Always perform fastlock. No phase cancellation is done. ROM=Y, EEPROM=N
4	DPLL2_PHS1_EN	R/W	0x1	Enable holdover exit phase slew control . ROM=Y, EEPROM=N
3	DPLL2_ZDM_EN	R/W	0x0	Enable Zero Delay ROM=Y, EEPROM=N
2	DPLL2_HIST_EN	R/W	0x1	Enable History word to be used during holdover ROM=Y, EEPROM=N
1	DPLL2_PHASE_CANCEL_ALWAYS	R/W	0x0	Force phase cancellation to always occur when DPLL is acquiring lock ROM=Y, EEPROM=N
0	RESERVED	R	0x0	Reserved

1.136 R398 (Offset = 0x18E)

Return to the [Summary Table](#).

Table 1-138. R398 Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL2_HOLD_SLEW_LIM_EN	R/W	0x0	Enable slew limiter when entering holdover ROM=Y, EEPROM=N
6:0	RESERVED	R	0x0	Reserved

1.137 R400 (Offset = 0x190)

Return to the [Summary Table](#).

Table 1-139. R400 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL2_PH_OFFSET_44:40	R/W	0x0	See Register 405

1.138 R401 (Offset = 0x191)

Return to the [Summary Table](#).

Table 1-140. R401 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_PH_OFFSET_39:32	R/W	0x0	See Register 405

1.139 R402 (Offset = 0x192)

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Table 1-141. R402 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_PH_OFFSET_31:24	R/W	0x0	See Register 405

1.140 R403 (Offset = 0x193)

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Table 1-142. R403 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_PH_OFFSET_23:16	R/W	0x0	See Register 405

1.141 R404 (Offset = 0x194)

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Table 1-143. R404 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_PH_OFFSET_15:8	R/W	0x0	See Register 405

1.142 R405 (Offset = 0x195)

Return to the [Summary Table](#).

Table 1-144. R405 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_PH_OFFSET	R/W	0x0	Phase offset to adjust and calibrate input to output phase in ZDM. This is a 2s complement number. ROM=Y, EEPROM=N

1.143 R406 (Offset = 0x196)

Return to the [Summary Table](#).

Table 1-145. R406 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FREE_RUN_39:32	R/W	0x0	See Register 410

1.144 R407 (Offset = 0x197)

Return to the [Summary Table](#).

Table 1-146. R407 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FREE_RUN_31:24	R/W	0x0	See Register 410

1.145 R408 (Offset = 0x198)

Return to the [Summary Table](#).

Table 1-147. R408 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FREE_RUN_23:16	R/W	0x0	See Register 410

1.146 R409 (Offset = 0x199)

Return to the [Summary Table](#).

Table 1-148. R409 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FREE_RUN_15:8	R/W	0x0	See Register 410

1.147 R410 (Offset = 0x19A)

Return to the [Summary Table](#).

Table 1-149. R410 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FREE_RUN	R/W	0x0	DPLL2 starting word. Also non-history holdover word. ROM=Y, EEPROM=N

1.148 R411 (Offset = 0x19B)

Return to the [Summary Table](#).

Table 1-150. R411 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	DPLL2_1PPS_MODE	R/W	0x0	Set when using 1-PPS input ROM=Y, EEPROM=N
5	DPLL2_1PPS_EN	R/W	0x0	Set when using 1-PPS input ROM=Y, EEPROM=N
4:0	RESERVED	R	0x0	Reserved

1.149 R440 (Offset = 0x1B8)

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Table 1-151. R440 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL2_LCK_TIMER_9:8	R/W	0x2	See Register 441

1.150 R441 (Offset = 0x1B9)

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Table 1-152. R441 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LCK_TIMER	R/W	0xB	Minimum amount of time until DPLL2_LOPL will be deasserted after starting to lock. Timer begins once device is within valid phase lock window. ROM=Y, EEPROM=N

1.151 R442 (Offset = 0x1BA)

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Table 1-153. R442 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL2_HIST_TIMER_9:8	R/W	0x1	See Register 443

1.152 R443 (Offset = 0x1BB)

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Table 1-154. R443 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_HIST_TIMER	R/W	0x92	Time interval between history update events. ROM=Y, EEPROM=N

1.153 R444 (Offset = 0x1BC)

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Table 1-155. R444 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R	0x0	Reserved
1:0	DPLL2_HOLD_TIMER_9:8	R/W	0x1	See Register 445

1.154 R445 (Offset = 0x1BD)

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Table 1-156. R445 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_HOLD_TIMER	R/W	0x42	Rate of change to DPLL or APLL numerator during phase slew control. See DPLLx_HOLD_SLEW_STEP. ROM=Y, EEPROM=N

1.155 R446 (Offset = 0x1BE)

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Table 1-157. R446 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL2_PHS1_TIMER_9:8	R/W	0x1	See Register 447

1.156 R447 (Offset = 0x1BF)

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Table 1-158. R447 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_PHS1_TIMER	R/W	0x40	Holdover exit phase slew control. Timer controlling update period. ROM=Y, EEPROM=N

1.157 R452 (Offset = 0x1C4)

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Table 1-159. R452 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL2_HIST_GAIN	R/W	0x8	History filter gain ROM=Y, EEPROM=N

1.158 R453 (Offset = 0x1C5)

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Table 1-160. R453 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_PL_THRESH	R/W	0x1B	Phase lock in-lock threshold ROM=Y, EEPROM=N

1.159 R454 (Offset = 0x1C6)

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Table 1-161. R454 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_PL_UNLK_THRESH	R/W	0x1D	Phase lock out-of-lock threshold ROM=Y, EEPROM=N

1.160 R455 (Offset = 0x1C7)

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Table 1-162. R455 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_PHS1_THRESH	R/W	0x7	Holdover exit phase slew control. Change per timer event. ROM=Y, EEPROM=N

1.161 R458 (Offset = 0x1CA)

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Table 1-163. R458 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_HOLD_SLEW_STEP	R/W	0x3F	When DPLL exits holdover, rate of phase change relates to DPLLx_HOLD_SLEW_STEP over DPLLx_HOLD_TIMER. DPLLx_HOLD_SLEW_STEP is applied to DPLL numerator when exiting holdover or APLL numerator when using APLL relative DCO. ROM=Y, EEPROM=N

1.162 R460 (Offset = 0x1CC)

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Table 1-164. R460 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	DPLL2_STATUS_PL	R	0x1	Readback the phase lock status ROM=N, EEPROM=N
4:0	RESERVED	R	0x0	Reserved

1.163 R461 (Offset = 0x1CD)

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Table 1-165. R461 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	DPLL2_DCO_SLEW_ACTIVE	R	0x0	Readback DCO slew status ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.164 R464 (Offset = 0x1D0)

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Table 1-166. R464 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL2_FB_DIV_32:32	R/W	0x0	See Register 468

1.165 R465 (Offset = 0x1D1)

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Table 1-167. R465 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DIV_31:24	R/W	0x0	See Register 468

1.166 R466 (Offset = 0x1D2)

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Table 1-168. R466 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DIV_23:16	R/W	0x0	See Register 468

1.167 R467 (Offset = 0x1D3)

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Table 1-169. R467 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DIV_15:8	R/W	0x11	See Register 468

1.168 R468 (Offset = 0x1D4)

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Table 1-170. R468 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DIV	R/W	0x94	DPLL Feedback Divider N Value used with DPLL2 feedback configuration 1. Divide value is programmed value except when using ZDM mode with FB div, actual divide value is +1. ROM=Y, EEPROM=N

1.169 R469 (Offset = 0x1D5)

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Table 1-171. R469 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_39:32	R/W	0x0	See Register 473

1.170 R470 (Offset = 0x1D6)

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Table 1-172. R470 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_31:24	R/W	0x0	See Register 473

1.171 R471 (Offset = 0x1D7)

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Table 1-173. R471 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_23:16	R/W	0x0	See Register 473

1.172 R472 (Offset = 0x1D8)

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Table 1-174. R472 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_15:8	R/W	0x0	See Register 473

1.173 R473 (Offset = 0x1D9)

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Table 1-175. R473 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM	R/W	0x0	DPLL Feedback Divider Numerator Value used with DPLL2 feedback configuration 1 ROM=Y, EEPROM=N

1.174 R474 (Offset = 0x1DA)

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Table 1-176. R474 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DEN_39:32	R/W	0x0	See Register 478

1.175 R475 (Offset = 0x1DB)

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Table 1-177. R475 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DEN_31:24	R/W	0x0	See Register 478

1.176 R476 (Offset = 0x1DC)

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Table 1-178. R476 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DEN_23:16	R/W	0x0	See Register 478

1.177 R477 (Offset = 0x1DD)

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Table 1-179. R477 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DEN_15:8	R/W	0x0	See Register 478

1.178 R478 (Offset = 0x1DE)

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Table 1-180. R478 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DEN	R/W	0x0	DPLL Feedback Divider Denominator Value used with DPLL2 feedback configuration 1 ROM=Y, EEPROM=N

1.179 R479 (Offset = 0x1DF)

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Table 1-181. R479 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL2_FB2_DIV_32:32	R/W	0x0	See Register 483

1.180 R480 (Offset = 0x1E0)

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Table 1-182. R480 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DIV_31:24	R/W	0x0	See Register 483

1.181 R481 (Offset = 0x1E1)

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Table 1-183. R481 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DIV_23:16	R/W	0x0	See Register 483

1.182 R482 (Offset = 0x1E2)

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Table 1-184. R482 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DIV_15:8	R/W	0x2	See Register 483

1.183 R483 (Offset = 0x1E3)

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Table 1-185. R483 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DIV	R/W	0x32	DPLL Feedback Divider N Value used with DPLL2 feedback configuration 2. Divide value is programmed value except when using ZDM mode with FB div, actual divide value is +1. ROM=Y, EEPROM=N

1.184 R484 (Offset = 0x1E4)

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Table 1-186. R484 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_NUM_39:32	R/W	0x80	See Register 488

1.185 R485 (Offset = 0x1E5)

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Table 1-187. R485 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_NUM_31:24	R/W	0x0	See Register 488

1.186 R486 (Offset = 0x1E6)

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Table 1-188. R486 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_NUM_23:16	R/W	0x0	See Register 488

1.187 R487 (Offset = 0x1E7)

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Table 1-189. R487 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_NUM_15:8	R/W	0x0	See Register 488

1.188 R488 (Offset = 0x1E8)

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Table 1-190. R488 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_NUM	R/W	0x0	DPLL Feedback Divider Numerator Value used with DPLL2 feedback configuration 2 ROM=Y, EEPROM=N

1.189 R489 (Offset = 0x1E9)

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Table 1-191. R489 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DEN_39:32	R/W	0x0	See Register 493

1.190 R490 (Offset = 0x1EA)

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Table 1-192. R490 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DEN_31:24	R/W	0x0	See Register 493

1.191 R491 (Offset = 0x1EB)

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Table 1-193. R491 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DEN_23:16	R/W	0x0	See Register 493

1.192 R492 (Offset = 0x1EC)

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Table 1-194. R492 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DEN_15:8	R/W	0x0	See Register 493

1.193 R493 (Offset = 0x1ED)

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Table 1-195. R493 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DEN	R/W	0x0	DPLL Feedback Divider Denominator Value used with DPLL2 feedback configuration 2 ROM=Y, EEPROM=N

1.194 R494 (Offset = 0x1EE)

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Table 1-196. R494 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	DPLL2_REF5_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF3. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
4	DPLL2_REF4_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF4. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
3:2	RESERVED	R	0x0	Reserved
1	DPLL2_REF1_FB_SEL	R/W	0x1	DPLL Feedback N, NUM, DEN select for REF1. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
0	DPLL2_REF0_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF0. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2

1.195 R495 (Offset = 0x1EF)

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Table 1-197. R495 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:3	RESERVED	R	0x0	Reserved
2:0	DPLL2_FB_MASH_ORDER	R/W	0x2	DPLL Feedback Divider MASH Order. ROM=Y, EEPROM=N 0x0 = Integer 0x1 = 1st order 0x2 = 2nd order 0x3 = 3rd order 0x4 = 4th order

1.196 R496 (Offset = 0x1F0)

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Table 1-198. R496 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_FB_FDEV_37:32	R/W	0x0	See Register 500

1.197 R497 (Offset = 0x1F1)

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Table 1-199. R497 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_FDEV_31:24	R/W	0x0	See Register 500

1.198 R498 (Offset = 0x1F2)

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Table 1-200. R498 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_FDEV_23:16	R/W	0x0	See Register 500

1.199 R499 (Offset = 0x1F3)

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Table 1-201. R499 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_FDEV_15:8	R/W	0x0	See Register 500

1.200 R500 (Offset = 0x1F4)

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Table 1-202. R500 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_FDEV	R/W	0x0	DPLL Feedback Divider DCO Frequency Deviation Value ROM=Y, EEPROM=N

1.201 R501 (Offset = 0x1F5)

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Table 1-203. R501 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL2_FB_FDEV_UPDATE	R/W	0x0	Increment/Decrement DPLL Feedback Numerator value with DPLL_FB_FDEV value ROM=Y, EEPROM=N

1.202 R502 (Offset = 0x1F6)

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Table 1-204. R502 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL2_FB_FDEV_EN	R/W	0x0	Enable DPLL DCO mode ROM=Y, EEPROM=N

1.203 R503 (Offset = 0x1F7)

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Table 1-205. R503 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_STAT_39:32	R	0x0	See Register 507

1.204 R504 (Offset = 0x1F8)

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Table 1-206. R504 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_STAT_31:24	R	0x0	See Register 507

1.205 R505 (Offset = 0x1F9)

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Table 1-207. R505 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_STAT_23:16	R	0x0	See Register 507

1.206 R506 (Offset = 0x1FA)

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Table 1-208. R506 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_STAT_15:8	R	0x0	See Register 507

1.207 R507 (Offset = 0x1FB)

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Table 1-209. R507 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_STAT	R	0x0	Readback DPLL Feedback Divider Numerator value as a result of DCO mode ROM=N, EEPROM=N

1.208 R508 (Offset = 0x1FC)

Return to the [Summary Table](#).

Table 1-210. R508 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	DPLL2_REF0_DBLR_EN	R/W	0x0	DPLL Reference 0 Doubler Enable ROM=Y, EEPROM=N
2	DPLL2_REF1_DBLR_EN	R/W	0x0	DPLL Reference 1 Doubler Enable ROM=Y, EEPROM=N
1:0	RESERVED	R	0x0	Reserved

1.209 R509 (Offset = 0x1FD)

Return to the [Summary Table](#).

Table 1-211. R509 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF0_RDIV_15:8	R/W	0x0	See Register 510

1.210 R510 (Offset = 0x1FE)

Return to the [Summary Table](#).

Table 1-212. R510 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF0_RDIV	R/W	0x7D	DPLL Reference 0 R divider value ROM=Y, EEPROM=N

1.211 R511 (Offset = 0x1FF)

Return to the [Summary Table](#).

Table 1-213. R511 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF1_RDIV_15:8	R/W	0x0	See Register 512

1.212 R512 (Offset = 0x200)

Return to the [Summary Table](#).

Table 1-214. R512 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF1_RDIV	R/W	0x8	DPLL Reference 1 R divider value ROM=Y, EEPROM=N

1.213 R517 (Offset = 0x205)

Return to the [Summary Table](#).

Table 1-215. R517 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF4_RDIV_15:8	R/W	0x0	See Register 518

1.214 R518 (Offset = 0x206)

Return to the [Summary Table](#).

Table 1-216. R518 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF4_RDIV	R/W	0x0	DPLL REF4 R-divider value ROM=Y, EEPROM=N

1.215 R519 (Offset = 0x207)

Return to the [Summary Table](#).

Table 1-217. R519 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF5_RDIV_15:8	R/W	0x0	See Register 520

1.216 R520 (Offset = 0x208)

Return to the [Summary Table](#).

Table 1-218. R520 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF5_RDIV	R/W	0x0	DPLL Reference 3 R divider value ROM=Y, EEPROM=N

1.217 R523 (Offset = 0x20B)

Return to the [Summary Table](#).

Table 1-219. R523 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	DPLL1_REF0_AUTO_PRTY	R/W	0x2	REF0 Priority for Automatic Switchover. Sets the priority for REF0 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th
2:0	DPLL1_REF1_AUTO_PRTY	R/W	0x1	REF1 Priority for Automatic Switchover. Sets the priority for REF1 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.218 R525 (Offset = 0x20D)

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Table 1-220. R525 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-220. R525 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:3	RESERVED	R	0x0	Reserved
2:0	DPLL1_REF5_AUTO_PRTY	R/W	0x0	REF5 Priority for Automatic Switchover. Sets the priority for REF5 feedback from APLL2 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.219 R526 (Offset = 0x20E)

Return to the [Summary Table](#).

Table 1-221. R526 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5:3	DPLL1_MAN_REFSEL	R/W	0x0	DPLL1 Manual Reference Selection Mode. Determines how the manually selected reference is chosen. If this is set to a '1', the manually selected reference is taken from a GPIO input pin. If it is set to a '0', the manually selected reference is taken from a register. ROM=Y, EEPROM=N 0x0 = REF0 0x1 = REF1 0x2 = Reserved 0x3 = Reserved 0x4 = Reserved 0x5 = PLL2
2	DPLL1_MAN_SWITCH_PIN_MODE	R/W	0x0	DPLL1 Manual Reference Selection Mode. Determines how the manually selected reference is chosen. If this is set to a '1', the manually selected reference is taken from a GPIO input pin. If it is set to a '0', the manually selected reference is taken from a register. ROM=Y, EEPROM=N 0x0 = Register 0x1 = Pin

Table 1-221. R526 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	DPLL1_SWITCH_MODE	R/W	0x1	DPLL1 Reference Switchover Mode. Selects between Automatic Non-revertive, Automatic Revertive, Manual Selection with Automatic Fallback, and Manual Selection with Automatic Holdover. ROM=Y, EEPROM=N 0x0 = Auto non-revertive 0x1 = Auto revertive 0x2 = Manual with fallback 0x3 = Manual with holdover

1.220 R527 (Offset = 0x20F)

Return to the [Summary Table](#).

Table 1-222. R527 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_REFSEL_STAT	R	0x2	Reads the DPLL1 selected reference ROM=N, EEPROM=N 0x0 = Holdover 0x1 = REF0 0x2 = REF1 0x4 = Reserved 0x8 = Reserved 0x10 = Reserved 0x20 = APLL2

1.221 R528 (Offset = 0x210)

Return to the [Summary Table](#).

Table 1-223. R528 Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL1_LOCKDET_PPM_EN	R/W	0x1	DPLL frequency lock detect enable ROM=Y, EEPROM=N
6:0	DPLL1_LOCKDET_PPM_MAX_14:8	R/W	0x0	See Register 529

1.222 R529 (Offset = 0x211)

Return to the [Summary Table](#).

Table 1-224. R529 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_PPM_MAX	R/W	0xA	DPLL frequency lock detect in-lock threshold ROM=Y, EEPROM=N

1.223 R530 (Offset = 0x212)

Return to the [Summary Table](#).

Table 1-225. R530 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	DPLL1_UNLOCKDET_PPM_MAX_1 4:8	R/W	0x0	See Register 531

1.224 R531 (Offset = 0x213)

Return to the [Summary Table](#).

Table 1-226. R531 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_UNLOCKDET_PPM_MAX	R/W	0x64	DPLL frequency lock detect out-of-lock threshold ROM=Y, EEPROM=N

1.225 R532 (Offset = 0x214)

Return to the [Summary Table](#).

Table 1-227. R532 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_LOCKDET2_PPM_CNTSTR T_29:24	R/W	0x0	See Register 535

1.226 R533 (Offset = 0x215)

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Table 1-228. R533 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET2_PPM_CNTSTR T_23:16	R/W	0x3	See Register 535

1.227 R534 (Offset = 0x216)

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Table 1-229. R534 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET2_PPM_CNTSTR T_15:8	R/W	0xD	See Register 535

1.228 R535 (Offset = 0x217)

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Table 1-230. R535 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET2_PPM_CNTSTR T	R/W	0x40	DPLL frequency lock detect reference count value used with DPLL1 feedback configuration 2 ROM=Y, EEPROM=N

1.229 R536 (Offset = 0x218)

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Table 1-231. R536 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_LOCKDET_PPM_CNTSTR T_29:24	R/W	0x0	See Register 539

1.230 R537 (Offset = 0x219)

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Table 1-232. R537 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_PPM_CNTSTRT_23:16	R/W	0x1	See Register 539

1.231 R538 (Offset = 0x21A)

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Table 1-233. R538 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_PPM_CNTSTRT_15:8	R/W	0xDC	See Register 539

1.232 R539 (Offset = 0x21B)

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Table 1-234. R539 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_PPM_CNTSTRT	R/W	0xD7	DPLL frequency lock detect reference count value used with DPLL1 feedback configuration 1 ROM=Y, EEPROM=N

1.233 R540 (Offset = 0x21C)

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Table 1-235. R540 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_LOCKDET_VCO_PPM_CNTSTRT_29:24	R/W	0x0	See Register 543

1.234 R541 (Offset = 0x21D)

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Table 1-236. R541 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_VCO_PPM_CNT STRT_23:16	R/W	0x98	See Register 543

1.235 R542 (Offset = 0x21E)

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Table 1-237. R542 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_VCO_PPM_CNT STRT_15:8	R/W	0x96	See Register 543

1.236 R543 (Offset = 0x21F)

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Table 1-238. R543 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_VCO_PPM_CNT STRT	R/W	0xB8	DPLL frequency lock detect VCO count value ROM=Y, EEPROM=N

1.237 R544 (Offset = 0x220)

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Table 1-239. R544 Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:1	RESERVED	R	0x0	Reserved
0	DPLL1_STATUS_PPM_LOCK	R	0x1	Readback lock indicator from DPLL PPM Checker ROM=N, EEPROM=N

1.238 R547 (Offset = 0x223)

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Table 1-240. R547 Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL1_LOOP_EN	R/W	0x1	Enable DPLL1 loop filter and R-Div mash engine ROM=Y, EEPROM=N
6	DPLL1_PHASE_CANCEL_EN	R/W	0x1	Enable Phase Cancellation ROM=Y, EEPROM=N
5	DPLL1_FASTLOCK_ALWAYS	R/W	0x0	Always perform fastlock. No phase cancellation is done. ROM=Y, EEPROM=N
4	DPLL1_PHS1_EN	R/W	0x1	Enable holdover exit phase slew control . ROM=Y, EEPROM=N
3	DPLL1_ZDM_EN	R/W	0x0	Enable Zero Delay mode ROM=Y, EEPROM=N
2	DPLL1_HIST_EN	R/W	0x1	Enable History word to be used during holdover ROM=Y, EEPROM=N
1	DPLL1_PHASE_CANCEL_ALWAYS	R/W	0x0	Force phase cancellation to always occur when DPLL is acquiring lock. ROM=Y, EEPROM=N
0	RESERVED	R	0x0	Reserved

1.239 R548 (Offset = 0x224)

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Table 1-241. R548 Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL1_HOLD_SLEW_LIM_EN	R/W	0x0	During holdover enable slew limiter ROM=Y, EEPROM=N
6:0	RESERVED	R	0x0	Reserved

1.240 R550 (Offset = 0x226)

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Table 1-242. R550 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL1_PH_OFFSET_44:40	R/W	0x0	See Register 555

1.241 R551 (Offset = 0x227)

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Table 1-243. R551 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DP1L1_PH_OFFSET_39:32	R/W	0x0	See Register 555

1.242 R552 (Offset = 0x228)

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Table 1-244. R552 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DP1L1_PH_OFFSET_31:24	R/W	0x0	See Register 555

1.243 R553 (Offset = 0x229)

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Table 1-245. R553 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DP1L1_PH_OFFSET_23:16	R/W	0x0	See Register 555

1.244 R554 (Offset = 0x22A)

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Table 1-246. R554 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DP1L1_PH_OFFSET_15:8	R/W	0x0	See Register 555

1.245 R555 (Offset = 0x22B)

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Table 1-247. R555 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DP1L1_PH_OFFSET	R/W	0x0	Phase offset to adjust and calibrate input to output phase in ZDM. This is a 2s complement number. ROM=Y, EEPROM=N

1.246 R556 (Offset = 0x22C)

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Table 1-248. R556 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FREE_RUN_39:32	R/W	0x0	See Register 560

1.247 R557 (Offset = 0x22D)

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Table 1-249. R557 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FREE_RUN_31:24	R/W	0x0	See Register 560

1.248 R558 (Offset = 0x22E)

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Table 1-250. R558 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FREE_RUN_23:16	R/W	0x0	See Register 560

1.249 R559 (Offset = 0x22F)

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Table 1-251. R559 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FREE_RUN_15:8	R/W	0x0	See Register 560

1.250 R560 (Offset = 0x230)

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Table 1-252. R560 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FREE_RUN	R/W	0x0	DPLL starting word. Also non-history holdover word. ROM=Y, EEPROM=N

1.251 R561 (Offset = 0x231)

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Table 1-253. R561 Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL1_PPM_REF_SEL	R/W	0x0	PPM Detector Reference Selection for DPLL1 LOFL. When set to 0, the selected DPLL input reference is used resulting in DPLL1 LOFL as expected. When set to 1, the XO is used as a frequency enabling LOFL for APLL1, no DPLL is required. This bit enables a "BAW LOCK" indicator. ROM=Y, EEPROM=N 0x0 = LOFL_DPLL1 = DPLL1 DLD 0x1 = LOFL_DPLL1 = APLL1 DLD
6	DPLL1_1PPS_MODE	R/W	0x0	Set when using 1-PPS input ROM=Y, EEPROM=N
5	DPLL1_1PPS_EN	R/W	0x0	Set when using 1-PPS input ROM=Y, EEPROM=N
4:0	RESERVED	R	0x0	Reserved

1.252 R590 (Offset = 0x24E)

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Table 1-254. R590 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL1_LCK_TIMER_9:8	R/W	0x3	See Register 591

1.253 R591 (Offset = 0x24F)

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Table 1-255. R591 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LCK_TIMER	R/W	0xCC	Minimum amount of time until DPLL1_LOPL will be deasserted after starting to lock. Timer begins once device is within valid phase lock window. ROM=Y, EEPROM=N

1.254 R592 (Offset = 0x250)

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Table 1-256. R592 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL1_HIST_TIMER_9:8	R/W	0x1	See Register 593

1.255 R593 (Offset = 0x251)

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Table 1-257. R593 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_HIST_TIMER	R/W	0x92	History timer ROM=Y, EEPROM=N

1.256 R594 (Offset = 0x252)

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Table 1-258. R594 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R	0x0	Reserved
1:0	DPLL1_HOLD_TIMER_9:8	R/W	0x1	See Register 595

1.257 R595 (Offset = 0x253)

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Table 1-259. R595 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_HOLD_TIMER	R/W	0x42	Rate of change to DPLL or APLL numerator during phase slew control. See DPLLx_HOLD_SLEW_STEP. ROM=Y, EEPROM=N

1.258 R596 (Offset = 0x254)

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Table 1-260. R596 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL1_PHS1_TIMER_9:8	R/W	0x1	See Register 597

1.259 R597 (Offset = 0x255)

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Table 1-261. R597 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_PHS1_TIMER	R/W	0x40	Holdover exit phase slew control. Timer controlling update period. ROM=Y, EEPROM=N

1.260 R602 (Offset = 0x25A)

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Table 1-262. R602 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL1_HIST_GAIN	R/W	0x8	History filter gain ROM=Y, EEPROM=N

1.261 R603 (Offset = 0x25B)

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Table 1-263. R603 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_PL_THRESH	R/W	0x1F	Phase lock in-lock threshold ROM=Y, EEPROM=N

1.262 R604 (Offset = 0x25C)

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Table 1-264. R604 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_PL_UNLK_THRESH	R/W	0x22	Phase lock out-of-lock threshold ROM=Y, EEPROM=N

1.263 R605 (Offset = 0x25D)

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Table 1-265. R605 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_PHS1_THRESH	R/W	0x7	Holdover exit phase slew control. Change per timer event. ROM=Y, EEPROM=N

1.264 R610 (Offset = 0x262)

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Table 1-266. R610 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	DPLL1_STATUS_PL	R	0x1	Readback the phase lock status ROM=N, EEPROM=N
4:0	RESERVED	R	0x0	Reserved

1.265 R611 (Offset = 0x263)

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Table 1-267. R611 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	DPLL1_DCO_SLEW_ACTIVE	R	0x0	Readback DCO slew status ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.266 R614 (Offset = 0x266)

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Table 1-268. R614 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL1_FB_DIV_32:32	R/W	0x0	See Register 618

1.267 R615 (Offset = 0x267)

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Table 1-269. R615 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DIV_31:24	R/W	0x0	See Register 618

1.268 R616 (Offset = 0x268)

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Table 1-270. R616 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DIV_23:16	R/W	0x0	See Register 618

1.269 R617 (Offset = 0x269)

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Table 1-271. R617 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DIV_15:8	R/W	0x7	See Register 618

1.270 R618 (Offset = 0x26A)

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Table 1-272. R618 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DIV	R/W	0xAE	DPLL Feedback Divider N Value used with DPLL1 feedback configuration 1. Divide value is programmed value except when using ZDM mode with FB div, actual divide value is +1. ROM=Y, EEPROM=N

1.271 R619 (Offset = 0x26B)

Return to the [Summary Table](#).

Table 1-273. R619 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_39:32	R/W	0x14	See Register 623

1.272 R620 (Offset = 0x26C)

Return to the [Summary Table](#).

Table 1-274. R620 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_31:24	R/W	0x7A	See Register 623

1.273 R621 (Offset = 0x26D)

Return to the [Summary Table](#).

Table 1-275. R621 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_23:16	R/W	0xE1	See Register 623

1.274 R622 (Offset = 0x26E)

Return to the [Summary Table](#).

Table 1-276. R622 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_15:8	R/W	0x47	See Register 623

1.275 R623 (Offset = 0x26F)

Return to the [Summary Table](#).

Table 1-277. R623 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM	R/W	0xAE	DPLL Feedback Divider Numerator Value used with DPLL1 feedback configuration 1 ROM=Y, EEPROM=N

1.276 R624 (Offset = 0x270)

Return to the [Summary Table](#).

Table 1-278. R624 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DEN_39:32	R/W	0xFF	See Register 628

1.277 R625 (Offset = 0x271)

Return to the [Summary Table](#).

Table 1-279. R625 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DEN_31:24	R/W	0xFF	See Register 628

1.278 R626 (Offset = 0x272)

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Table 1-280. R626 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DEN_23:16	R/W	0xFF	See Register 628

1.279 R627 (Offset = 0x273)

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Table 1-281. R627 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DEN_15:8	R/W	0xFF	See Register 628

1.280 R628 (Offset = 0x274)

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Table 1-282. R628 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DEN	R/W	0xFF	DPLL Feedback Divider Denominator Value used with DPLL1 feedback configuration 1 ROM=Y, EEPROM=N

1.281 R629 (Offset = 0x275)

Return to the [Summary Table](#).

Table 1-283. R629 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL1_FB2_DIV_32:32	R/W	0x0	See Register 633

1.282 R630 (Offset = 0x276)

Return to the [Summary Table](#).

Table 1-284. R630 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DIV_31:24	R/W	0x0	See Register 633

1.283 R631 (Offset = 0x277)

Return to the [Summary Table](#).

Table 1-285. R631 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DIV_23:16	R/W	0x0	See Register 633

1.284 R632 (Offset = 0x278)

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Table 1-286. R632 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DIV_15:8	R/W	0x0	See Register 633

1.285 R633 (Offset = 0x279)

Return to the [Summary Table](#).

Table 1-287. R633 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DIV	R/W	0xF5	DPLL Feedback Divider N Value used with DPLL1 feedback configuration 2. Divide value is programmed value except when using ZDM mode with FB div, actual divide value is +1. ROM=Y, EEPROM=N

1.286 R634 (Offset = 0x27A)

Return to the [Summary Table](#).

Table 1-288. R634 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_NUM_39:32	R/W	0xC2	See Register 638

1.287 R635 (Offset = 0x27B)

Return to the [Summary Table](#).

Table 1-289. R635 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_NUM_31:24	R/W	0x8F	See Register 638

1.288 R636 (Offset = 0x27C)

Return to the [Summary Table](#).

Table 1-290. R636 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_NUM_23:16	R/W	0x5C	See Register 638

1.289 R637 (Offset = 0x27D)

Return to the [Summary Table](#).

Table 1-291. R637 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_NUM_15:8	R/W	0x28	See Register 638

1.290 R638 (Offset = 0x27E)

Return to the [Summary Table](#).

Table 1-292. R638 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_NUM	R/W	0xF5	DPLL Feedback Divider Numerator Value used with DPLL1 feedback configuration 2 ROM=Y, EEPROM=N

1.291 R639 (Offset = 0x27F)

Return to the [Summary Table](#).

Table 1-293. R639 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DEN_39:32	R/W	0xFF	See Register 643

1.292 R640 (Offset = 0x280)

Return to the [Summary Table](#).

Table 1-294. R640 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DEN_31:24	R/W	0xFF	See Register 643

1.293 R641 (Offset = 0x281)

Return to the [Summary Table](#).

Table 1-295. R641 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DEN_23:16	R/W	0xFF	See Register 643

1.294 R642 (Offset = 0x282)

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Table 1-296. R642 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DEN_15:8	R/W	0xFF	See Register 643

1.295 R643 (Offset = 0x283)

Return to the [Summary Table](#).

Table 1-297. R643 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DEN	R/W	0xFF	DPLL Feedback Divider Denominator Value used with DPLL1 feedback configuration 2 ROM=Y, EEPROM=N

1.296 R644 (Offset = 0x284)

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Table 1-298. R644 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	DPLL1_REF5_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF5. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
4	DPLL1_REF4_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF4. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
3:2	RESERVED	R	0x0	Reserved
1	DPLL1_REF1_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF1. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2

Table 1-298. R644 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DPLL1_REF0_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF0. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2

1.297 R645 (Offset = 0x285)

Return to the [Summary Table](#).

Table 1-299. R645 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:3	RESERVED	R	0x0	Reserved
2:0	DPLL1_FB_MASH_ORDER	R/W	0x3	DPLL Feedback Divider MASH Order. ROM=Y, EEPROM=N 0x0 = Integer 0x1 = 1st order 0x2 = 2nd order 0x3 = 3rd order 0x4 = 4th order

1.298 R646 (Offset = 0x286)

Return to the [Summary Table](#).

Table 1-300. R646 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_FB_FDEV_37:32	R/W	0x0	See Register 650

1.299 R647 (Offset = 0x287)

Return to the [Summary Table](#).

Table 1-301. R647 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_FDEV_31:24	R/W	0x0	See Register 650

1.300 R648 (Offset = 0x288)

Return to the [Summary Table](#).

Table 1-302. R648 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_FDEV_23:16	R/W	0x0	See Register 650

1.301 R649 (Offset = 0x289)

Return to the [Summary Table](#).

Table 1-303. R649 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_FDEV_15:8	R/W	0x0	See Register 650

1.302 R650 (Offset = 0x28A)

Return to the [Summary Table](#).

Table 1-304. R650 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_FDEV	R/W	0x0	DPLL Feedback Divider DCO Frequency Deviation Value ROM=Y, EEPROM=N

1.303 R651 (Offset = 0x28B)

Return to the [Summary Table](#).

Table 1-305. R651 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL1_FB_FDEV_UPDATE	R/W	0x0	Increment/Decrement DPLL Feedback Numerator value with DPLL_FB_FDEV value ROM=Y, EEPROM=N

1.304 R652 (Offset = 0x28C)

Return to the [Summary Table](#).

Table 1-306. R652 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPPLL1_FB_FDEV_EN	R/W	0x0	Enable DPPLL DCO mode ROM=Y, EEPROM=N

1.305 R653 (Offset = 0x28D)

Return to the [Summary Table](#).

Table 1-307. R653 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPPLL1_FB_NUM_STAT_39:32	R	0x14	See Register 657

1.306 R654 (Offset = 0x28E)

Return to the [Summary Table](#).

Table 1-308. R654 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPPLL1_FB_NUM_STAT_31:24	R	0x7A	See Register 657

1.307 R655 (Offset = 0x28F)

Return to the [Summary Table](#).

Table 1-309. R655 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPPLL1_FB_NUM_STAT_23:16	R	0xE1	See Register 657

1.308 R656 (Offset = 0x290)

Return to the [Summary Table](#).

Table 1-310. R656 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPPLL1_FB_NUM_STAT_15:8	R	0x47	See Register 657

1.309 R657 (Offset = 0x291)

Return to the [Summary Table](#).

Table 1-311. R657 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_STAT	R	0xAE	Readback DPLL Feedback Divider Numerator value as a result of DCO mode ROM=N, EEPROM=N

1.310 R658 (Offset = 0x292)

Return to the [Summary Table](#).

Table 1-312. R658 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	DPLL1_REF0_DBLR_EN	R/W	0x0	DPLL Reference 0 Doubler Enable ROM=Y, EEPROM=N
2	DPLL1_REF1_DBLR_EN	R/W	0x0	DPLL Reference 1 Doubler Enable ROM=Y, EEPROM=N
1:0	RESERVED	R	0x0	Reserved

1.311 R659 (Offset = 0x293)

Return to the [Summary Table](#).

Table 1-313. R659 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF0_RDIV_15:8	R/W	0x0	See Register 660

1.312 R660 (Offset = 0x294)

Return to the [Summary Table](#).

Table 1-314. R660 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF0_RDIV	R/W	0x7D	DPLL Reference 0 R divider value ROM=Y, EEPROM=N

1.313 R661 (Offset = 0x295)

Return to the [Summary Table](#).

Table 1-315. R661 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF1_RDIV_15:8	R/W	0x0	See Register 662

1.314 R662 (Offset = 0x296)

Return to the [Summary Table](#).

Table 1-316. R662 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF1_RDIV	R/W	0x8	DPLL Reference 1 R divider value ROM=Y, EEPROM=N

1.315 R669 (Offset = 0x29D)

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Table 1-317. R669 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF5_RDIV_15:8	R/W	0x1	See Register 670

1.316 R670 (Offset = 0x29E)

Return to the [Summary Table](#).

Table 1-318. R670 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF5_RDIV	R/W	0x1	DPLL Reference 5 R divider value ROM=Y, EEPROM=N

1.317 R745 (Offset = 0x2E9)

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Table 1-319. R745 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-319. R745 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RESERVED	R	0x0	Reserved
5	PLL3_NDIV_OUTPUT_EN	R/W	0x0	If GPIOx_SEL selects PLL1 N/2 as an output. Then this bit must be set along with STATUS_MUX_DIV2_EN=1. ROM=N, EEPROM=N
4:0	RESERVED	R	0x0	Reserved

1.318 R773 (Offset = 0x305)

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Table 1-320. R773 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	RESERVED	R	0x0	Reserved

1.319 R777 (Offset = 0x309)

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Table 1-321. R777 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_CP_PU_R	R/W	0x22	PLL charge pump pull-up resistor selection ROM=Y, EEPROM=N 0x0 = Disabled 0x1 = 78 kΩ 0x2 = 39 kΩ 0x3 = 26 kΩ 0x4 = 20 kΩ 0x5 = 15.9 kΩ 0x6 = 13.2 kΩ 0x7 = 11.3 kΩ 0x8 = 9.8 kΩ 0x9 = 8.71 kΩ 0xA = 7.83 kΩ 0xB = 7.12 kΩ 0xC = 6.58 kΩ 0xD = 6.07 kΩ 0xE = 5.63 kΩ 0xF = 5.25 kΩ 0x10 = 4.9 kΩ 0x11 = 4.61 kΩ 0x12 = 4.35 kΩ 0x13 = 4.12 kΩ 0x14 = 3.94 kΩ 0x15 = 3.75 kΩ 0x16 = 3.57 kΩ 0x17 = 3.42 kΩ 0x18 = 3.27 kΩ 0x19 = 3.14 kΩ 0x1A = 3.01 kΩ 0x1B = 2.9 kΩ 0x1C = 2.81 kΩ 0x1D = 2.71 kΩ 0x1E = 2.62 kΩ 0x1F = 2.53 kΩ 0x20 = 2.4 kΩ 0x21 = 2.33 kΩ 0x22 = 2.26 kΩ 0x23 = 2.2 kΩ 0x24 = 2.14 kΩ 0x25 = 2.09 kΩ 0x26 = 2.03 kΩ 0x27 = 1.98 kΩ 0x28 = 1.93 kΩ 0x29 = 1.88 kΩ 0x2A = 1.84 kΩ 0x2B = 1.79 kΩ 0x2C = 1.76 kΩ 0x2D = 1.72 kΩ 0x2E = 1.68 kΩ

Table 1-321. R777 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 1.65 kΩ
				0x30 = 1.61 kΩ
				0x31 = 1.58 kΩ
				0x32 = 1.55 kΩ
				0x33 = 1.52 kΩ
				0x34 = 1.49 kΩ
				0x35 = 1.46 kΩ
				0x36 = 1.44 kΩ
				0x37 = 1.41 kΩ
				0x38 = 1.38 kΩ
				0x39 = 1.36 kΩ
				0x3A = 1.34 kΩ
				0x3B = 1.31 kΩ
				0x3C = 1.29 kΩ
				0x3D = 1.27 kΩ
				0x3E = 1.25 kΩ
				0x3F = 1.23 kΩ
				0x40 = 1.2 kΩ
				0x41 = 1.18 kΩ
				0x42 = 1.16 kΩ
				0x43 = 1.15 kΩ
				0x44 = 1.13 kΩ
				0x45 = 1.12 kΩ
				0x46 = 1.1 kΩ
				0x47 = 1.08 kΩ
				0x48 = 1.07 kΩ
				0x49 = 1.05 kΩ
				0x4A = 1.04 kΩ
				0x4B = 1.03 kΩ
				0x4C = 1.01 kΩ
				0x4D = 1 kΩ
				0x4E = 0.989 kΩ
				0x4F = 0.977 kΩ
				0x50 = 0.964 kΩ
				0x51 = 0.952 kΩ
				0x52 = 0.941 kΩ
				0x53 = 0.929 kΩ
				0x54 = 0.92 kΩ
				0x55 = 0.909 kΩ
				0x56 = 0.898 kΩ
				0x57 = 0.888 kΩ
				0x58 = 0.878 kΩ
				0x59 = 0.868 kΩ
				0x5A = 0.858 kΩ
				0x5B = 0.849 kΩ
				0x5C = 0.841 kΩ
				0x5D = 0.832 kΩ
				0x5E = 0.823 kΩ
				0x5F = 0.814 kΩ

Table 1-321. R777 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x60 = 0.8 kΩ
				0x61 = 0.792 kΩ
				0x62 = 0.784 kΩ
				0x63 = 0.776 kΩ
				0x64 = 0.769 kΩ
				0x65 = 0.762 kΩ
				0x66 = 0.754 kΩ
				0x67 = 0.747 kΩ
				0x68 = 0.74 kΩ
				0x69 = 0.733 kΩ
				0x6A = 0.726 kΩ
				0x6B = 0.719 kΩ
				0x6C = 0.713 kΩ
				0x6D = 0.707 kΩ
				0x6E = 0.7 kΩ
				0x6F = 0.694 kΩ
				0x70 = 0.688 kΩ
				0x71 = 0.682 kΩ
				0x72 = 0.676 kΩ
				0x73 = 0.67 kΩ
				0x74 = 0.665 kΩ
				0x75 = 0.659 kΩ
				0x76 = 0.654 kΩ
				0x77 = 0.648 kΩ
				0x78 = 0.643 kΩ
				0x79 = 0.637 kΩ
				0x7A = 0.632 kΩ
				0x7B = 0.627 kΩ
				0x7C = 0.623 kΩ
				0x7D = 0.618 kΩ
				0x7E = 0.613 kΩ
				0x7F = 0.608 kΩ
				0x80 = 0.6 kΩ
				0x81 = 0.595 kΩ
				0x82 = 0.591 kΩ
				0x83 = 0.586 kΩ
				0x84 = 0.583 kΩ
				0x85 = 0.578 kΩ
				0x86 = 0.574 kΩ
				0x87 = 0.57 kΩ
				0x88 = 0.565 kΩ
				0x89 = 0.561 kΩ
				0x8A = 0.557 kΩ
				0x8B = 0.553 kΩ
				0x8C = 0.55 kΩ
				0x8D = 0.546 kΩ
				0x8E = 0.542 kΩ
				0x8F = 0.538 kΩ
				0x90 = 0.535 kΩ

Table 1-321. R777 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x91 = 0.531 kΩ
				0x92 = 0.527 kΩ
				0x93 = 0.524 kΩ
				0x94 = 0.521 kΩ
				0x95 = 0.517 kΩ
				0x96 = 0.514 kΩ
				0x97 = 0.51 kΩ
				0x98 = 0.507 kΩ
				0x99 = 0.504 kΩ
				0x9A = 0.5 kΩ
				0x9B = 0.497 kΩ
				0x9C = 0.494 kΩ
				0x9D = 0.491 kΩ
				0x9E = 0.488 kΩ
				0x9F = 0.485 kΩ
				0xA0 = 0.48 kΩ
				0xA1 = 0.477 kΩ
				0xA2 = 0.474 kΩ
				0xA3 = 0.471 kΩ
				0xA4 = 0.469 kΩ
				0xA5 = 0.466 kΩ
				0xA6 = 0.463 kΩ
				0xA7 = 0.46 kΩ
				0xA8 = 0.458 kΩ
				0xA9 = 0.455 kΩ
				0xAA = 0.452 kΩ
				0xAB = 0.45 kΩ
				0xAC = 0.447 kΩ
				0xAD = 0.445 kΩ
				0xAE = 0.442 kΩ
				0xAF = 0.44 kΩ
				0xB0 = 0.437 kΩ
				0xB1 = 0.435 kΩ
				0xB2 = 0.432 kΩ
				0xB3 = 0.43 kΩ
				0xB4 = 0.428 kΩ
				0xB5 = 0.425 kΩ
				0xB6 = 0.423 kΩ
				0xB7 = 0.421 kΩ
				0xB8 = 0.419 kΩ
				0xB9 = 0.416 kΩ
				0xBA = 0.414 kΩ
				0xBB = 0.412 kΩ
				0xBC = 0.41 kΩ
				0xBD = 0.408 kΩ
				0xBE = 0.406 kΩ
				0xBF = 0.404 kΩ
				0xC0 = 0.4 kΩ
				0xC1 = 0.398 kΩ

Table 1-321. R777 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xC2 = 0.396 kΩ 0xC3 = 0.394 kΩ 0xC4 = 0.392 kΩ 0xC5 = 0.39 kΩ 0xC6 = 0.388 kΩ 0xC7 = 0.386 kΩ 0xC8 = 0.384 kΩ 0xC9 = 0.382 kΩ 0xCA = 0.381 kΩ 0xCB = 0.379 kΩ 0xCC = 0.377 kΩ 0xCD = 0.375 kΩ 0xCE = 0.373 kΩ 0xCF = 0.372 kΩ 0xD0 = 0.37 kΩ 0xD1 = 0.368 kΩ 0xD2 = 0.366 kΩ 0xD3 = 0.365 kΩ 0xD4 = 0.363 kΩ 0xD5 = 0.361 kΩ 0xD6 = 0.36 kΩ 0xD7 = 0.358 kΩ 0xD8 = 0.356 kΩ 0xD9 = 0.355 kΩ 0xDA = 0.353 kΩ 0xDB = 0.352 kΩ 0xDC = 0.35 kΩ 0xDD = 0.349 kΩ 0xDE = 0.347 kΩ 0xDF = 0.345 kΩ 0xE0 = 0.343 kΩ 0xE1 = 0.341 kΩ 0xE2 = 0.34 kΩ 0xE3 = 0.338 kΩ 0xE4 = 0.337 kΩ 0xE5 = 0.336 kΩ 0xE6 = 0.334 kΩ 0xE7 = 0.333 kΩ 0xE8 = 0.331 kΩ 0xE9 = 0.33 kΩ 0xEA = 0.328 kΩ 0xEB = 0.327 kΩ 0xEC = 0.326 kΩ 0xED = 0.325 kΩ 0xEE = 0.323 kΩ 0xEF = 0.322 kΩ 0xF0 = 0.32 kΩ 0xF1 = 0.319 kΩ 0xF2 = 0.318 kΩ

Table 1-321. R777 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xF3 = 0.317 kΩ 0xF4 = 0.315 kΩ 0xF5 = 0.314 kΩ 0xF6 = 0.313 kΩ 0xF7 = 0.312 kΩ 0xF8 = 0.31 kΩ 0xF9 = 0.309 kΩ 0xFA = 0.308 kΩ 0xFB = 0.307 kΩ 0xFC = 0.306 kΩ 0xFD = 0.304 kΩ 0xFE = 0.303 kΩ 0xFF = 0.302 kΩ

1.320 R778 (Offset = 0x30A)

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Table 1-322. R778 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	PLL2_CP_PU_DIS	R/W	0x0	PLL charge pump - pump up disable ROM=Y, EEPROM=N
3:0	PLL2_CPG	R/W	0x9	PLL charge pump gain ROM=Y, EEPROM=Y 0x0 = 0 mA 0x1 = 0.4 mA 0x2 = 0.8 mA 0x3 = 1.2 mA 0x4 = 1.6 mA 0x5 = 2.0 mA 0x6 = 2.4 mA 0x7 = 2.8 mA 0x8 = 3.0 mA 0x9 = 3.4 mA 0xA = 3.8 mA 0xB = 4.2 mA 0xC = 4.6 mA 0xD = 5.0 mA 0xE = 5.4 mA 0xF = 5.8 mA

1.321 R779 (Offset = 0x30B)

Return to the [Summary Table](#).

Table 1-323. R779 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_LF_R2	R/W	0x7	PLL Loop Filter R2 setting ROM=Y, EEPROM=N 0x0 = 0.016 kΩ 0x1 = 0.301 kΩ 0x2 = 0.551 kΩ 0x3 = 0.209 kΩ 0x4 = 1.05 kΩ 0x5 = 0.244 kΩ 0x6 = 0.375 kΩ 0x7 = 0.183 kΩ 0x8 = 2.05 kΩ 0x9 = 0.269 kΩ 0xA = 0.444 kΩ 0xB = 0.194 kΩ 0xC = 0.709 kΩ 0xD = 0.224 kΩ 0xE = 0.0446 kΩ 0xF = 0.0421 kΩ 0x10 = 0.932 kΩ 0x11 = 1.18 kΩ 0x12 = 1.43 kΩ 0x13 = 1.09 kΩ 0x14 = 1.93 kΩ 0x15 = 1.13 kΩ 0x16 = 1.26 kΩ 0x17 = 1.07 kΩ 0x18 = 2.93 kΩ 0x19 = 1.15 kΩ 0x1A = 1.33 kΩ 0x1B = 1.08 kΩ 0x1C = 1.59 kΩ 0x1D = 1.11 kΩ 0x1E = 0.929 kΩ 0x1F = 0.926 kΩ 0x20 = 1.83 kΩ 0x21 = 2.08 kΩ 0x22 = 2.33 kΩ 0x23 = 1.99 kΩ 0x24 = 2.83 kΩ 0x25 = 2.03 kΩ 0x26 = 2.16 kΩ 0x27 = 1.97 kΩ 0x28 = 3.83 kΩ 0x29 = 2.05 kΩ 0x2A = 2.23 kΩ 0x2B = 1.98 kΩ 0x2C = 2.49 kΩ 0x2D = 2.01 kΩ 0x2E = 1.83 kΩ

Table 1-323. R779 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 1.83 kΩ 0x30 = 2.72 kΩ 0x31 = 2.97 kΩ 0x32 = 3.22 kΩ 0x33 = 2.88 kΩ 0x34 = 3.72 kΩ 0x35 = 2.91 kΩ 0x36 = 3.04 kΩ 0x37 = 2.85 kΩ 0x38 = 4.72 kΩ 0x39 = 2.94 kΩ 0x3A = 3.11 kΩ 0x3B = 2.86 kΩ 0x3C = 3.38 kΩ 0x3D = 2.89 kΩ 0x3E = 2.71 kΩ 0x3F = 2.71 kΩ

1.322 R780 (Offset = 0x30C)Return to the [Summary Table](#).**Table 1-324. R780 Field Descriptions**

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-324. R780 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL2_LF_R3	R/W	0x2	PLL Loop Filter R3 setting ROM=Y, EEPROM=N 0x0 = 0.016 kΩ 0x1 = 0.277 kΩ 0x2 = 0.657 kΩ 0x3 = 0.214 kΩ 0x4 = 0.754 kΩ 0x5 = 0.221 kΩ 0x6 = 0.375 kΩ 0x7 = 0.183 kΩ 0x8 = 0.863 kΩ 0x9 = 1.08 kΩ 0xA = 1.46 kΩ 0xB = 1.01 kΩ 0xC = 1.55 kΩ 0xD = 1.02 kΩ 0xE = 1.17 kΩ 0xF = 0.982 kΩ 0x10 = 1.68 kΩ 0x11 = 1.89 kΩ 0x12 = 2.27 kΩ 0x13 = 1.83 kΩ 0x14 = 2.37 kΩ 0x15 = 1.84 kΩ 0x16 = 1.99 kΩ 0x17 = 1.8 kΩ 0x18 = 2.48 kΩ 0x19 = 2.69 kΩ 0x1A = 3.07 kΩ 0x1B = 2.63 kΩ 0x1C = 3.17 kΩ 0x1D = 2.63 kΩ 0x1E = 2.79 kΩ 0x1F = 2.6 kΩ 0x20 = 3.31 kΩ 0x21 = 3.52 kΩ 0x22 = 3.9 kΩ 0x23 = 3.46 kΩ 0x24 = 4 kΩ 0x25 = 3.47 kΩ 0x26 = 3.62 kΩ 0x27 = 3.43 kΩ 0x28 = 4.11 kΩ 0x29 = 4.32 kΩ 0x2A = 4.7 kΩ 0x2B = 4.26 kΩ 0x2C = 4.8 kΩ 0x2D = 4.26 kΩ 0x2E = 4.42 kΩ

Table 1-324. R780 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 4.23 kΩ 0x30 = 4.92 kΩ 0x31 = 5.14 kΩ 0x32 = 5.52 kΩ 0x33 = 5.07 kΩ 0x34 = 5.61 kΩ 0x35 = 5.08 kΩ 0x36 = 5.23 kΩ 0x37 = 5.04 kΩ 0x38 = 5.72 kΩ 0x39 = 5.94 kΩ 0x3A = 6.32 kΩ 0x3B = 5.87 kΩ 0x3C = 6.41 kΩ 0x3D = 5.88 kΩ 0x3E = 6.03 kΩ 0x3F = 5.84 kΩ

1.323 R781 (Offset = 0x30D)

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Table 1-325. R781 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-325. R781 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL2_LF_R4	R/W	0x2	PLL Loop Filter R4 setting ROM=Y, EEPROM=N 0x0 = 0.016 kΩ 0x1 = 0.277 kΩ 0x2 = 0.657 kΩ 0x3 = 0.214 kΩ 0x4 = 0.754 kΩ 0x5 = 0.221 kΩ 0x6 = 0.375 kΩ 0x7 = 0.183 kΩ 0x8 = 0.863 kΩ 0x9 = 1.08 kΩ 0xA = 1.46 kΩ 0xB = 1.01 kΩ 0xC = 1.55 kΩ 0xD = 1.02 kΩ 0xE = 1.17 kΩ 0xF = 0.982 kΩ 0x10 = 1.68 kΩ 0x11 = 1.89 kΩ 0x12 = 2.27 kΩ 0x13 = 1.83 kΩ 0x14 = 2.37 kΩ 0x15 = 1.84 kΩ 0x16 = 1.99 kΩ 0x17 = 1.8 kΩ 0x18 = 2.48 kΩ 0x19 = 2.69 kΩ 0x1A = 3.07 kΩ 0x1B = 2.63 kΩ 0x1C = 3.17 kΩ 0x1D = 2.63 kΩ 0x1E = 2.79 kΩ 0x1F = 2.6 kΩ 0x20 = 3.31 kΩ 0x21 = 3.52 kΩ 0x22 = 3.9 kΩ 0x23 = 3.46 kΩ 0x24 = 4 kΩ 0x25 = 3.47 kΩ 0x26 = 3.62 kΩ 0x27 = 3.43 kΩ 0x28 = 4.11 kΩ 0x29 = 4.32 kΩ 0x2A = 4.7 kΩ 0x2B = 4.26 kΩ 0x2C = 4.8 kΩ 0x2D = 4.26 kΩ 0x2E = 4.42 kΩ

Table 1-325. R781 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 4.23 kΩ 0x30 = 4.92 kΩ 0x31 = 5.14 kΩ 0x32 = 5.52 kΩ 0x33 = 5.07 kΩ 0x34 = 5.61 kΩ 0x35 = 5.08 kΩ 0x36 = 5.23 kΩ 0x37 = 5.04 kΩ 0x38 = 5.72 kΩ 0x39 = 5.94 kΩ 0x3A = 6.32 kΩ 0x3B = 5.87 kΩ 0x3C = 6.41 kΩ 0x3D = 5.88 kΩ 0x3E = 6.03 kΩ 0x3F = 5.84 kΩ

1.324 R782 (Offset = 0x30E)

Return to the [Summary Table](#).

Table 1-326. R782 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	PLL2_DISABLE_3RD4TH	R/W	0x3	PLL Loop Filter Disconnects C3 and C4 ROM=Y, EEPROM=N 0x0 = C3/C4 Disconnected 0x1 = C3=Enabled, C4=Disconnected 0x2 = C3=Disconnected, C4=Enabled 0x3 = C3=Enabled, C4=Enabled
5:3	PLL2_LF_C3	R/W	0x7	PLL Loop Filter C3 setting ROM=Y, EEPROM=N 0x0 = 0 pF 0x1 = 10 pF 0x2 = 20 pF 0x3 = 30 pF 0x4 = 40 pF 0x5 = 50 pF 0x6 = 60 pF 0x7 = 70 pF

Table 1-326. R782 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	PLL2_LF_C4	R/W	0x7	PLL Loop Filter C4 setting ROM=Y, EEPROM=N 0x0 = 0 pF 0x1 = 10 pF 0x2 = 20 pF 0x3 = 30 pF 0x4 = 40 pF 0x5 = 50 pF 0x6 = 60 pF 0x7 = 70 pF

1.325 R783 (Offset = 0x30F)

Return to the [Summary Table](#).

Table 1-327. R783 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL2_RDIV_8:8	R/W	0x0	See Register 784

1.326 R784 (Offset = 0x310)

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Table 1-328. R784 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_RDIV	R/W	0x8	PLL R Divider ROM=Y, EEPROM=Y

1.327 R785 (Offset = 0x311)

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Table 1-329. R785 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	PLL2_RDIV_XO_EN	R/W	0x0	APLL reference source is from XO. Must also enable XO to drive this APLL with XO_OUT_BUF_EN[2] = 1 ROM=Y, EEPROM=Y

Table 1-329. R785 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PLL2_RDIV_XO_DBLR_EN	R/W	0x0	Enables XO Doubler ROM=Y, EEPROM=Y
2	PLL2_RDIV_BYPASS_EN	R/W	0x0	Bypass R Divider ROM=Y, EEPROM=Y
1:0	PLL2_RDIV_MUX_SEL	R/W	0x2	Select R Divider input: 0=XO, 1=VCO1 feedback divider, 2=VCO1 feedback divider ROM=Y, EEPROM=Y 0x0 = XO 0x1 = Reserved 0x2 = VCO1 feedback divider

1.328 R786 (Offset = 0x312)

Return to the [Summary Table](#).

Table 1-330. R786 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL2_NDIV_8:8	R/W	0x0	See Register 787

1.329 R787 (Offset = 0x313)

Return to the [Summary Table](#).

Table 1-331. R787 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NDIV	R/W	0x2D	PLL N Divider ROM=Y, EEPROM=Y

1.330 R788 (Offset = 0x314)

Return to the [Summary Table](#).

Table 1-332. R788 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_MSB	R/W	0x63	When PLL2_MODE is set for 24 bit fractional. PLL2_NUM_MSB is effective PLL2_NUM[23:16]. Other PLL2_NUM and PLL2_DEN bits in programmable mode are in PLL2_NUM field. When in 40-bit fixed denominator PLL mode, then PLL2_NUM_MSB is unused. ROM=Y, EEPROM=Y

1.331 R789 (Offset = 0x315)

Return to the [Summary Table](#).

Table 1-333. R789 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_39:32	R/W	0x60	See Register 793

1.332 R790 (Offset = 0x316)

Return to the [Summary Table](#).

Table 1-334. R790 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_31:24	R/W	0x0	See Register 793

1.333 R791 (Offset = 0x317)

Return to the [Summary Table](#).

Table 1-335. R791 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_23:16	R/W	0x80	See Register 793

1.334 R792 (Offset = 0x318)

Return to the [Summary Table](#).

Table 1-336. R792 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_15:8	R/W	0x0	See Register 793

1.335 R793 (Offset = 0x319)

Return to the [Summary Table](#).

Table 1-337. R793 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM	R/W	0x0	When PLL2_MODE = 1 (40-bit fixed denominator) mode then PLL2_NUM contains the APLL2 numerator. When PLL2_MODE = 0 (24-bit programmable denominator) then PLL2_NUM[23:0] stores the programmable PLL2 denominator and PLL2_NUM[39:24] stores the 16 LSBs of the PLL2 numerator. Total PLL2 numerator is calculated with PLL2_NUM_MSB as the 8 MSBs. In 24-bit programmable denominator mode PLL2_NUM[23:0] = 0 is 2^{24} . ROM=Y, EEPROM=Y

1.336 R794 (Offset = 0x31A)

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Table 1-338. R794 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:4	PLL2_DTHRMODE	R/W	0x0	PLL MASH Dither Mode ROM=Y, EEPROM=N 0x0 = Constant Dither MACC2 0x1 = Constant Dither MACC2 and MACC3 0x2 = LFSR Dither MACC2 0x3 = Dither Disabled
3:1	PLL2_ORDER	R/W	0x3	PLL MASH Order ROM=Y, EEPROM=N 0x0 = Integer Mode Divider 0x1 = 1st 0x2 = 2nd 0x3 = 3rd
0	PLL2_MODE	R/W	0x0	In APLL 24-bit num/den mode, APLL denominator is programmable. Not for use with DPLL mode. In 24-bit mode, the denominator is stored in PLL2_NUM[23:0] The numerator is stored in (PLL2_NUM_MSB << 16) + PLL2_NUM[39:24]. In APLL 40-bit mode, APLL denominator is fixed. For use with DPLL. ROM=Y, EEPROM=Y 0x0 = APLL 24-bit num/den 0x1 = APLL 40-bit num (Req for DPLL)

1.337 R795 (Offset = 0x31B)

Return to the [Summary Table](#).

Table 1-339. R795 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL2_NUM_STAT_39:32	R	0x40	See Register 799

1.338 R796 (Offset = 0x31C)

Return to the [Summary Table](#).

Table 1-340. R796 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL2_NUM_STAT_31:24	R	0x0	See Register 799

1.339 R797 (Offset = 0x31D)

Return to the [Summary Table](#).

Table 1-341. R797 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL2_NUM_STAT_23:16	R	0x80	See Register 799

1.340 R798 (Offset = 0x31E)

Return to the [Summary Table](#).

Table 1-342. R798 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL2_NUM_STAT_15:8	R	0x0	See Register 799

1.341 R799 (Offset = 0x31F)

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Table 1-343. R799 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL2_NUM_STAT	R	0x0	Readback current effective APLL2 Numerator after FDEV and/or DPLL correction ROM=N, EEPROM=N

1.342 R803 (Offset = 0x323)

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Table 1-344. R803 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved

Table 1-344. R803 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	PLL2_VCO_BUF_EN	R/W	0x0	Enables the VCO2 Buffer which drives the DPLL feedback, reference window detector, DPLL reference for cascade mode, and test mode ROM=Y, EEPROM=N
3:2	PLL2_VCO_BUF_2REF_EN	R/W	0x0	Enables the APLL2 Div-by-4 cascade divider to [0] -> APLL1 and [1] -> APLL1 reference input for cascade mode. ROM=Y, EEPROM=Y
1	PLL2_VCO_BUF_2DPLL_EN	R/W	0x0	Enables the VCO2 Buffer output driver to DPLL2 feedback divider ROM=Y, EEPROM=N
0	PLL2_VCO_BUF_2WNDDDET_EN	R/W	0x0	Enables the APLL2 Div-by-5 cascade divider to reference window detectors input buffer and prepares pre-divided clock for DPLL2 loop filter and PPM/Frequency detector. ROM=Y, EEPROM=N

1.343 R804 (Offset = 0x324)

Return to the [Summary Table](#).

Table 1-345. R804 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	PLL2_VCO_DIV_SYNC_EN	R/W	0x1	PLL2 Divider Sync Enable. Enables synchronization of post-dividers and reference dividers for PLL2. ROM=Y, EEPROM=N
4	PLL2_VCO_DIV_EN	R/W	0x1	Enables the VCO2 Div By 2 to 13 divide block. ROM=Y, EEPROM=Y
3:0	PLL2_VCO_DIV	R/W	0x9	Sets the VCO2 divider divide value from 2 to 13 ROM=Y, EEPROM=Y 0x0 = 2 (Reserved) 0x1 = 2 (Reserved) 0x2 = 2 0x3 = 3 0x4 = 4 0x5 = 5 0x6 = 6 0x7 = 7 0x8 = 8 0x9 = 9 0xA = 10 0xB = 11 0xC = 12 0xD = 13

1.344 R805 (Offset = 0x325)

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Table 1-346. R805 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:5	PLL2_VCO_BUF_FB_TDC_EN	R/W	0x0	Enables APLL2 Div-by-10 cascade divider to TDC1 for cascade mode [0] = Reserved [1] = TDC1 driver enable ROM=Y, EEPROM=N
4	PLL2_P1_OUT14_15_EN	R/W	0x0	Enable VCO2 P1 divider output driver to channel output bank OUT14_15 ROM=Y, EEPROM=Y
3	PLL2_P1_OUT8_13_EN	R/W	0x0	Enable VCO2 P1 divider output driver to channel output bank OUT8_13 ROM=Y, EEPROM=Y
2	PLL2_P1_OUT4_7_EN	R/W	0x0	Enable VCO2 P1 divider output driver to channel output bank OUT4_7 ROM=Y, EEPROM=Y
1	PLL2_P1_OUT2_3_EN	R/W	0x0	Enable VCO2 P1 divider output driver to channel output bank OUT2_3 ROM=Y, EEPROM=Y
0	PLL2_P1_OUT0_1_EN	R/W	0x0	Enable VCO2 P1 divider output driver to channel output bank OUT0_1 ROM=Y, EEPROM=Y

1.345 R808 (Offset = 0x328)

Return to the [Summary Table](#).

Table 1-347. R808 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	PLL2_RDIV_OUTPUT_EN	R/W	0x0	If GPIOx_SEL selects PLL2 R/2 as an output. Then this bit must be set along with STATUS_MUX_DIV2_EN=1. ROM=N, EEPROM=N
2:0	RESERVED	R	0x0	Reserved

1.346 R813 (Offset = 0x32D)

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Table 1-348. R813 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	PLL2_VM_INSIDE	R	0x1	Denotes if the VCO tuning voltage is within operational range. ROM=N, EEPROM=N

Table 1-348. R813 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	PLL2_VM_HI	R	0x0	Denotes if the charge pump voltage is too high and outside range. If PLL2_VM_INSIDE = 0 and VM_HI = 0, then charge pump voltage is too low. ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.347 R818 (Offset = 0x332)

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Table 1-349. R818 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	PLL2_NDIV_OUTPUT_EN	R/W	0x0	If GPIOx_SEL selects PLL2 N/2 as an output. Then this bit must be set along with STATUS_MUX_DIV2_EN=1. ROM=N, EEPROM=N
4:0	RESERVED	R	0x0	Reserved

1.348 R819 (Offset = 0x333)

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Table 1-350. R819 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL2_VCO_PREBUF_EN	R/W	0x1	Set to same value as APLL2_EN. ROM=Y, EEPROM=Y

1.349 R840 (Offset = 0x348)

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Table 1-351. R840 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_CPBAW_BLEED	R/W	0x22	PLL charge pump pull-up resistor selection ROM=Y, EEPROM=N 0x0 = Disabled 0x1 = 78 kΩ 0x2 = 39 kΩ 0x3 = 26 kΩ 0x4 = 20 kΩ 0x5 = 15.9 kΩ 0x6 = 13.2 kΩ 0x7 = 11.3 kΩ 0x8 = 9.8 kΩ 0x9 = 8.71 kΩ 0xA = 7.83 kΩ 0xB = 7.12 kΩ 0xC = 6.58 kΩ 0xD = 6.07 kΩ 0xE = 5.63 kΩ 0xF = 5.25 kΩ 0x10 = 4.9 kΩ 0x11 = 4.61 kΩ 0x12 = 4.35 kΩ 0x13 = 4.12 kΩ 0x14 = 3.94 kΩ 0x15 = 3.75 kΩ 0x16 = 3.57 kΩ 0x17 = 3.42 kΩ 0x18 = 3.27 kΩ 0x19 = 3.14 kΩ 0x1A = 3.01 kΩ 0x1B = 2.9 kΩ 0x1C = 2.81 kΩ 0x1D = 2.71 kΩ 0x1E = 2.62 kΩ 0x1F = 2.53 kΩ 0x20 = 2.4 kΩ 0x21 = 2.33 kΩ 0x22 = 2.26 kΩ 0x23 = 2.2 kΩ 0x24 = 2.14 kΩ 0x25 = 2.09 kΩ 0x26 = 2.03 kΩ 0x27 = 1.98 kΩ 0x28 = 1.93 kΩ 0x29 = 1.88 kΩ 0x2A = 1.84 kΩ 0x2B = 1.79 kΩ 0x2C = 1.76 kΩ 0x2D = 1.72 kΩ 0x2E = 1.68 kΩ

Table 1-351. R840 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 1.65 kΩ
				0x30 = 1.61 kΩ
				0x31 = 1.58 kΩ
				0x32 = 1.55 kΩ
				0x33 = 1.52 kΩ
				0x34 = 1.49 kΩ
				0x35 = 1.46 kΩ
				0x36 = 1.44 kΩ
				0x37 = 1.41 kΩ
				0x38 = 1.38 kΩ
				0x39 = 1.36 kΩ
				0x3A = 1.34 kΩ
				0x3B = 1.31 kΩ
				0x3C = 1.29 kΩ
				0x3D = 1.27 kΩ
				0x3E = 1.25 kΩ
				0x3F = 1.23 kΩ
				0x40 = 1.2 kΩ
				0x41 = 1.18 kΩ
				0x42 = 1.16 kΩ
				0x43 = 1.15 kΩ
				0x44 = 1.13 kΩ
				0x45 = 1.12 kΩ
				0x46 = 1.1 kΩ
				0x47 = 1.08 kΩ
				0x48 = 1.07 kΩ
				0x49 = 1.05 kΩ
				0x4A = 1.04 kΩ
				0x4B = 1.03 kΩ
				0x4C = 1.01 kΩ
				0x4D = 1 kΩ
				0x4E = 0.989 kΩ
				0x4F = 0.977 kΩ
				0x50 = 0.964 kΩ
				0x51 = 0.952 kΩ
				0x52 = 0.941 kΩ
				0x53 = 0.929 kΩ
				0x54 = 0.92 kΩ
				0x55 = 0.909 kΩ
				0x56 = 0.898 kΩ
				0x57 = 0.888 kΩ
				0x58 = 0.878 kΩ
				0x59 = 0.868 kΩ
				0x5A = 0.858 kΩ
				0x5B = 0.849 kΩ
				0x5C = 0.841 kΩ
				0x5D = 0.832 kΩ
				0x5E = 0.823 kΩ
				0x5F = 0.814 kΩ

Table 1-351. R840 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x60 = 0.8 kΩ
				0x61 = 0.792 kΩ
				0x62 = 0.784 kΩ
				0x63 = 0.776 kΩ
				0x64 = 0.769 kΩ
				0x65 = 0.762 kΩ
				0x66 = 0.754 kΩ
				0x67 = 0.747 kΩ
				0x68 = 0.74 kΩ
				0x69 = 0.733 kΩ
				0x6A = 0.726 kΩ
				0x6B = 0.719 kΩ
				0x6C = 0.713 kΩ
				0x6D = 0.707 kΩ
				0x6E = 0.7 kΩ
				0x6F = 0.694 kΩ
				0x70 = 0.688 kΩ
				0x71 = 0.682 kΩ
				0x72 = 0.676 kΩ
				0x73 = 0.67 kΩ
				0x74 = 0.665 kΩ
				0x75 = 0.659 kΩ
				0x76 = 0.654 kΩ
				0x77 = 0.648 kΩ
				0x78 = 0.643 kΩ
				0x79 = 0.637 kΩ
				0x7A = 0.632 kΩ
				0x7B = 0.627 kΩ
				0x7C = 0.623 kΩ
				0x7D = 0.618 kΩ
				0x7E = 0.613 kΩ
				0x7F = 0.608 kΩ
				0x80 = 0.6 kΩ
				0x81 = 0.595 kΩ
				0x82 = 0.591 kΩ
				0x83 = 0.586 kΩ
				0x84 = 0.583 kΩ
				0x85 = 0.578 kΩ
				0x86 = 0.574 kΩ
				0x87 = 0.57 kΩ
				0x88 = 0.565 kΩ
				0x89 = 0.561 kΩ
				0x8A = 0.557 kΩ
				0x8B = 0.553 kΩ
				0x8C = 0.55 kΩ
				0x8D = 0.546 kΩ
				0x8E = 0.542 kΩ
				0x8F = 0.538 kΩ
				0x90 = 0.535 kΩ

Table 1-351. R840 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x91 = 0.531 kΩ
				0x92 = 0.527 kΩ
				0x93 = 0.524 kΩ
				0x94 = 0.521 kΩ
				0x95 = 0.517 kΩ
				0x96 = 0.514 kΩ
				0x97 = 0.51 kΩ
				0x98 = 0.507 kΩ
				0x99 = 0.504 kΩ
				0x9A = 0.5 kΩ
				0x9B = 0.497 kΩ
				0x9C = 0.494 kΩ
				0x9D = 0.491 kΩ
				0x9E = 0.488 kΩ
				0x9F = 0.485 kΩ
				0xA0 = 0.48 kΩ
				0xA1 = 0.477 kΩ
				0xA2 = 0.474 kΩ
				0xA3 = 0.471 kΩ
				0xA4 = 0.469 kΩ
				0xA5 = 0.466 kΩ
				0xA6 = 0.463 kΩ
				0xA7 = 0.46 kΩ
				0xA8 = 0.458 kΩ
				0xA9 = 0.455 kΩ
				0xAA = 0.452 kΩ
				0xAB = 0.45 kΩ
				0xAC = 0.447 kΩ
				0xAD = 0.445 kΩ
				0xAE = 0.442 kΩ
				0xAF = 0.44 kΩ
				0xB0 = 0.437 kΩ
				0xB1 = 0.435 kΩ
				0xB2 = 0.432 kΩ
				0xB3 = 0.43 kΩ
				0xB4 = 0.428 kΩ
				0xB5 = 0.425 kΩ
				0xB6 = 0.423 kΩ
				0xB7 = 0.421 kΩ
				0xB8 = 0.419 kΩ
				0xB9 = 0.416 kΩ
				0xBA = 0.414 kΩ
				0xBB = 0.412 kΩ
				0xBC = 0.41 kΩ
				0xBD = 0.408 kΩ
				0xBE = 0.406 kΩ
				0xBF = 0.404 kΩ
				0xC0 = 0.4 kΩ
				0xC1 = 0.398 kΩ

Table 1-351. R840 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xC2 = 0.396 kΩ
				0xC3 = 0.394 kΩ
				0xC4 = 0.392 kΩ
				0xC5 = 0.39 kΩ
				0xC6 = 0.388 kΩ
				0xC7 = 0.386 kΩ
				0xC8 = 0.384 kΩ
				0xC9 = 0.382 kΩ
				0xCA = 0.381 kΩ
				0xCB = 0.379 kΩ
				0xCC = 0.377 kΩ
				0xCD = 0.375 kΩ
				0xCE = 0.373 kΩ
				0xCF = 0.372 kΩ
				0xD0 = 0.37 kΩ
				0xD1 = 0.368 kΩ
				0xD2 = 0.366 kΩ
				0xD3 = 0.365 kΩ
				0xD4 = 0.363 kΩ
				0xD5 = 0.361 kΩ
				0xD6 = 0.36 kΩ
				0xD7 = 0.358 kΩ
				0xD8 = 0.356 kΩ
				0xD9 = 0.355 kΩ
				0xDA = 0.353 kΩ
				0xDB = 0.352 kΩ
				0xDC = 0.35 kΩ
				0xDD = 0.349 kΩ
				0xDE = 0.347 kΩ
				0xDF = 0.345 kΩ
				0xE0 = 0.343 kΩ
				0xE1 = 0.341 kΩ
				0xE2 = 0.34 kΩ
				0xE3 = 0.338 kΩ
				0xE4 = 0.337 kΩ
				0xE5 = 0.336 kΩ
				0xE6 = 0.334 kΩ
				0xE7 = 0.333 kΩ
				0xE8 = 0.331 kΩ
				0xE9 = 0.33 kΩ
				0xEA = 0.328 kΩ
				0xEB = 0.327 kΩ
				0xEC = 0.326 kΩ
				0xED = 0.325 kΩ
				0xEE = 0.323 kΩ
				0xEF = 0.322 kΩ
				0xF0 = 0.32 kΩ
				0xF1 = 0.319 kΩ
				0xF2 = 0.318 kΩ

Table 1-351. R840 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xF3 = 0.317 kΩ 0xF4 = 0.315 kΩ 0xF5 = 0.314 kΩ 0xF6 = 0.313 kΩ 0xF7 = 0.312 kΩ 0xF8 = 0.31 kΩ 0xF9 = 0.309 kΩ 0xFA = 0.308 kΩ 0xFB = 0.307 kΩ 0xFC = 0.306 kΩ 0xFD = 0.304 kΩ 0xFE = 0.303 kΩ 0xFF = 0.302 kΩ

1.350 R841 (Offset = 0x349)

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Table 1-352. R841 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	PLL1_CP_PU_DIS	R/W	0x1	PLL charge pump pump-up disable ROM=Y, EEPROM=N
3:0	PLL1_CPG	R/W	0x5	PLL charge pump gain ROM=Y, EEPROM=N 0x0 = 0 mA 0x1 = 0.4 mA 0x2 = 0.8 mA 0x3 = 1.2 mA 0x4 = 1.6 mA 0x5 = 2.0 mA 0x6 = 2.4 mA 0x7 = 2.8 mA 0x8 = 3.0 mA 0x9 = 3.4 mA 0xA = 3.8 mA 0xB = 4.2 mA 0xC = 4.6 mA 0xD = 5.0 mA 0xE = 5.4 mA 0xF = 5.8 mA

1.351 R842 (Offset = 0x34A)

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Table 1-353. R842 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-353. R842 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL1_LF_R2	R/W	0x1	PLL Loop Filter R2 setting ROM=Y, EEPROM=N 0x0 = 0.016 kΩ 0x1 = 0.301 kΩ 0x2 = 0.551 kΩ 0x3 = 0.209 kΩ 0x4 = 1.05 kΩ 0x5 = 0.244 kΩ 0x6 = 0.375 kΩ 0x7 = 0.183 kΩ 0x8 = 2.05 kΩ 0x9 = 0.269 kΩ 0xA = 0.444 kΩ 0xB = 0.194 kΩ 0xC = 0.709 kΩ 0xD = 0.224 kΩ 0xE = 0.0446 kΩ 0xF = 0.0421 kΩ 0x10 = 0.932 kΩ 0x11 = 1.18 kΩ 0x12 = 1.43 kΩ 0x13 = 1.09 kΩ 0x14 = 1.93 kΩ 0x15 = 1.13 kΩ 0x16 = 1.26 kΩ 0x17 = 1.07 kΩ 0x18 = 2.93 kΩ 0x19 = 1.15 kΩ 0x1A = 1.33 kΩ 0x1B = 1.08 kΩ 0x1C = 1.59 kΩ 0x1D = 1.11 kΩ 0x1E = 0.929 kΩ 0x1F = 0.926 kΩ 0x20 = 1.83 kΩ 0x21 = 2.08 kΩ 0x22 = 2.33 kΩ 0x23 = 1.99 kΩ 0x24 = 2.83 kΩ 0x25 = 2.03 kΩ 0x26 = 2.16 kΩ 0x27 = 1.97 kΩ 0x28 = 3.83 kΩ 0x29 = 2.05 kΩ 0x2A = 2.23 kΩ 0x2B = 1.98 kΩ 0x2C = 2.49 kΩ 0x2D = 2.01 kΩ 0x2E = 1.83 kΩ

Table 1-353. R842 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 1.83 kΩ 0x30 = 2.72 kΩ 0x31 = 2.97 kΩ 0x32 = 3.22 kΩ 0x33 = 2.88 kΩ 0x34 = 3.72 kΩ 0x35 = 2.91 kΩ 0x36 = 3.04 kΩ 0x37 = 2.85 kΩ 0x38 = 4.72 kΩ 0x39 = 2.94 kΩ 0x3A = 3.11 kΩ 0x3B = 2.86 kΩ 0x3C = 3.38 kΩ 0x3D = 2.89 kΩ 0x3E = 2.71 kΩ 0x3F = 2.71 kΩ

1.352 R843 (Offset = 0x34B)

Return to the [Summary Table](#).

Table 1-354. R843 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-354. R843 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL1_LF_R3	R/W	0xD	PLL Loop Filter R3 setting ROM=Y, EEPROM=N 0x0 = 0.0139 kΩ 0x1 = 0.51 kΩ 0x2 = 0.826 kΩ 0x3 = 1.23 kΩ 0x4 = 1.85 kΩ 0x5 = 2.26 kΩ 0x6 = 2.57 kΩ 0x7 = 2.97 kΩ 0x8 = 3.3 kΩ 0x9 = 3.75 kΩ 0xA = 4.07 kΩ 0xB = 4.47 kΩ 0xC = 5.09 kΩ 0xD = 5.5 kΩ 0xE = 5.81 kΩ 0xF = 6.22 kΩ 0x10 = 6.57 kΩ 0x11 = 7.01 kΩ 0x12 = 7.33 kΩ 0x13 = 7.73 kΩ 0x14 = 8.36 kΩ 0x15 = 8.76 kΩ 0x16 = 9.08 kΩ 0x17 = 9.48 kΩ 0x18 = 9.81 kΩ 0x19 = 10.3 kΩ 0x1A = 10.6 kΩ 0x1B = 11 kΩ 0x1C = 11.6 kΩ 0x1D = 12 kΩ 0x1E = 12.3 kΩ 0x1F = 12.7 kΩ 0x20 = 13 kΩ 0x21 = 13.5 kΩ 0x22 = 13.8 kΩ 0x23 = 14.2 kΩ 0x24 = 14.8 kΩ 0x25 = 15.2 kΩ 0x26 = 15.6 kΩ 0x27 = 16 kΩ 0x28 = 16.3 kΩ 0x29 = 16.7 kΩ 0x2A = 17.1 kΩ 0x2B = 17.5 kΩ 0x2C = 18.1 kΩ 0x2D = 18.5 kΩ 0x2E = 18.8 kΩ

Table 1-354. R843 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 19.2 kΩ 0x30 = 19.6 kΩ 0x31 = 20 kΩ 0x32 = 20.3 kΩ 0x33 = 20.7 kΩ 0x34 = 21.3 kΩ 0x35 = 21.7 kΩ 0x36 = 22.1 kΩ 0x37 = 22.5 kΩ 0x38 = 22.8 kΩ 0x39 = 23.2 kΩ 0x3A = 23.6 kΩ 0x3B = 24 kΩ 0x3C = 24.6 kΩ 0x3D = 25 kΩ 0x3E = 25.3 kΩ 0x3F = 25.7 kΩ

1.353 R844 (Offset = 0x34C)

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Table 1-355. R844 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-355. R844 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL1_LF_R4	R/W	0xD	PLL Loop Filter R4 setting ROM=Y, EEPROM=N 0x0 = 0.0139 kΩ 0x1 = 0.51 kΩ 0x2 = 0.826 kΩ 0x3 = 1.23 kΩ 0x4 = 1.85 kΩ 0x5 = 2.26 kΩ 0x6 = 2.57 kΩ 0x7 = 2.97 kΩ 0x8 = 3.3 kΩ 0x9 = 3.75 kΩ 0xA = 4.07 kΩ 0xB = 4.47 kΩ 0xC = 5.09 kΩ 0xD = 5.5 kΩ 0xE = 5.81 kΩ 0xF = 6.22 kΩ 0x10 = 6.57 kΩ 0x11 = 7.01 kΩ 0x12 = 7.33 kΩ 0x13 = 7.73 kΩ 0x14 = 8.36 kΩ 0x15 = 8.76 kΩ 0x16 = 9.08 kΩ 0x17 = 9.48 kΩ 0x18 = 9.81 kΩ 0x19 = 10.3 kΩ 0x1A = 10.6 kΩ 0x1B = 11 kΩ 0x1C = 11.6 kΩ 0x1D = 12 kΩ 0x1E = 12.3 kΩ 0x1F = 12.7 kΩ 0x20 = 13 kΩ 0x21 = 13.5 kΩ 0x22 = 13.8 kΩ 0x23 = 14.2 kΩ 0x24 = 14.8 kΩ 0x25 = 15.2 kΩ 0x26 = 15.6 kΩ 0x27 = 16 kΩ 0x28 = 16.3 kΩ 0x29 = 16.7 kΩ 0x2A = 17.1 kΩ 0x2B = 17.5 kΩ 0x2C = 18.1 kΩ 0x2D = 18.5 kΩ 0x2E = 18.8 kΩ

Table 1-355. R844 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 19.2 kΩ 0x30 = 19.6 kΩ 0x31 = 20 kΩ 0x32 = 20.3 kΩ 0x33 = 20.7 kΩ 0x34 = 21.3 kΩ 0x35 = 21.7 kΩ 0x36 = 22.1 kΩ 0x37 = 22.5 kΩ 0x38 = 22.8 kΩ 0x39 = 23.2 kΩ 0x3A = 23.6 kΩ 0x3B = 24 kΩ 0x3C = 24.6 kΩ 0x3D = 25 kΩ 0x3E = 25.3 kΩ 0x3F = 25.7 kΩ

1.354 R845 (Offset = 0x34D)

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Table 1-356. R845 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	PLL1_LF_C3	R/W	0x7	PLL Loop Filter C3 setting ROM=Y, EEPROM=N 0x0 = 0 pF 0x1 = 10 pF 0x2 = 20 pF 0x3 = 30 pF 0x4 = 40 pF 0x5 = 50 pF 0x6 = 60 pF 0x7 = 70 pF

Table 1-356. R845 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	PLL1_LF_C4	R/W	0x7	PLL Loop Filter C4 setting ROM=Y, EEPROM=N 0x0 = 0 pF 0x1 = 10 pF 0x2 = 20 pF 0x3 = 30 pF 0x4 = 40 pF 0x5 = 50 pF 0x6 = 60 pF 0x7 = 70 pF

1.355 R846 (Offset = 0x34E)

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Table 1-357. R846 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL1_RDIV_8:8	R/W	0x0	See Register 847

1.356 R847 (Offset = 0x34F)

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Table 1-358. R847 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_RDIV	R/W	0x0	PLL R Divider ROM=Y, EEPROM=Y

1.357 R848 (Offset = 0x350)

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Table 1-359. R848 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	PLL1_RDIV_XO_EN	R/W	0x1	APLL reference source is from XO. Must also enable XO to drive this APLL with XO_OUT_BUF_EN[3] = 1 ROM=Y, EEPROM=Y

Table 1-359. R848 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PLL1_RDIV_XO_DBLR_EN	R/W	0x1	Enables XO Doubler ROM=Y, EEPROM=Y
2	PLL1_RDIV_BYPASS_EN	R/W	0x1	Bypass R Divider ROM=Y, EEPROM=Y
1:0	PLL1_RDIV_MUX_SEL	R/W	0x0	Select R Divider input: 0=XO, 1=VCO1 feedback divider, 2=VCO2 feedback divider ROM=Y, EEPROM=Y 0x0 = XO 0x1 = Reserved 0x2 = VCO2 feedback divider

1.358 R849 (Offset = 0x351)

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Table 1-360. R849 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL1_NDIV_8:8	R/W	0x0	See Register 850

1.359 R850 (Offset = 0x352)

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Table 1-361. R850 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NDIV	R/W	0x19	PLL N Divider ROM=Y, EEPROM=Y

1.360 R851 (Offset = 0x353)

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Table 1-362. R851 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_MSB	R/W	0x4C	When PLL3_MODE is set for 24 bit fractional. PLL3_NUM_MSB is effective PLL3_NUM[23:16]. Other PLL3_NUM and PLL3_DEN bits in programmable mode are in PLL3_NUM field. When in 40-bit fixed denominator PLL mode, then PLL3_NUM_MSB is unused. ROM=Y, EEPROM=Y

1.361 R852 (Offset = 0x354)

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Table 1-363. R852 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_39:32	R/W	0x99	See Register 856

1.362 R853 (Offset = 0x355)

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Table 1-364. R853 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_31:24	R/W	0x99	See Register 856

1.363 R854 (Offset = 0x356)

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Table 1-365. R854 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_23:16	R/W	0x99	See Register 856

1.364 R855 (Offset = 0x357)

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Table 1-366. R855 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_15:8	R/W	0x99	See Register 856

1.365 R856 (Offset = 0x358)

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Table 1-367. R856 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM	R/W	0x9A	When PLL1_MODE = 1 (40-bit fixed denominator) mode then PLL1_NUM contains the APLL1 numerator. When PLL1_MODE = 0 (24-bit programmable denominator) then PLL1_NUM[23:0] stores the programmable PLL1 denominator and PLL1_NUM[39:24] stores the 16 LSBs of the PLL1 numerator. Total PLL1 numerator is calculated with PLL1_NUM_MSB as the 8 MSBs. In 24-bit programmable denominator mode PLL1_NUM[23:0] = 0 is 2^{24} . ROM=Y, EEPROM=Y

1.366 R857 (Offset = 0x359)

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Table 1-368. R857 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:4	PLL1_DTHRMODE	R/W	0x0	PLL MASH Dither Mode ROM=Y, EEPROM=N 0x0 = Constant Dither MACC2 0x1 = Constant Dither MACC2 and MACC3 0x2 = LFSR Dither MACC2 0x3 = Dither Disabled
3:1	PLL1_ORDER	R/W	0x3	PLL MASH Order ROM=Y, EEPROM=N 0x0 = Integer Mode Divider 0x1 = 1st 0x2 = 2nd 0x3 = 3rd
0	PLL1_MODE	R/W	0x1	In APLL 24-bit num/den mode, APLL denominator is programmable. Recommended not for use with DPLL mode. In 24-bit mode, the denominator is stored in PLL1_NUM_MSB << 16) + PLL1_NUM[39:24]. The numerator is stored in (PLL1_NUM_MSB << 16) + PLL1_NUM[39:24]. In APLL 40-bit mode, APLL denominator is fixed. For use with DPLL. ROM=Y, EEPROM=Y 0x0 = APLL 24-bit num/den 0x1 = APLL 40-bit num (Req for DPLL)

1.367 R858 (Offset = 0x35A)

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Table 1-369. R858 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL1_NUM_STAT_39:32	R	0x9A	See Register 862

1.368 R859 (Offset = 0x35B)

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Table 1-370. R859 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL1_NUM_STAT_31:24	R	0xDD	See Register 862

1.369 R860 (Offset = 0x35C)

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Table 1-371. R860 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL1_NUM_STAT_23:16	R	0x3C	See Register 862

1.370 R861 (Offset = 0x35D)

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Table 1-372. R861 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL1_NUM_STAT_15:8	R	0xC	See Register 862

1.371 R862 (Offset = 0x35E)

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Table 1-373. R862 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL1_NUM_STAT	R	0xA4	Readback current effective APLL1 Numerator after FDEV and/or DPLL correction ROM=N, EEPROM=N

1.372 R864 (Offset = 0x360)

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Table 1-374. R864 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	PLL1_VCO_BUF_OUT_EN	R/W	0xF	Enables VCO1 to: [0] -> VCO1 Post-divider, [1] -> VCO1 Auxiliary Buffer (TDC2 Reference Clock Buffer, APLL2 Reference Clock Buffer, Window Monitor), [2] -> APLL1 N-Divider, [3] -> DPLL1 N-Divider ROM=Y, EEPROM=Y
3	PLL1_VCO_DIV_SYNC_EN	R/W	0x0	PLL1 Divider Sync Enable. Enables synchronization of post-dividers and reference dividers for PLL1. ROM=Y, EEPROM=N
2:0	PLL1_PRI_DIV	R/W	0x4	Sets the VCO1 primary divider divide value from 1 to 8 (div = field value + 1) ROM=Y, EEPROM=Y 0x0 = 1 0x1 = 2 0x2 = 3 0x3 = 4 0x4 = 5 0x5 = 6 0x6 = 7 0x7 = 8

1.373 R865 (Offset = 0x361)

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Table 1-375. R865 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	PLL1_VCO_DIV_SEL	R/W	0x0	Selects APLL1 P1 post-divider block or APLL1 P1 followed by additional divide-by 2 block. ROM=Y, EEPROM=Y 0x0 = PLL1 drive off 0x1 = Reserved 0x2 = Divide-by-1-to-8 direct 0x3 = Divide-by-1-to-8 and /2
5	PLL1_VCO_CHAN_DRV_IN_EN	R/W	0x1	Enables the selected clock (div1to8 or div2) to the VCO3 to Outputs Output Buffer. See PLL1_VCO_DIV1TO8_EN and PLL1_VCO_DIV2_EN. Optimization to prevent unused domain from interacting with active domains. Always on if using PLL1. Might be on to help reduce crosstalk from APLL1. ROM=Y, EEPROM=Y
4	PLL1_P1_OUT14_15_EN	R/W	0x0	Enable VCO1 P1 divider output driver to channel output bank OUT14_15 ROM=Y, EEPROM=Y
3	PLL1_P1_OUT8_13_EN	R/W	0x0	Enable VCO1 P1 divider output driver to channel output bank OUT8_13 ROM=Y, EEPROM=Y
2	PLL1_P1_OUT4_7_EN	R/W	0x0	Enable VCO1 P1 divider output driver to channel output bank OUT4_7 ROM=Y, EEPROM=Y
1	PLL1_P1_OUT2_3_EN	R/W	0x0	Enable VCO1 P1 divider output driver to channel output bank OUT2_3 ROM=Y, EEPROM=Y

Table 1-375. R865 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PLL1_P1_OUT0_1_EN	R/W	0x0	Enable VCO1 P1 divider output driver to channel output bank OUT0_1 ROM=Y, EEPROM=Y

1.374 R866 (Offset = 0x362)

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Table 1-376. R866 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:3	PLL1_VCO_BUF_2REF_EN	R/W	0x2	Enables the APLL1 Div-by-2 cascade divider to [0] -> Reserved and [1] -> APLL2 reference input for cascade mode. ROM=Y, EEPROM=Y
2	PLL1_WIN_DET_DRVR_EN	R/W	0x1	Enables the APLL1 Div-by-2 cascade divider to reference window detectors input buffer, ROM=Y, EEPROM=N
1:0	PLL1_VCO_BUF_FB_TDC_EN	R/W	0x0	Enables APLL1 Div-by-4 cascade divider to TDC2 for cascade mode [0] = Reserved [1] = TDC2 driver enable. ROM=Y, EEPROM=N

1.375 R872 (Offset = 0x368)

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Table 1-377. R872 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:4	RESERVED	R	0x0	Reserved
3	PLL1_RDIV_OUTPUT_EN	R/W	0x0	If GPIOx_SEL selects PLL1 R/2 as an output. Then this bit must be set along with STATUS_MUX_DIV2_EN=1. ROM=N, EEPROM=N
2:0	RESERVED	R	0x0	Reserved

1.376 R882 (Offset = 0x372)

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Table 1-378. R882 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-378. R882 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RESERVED	R	0x0	Reserved
5	PLL1_NDIV_OUTPUT_EN	R/W	0x0	If GPIOx_SEL selects PLL1 N/2 as an output. Then this bit must be set along with STATUS_MUX_DIV2_EN=1. ROM=N, EEPROM=N
4:0	RESERVED	R	0x0	Reserved

1.377 R961 (Offset = 0x3C1)

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Table 1-379. R961 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_0_EN	R/W	0x1	OUT0 Enable. If CMOS on OUT0 is used, this enable must also be set. ROM=Y, EEPROM=Y
5:0	OUT_0_FMT	R/W	0x0	Remix of OUT_0_VOD and OUT_0_VOS to display datasheet specified settings available to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.378 R962 (Offset = 0x3C2)

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Table 1-380. R962 Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_0_CAP_EN	R/W	0x0	If enable, this output capacitor reduces the slew rate of the output clock. ROM=Y, EEPROM=N

Table 1-380. R962 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	OUT_0_STATIC_LOW	R/W	0x0	When OUT0 is forced to a static output, this bit determines if the output voltage will be 0: Static Low 1: Static High ROM=Y, EEPROM=N 0x0 = L 0x1 = H
5	OUT_0_P_CMOS_EN	R/W	0x0	OUT0P CMOS Enable. Overrides the OUT_0_VOD setting and makes OUT_0 CMOS. Setting this bit enables of the positive terminal of OUT0 for CMOS outputs. OUT_0_ENABLE must also be set. ROM=Y, EEPROM=Y
4	OUT_0_N_CMOS_EN	R/W	0x0	OUT0N CMOS Enable. Setting this bit enables of the negative terminal of OUT0 for CMOS outputs. OUT_0_ENABLE must also be set. ROM=Y, EEPROM=Y
3	OUT_0_P_INVERT_POLARITY	R/W	0x0	OUT0P CMOS Invert Polarity. Setting this bit inverts the polarity of the positive terminal of OUT0 for CMOS outputs. ROM=Y, EEPROM=N
2	OUT_0_N_INVERT_POLARITY	R/W	0x0	OUT0N CMOS Invert Polarity. Setting this bit inverts the polarity of the negative terminal of OUT0 for CMOS outputs. ROM=Y, EEPROM=N
1	OUT_0_P_FORCELOW	R/W	0x0	OUT0P CMOS Force Low. Setting this bit forces the positive terminal of OUT0 low. ROM=Y, EEPROM=N
0	OUT_0_N_FORCELOW	R/W	0x0	OUT0N CMOS Force Low. Setting this bit forces the negative terminal of OUT0 low. ROM=Y, EEPROM=N

1.379 R963 (Offset = 0x3C3)

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Table 1-381. R963 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_CONFIGURATION	R/W	0x0	OUT0 configuration. Selects from CH0 Bypass, CH1 Bypass, CHDIV0, CHDIV1, CH0/2 low-noise divide by two path, SYSREF, SYSREF + Analog Delay, or static DC H/L. ROM=Y, EEPROM=Y and N 0x0 = CH0/2 0x14 = CHDIV1 0x20 = SYSREF+ADLY 0x21 = SYSREF 0x22 = Static DC 0x28 = CHDIV0 0x40 = CH1 Bypass 0x80 = CH0 Bypass

1.380 R964 (Offset = 0x3C4)

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Table 1-382. R964 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_1_EN	R/W	0x1	OUT1 Enable. If CMOS on OUT1 is used, this enable must also be set. ROM=Y, EEPROM=Y
5:0	OUT_1_FMT	R/W	0x0	Remix of OUT_1_VOD and OUT_1_VOS to display datasheet specified settings available to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.381 R965 (Offset = 0x3C5)

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Table 1-383. R965 Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_1_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
6	OUT_1_STATIC_LOW	R/W	0x0	When OUT1 is forced to a static output, this bit determines if the output voltage will be 0=Static Low or 1=Static High ROM=Y, EEPROM=N 0x0 = L 0x1 = H
5	OUT_1_P_CMOS_EN	R/W	0x0	OUT1P CMOS Enable. Setting this bit enables the positive terminal of OUT1 for CMOS outputs. ROM=Y, EEPROM=Y
4	OUT_1_N_CMOS_EN	R/W	0x0	OUT1N CMOS Enable. Setting this bit enables the negative terminal of OUT1 for CMOS outputs. ROM=Y, EEPROM=Y

Table 1-383. R965 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	OUT_1_P_INVERT_POLARITY	R/W	0x0	OUT1P CMOS Invert Polarity. Setting this bit inverts the polarity of the positive terminal of OUT1 for CMOS outputs. ROM=Y, EEPROM=N
2	OUT_1_N_INVERT_POLARITY	R/W	0x0	OUT1N CMOS Invert Polarity. Setting this bit inverts the polarity of the negative terminal of OUT1 for CMOS outputs. ROM=Y, EEPROM=N
1	OUT_1_P_FORCELOW	R/W	0x0	OUT1P CMOS Force Low. Setting this bit forces the positive terminal of OUT1 low. ROM=Y, EEPROM=N
0	OUT_1_N_FORCELOW	R/W	0x0	OUT1N CMOS Force Low. Setting this bit forces the negative terminal of OUT1 low. ROM=Y, EEPROM=N

1.382 R966 (Offset = 0x3C6)

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Table 1-384. R966 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_1_CONFIGURATION	R/W	0x0	OUT1 configuration. Selects from CH0 Bypass, CH1 Bypass, CHDIV0, CHDIV1, CH0/2 low-noise divide by two path, SYSREF, SYSREF + Analog Delay, or static DC H/L. ROM=Y, EEPROM=Y and N 0x0 = CH0/2 0x14 = CHDIV1 0x20 = SYSREF+ADLY 0x21 = SYSREF 0x22 = Static DC 0x28 = CHDIV0 0x40 = CH1 Bypass 0x80 = CH0 Bypass

1.383 R967 (Offset = 0x3C7)

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Table 1-385. R967 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1	OUT_0_1_CMOS_OUT_VOLTAGE_SEL	R/W	0x0	CMOS LDO Voltage. Selects CMOS LDO voltage. ROM=Y, EEPROM=Y 0x0 = 1.8 V 0x1 = 2.65 V

Table 1-385. R967 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	OUT_0_1_CMOS_OUT_LDO_EN	R/W	0x0	CMOS LDO Enable. Enables LDO used for CMOS outputs. Must be enabled for CMOS mode. ROM=Y, EEPROM=Y

1.384 R968 (Offset = 0x3C8)

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Table 1-386. R968 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:1	OUT_0_1_ZDM_TDC_SEL	R/W	0x0	Select zero delay output to TDC's ROM=Y, EEPROM=N 0x0 = None 0x1 = TDC1 0x2 = TDC2 0x4 = TDC3
0	OUT_0_1_ZDM_EN	R/W	0x0	Enable the output from CH_DIV0_1 to be used as DPLL feedback input for zero delay mode ROM=Y, EEPROM=N

1.385 R969 (Offset = 0x3C9)

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Table 1-387. R969 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_0_1_DIV_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
5	OUT_0_1_DIV_SYNC_EN	R/W	0x1	OUT0_1 Divider Sync Enable. Enables synchronization of chandiv and div2 dividers for OUT0_1. ROM=Y, EEPROM=N
4	OUT_0_1_SR_DIV_SYNC_EN	R/W	0x1	OUT0_1 SYSREF Divider Sync Enable. Enables synchronization of SYSREF dividers for OUT0_1. ROM=Y, EEPROM=N
3	OUT_0_1_CH0_CHAN_POL_SEL	R/W	0x0	OUT0_1 Ch0 ChanDiv Polarity Select. This bit flips the polarity of the clock into SYSREF and the polarity of the clock into the channel divider.
2	OUT_0_1_CH1_CHAN_POL_SEL	R/W	0x0	OUT0_1 Ch1 ChanDiv Polarity Select. This bit flips the polarity of the clock into SYSREF and the polarity of the clock into the channel divider.

Table 1-387. R969 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	OUT_0_1_CH0_DIV_EN	R/W	0x1	OUT0_1 Ch0 ChanDiv Enable. Enables the Ch0 channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y
0	OUT_0_1_CH1_DIV_EN	R/W	0x1	OUT0_1 Ch1 ChanDiv Enable. Enables the Ch1 channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y

1.386 R971 (Offset = 0x3CB)

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Table 1-388. R971 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_CLK_IN_SEL	R/W	0x0	OUT0_1 grouped clock input control to CH0 and CH1. ROM=Y, EEPROM=Y 0x0 = CH0 DISABLED, CH1 DISABLED 0x40 = CH0 DISABLED, PLL1 to CH1 0x80 = PLL1 to CH0, CH1 DISABLED 0xC0 = PLL1 to CH0, PLL1 to CH1 0x100 = CH0 DISABLED, REFx to CH1 0x101 = CH0 DISABLED, XO to CH1 0x102 = Reserved 0x103 = Reserved 0x104 = CH0 DISABLED, PLL2 to CH1 0x180 = PLL1 to CH0, REFx to CH1 0x181 = PLL1 to CH0, XO to CH1 0x182 = Reserved 0x183 = Reserved 0x184 = PLL1 to CH0, PLL2 to CH1 0x200 = REFx to CH0, CH1 DISABLED 0x208 = XO to CH0, CH1 DISABLED 0x210 = Reserved 0x218 = Reserved 0x220 = PLL2 to CH0, CH1 DISABLED 0x240 = REFx to CH0, PLL1 to CH1 0x248 = XO to CH0, PLL1 to CH1 0x250 = Reserved 0x258 = Reserved 0x260 = PLL2 to CH0, PLL1 to CH1 0x300 = REFx to CH0, REFx to CH1 0x301 = REFx to CH0, XO to CH1 0x302 = Reserved 0x303 = Reserved 0x304 = REFx to CH0, PLL2 to CH1 0x308 = XO to CH0, REFx to CH1 0x309 = XO to CH0, XO to CH1 0x30A = Reserved 0x30B = Reserved 0x30C = XO to CH0, PLL2 to CH1 0x310 = Reserved 0x311 = Reserved 0x312 = Reserved 0x313 = Reserved 0x314 = Reserved 0x318 = Reserved 0x319 = Reserved 0x31A = Reserved 0x31B = Reserved 0x31C = Reserved 0x320 = PLL2 to CH0, REFx to CH1 0x321 = PLL2 to CH0, XO to CH1 0x322 = Reserved

Table 1-388. R971 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x323 = Reserved 0x324 = PLL2 to CH0, PLL2 to CH1

1.387 R972 (Offset = 0x3CC)

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Table 1-389. R972 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1	OUT_0_1_CH0_CH_DIV_SR_MUX_CLK_SEL	R/W	0x0	OUT0_1 Ch0 ChanDiv to SYSREF Input Clock Select. When set, the Ch0 channel divider output is inverted before being fed to the SYSREF. ROM=Y, EEPROM=N 0x0 = POS POL to SR_DIV 0x1 = NEG POL to SR_DIV
0	RESERVED	R	0x0	Reserved

1.388 R973 (Offset = 0x3CD)

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Table 1-390. R973 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	OUT_0_1_CLK_IN_FANOUT	R/W	0x0	OUT0_1 input clock fanout. Distributes the input clock to the channel dividers and the standalone divide-by-2s. ROM=Y, EEPROM=Y 0x0 = DISABLED 0x3 = IN1 to CHDIV1 0x4 = IN0 to SYSREF 0x7 = IN0 to SYSREF, IN1 to CHDIV1 0xC = IN0 to CHDIV0 0xF = IN0 to CHDIV0, IN1 to CHDIV1 0x10 = IN0 to CH0/2 (OUT0) 0x13 = IN0 to CH0/2 (OUT0), IN1 to CHDIV1 (OUT1) 0x14 = IN0 to CH0/2 (OUT0) and SYSREF (OUT1) 0x1C = IN0 to CH0/2 (OUT0) and CHDIV0 (OUT1) 0x20 = IN0 to CH0/2 (OUT1) 0x23 = IN0 to CH0/2 (OUT1), IN1 to CHDIV1 (OUT0) 0x24 = IN0 to CH0/2 (OUT1) and SYSREF (OUT0) 0x2C = IN0 to CH0/2 (OUT1) and CHDIV0 (OUT0) 0x30 = IN0 to CH0/2 (OUT0 and OUT1)

Table 1-390. R973 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	OUT_0_1_CLK_IN_SEL_9:8	R/W	0x0	OUT0_1 grouped clock input control to CH0 and CH1. ROM=Y, EEPROM=Y 0x0 = CH0 DISABLED, CH1 DISABLED 0x40 = Reserved 0x80 = PLL1 to CH0, CH1 DISABLED 0xC0 = PLL1 to CH0, PLL1 to CH1 0x100 = CH0 DISABLED, REFx to CH1 0x101 = CH0 DISABLED, XO to CH1 0x102 = Reserved 0x103 = Reserved 0x104 = CH0 DISABLED, PLL2 to CH1 0x180 = PLL1 to CH0, REFx to CH1 0x181 = PLL1 to CH0, XO to CH1 0x182 = Reserved 0x183 = Reserved 0x184 = PLL1 to CH0, PLL2 to CH1 0x200 = REFx to CH0, CH1 DISABLED 0x208 = XO to CH0, CH1 DISABLED 0x210 = Reserved 0x218 = Reserved 0x220 = PLL2 to CH0, CH1 DISABLED 0x240 = REFx to CH0, PLL1 to CH1 0x248 = XO to CH0, PLL1 to CH1 0x250 = Reserved 0x258 = Reserved 0x260 = PLL2 to CH0, PLL1 to CH1 0x300 = REFx to CH0, REFx to CH1 0x301 = REFx to CH0, XO to CH1 0x302 = Reserved 0x303 = Reserved 0x304 = REFx to CH0, PLL2 to CH1 0x308 = XO to CH0, REFx to CH1 0x309 = XO to CH0, XO to CH1 0x30A = Reserved 0x30B = Reserved 0x30C = XO to CH0, PLL2 to CH1 0x310 = Reserved 0x311 = Reserved 0x312 = Reserved 0x313 = Reserved 0x314 = Reserved 0x318 = Reserved 0x319 = Reserved 0x31A = Reserved 0x31B = Reserved 0x31C = Reserved 0x320 = PLL2 to CH0, REFx to CH1 0x321 = PLL2 to CH0, XO to CH1 0x322 = Reserved

Table 1-390. R973 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x323 = Reserved 0x324 = PLL2 to CH0, PLL2 to CH1

1.389 R974 (Offset = 0x3CE)

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Table 1-391. R974 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_0_1_CH0_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 975

1.390 R975 (Offset = 0x3CF)

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Table 1-392. R975 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_CH0_CH_STATIC_OFFSET	R/W	0x0	CH0_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.391 R976 (Offset = 0x3D0)

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Table 1-393. R976 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_0_1_CH1_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 977

1.392 R977 (Offset = 0x3D1)

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Table 1-394. R977 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_CH1_CH_STATIC_OFFS ET	R/W	0x0	CH1_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.393 R978 (Offset = 0x3D2)

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Table 1-395. R978 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_0_1_CH0_CH_DIV_11:8	R/W	0x0	See Register 979

1.394 R979 (Offset = 0x3D3)

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Table 1-396. R979 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_CH0_CH_DIV	R/W	0x4	OUT0_1 Ch0 Channel Divider (ChanDiv) Divide Value. For this 12-bit divider all bits are set by ROM, but 8 LSBs may be overwritten by EEPROM if EEPROM overlay (ROM_PLUS_EE=1) is enabled. ROM=Y, EEPROM=Y

1.395 R980 (Offset = 0x3D4)

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Table 1-397. R980 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_0_1_CH1_CH_DIV_11:8	R/W	0x0	See Register 981

1.396 R981 (Offset = 0x3D5)

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Table 1-398. R981 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_CH1_CH_DIV	R/W	0x4	OUT0_1 Ch1 Channel Divider (ChanDiv) Divide Value. For this 12-bit divider all bits are set by ROM, but 8 LSBs may be overwritten by EEPROM if EEPROM overlay (ROM_PLUS_EE=1) is enabled. ROM=Y, EEPROM=Y

1.397 R982 (Offset = 0x3D6)

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Table 1-399. R982 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_0_1_SR_ANA_DELAY	R/W	0x0	OUT0_1 SYSREF Analog Delay. Specified here in multiples of one delay step duration. ROM=Y, EEPROM=N

1.398 R983 (Offset = 0x3D7)

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Table 1-400. R983 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_0_1_SR_ANA_DELAY_DIV2_SEL	R/W	0x0	OUT0_1 SYSREF Analog Delay Div By 2 Select. Divides the incoming clock by 2 to double the delay step size. Useful for increasing analog delay range, given high incoming clock frequencies. ROM=Y, EEPROM=N
4	OUT_0_1_SR_ANA_DELAY_EN	R/W	0x0	OUT0_1 SYSREF Analog Delay Enable. ROM=Y, EEPROM=N
3	OUT_0_1_SR_ANA_DELAY_SMALL_STEP_EN	R/W	0x1	OUT0_1 SYSREF Analog Delay Small Step Enable. If set to 1, the analog delay generator will use both rising and falling edges of the incoming clock to halve delay step size. Useful for when large pre-divider values have been used. ROM=Y, EEPROM=N

Table 1-400. R983 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	OUT_0_1_SR_ANA_DELAY_RANGE	R/W	0x5	Analog delay range is set according to the period entering the SYSREF analog delay block. The period can be calculated as $(OUT_x_y_SR_ANA_DELAY_DIV2_SEL + 1) / (OUT_x_y_SR_ANA_DELAY_SMALL_STEP_EN + 1) / VCO$ post divider frequency. Calculated range must fall between 333 ps and 1050 ps. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = 333 ps to 450 ps 0x3 = > 450 ps to 600 ps 0x4 = > 600 ps to 750 ps 0x5 = > 750 ps to 1050 ps 0x6 = Reserved 0x7 = Reserved

1.399 R984 (Offset = 0x3D8)

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Table 1-401. R984 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_0_1_SR_DDLY	R/W	0x0	OUT0_1 SYSREF Digital Delay Value. Measured in VCO half-cycles. ROM=Y, EEPROM=N

1.400 R985 (Offset = 0x3D9)

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Table 1-402. R985 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_0_1_SR_DIV_19:16	R/W	0x0	See Register 987

1.401 R986 (Offset = 0x3DA)

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Table 1-403. R986 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_SR_DIV_15:8	R/W	0x1	See Register 987

1.402 R987 (Offset = 0x3DB)

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Table 1-404. R987 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_SR_DIV	R/W	0x0	OUT0_1 SYSREF Divide Value. ROM=Y, EEPROM=N

1.403 R988 (Offset = 0x3DC)

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Table 1-405. R988 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	OUT_0_1_SR_DIV_STATIC_OFFSE T_14:8	R/W	0x0	See Register 989

1.404 R989 (Offset = 0x3DD)

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Table 1-406. R989 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_SR_DIV_STATIC_OFFSE T	R/W	0x0	OUT_0_1_SR_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization ROM=Y, EEPROM=N

1.405 R990 (Offset = 0x3DE)

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Table 1-407. R990 Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_0_1_SR_REQ_MODE	R/W	0x0	OUT0_1 SYSREF Mute Enable ROM=Y, EEPROM=N
6	OUT_0_1_SR_GPIO_EN	R/W	0x0	Enable SYSREF to digital for SYSREF request resampling, continuous SYSREF, 1-PPS GPIO output, 1-PPS phase validation. Only one OUT_x_y_SR_GPIO_EN should be enabled at a time. ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved

Table 1-407. R990 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:2	OUT_0_1_PULSE_COUNT	R/W	0x0	OUT0_1 SYSREF Pulse Count. The number of SYSREF pulses which will be generated by a SYSREF request. ROM=Y, EEPROM=N
1:0	OUT_0_1_SR_MODE	R/W	0x0	OUT0_1 SYSREF Mode. Selects Pulser mode, Continuous mode, or None. ROM=Y, EEPROM=N 0x0 = None 0x1 = Continuous 0x2 = Pulser

1.406 R991 (Offset = 0x3DF)

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Table 1-408. R991 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_0_1_SR_CH0_DIV_BYPASS	R/W	0x1	OUT0_1 cascaded SYSREF bypass mux. If set, bypasses CHDIV0 for the SYSREF input clock. Using CHDIV bypass is practical when SYSREF is required but CHDIV is not used. VCO post divide frequency must be ≤ 2 GHz to bypass CHDIV. ROM=Y, EEPROM=N 0x0 = CHDIV 0x1 = CHDIV Byp
4:0	RESERVED	R	0x0	Reserved

1.407 R1024 (Offset = 0x400)

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Table 1-409. R1024 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_2_EN	R/W	0x1	OUT2 Enable. ROM=Y, EEPROM=Y

Table 1-409. R1024 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	OUT_2_FMT	R/W	0x0	Remix of OUT_2_VOD and OUT_2_VOS to display datasheet specified settings available to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.408 R1025 (Offset = 0x401)

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Table 1-410. R1025 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	OUT_2_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
2:0	OUT_2_CONFIGURATION	R/W	0x0	OUT2 configuration. ROM=Y, EEPROM=Y and N 0x2 = Static DC 0x3 = CHDIV 0x4 = BYPASS 0x5 = BYPASS

1.409 R1026 (Offset = 0x402)

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Table 1-411. R1026 Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_2_CHAN_POL_SEL	R/W	0x0	OUT2 ChanDiv Polarity Select. This bit flips the polarity of the clock into SYSREF and the polarity of the clock into the channel divider.

Table 1-411. R1026 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:5	OUT_2_CLK_MUX	R/W	0x0	OUT2 Input Clock Select. Selects the input clock which will be used to drive the output. ROM=Y, EEPROM=Y 0x0 = PLL1 0x1 = PLL2 0x2 = Reserved
4	RESERVED	R	0x0	Reserved
3	OUT_2_DIV_EN	R/W	0x1	OUT2 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y
2:0	OUT_2_CH_MUX_SEL	R/W	0x7	OUT2 Clock Enable. Bit 2, if set, passes the selected VCO1 clock (VCO1P or VCO1S), to the second stage of clock selection. Bit 1 and Bit0 enable the selected clock to drive the channel divider and the channel divider retimer respectively. ROM=Y, EEPROM=Y 0x0 = PLL2->BYPASS 0x3 = PLL2->CHDIV 0x4 = Reserved 0x7 = Reserved

1.410 R1027 (Offset = 0x403)

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Table 1-412. R1027 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	OUT_2_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
3	OUT_2_SYNC_EN	R/W	0x1	OUT2 ChanDiv Sync Enable. Enables synchronization of chandiv dividers for OUT2. ROM=Y, EEPROM=N
2:0	RESERVED	R	0x0	Reserved

1.411 R1028 (Offset = 0x404)

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Table 1-413. R1028 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_2_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1029

1.412 R1029 (Offset = 0x405)

Return to the [Summary Table](#).

Table 1-414. R1029 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_2_CH_STATIC_OFFSET	R/W	0x0	OUT_2_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.413 R1030 (Offset = 0x406)

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Table 1-415. R1030 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_2_CH_DIV_11:8	R/W	0x0	See Register 1031

1.414 R1031 (Offset = 0x407)

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Table 1-416. R1031 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_2_CH_DIV	R/W	0x4	OUT2 ChanDiv Divide Value. For this 12-bit divider all bits are set by ROM, but 8 LSBs may be overwritten by EEPROM if EEPROM overlay (ROM_PLUS_EE=1) is enabled. ROM=Y, EEPROM=Y

1.415 R1056 (Offset = 0x420)

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Table 1-417. R1056 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_3_EN	R/W	0x1	OUT3 Enable. ROM=Y, EEPROM=Y

Table 1-417. R1056 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	OUT_3_FMT	R/W	0x0	Remix of OUT_3_VOD and OUT_3_VOS to display datasheet specified settings available to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.416 R1057 (Offset = 0x421)

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Table 1-418. R1057 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	OUT_3_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
2:0	OUT_3_CONFIGURATION	R/W	0x0	OUT3 configuration. ROM=Y, EEPROM=Y and N 0x2 = Static DC 0x3 = CHDIV 0x4 = BYPASS 0x5 = BYPASS

1.417 R1058 (Offset = 0x422)

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Table 1-419. R1058 Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_3_CHAN_POL_SEL	R/W	0x0	OUT3 ChanDiv Polarity Select. This bit flips the polarity of the clock into SYSREF and the polarity of the clock into the channel divider.

Table 1-419. R1058 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:5	OUT_3_CLK_MUX	R/W	0x0	OUT3 Input Clock Select. Selects the input clock which will be used to drive the output. ROM=Y, EEPROM=Y 0x0 = PLL1 0x1 = PLL2 0x2 = Reserved
4	RESERVED	R	0x0	Reserved
3	OUT_3_DIV_EN	R/W	0x1	OUT3 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y
2:0	OUT_3_CH_MUX_SEL	R/W	0x7	OUT3 Clock Enable. Bit 2, if set, passes the selected VCO1 clock (VCO1P or VCO1S), to the second stage of clock selection. Bit 1 and Bit0 enable the selected clock to drive the channel divider and the channel divider retimer respectively. ROM=Y, EEPROM=Y 0x0 = PLL2->BYPASS 0x3 = PLL2->CHDIV 0x4 = Reserved 0x7 = Reserved

1.418 R1059 (Offset = 0x423)

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Table 1-420. R1059 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	OUT_3_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
3	OUT_3_SYNC_EN	R/W	0x1	OUT3 ChanDiv Sync Enable. Enables synchronization of chandiv dividers for OUT3. ROM=Y, EEPROM=N
2:0	RESERVED	R	0x0	Reserved

1.419 R1060 (Offset = 0x424)

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Table 1-421. R1060 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_3_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1061

1.420 R1061 (Offset = 0x425)

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Table 1-422. R1061 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_3_CH_STATIC_OFFSET	R/W	0x0	OUT_3_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.421 R1062 (Offset = 0x426)

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Table 1-423. R1062 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_3_CH_DIV_11:8	R/W	0x0	See Register 1063

1.422 R1063 (Offset = 0x427)

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Table 1-424. R1063 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_3_CH_DIV	R/W	0x2	OUT3 ChanDiv Divide Value. For this 12-bit divider all bits are set by ROM, but 8 LSBs may be overwritten by EEPROM if EEPROM overlay (ROM_PLUS_EE=1) is enabled. ROM=Y, EEPROM=Y

1.423 R1088 (Offset = 0x440)

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Table 1-425. R1088 Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:0	OUT_4_5_SR_ANA_DLY_BIASTRIM	R/W	0x4	Channel Analog Delay Bias Trim ROM=N, EEPROM=Y

1.424 R1089 (Offset = 0x441)

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Table 1-426. R1089 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_4_EN	R/W	0x1	OUT4 Enable. ROM=Y, EEPROM=Y
5:0	OUT_4_FMT	R/W	0x0	Remix of OUT_4_VOD and OUT_4_VOS to display datasheet specified settings available to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.425 R1090 (Offset = 0x442)

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Table 1-427. R1090 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_4_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OUT_4_CONFIGURATION	R/W	0x0	OUT4 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.426 R1091 (Offset = 0x443)

Return to the [Summary Table](#).

Table 1-428. R1091 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_5_EN	R/W	0x1	OUT5 Enable. ROM=Y, EEPROM=Y
5:0	OUT_5_FMT	R/W	0x0	Remix of OUT_5_VOD and OUT_5_VOS to display datasheet specified settings available to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.427 R1092 (Offset = 0x444)

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Table 1-429. R1092 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_5_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OUT_5_CONFIGURATION	R/W	0x0	OUT5 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.428 R1093 (Offset = 0x445)

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Table 1-430. R1093 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_4_5_DIV_SYNC_EN	R/W	0x1	OUT4_5 Divider Sync Enable. Enables synchronization of chandiv dividers for OUT4_5. ROM=Y, EEPROM=N
4	OUT_4_5_SR_DIV_SYNC_EN	R/W	0x1	OUT4_5 SYSREF Divider Sync Enable. Enables synchronization of SYSREF dividers for OUT4_5. ROM=Y, EEPROM=N
3:2	RESERVED	R	0x0	Reserved
1	OUT_4_5_CHAN_POL_SEL	R/W	0x0	OUT4_5 ChanDiv Polarity Select. This bit flips the polarity of the clock into SYSREF and the polarity of the clock into the channel divider.
0	OUT_4_5_DIV_EN	R/W	0x1	OUT4_5 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y

1.429 R1094 (Offset = 0x446)

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Table 1-431. R1094 Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_4_5_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
6	OUT_4_5_ZDM_EN	R/W	0x0	OUT4_5 zero delay output enable ROM=Y, EEPROM=N
5	OUT_4_5_CLK_IN_SEL	R/W	0x0	OUT4_5 Input Clock Select. Selects the input clock which will be used to drive the output: 0 = VCO2, 1 = VCO1 ROM=Y, EEPROM=Y 0x0 = PLL2 0x1 = PLL1
4	OUT_4_5_CH_DIV_SR_MUX_CLK_SEL	R/W	0x0	OUT4_5 ChanDiv to SYSREF Clock Select. When set, the channel divider output is inverted before being fed to the SYSREF. ROM=Y, EEPROM=N

Table 1-431. R1094 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	OUT_4_5_CH_MUX_SEL	R/W	0x3	OUT4_5 Input Clock Enable. Enables the selected clock to various inputs: [0] -> ChanDiv, [1] -> ChanDiv Retimer, [2] -> Div2 to OUT4, [3] -> Div2 to OUT5 ROM=Y, EEPROM=Y 0x0 = OFF 0x1 = SYSREF 0x3 = CHDIV 0x4 = DIV2->OUT4 0x5 = DIV2->OUT4, SYSREF->OUT5 0x7 = DIV2->OUT4, CHDIV->OUT5 0x8 = DIV2->OUT5 0x9 = SYSREF->OUT4, DIV2->OUT5 0xB = CHDIV->OUT4, DIV2->OUT5 0xC = DIV2->OUT4, DIV2->OUT5

1.430 R1095 (Offset = 0x447)

Return to the [Summary Table](#).

Table 1-432. R1095 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_4_5_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1096

1.431 R1096 (Offset = 0x448)

Return to the [Summary Table](#).

Table 1-433. R1096 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_4_5_CH_STATIC_OFFSET	R/W	0x0	OUT_4_5_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.432 R1097 (Offset = 0x449)

Return to the [Summary Table](#).

Table 1-434. R1097 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_4_5_CH_DIV_11:8	R/W	0x0	See Register 1098

1.433 R1098 (Offset = 0x44A)

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Table 1-435. R1098 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_4_5_CH_DIV	R/W	0x2	OUT4_5 ChanDiv Divide Value. For this 12-bit divider all bits are set by ROM, but 8 LSBs may be overwritten by EEPROM if EEPROM overlay (ROM_PLUS_EE=1) is enabled. ROM=Y, EEPROM=Y

1.434 R1099 (Offset = 0x44B)

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Table 1-436. R1099 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_4_5_SR_ANA_DELAY	R/W	0x0	OUT4_5 SYSREF Analog Delay. Specified here in multiples of one delay step duration. ROM=Y, EEPROM=N

1.435 R1100 (Offset = 0x44C)

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Table 1-437. R1100 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_4_5_SR_ANA_DELAY_DIV2_SEL	R/W	0x0	OUT4_5 SYSREF Analog Delay Div By 2 Select. Divides the incoming clock by 2 to double the delay step size. Useful for increasing analog delay range, given high incoming clock frequencies. ROM=Y, EEPROM=N
4	OUT_4_5_SR_ANA_DELAY_EN	R/W	0x0	OUT4_5 SYSREF Analog Delay Enable. Enables the analog delay generator. Set to a 0 to save power if analog delay generator is not needed. ROM=Y, EEPROM=N

Table 1-437. R1100 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	OUT_4_5_SR_ANA_DELAY_SMALL_STEP_EN	R/W	0x1	OUT4_5 SYSREF Analog Delay Small Step Enable. If set to 1, the analog delay generator will use both rising and falling edges of the incoming clock to halve delay step size. Useful for when large pre-divider values have been used. ROM=Y, EEPROM=N
2:0	OUT_4_5_SR_ANA_DELAY_RANGE	R/W	0x5	Analog delay range is set according to the period entering the SYSREF analog delay block. The period can be calculated as $(OUT_x_y_SR_ANA_DELAY_DIV2_SEL + 1) / (OUT_x_y_SR_ANA_DELAY_SMALL_STEP_EN + 1) / VCO$ post divider frequency. Calculated range must fall between 333 ps and 1050 ps. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = 333 ps to 450 ps 0x3 = > 450 ps to 600 ps 0x4 = > 600 ps to 750 ps 0x5 = > 750 ps to 1050 ps 0x6 = Reserved 0x7 = Reserved

1.436 R1101 (Offset = 0x44D)

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Table 1-438. R1101 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_4_5_SR_DDLY	R/W	0x0	OUT4_5 SYSREF Digital Delay Value. Measured in VCO half-cycles. ROM=Y, EEPROM=N

1.437 R1102 (Offset = 0x44E)

Return to the [Summary Table](#).

Table 1-439. R1102 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_4_5_SR_DIV_19:16	R/W	0x0	See Register 1104

1.438 R1103 (Offset = 0x44F)

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Table 1-440. R1103 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_4_5_SR_DIV_15:8	R/W	0x0	See Register 1104

1.439 R1104 (Offset = 0x450)

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Table 1-441. R1104 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_4_5_SR_DIV	R/W	0xB4	OUT4_5 SYSREF Divide Value. ROM=Y, EEPROM=N

1.440 R1105 (Offset = 0x451)

Return to the [Summary Table](#).

Table 1-442. R1105 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	OUT_4_5_SR_DIV_STATIC_OFFSE T_14:8	R/W	0x0	See Register 1106

1.441 R1106 (Offset = 0x452)

Return to the [Summary Table](#).

Table 1-443. R1106 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_4_5_SR_DIV_STATIC_OFFSE T	R/W	0x0	OUT_4_5_SR_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization ROM=Y, EEPROM=N

1.442 R1107 (Offset = 0x453)

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Table 1-444. R1107 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-444. R1107 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	OUT_4_5_SR_REQ_MODE	R/W	0x0	OUT4_5 SYSREF Mute Enable ROM=Y, EEPROM=N
5:3	OUT_4_5_PULSE_COUNT	R/W	0x0	OUT4_5 SYSREF Pulse Count. The number of SYSREF pulses which will be generated by a SYSREF request. ROM=Y, EEPROM=N
2	OUT_4_5_SR_GPIO_EN	R/W	0x0	Enables SYSREF to digital for SYSREF request resampling, continuous SYSREF, or 1-PPS GPIO output. Only one OUT_x_y_SR_GPIO_EN should be enabled at a time. ROM=Y, EEPROM=N
1:0	OUT_4_5_SR_MODE	R/W	0x0	OUT4_5 SYSREF Mode. When these bits are set, the SYSREF operates in Continuous Mode. When cleared, the SYSREF operates in Pulse Mode. ROM=Y, EEPROM=N 0x0 = None 0x1 = Continuous 0x2 = Pulser

1.443 R1108 (Offset = 0x454)

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Table 1-445. R1108 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4	OUT_4_5_SR_CH_DIV_BYPASS	R/W	0x1	OUT4_5 cascaded SYSREF bypass mux. If set, bypasses OUT4_5 channel divider for the SYSREF input clock. Using CHDIV bypass is practical when SYSREF is required but CHDIV is not used. VCO post divide frequency must be ≤ 2 GHz to bypass CHDIV. ROM=Y, EEPROM=N 0x0 = CHDIV 0x1 = CHDIV Byp
3:0	RESERVED	R	0x0	Reserved

1.444 R1121 (Offset = 0x461)

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Table 1-446. R1121 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_6_EN	R/W	0x1	OUT6 Enable. ROM=Y, EEPROM=Y

Table 1-446. R1121 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	OUT_6_FMT	R/W	0x0	Remix of OUT_6_VOD and OUT_6_VOS to display datasheet specified settings available to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.445 R1122 (Offset = 0x462)

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Table 1-447. R1122 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_6_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OUT_6_CONFIGURATION	R/W	0x0	OUT6 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.446 R1123 (Offset = 0x463)

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Table 1-448. R1123 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-448. R1123 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	OUT_7_EN	R/W	0x1	OUT7 Enable. ROM=Y, EEPROM=Y
5:0	OUT_7_FMT	R/W	0x0	Remix of OUT_7_VOD and OUT_7_VOS to display datasheet specified settings available to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.447 R1124 (Offset = 0x464)

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Table 1-449. R1124 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_7_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OUT_7_CONFIGURATION	R/W	0x0	OUT7 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.448 R1125 (Offset = 0x465)

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Table 1-450. R1125 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_6_7_DIV_SYNC_EN	R/W	0x1	OUT6_7 Divider Sync Enable. Enables synchronization of chandiv dividers for OUT6_7. ROM=Y, EEPROM=N
4	OUT_6_7_SR_DIV_SYNC_EN	R/W	0x1	OUT6_7 SYSREF Divider Sync Enable. Enables synchronization of SYSREF dividers for OUT6_7. ROM=Y, EEPROM=N
3:2	RESERVED	R	0x0	Reserved
1	OUT_6_7_CHAN_POL_SEL	R/W	0x0	OUT6_7 ChanDiv Polarity Select. This bit flips the polarity of the clock into SYSREF and the polarity of the clock into the channel divider.
0	OUT_6_7_DIV_EN	R/W	0x1	OUT6_7 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y

1.449 R1126 (Offset = 0x466)

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Table 1-451. R1126 Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_6_7_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
6	RESERVED	R	0x0	Reserved
5	OUT_6_7_CLK_IN_SEL	R/W	0x0	OUT6_7 Input Clock Select. Selects the input clock which will be used to drive the output: 0 = VCO2, 1 = VCO1 ROM=Y, EEPROM=Y 0x0 = PLL2 0x1 = PLL1
4	OUT_6_7_CH_DIV_SR_MUX_CLK_SEL	R/W	0x0	OUT6_7 ChanDiv to SYSREF Clock Select. When set, the channel divider output is inverted before being fed to the SYSREF. ROM=Y, EEPROM=N

Table 1-451. R1126 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	OUT_6_7_CH_MUX_SEL	R/W	0x3	OUT6_7 Input Clock Enable. Enables the selected clock to various inputs: [0] -> ChanDiv, [1] -> ChanDiv Retimer, [2] -> Div2 to OUT6, [3] -> Div2 to OUT7 ROM=Y, EEPROM=Y 0x0 = OFF 0x1 = SYSREF 0x3 = CHDIV 0x4 = DIV2->OUT6 0x5 = DIV2->OUT6, SYSREF->OUT7 0x7 = DIV2->OUT6, CHDIV->OUT7 0x8 = DIV2->OUT7 0x9 = SYSREF->OUT6, DIV2->OUT7 0xB = CHDIV->OUT6, DIV2->OUT7 0xC = DIV2->OUT6, DIV2->OUT7

1.450 R1127 (Offset = 0x467)

Return to the [Summary Table](#).

Table 1-452. R1127 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_6_7_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1128

1.451 R1128 (Offset = 0x468)

Return to the [Summary Table](#).

Table 1-453. R1128 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_6_7_CH_STATIC_OFFSET	R/W	0x0	OUT_6_7_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.452 R1129 (Offset = 0x469)

Return to the [Summary Table](#).

Table 1-454. R1129 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_6_7_CH_DIV_11:8	R/W	0x0	See Register 1130

1.453 R1130 (Offset = 0x46A)

Return to the [Summary Table](#).

Table 1-455. R1130 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_6_7_CH_DIV	R/W	0x2	OUT6_7 ChanDiv Divide Value. For this 12-bit divider all bits are set by ROM, but 8 LSBs may be overwritten by EEPROM if EEPROM overlay (ROM_PLUS_EE=1) is enabled. ROM=Y, EEPROM=Y

1.454 R1131 (Offset = 0x46B)

Return to the [Summary Table](#).

Table 1-456. R1131 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_6_7_SR_ANA_DELAY	R/W	0x0	OUT6_7 SYSREF Analog Delay. Specified here in multiples of one delay step duration. ROM=Y, EEPROM=N

1.455 R1132 (Offset = 0x46C)

Return to the [Summary Table](#).

Table 1-457. R1132 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_6_7_SR_ANA_DELAY_DIV2_SEL	R/W	0x0	OUT6_7 SYSREF Analog Delay Div By 2 Select. Divides the incoming clock by 2 to double the delay step size. Useful for increasing analog delay range, given high incoming clock frequencies. ROM=Y, EEPROM=N
4	OUT_6_7_SR_ANA_DELAY_EN	R/W	0x0	OUT6_7 SYSREF Analog Delay Enable. Enables the analog delay generator. Set to a 0 to save power if analog delay generator is not needed. ROM=Y, EEPROM=N

Table 1-457. R1132 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	OUT_6_7_SR_ANA_DELAY_SMALL_STEP_EN	R/W	0x1	OUT6_7 SYSREF Analog Delay Small Step Enable. If set to 1, the analog delay generator will use both rising and falling edges of the incoming clock to halve delay step size. Useful for when large pre-divider values have been used. ROM=Y, EEPROM=N
2:0	OUT_6_7_SR_ANA_DELAY_RANGE	R/W	0x5	Analog delay range is set according to the period entering the SYSREF analog delay block. The period can be calculated as $(\text{OUT_x_y_SR_ANA_DELAY_DIV2_SEL} + 1) / (\text{OUT_x_y_SR_ANA_DELAY_SMALL_STEP_EN} + 1) / \text{VCO post divider frequency}$. Calculated range must fall between 333 ps and 1050 ps. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = 333 ps to 450 ps 0x3 = > 450 ps to 600 ps 0x4 = > 600 ps to 750 ps 0x5 = > 750 ps to 1050 ps 0x6 = Reserved 0x7 = Reserved

1.456 R1133 (Offset = 0x46D)

Return to the [Summary Table](#).

Table 1-458. R1133 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_6_7_SR_DDLY	R/W	0x0	OUT6_7 SYSREF Digital Delay Value. Measured in VCO half-cycles. ROM=Y, EEPROM=N

1.457 R1134 (Offset = 0x46E)

Return to the [Summary Table](#).

Table 1-459. R1134 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_6_7_SR_DIV_19:16	R/W	0x0	See Register 1136

1.458 R1135 (Offset = 0x46F)

Return to the [Summary Table](#).

Table 1-460. R1135 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_6_7_SR_DIV_15:8	R/W	0x0	See Register 1136

1.459 R1136 (Offset = 0x470)

Return to the [Summary Table](#).

Table 1-461. R1136 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_6_7_SR_DIV	R/W	0x5A	OUT6_7 SYSREF Divide Value. ROM=Y, EEPROM=N

1.460 R1137 (Offset = 0x471)

Return to the [Summary Table](#).

Table 1-462. R1137 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	OUT_6_7_SR_DIV_STATIC_OFFSE T_14:8	R/W	0x0	See Register 1138

1.461 R1138 (Offset = 0x472)

Return to the [Summary Table](#).

Table 1-463. R1138 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_6_7_SR_DIV_STATIC_OFFSE T	R/W	0x0	OUT_6_7_SR_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization ROM=Y, EEPROM=N

1.462 R1139 (Offset = 0x473)

Return to the [Summary Table](#).

Table 1-464. R1139 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-464. R1139 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	OUT_6_7_SR_REQ_MODE	R/W	0x0	OUT6_7 SYSREF Mute Enable ROM=Y, EEPROM=N
5:3	OUT_6_7_PULSE_COUNT	R/W	0x0	OUT6_7 SYSREF Pulse Count. The number of SYSREF pulses which will be generated by a SYSREF request. ROM=Y, EEPROM=N
2	OUT_6_7_SR_GPIO_EN	R/W	0x0	Enables SYSREF to digital for SYSREF request resampling, continuous SYSREF, or 1-PPS GPIO output. Only one OUT_x_y_SR_GPIO_EN should be enabled at a time. ROM=Y, EEPROM=N
1:0	OUT_6_7_SR_MODE	R/W	0x0	OUT6_7 SYSREF Mode. When these bits are set, the SYSREF operates in Continuous Mode. When cleared, the SYSREF operates in PULSE MODE. ROM=Y, EEPROM=N 0x0 = None 0x1 = Continuous 0x2 = Pulser

1.463 R1140 (Offset = 0x474)

Return to the [Summary Table](#).

Table 1-465. R1140 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4	OUT_6_7_SR_CH_DIV_BYPASS	R/W	0x1	OUT6_7 cascaded SYSREF bypass mux. If set, bypasses OUT6_7 channel divider for the SYSREF input clock. Using CHDIV bypass is practical when SYSREF is required but CHDIV is not used. VCO post divide frequency must be ≤ 2 GHz to bypass CHDIV. ROM=Y, EEPROM=N 0x0 = CHDIV 0x1 = CHDIV Byp
3:0	RESERVED	R	0x0	Reserved

1.464 R1153 (Offset = 0x481)

Return to the [Summary Table](#).

Table 1-466. R1153 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_8_EN	R/W	0x1	OUT8 Enable. ROM=Y, EEPROM=Y

Table 1-466. R1153 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	OUT_8_FMT	R/W	0x0	Remix of OUT_8_VOD and OUT_8_VOS to display datasheet specified settings available to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.465 R1154 (Offset = 0x482)

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Table 1-467. R1154 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_8_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OUT_8_CONFIGURATION	R/W	0x0	OUT8 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.466 R1155 (Offset = 0x483)

Return to the [Summary Table](#).

Table 1-468. R1155 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-468. R1155 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	OUT_9_EN	R/W	0x1	OUT9 Enable. ROM=Y, EEPROM=Y
5:0	OUT_9_FMT	R/W	0x0	Remix of OUT_9_VOD and OUT_9_VOS to display datasheet specified settings available to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.467 R1156 (Offset = 0x484)

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Table 1-469. R1156 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_9_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OUT_9_CONFIGURATION	R/W	0x0	OUT9 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.468 R1157 (Offset = 0x485)

Return to the [Summary Table](#).

Table 1-470. R1157 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_8_9_DIV_SYNC_EN	R/W	0x1	OUT8_9 Divider Sync Enable. Enables synchronization of chandiv dividers for OUT8_9. ROM=Y, EEPROM=N
4	OUT_8_9_SR_DIV_SYNC_EN	R/W	0x1	OUT8_9 SYSREF Divider Sync Enable. Enables synchronization of SYSREF dividers for OUT8_9. ROM=Y, EEPROM=N
3:2	RESERVED	R	0x0	Reserved
1	OUT_8_9_CHAN_POL_SEL	R/W	0x0	OUT8_9 ChanDiv Polarity Select. This bit flips the polarity of the clock into SYSREF and the polarity of the clock into the channel divider.
0	OUT_8_9_DIV_EN	R/W	0x0	OUT8_9 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y

1.469 R1158 (Offset = 0x486)

Return to the [Summary Table](#).

Table 1-471. R1158 Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_8_9_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
6	RESERVED	R	0x0	Reserved
5	OUT_8_9_CLK_IN_SEL	R/W	0x1	OUT8_9 Input Clock Select. Selects the input clock which will be used to drive the output: 0 = VCO2, 1 = VCO1 ROM=Y, EEPROM=Y 0x0 = PLL2 0x1 = PLL1
4	OUT_8_9_CH_DIV_SR_MUX_CLK_SEL	R/W	0x0	OUT8_9 ChanDiv to SYSREF Clock Select. When set, the channel divider output is inverted before being fed to the SYSREF. ROM=Y, EEPROM=N

Table 1-471. R1158 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	OUT_8_9_CH_MUX_SEL	R/W	0x1	OUT8_9 Input Clock Enable. Enables the selected clock to various inputs: [0] -> ChanDiv, [1] -> ChanDiv Retimer, [2] -> Div2 to OUT8, [3] -> Div2 to OUT9 ROM=Y, EEPROM=Y 0x0 = OFF 0x1 = SYSREF 0x3 = CHDIV 0x4 = DIV2->OUT8 0x5 = DIV2->OUT8, SYSREF->OUT9 0x7 = DIV2->OUT8, CHDIV->OUT9 0x8 = DIV2->OUT9 0x9 = SYSREF->OUT8, DIV2->OUT9 0xB = CHDIV->OUT8, DIV2->OUT9 0xC = DIV2->OUT8, DIV2->OUT9

1.470 R1159 (Offset = 0x487)

Return to the [Summary Table](#).

Table 1-472. R1159 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_8_9_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1160

1.471 R1160 (Offset = 0x488)

Return to the [Summary Table](#).

Table 1-473. R1160 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_8_9_CH_STATIC_OFFSET	R/W	0x0	OUT_8_9_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.472 R1161 (Offset = 0x489)

Return to the [Summary Table](#).

Table 1-474. R1161 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_8_9_CH_DIV_11:8	R/W	0x0	See Register 1162

1.473 R1162 (Offset = 0x48A)

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Table 1-475. R1162 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_8_9_CH_DIV	R/W	0x4	OUT8_9 ChanDiv Divide Value. For this 12-bit divider all bits are set by ROM, but 8 LSBs may be overwritten by EEPROM if EEPROM overlay (ROM_PLUS_EE=1) is enabled. ROM=Y, EEPROM=Y

1.474 R1163 (Offset = 0x48B)

Return to the [Summary Table](#).

Table 1-476. R1163 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_8_9_SR_ANA_DELAY	R/W	0x0	OUT8_9 SYSREF Analog Delay. Specified here in multiples of one delay step duration. ROM=Y, EEPROM=N

1.475 R1164 (Offset = 0x48C)

Return to the [Summary Table](#).

Table 1-477. R1164 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_8_9_SR_ANA_DELAY_DIV2_SEL	R/W	0x0	OUT8_9 SYSREF Analog Delay Div By 2 Select. Divides the incoming clock by 2 to double the delay step size. Useful for increasing analog delay range, given high incoming clock frequencies. ROM=Y, EEPROM=N
4	OUT_8_9_SR_ANA_DELAY_EN	R/W	0x1	OUT8_9 SYSREF Analog Delay Enable. Enables the analog delay generator. Set to a 0 to save power if analog delay generator is not needed. ROM=Y, EEPROM=N

Table 1-477. R1164 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	OUT_8_9_SR_ANA_DELAY_SMALL_STEP_EN	R/W	0x1	OUT8_9 SYSREF Analog Delay Small Step Enable. If set to 1, the analog delay generator will use both rising and falling edges of the incoming clock to halve delay step size. Useful for when large pre-divider values have been used. ROM=Y, EEPROM=N
2:0	OUT_8_9_SR_ANA_DELAY_RANGE	R/W	0x5	Analog delay range is set according to the period entering the SYSREF analog delay block. The period can be calculated as $(OUT_x_y_SR_ANA_DELAY_DIV2_SEL + 1) / (OUT_x_y_SR_ANA_DELAY_SMALL_STEP_EN + 1) / VCO$ post divider frequency. Calculated range must fall between 333 ps and 1050 ps. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = 333 ps to 450 ps 0x3 = > 450 ps to 600 ps 0x4 = > 600 ps to 750 ps 0x5 = > 750 ps to 1050 ps 0x6 = Reserved 0x7 = Reserved

1.476 R1165 (Offset = 0x48D)

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Table 1-478. R1165 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_8_9_SR_DDLY	R/W	0x0	OUT8_9 SYSREF Digital Delay Value. Measured in VCO half-cycles. ROM=Y, EEPROM=N

1.477 R1166 (Offset = 0x48E)

Return to the [Summary Table](#).

Table 1-479. R1166 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_8_9_SR_DIV_19:16	R/W	0x0	See Register 1168

1.478 R1167 (Offset = 0x48F)

Return to the [Summary Table](#).

Table 1-480. R1167 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_8_9_SR_DIV_15:8	R/W	0x1	See Register 1168

1.479 R1168 (Offset = 0x490)

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Table 1-481. R1168 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_8_9_SR_DIV	R/W	0x0	OUT8_9 SYSREF Divide Value. ROM=Y, EEPROM=N

1.480 R1169 (Offset = 0x491)

Return to the [Summary Table](#).

Table 1-482. R1169 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	OUT_8_9_SR_DIV_STATIC_OFFSE T_14:8	R/W	0x0	See Register 1170

1.481 R1170 (Offset = 0x492)

Return to the [Summary Table](#).

Table 1-483. R1170 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_8_9_SR_DIV_STATIC_OFFSE T	R/W	0x0	OUT_8_9_SR_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization ROM=Y, EEPROM=N

1.482 R1171 (Offset = 0x493)

Return to the [Summary Table](#).

Table 1-484. R1171 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-484. R1171 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	OUT_8_9_SR_REQ_MODE	R/W	0x0	OUT8_9 SYSREF Mute Enable ROM=Y, EEPROM=N
5:3	OUT_8_9_PULSE_COUNT	R/W	0x0	OUT8_9 SYSREF Pulse Count. The number of SYSREF pulses which will be generated by a SYSREF request. ROM=Y, EEPROM=N
2	OUT_8_9_SR_GPIO_EN	R/W	0x1	Enables SYSREF to digital for SYSREF request resampling, continuous SYSREF, or 1-PPS GPIO output. Only one OUT_x_y_SR_GPIO_EN should be enabled at a time. ROM=Y, EEPROM=N
1:0	OUT_8_9_SR_MODE	R/W	0x0	OUT8_9 SYSREF Mode. When these bits are set, the SYSREF operates in Continuous Mode. When cleared, the SYSREF operates in PULSE MODE. ROM=Y, EEPROM=N 0x0 = None 0x1 = Continuous 0x2 = Pulser

1.483 R1185 (Offset = 0x4A1)

Return to the [Summary Table](#).

Table 1-485. R1185 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_10_EN	R/W	0x1	OUT10 Enable. ROM=Y, EEPROM=Y
5:0	OUT_10_FMT	R/W	0x0	Remix of OUT_10_VOD and OUT_10_VOS to display datasheet specified settings available to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.484 R1186 (Offset = 0x4A2)

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Table 1-486. R1186 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_10_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OUT_10_CONFIGURATION	R/W	0x0	OUT10 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.485 R1187 (Offset = 0x4A3)

Return to the [Summary Table](#).

Table 1-487. R1187 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_11_EN	R/W	0x1	OUT11 Enable. ROM=Y, EEPROM=Y
5:0	OUT_11_FMT	R/W	0x0	Remix of OUT_11_VOD and OUT_11_VOS to display datasheet specified settings available to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.486 R1188 (Offset = 0x4A4)

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Table 1-488. R1188 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_11_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OUT_11_CONFIGURATION	R/W	0x0	OUT11 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.487 R1189 (Offset = 0x4A5)

Return to the [Summary Table](#).

Table 1-489. R1189 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_10_11_DIV_SYNC_EN	R/W	0x1	OUT10_11 Divider Sync Enable. Enables synchronization of chandiv dividers for OUT10_11. ROM=Y, EEPROM=N
4	OUT_10_11_SR_DIV_SYNC_EN	R/W	0x1	OUT10_11 SYSREF Divider Sync Enable. Enables synchronization of SYSREF dividers for OUT10_11. ROM=Y, EEPROM=N
3:2	RESERVED	R	0x0	Reserved
1	OUT_10_11_CHAN_POL_SEL	R/W	0x0	OUT10_11 ChanDiv Polarity Select. This bit flips the polarity of the clock into SYSREF and the polarity of the clock into the channel divider.
0	OUT_10_11_DIV_EN	R/W	0x0	OUT10_11 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y

1.488 R1190 (Offset = 0x4A6)

Return to the [Summary Table](#).

Table 1-490. R1190 Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_10_11_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
6	OUT_10_11_ZDM_EN	R/W	0x0	OUT10_11 zero delay output enable. ROM=Y, EEPROM=N
5	OUT_10_11_CLK_IN_SEL	R/W	0x1	OUT10_11 Input Clock Select. Selects the input clock which will be used to drive the output: 0 = VCO2, 1 = VCO1 ROM=Y, EEPROM=Y 0x0 = PLL2 0x1 = PLL1
4	OUT_10_11_CH_DIV_SR_MUX_CLK_SEL	R/W	0x0	OUT10_11 ChanDiv to SYSREF Clock Select. When set, the channel divider output is inverted before being fed to the SYSREF. ROM=Y, EEPROM=N
3:0	OUT_10_11_CH_MUX_SEL	R/W	0x1	OUT10_11 Input Clock Enable. Enables the selected clock to various inputs: [0] -> ChanDiv, [1] -> ChanDiv Retimer, [2] -> Div2 to OUT10, [3] -> Div2 to OUT11 ROM=Y, EEPROM=Y 0x0 = OFF 0x1 = SYSREF 0x3 = CHDIV 0x4 = DIV2->OUT10 0x5 = DIV2->OUT10, SYSREF->OUT11 0x7 = DIV2->OUT10, CHDIV->OUT11 0x8 = DIV2->OUT11 0x9 = SYSREF->OUT10, DIV2->OUT11 0xB = CHDIV->OUT10, DIV2->OUT11 0xC = DIV2->OUT10, DIV2->OUT11

1.489 R1191 (Offset = 0x4A7)

Return to the [Summary Table](#).

Table 1-491. R1191 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_10_11_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1192

1.490 R1192 (Offset = 0x4A8)

Return to the [Summary Table](#).

Table 1-492. R1192 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_10_11_CH_STATIC_OFFSET	R/W	0x0	OUT_10_11_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.491 R1193 (Offset = 0x4A9)

Return to the [Summary Table](#).

Table 1-493. R1193 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_10_11_CH_DIV_11:8	R/W	0x0	See Register 1194

1.492 R1194 (Offset = 0x4AA)

Return to the [Summary Table](#).

Table 1-494. R1194 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_10_11_CH_DIV	R/W	0x4	OUT10_11 ChanDiv Divide Value. For this 12-bit divider all bits are set by ROM, but 8 LSBs may be overwritten by EEPROM if EEPROM overlay (ROM_PLUS_EE=1) is enabled. ROM=Y, EEPROM=Y

1.493 R1195 (Offset = 0x4AB)

Return to the [Summary Table](#).

Table 1-495. R1195 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_10_11_SR_ANA_DELAY	R/W	0x0	OUT10_11 SYSREF Analog Delay. Specified here in multiples of one delay step duration. ROM=Y, EEPROM=N

1.494 R1196 (Offset = 0x4AC)

Return to the [Summary Table](#).

Table 1-496. R1196 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_10_11_SR_ANA_DELAY_DIV2_SEL	R/W	0x0	OUT10_11 SYSREF Analog Delay Div By 2 Select. Divides the incoming clock by 2 to double the delay step size. Useful for increasing analog delay range, given high incoming clock frequencies. ROM=Y, EEPROM=N
4	OUT_10_11_SR_ANA_DELAY_EN	R/W	0x1	OUT10_11 SYSREF Analog Delay Enable. Enables the analog delay generator. Set to a 0 to save power if analog delay generator is not needed. ROM=Y, EEPROM=N
3	OUT_10_11_SR_ANA_DELAY_SMALL_STEP_EN	R/W	0x1	OUT10_11 SYSREF Analog Delay Small Step Enable. If set to 1, the analog delay generator will use both rising and falling edges of the incoming clock to halve delay step size. Useful for when large pre-divider values have been used. ROM=Y, EEPROM=N
2:0	OUT_10_11_SR_ANA_DELAY_RANGE	R/W	0x5	Analog delay range is set according to the period entering the SYSREF analog delay block. The period can be calculated as $(OUT_x_y_SR_ANA_DELAY_DIV2_SEL + 1) / (OUT_x_y_SR_ANA_DELAY_SMALL_STEP_EN + 1) / VCO$ post divider frequency. Calculated range must fall between 333 ps and 1050 ps. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = 333 ps to 450 ps 0x3 = > 450 ps to 600 ps 0x4 = > 600 ps to 750 ps 0x5 = > 750 ps to 1050 ps 0x6 = Reserved 0x7 = Reserved

1.495 R1197 (Offset = 0x4AD)

Return to the [Summary Table](#).

Table 1-497. R1197 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_10_11_SR_DDLY	R/W	0x0	OUT10_11 SYSREF Digital Delay Value. Measured in VCO half-cycles. ROM=Y, EEPROM=N

1.496 R1198 (Offset = 0x4AE)

Return to the [Summary Table](#).

Table 1-498. R1198 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_10_11_SR_DIV_19:16	R/W	0x0	See Register 1200

1.497 R1199 (Offset = 0x4AF)

Return to the [Summary Table](#).

Table 1-499. R1199 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_10_11_SR_DIV_15:8	R/W	0x1	See Register 1200

1.498 R1200 (Offset = 0x4B0)

Return to the [Summary Table](#).

Table 1-500. R1200 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_10_11_SR_DIV	R/W	0x0	OUT10_11 SYSREF Divide Value. ROM=Y, EEPROM=N

1.499 R1201 (Offset = 0x4B1)

Return to the [Summary Table](#).

Table 1-501. R1201 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	OUT_10_11_SR_DIV_STATIC_OFF SET_14:8	R/W	0x0	See Register 1202

1.500 R1202 (Offset = 0x4B2)

Return to the [Summary Table](#).

Table 1-502. R1202 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_10_11_SR_DIV_STATIC_OFF SET	R/W	0x0	OUT_10_11_SR_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization ROM=Y, EEPROM=N

1.501 R1203 (Offset = 0x4B3)

Return to the [Summary Table](#).

Table 1-503. R1203 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_10_11_SR_REQ_MODE	R/W	0x0	OUT10_11 SYSREF Mute Enable ROM=Y, EEPROM=N
5:3	OUT_10_11_PULSE_COUNT	R/W	0x0	OUT10_11 SYSREF Pulse Count. The number of SYSREF pulses which will be generated by a SYSREF request. ROM=Y, EEPROM=N
2	OUT_10_11_SR_GPIO_EN	R/W	0x0	Enables SYSREF to digital for SYSREF request resampling, continuous SYSREF, or 1-PPS GPIO output. Only one OUT_x_y_SR_GPIO_EN should be enabled at a time. ROM=Y, EEPROM=N
1:0	OUT_10_11_SR_MODE	R/W	0x0	OUT10_11 SYSREF Mode. When these bits are set, the SYSREF operates in Continuous Mode. When cleared, the SYSREF operates in PULSE MODE. ROM=Y, EEPROM=N 0x0 = None 0x1 = Continuous 0x2 = Pulser

1.502 R1204 (Offset = 0x4B4)

Return to the [Summary Table](#).

Table 1-504. R1204 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4	OUT_10_11_SR_CH_DIV_BYPASS	R/W	0x1	OUT10_11 cascaded SYSREF bypass mux. If set, bypasses OUT10_11 channel divider for the SYSREF input clock. Using CHDIV bypass is practical when SYSREF is required but CHDIV is not used. VCO post divide frequency must be ≤ 2 GHz to bypass CHDIV. ROM=Y, EEPROM=N 0x0 = CHDIV 0x1 = CHDIV Byp

Table 1-504. R1204 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	RESERVED	R	0x0	Reserved

1.503 R1217 (Offset = 0x4C1)

Return to the [Summary Table](#).

Table 1-505. R1217 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OPTIMIZE_R1217_b6	R/W	0x0	Set this field to 0 for optimal power and noise performance. ROM=Y, EEPROM=Y
5:0	OUT_12_FMT	R/W	0x0	Remix of OUT_12_VOD and OUT_12_VOS to display datasheet specified settings available to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.504 R1218 (Offset = 0x4C2)

Return to the [Summary Table](#).

Table 1-506. R1218 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_12_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved

Table 1-506. R1218 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	OPTIMIZE_R1218_b4to0	R/W	0x0	Set this field to 0 for optimal power and noise performance. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.505 R1219 (Offset = 0x4C3)

Return to the [Summary Table](#).

Table 1-507. R1219 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OPTIMIZE_R1219_b6	R/W	0x0	Set this field to 0 for optimal power and noise performance. ROM=Y, EEPROM=Y
5:0	OUT_13_FMT	R/W	0x0	Remix of OUT_13_VOD and OUT_13_VOS to display datasheet specified settings available to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.506 R1220 (Offset = 0x4C4)

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Table 1-508. R1220 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-508. R1220 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	OUT_13_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OPTIMIZE_R1220_b4to0	R/W	0x0	Set this field to 0 for optimal power and noise performance. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.507 R1221 (Offset = 0x4C5)

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Table 1-509. R1221 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_12_13_DIV_SYNC_EN	R/W	0x1	OUT12_13 Divider Sync Enable. Enables synchronization of chandiv dividers for OUT12_13. ROM=Y, EEPROM=N
4	OUT_12_13_SR_DIV_SYNC_EN	R/W	0x1	OUT12_13 SYSREF Divider Sync Enable. Enables synchronization of SYSREF dividers for OUT12_13. ROM=Y, EEPROM=N
3:2	RESERVED	R	0x0	Reserved
1	OUT_12_13_CHAN_POL_SEL	R/W	0x0	OUT12_13 ChanDiv Polarity Select. This bit flips the polarity of the clock into SYSREF and the polarity of the clock into the channel divider.
0	OUT_12_13_DIV_EN	R/W	0x0	OUT12_13 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y

1.508 R1222 (Offset = 0x4C6)

Return to the [Summary Table](#).

Table 1-510. R1222 Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_12_13_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
6	RESERVED	R	0x0	Reserved

Table 1-510. R1222 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	OPTIMIZE_R1222_b5	R/W	0x1	Set this field to 0 for optimal power and noise performance. ROM=Y, EEPROM=Y 0x0 = R1222[5] = 0 0x1 = R1222[5] = 1
4	OUT_12_13_CH_DIV_SR_MUX_CLK_SEL	R/W	0x0	OUT12_13 ChanDiv to SYSREF Clock Select. When set, the channel divider output is inverted before being fed to the SYSREF. ROM=Y, EEPROM=N
3:0	OUT_12_13_CH_MUX_SEL	R/W	0x1	OUT12_13 Input Clock Enable. Enables the selected clock to various inputs: [0] -> ChanDiv, [1] -> ChanDiv Retimer, [2] -> Div2 to OUT12, [3] -> Div2 to OUT13 ROM=Y, EEPROM=Y 0x0 = OFF 0x1 = SYSREF 0x3 = CHDIV 0x4 = DIV2->OUT12 0x5 = DIV2->OUT12, SYSREF->OUT13 0x7 = DIV2->OUT12, CHDIV->OUT13 0x8 = DIV2->OUT13 0x9 = SYSREF->OUT12, DIV2->OUT13 0xB = CHDIV->OUT12, DIV2->OUT13 0xC = DIV2->OUT12, DIV2->OUT13

1.509 R1223 (Offset = 0x4C7)

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Table 1-511. R1223 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_12_13_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1224

1.510 R1224 (Offset = 0x4C8)

Return to the [Summary Table](#).

Table 1-512. R1224 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_12_13_CH_STATIC_OFFSET	R/W	0x0	OUT_12_13_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.511 R1225 (Offset = 0x4C9)

Return to the [Summary Table](#).

Table 1-513. R1225 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_12_13_CH_DIV_11:8	R/W	0x0	See Register 1226

1.512 R1226 (Offset = 0x4CA)

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Table 1-514. R1226 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_12_13_CH_DIV	R/W	0x4	OUT12_13 ChanDiv Divide Value. For this 12-bit divider all bits are set by ROM, but 8 LSBs may be overwritten by EEPROM if EEPROM overlay (ROM_PLUS_EE=1) is enabled. ROM=Y, EEPROM=Y

1.513 R1227 (Offset = 0x4CB)

Return to the [Summary Table](#).

Table 1-515. R1227 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_12_13_SR_ANA_DELAY	R/W	0x0	OUT12_13 SYSREF Analog Delay. Specified here in multiples of one delay step duration. ROM=Y, EEPROM=N

1.514 R1228 (Offset = 0x4CC)

Return to the [Summary Table](#).

Table 1-516. R1228 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_12_13_SR_ANA_DELAY_DIV_2_SEL	R/W	0x0	OUT12_13 SYSREF Analog Delay Div By 2 Select. Divides the incoming clock by 2 to double the delay step size. Useful for increasing analog delay range, given high incoming clock frequencies. ROM=Y, EEPROM=N

Table 1-516. R1228 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	OUT_12_13_SR_ANA_DELAY_EN	R/W	0x0	OUT12_13 SYSREF Analog Delay Enable. Enables the analog delay generator. Set to a 0 to save power if analog delay generator is not needed. ROM=Y, EEPROM=N
3	OUT_12_13_SR_ANA_DELAY_SM ALL_STEP_EN	R/W	0x1	OUT12_13 SYSREF Analog Delay Small Step Enable. If set to 1, the analog delay generator will use both rising and falling edges of the incoming clock to halve delay step size. Useful for when large pre-divider values have been used. ROM=Y, EEPROM=N
2:0	OUT_12_13_SR_ANA_DELAY_RA NGE	R/W	0x5	Analog delay range is set according to the period entering the SYSREF analog delay block. The period can be calculated as $(\text{OUT_x_y_SR_ANA_DELAY_DIV2_SEL} + 1) / (\text{OUT_x_y_SR_ANA_DELAY_SMALL_STEP_EN} + 1) / \text{VCO post divider frequency}$. Calculated range must fall between 333 ps and 1050 ps. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = 333 ps to 450 ps 0x3 = > 450 ps to 600 ps 0x4 = > 600 ps to 750 ps 0x5 = > 750 ps to 1050 ps 0x6 = Reserved 0x7 = Reserved

1.515 R1229 (Offset = 0x4CD)

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Table 1-517. R1229 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_12_13_SR_DDLY	R/W	0x0	OUT12_13 SYSREF Digital Delay Value. Measured in VCO half-cycles. ROM=Y, EEPROM=N

1.516 R1230 (Offset = 0x4CE)

Return to the [Summary Table](#).

Table 1-518. R1230 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_12_13_SR_DIV_19:16	R/W	0x0	See Register 1232

1.517 R1231 (Offset = 0x4CF)

Return to the [Summary Table](#).

Table 1-519. R1231 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_12_13_SR_DIV_15:8	R/W	0x1	See Register 1232

1.518 R1232 (Offset = 0x4D0)

Return to the [Summary Table](#).

Table 1-520. R1232 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_12_13_SR_DIV	R/W	0x0	OUT12_13 SYSREF Divide Value. ROM=Y, EEPROM=N

1.519 R1233 (Offset = 0x4D1)

Return to the [Summary Table](#).

Table 1-521. R1233 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	OUT_12_13_SR_DIV_STATIC_OFF SET_14:8	R/W	0x0	See Register 1234

1.520 R1234 (Offset = 0x4D2)

Return to the [Summary Table](#).

Table 1-522. R1234 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_12_13_SR_DIV_STATIC_OFF SET	R/W	0x0	OUT_12_13_SR_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization ROM=Y, EEPROM=N

1.521 R1235 (Offset = 0x4D3)

Return to the [Summary Table](#).

Table 1-523. R1235 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_12_13_SR_REQ_MODE	R/W	0x0	OUT12_13 SYSREF Mute Enable ROM=Y, EEPROM=N
5:3	OUT_12_13_PULSE_COUNT	R/W	0x0	OUT12_13 SYSREF Pulse Count. The number of SYSREF pulses which will be generated by a SYSREF request. ROM=Y, EEPROM=N
2	OUT_12_13_SR_GPIO_EN	R/W	0x0	Enables SYSREF to digital for SYSREF request resampling, continuous SYSREF, or 1-PPS GPIO output. Only one OUT_x_y_SR_GPIO_EN should be enabled at a time. ROM=Y, EEPROM=N
1:0	OUT_12_13_SR_MODE	R/W	0x0	OUT12_13 SYSREF Mode. When these bits are set, the SYSREF operates in Continuous Mode. When cleared, the SYSREF operates in PULSE MODE. ROM=Y, EEPROM=N 0x0 = None 0x1 = Continuous 0x2 = Pulser

1.522 R1236 (Offset = 0x4D4)

Return to the [Summary Table](#).

Table 1-524. R1236 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4	OUT_12_13_SR_CH_DIV_BYPASS	R/W	0x1	OUT12_13 cascaded SYSREF bypass mux. If set, bypasses OUT12_13 channel divider for the SYSREF input clock. Using CHDIV bypass is practical when SYSREF is required but CHDIV is not used. VCO post divide frequency must be ≤ 2 GHz to bypass CHDIV. ROM=Y, EEPROM=N 0x0 = CHDIV 0x1 = CHDIV Byp
3:0	RESERVED	R	0x0	Reserved

1.523 R1248 (Offset = 0x4E0)

Return to the [Summary Table](#).

Table 1-525. R1248 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-525. R1248 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	OPTIMIZE_R1248_b6	R/W	0x0	Set this field to 0 for optimal power and noise performance. ROM=Y, EEPROM=Y
5:0	OUT_14_FMT	R/W	0x0	Remix of OUT_14_VOD and OUT_14_VOS to display datasheet specified settings available to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.524 R1249 (Offset = 0x4E1)

Return to the [Summary Table](#).

Table 1-526. R1249 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	OUT_14_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
2:0	OUT_14_CONFIGURATION	R/W	0x0	OUT14 configuration. ROM=Y, EEPROM=Y and N 0x2 = Static DC 0x3 = CHDIV 0x4 = BYPASS 0x5 = BYPASS

1.525 R1250 (Offset = 0x4E2)

Return to the [Summary Table](#).

Table 1-527. R1250 Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_14_CHAN_POL_SEL	R/W	0x0	OUT14 ChanDiv Polarity Select. This bit flips the polarity of the clock into SYSREF and the polarity of the clock into the channel divider.

Table 1-527. R1250 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:5	OUT_14_CLK_MUX	R/W	0x0	OUT14 Input Clock Select. Selects the input clock which will be used to drive the output. ROM=Y, EEPROM=Y 0x0 = VCO3 0x1 = VCO2 0x2 = VCO1_PRI
4	RESERVED	R	0x0	Reserved
3	OUT_14_DIV_EN	R/W	0x0	OUT14 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y
2:0	OUT_14_CH_MUX_SEL	R/W	0x4	OUT14 Clock Enable. Bit 2, if set, passes the selected clock (VCO3 or VCO1P), to the second stage of clock selection. Bit 1 and Bit0 enable the selected clock to drive the channel divider and the channel divider retimer respectively. ROM=Y, EEPROM=Y 0x0 = PLL2->BYPASS 0x3 = PLL2->CHDIV 0x4 = PLL1->BYPASS 0x7 = PLL1->CHDIV

1.526 R1251 (Offset = 0x4E3)

Return to the [Summary Table](#).

Table 1-528. R1251 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	OUT_14_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
3	OUT_14_SYNC_EN	R/W	0x1	OUT14 ChanDiv Sync Enable. Enables synchronization of chandiv dividers for OUT14. ROM=Y, EEPROM=N
2:0	RESERVED	R	0x0	Reserved

1.527 R1252 (Offset = 0x4E4)

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Table 1-529. R1252 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_14_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1253

1.528 R1253 (Offset = 0x4E5)

Return to the [Summary Table](#).

Table 1-530. R1253 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_14_CH_STATIC_OFFSET	R/W	0x0	OUT_14_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.529 R1254 (Offset = 0x4E6)

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Table 1-531. R1254 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_14_CH_DIV_11:8	R/W	0x0	See Register 1255

1.530 R1255 (Offset = 0x4E7)

Return to the [Summary Table](#).

Table 1-532. R1255 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_14_CH_DIV	R/W	0xA	OUT14 ChanDiv Divide Value. For this 12-bit divider all bits are set by ROM, but 8 LSBs may be overwritten by EEPROM if EEPROM overlay (ROM_PLUS_EE=1) is enabled. ROM=Y, EEPROM=Y

1.531 R1280 (Offset = 0x500)

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Table 1-533. R1280 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OPTIMIZE_R1280_b6	R/W	0x0	Set this field to 0 for optimal power and noise performance. ROM=Y, EEPROM=Y

Table 1-533. R1280 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	OUT_15_FMT	R/W	0x0	Remix of OUT_15_VOD and OUT_15_VOS to display datasheet specified settings available to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.532 R1281 (Offset = 0x501)

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Table 1-534. R1281 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	OUT_15_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
2:0	OUT_15_CONFIGURATION	R/W	0x0	OUT15 configuration. ROM=Y, EEPROM=Y and N 0x2 = Static DC 0x3 = CHDIV 0x4 = BYPASS 0x5 = BYPASS

1.533 R1282 (Offset = 0x502)

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Table 1-535. R1282 Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_15_CHAN_POL_SEL	R/W	0x0	OUT15 ChanDiv Polarity Select. This bit flips the polarity of the clock into SYSREF and the polarity of the clock into the channel divider.

Table 1-535. R1282 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:5	OUT_15_CLK_MUX	R/W	0x0	OUT15 Input Clock Select. Selects the input clock which will be used to drive the output. ROM=Y, EEPROM=Y 0x0 = VCO3 0x1 = VCO2 0x2 = VCO1_PRI
4	RESERVED	R	0x0	Reserved
3	OUT_15_DIV_EN	R/W	0x0	OUT15 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y
2:0	OUT_15_CH_MUX_SEL	R/W	0x4	OUT15 Clock Enable. Bit 2, if set, passes the selected VCO1 clock (VCO1P or VCO1S), to the second stage of clock selection. Bit 1 and Bit0 enable the selected clock to drive the channel divider and the channel divider retimer respectively. ROM=Y, EEPROM=Y 0x0 = PLL2->BYPASS 0x3 = PLL2->CHDIV 0x4 = PLL1->BYPASS 0x7 = PLL1->CHDIV

1.534 R1283 (Offset = 0x503)

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Table 1-536. R1283 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	OUT_15_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
3	OUT_15_SYNC_EN	R/W	0x1	OUT15 ChanDiv Sync Enable. Enables synchronization of chandiv dividers for OUT15. ROM=Y, EEPROM=N
2:0	RESERVED	R	0x0	Reserved

1.535 R1284 (Offset = 0x504)

Return to the [Summary Table](#).

Table 1-537. R1284 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_15_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1285

1.536 R1285 (Offset = 0x505)

Return to the [Summary Table](#).

Table 1-538. R1285 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_15_CH_STATIC_OFFSET	R/W	0x0	OUT_15_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.537 R1286 (Offset = 0x506)

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Table 1-539. R1286 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_15_CH_DIV_11:8	R/W	0x0	See Register 1287

1.538 R1287 (Offset = 0x507)

Return to the [Summary Table](#).

Table 1-540. R1287 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_15_CH_DIV	R/W	0xA	OUT15 ChanDiv Divide Value. For this 12-bit divider all bits are set by ROM, but 8 LSBs may be overwritten by EEPROM if EEPROM overlay (ROM_PLUS_EE=1) is enabled. ROM=Y, EEPROM=Y

2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from April 30, 2025 to November 30, 2025 (from Revision * (April 2025) to Revision A (November 2025))

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