An overview on basic operational amplifier stability

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One of the most common issues with operational amplifier (op amp) circuits is stability. In this article, I'll answer three important questions with regards to stability:

- How much phase margin do you need for a reliable design?
- How do you compensate an unstable circuit?
- What drop-in solutions are available for stability issues?

How much phase margin do you need?

Op-amp loop stability is measured in phase margin, which is the difference in the output signal phase shift from 360 degrees when the output closed-loop gain goes below unity. Some shift is inherent to every op amp (for example, the dominant pole), while additional shift depends on the application and components surrounding the amplifier.

Different rules of thumb recommend 30, 45 or even 60 degrees of phase margin, but how much do you really need to ensure reliable performance? For traditional Miller-compensated op amps, it is possible to simulate typical process variations and observe the resulting impact on phase margin.

Figure 1 approximates the open-loop gain (Aol) and output impedance (Zo) of an op amp with a 1MHz unity-gain bandwidth and Zo = 300Ω. Over process variation, the value of the Miller capacitor (C26) can vary approximately ±30%, and an additional ±30% (approximate) over temperature. This variation gives a total error of ±30% × ±30%, which is the same as ±30% + ±9%, or ±39% variation. Since the value of the Miller capacitor changes the placement of the dominant pole in the Aol of the op amp, this variation can significantly impact the unity-gain bandwidth and phase margin, which is why these specifications are always given as typical values, even for precision amplifiers and high-speed amplifiers.

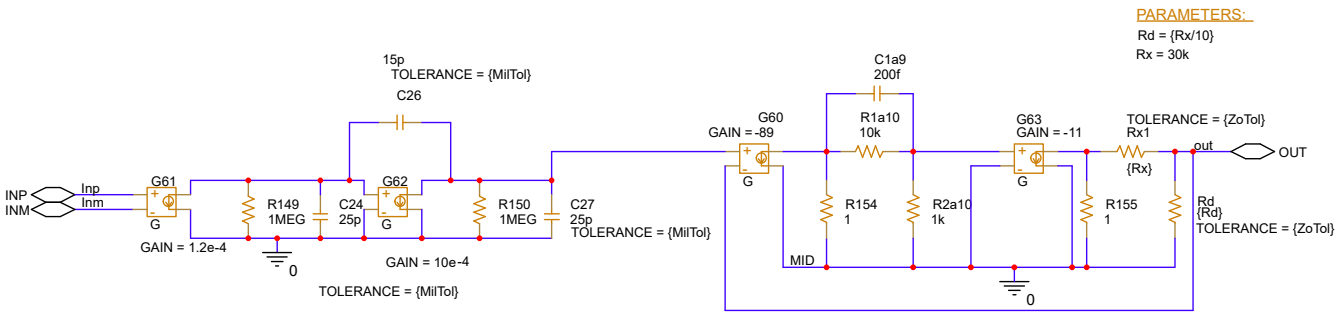

Figure 1. *Open-loop gain and output impedance PSpice® for TI circuit*

The amplifier in **Figure 1** is set with a load resistance and capacitance so that the feedback loop has 45 degrees of phase margin. Running a Monte Carlo analysis on the dominant factors of the loop stability – the Miller capacitor, open-loop output impedance and passive devices surrounding the amplifier – will show an estimate of how changes over process variation and temperature will impact the phase margin of the circuit.

Figure 2 plots the resulting phase margin. For this analysis, I applied ±40% variation to the Miller capacitor, ±15% variation for Zo, ±10% for the load capacitor and ±5% for the load resistor. These are the expected internal tolerances for the Miller capacitor and Zo, as well as typical component precision for many general-purpose applications.

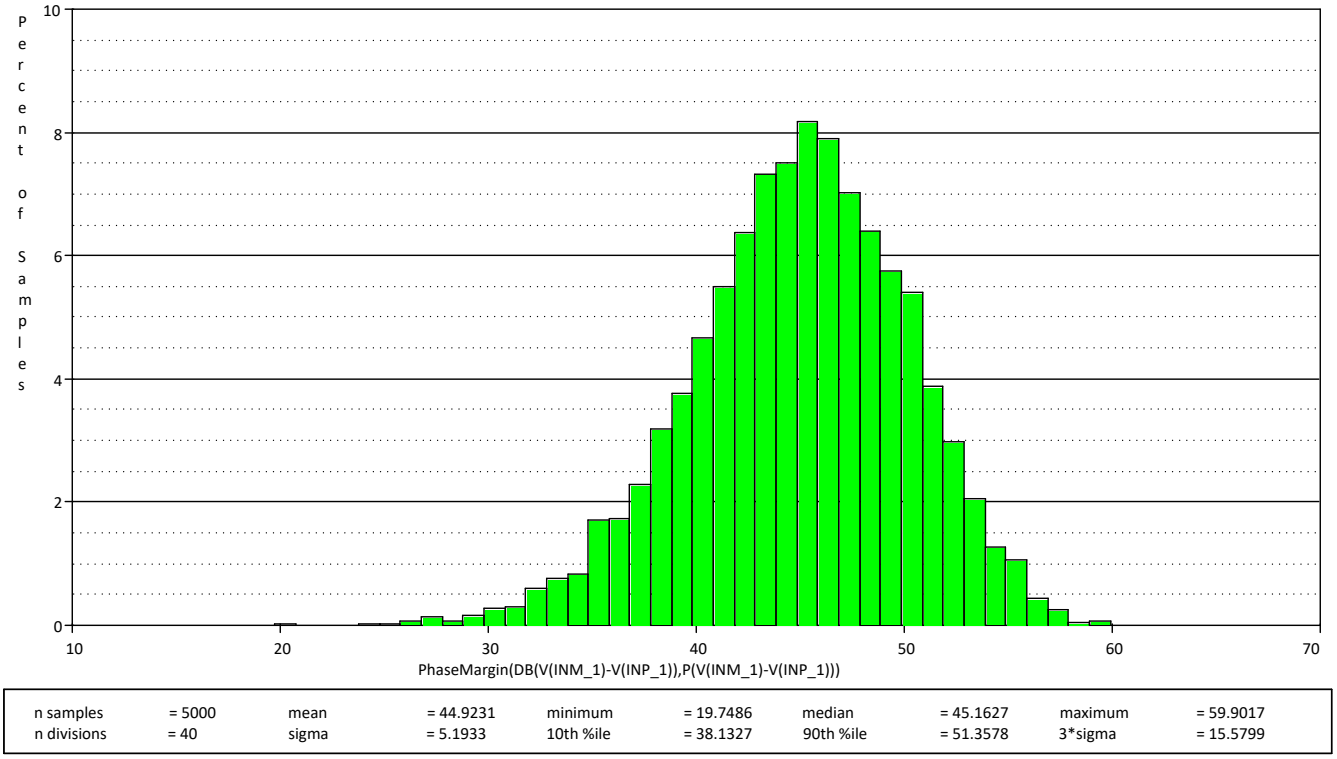

Figure 2. *5,000-run Monte-Carlo analysis across estimated process variation and temperature shifts*

Across this variation, the phase margin of the feedback loop sees a minimum phase margin of 19 degrees, a 26 degree shift from 45 degrees. Over process variation and temperature, the circuit would remain stable if it had approximately 27 degrees of phase margin, although 45 degrees will offer both good transient performance and settling time. The closer the phase margin gets to 0 degrees, the more the output will overshoot the final value, and the longer it will take to settle to the final output value. 45 degrees of phase margin provides enough design tolerance to allow a shift in phase margin without compromising settling time or seeing excessive overshoot.

While these simulations are helpful in understanding the effects of Miller capacitor variation on performance, it's the circuit designer who is ultimately responsible for the performance of their design. Simulations are only as accurate as the included nonidealites, assuming many ideal properties in order to make the calculation less intensive.

Compensation schemes

There are cases where it is not possible to reduce a capacitor on the output of an op amp, for either voltage rail regulation, filter capacitance for an analog-to-digital converter, or other circuit needs. In such cases, how do you achieve proper phase margin? There are multiple compensation schemes that can increase phase margin, but in this article, I'll focus on two, shown in **Figure 3** and **Figure 4**: an isolation resistor (Riso) and Riso dual feedback. When designing these circuits, it can be difficult to determine what value of Riso you need to stabilize the feedback loop.

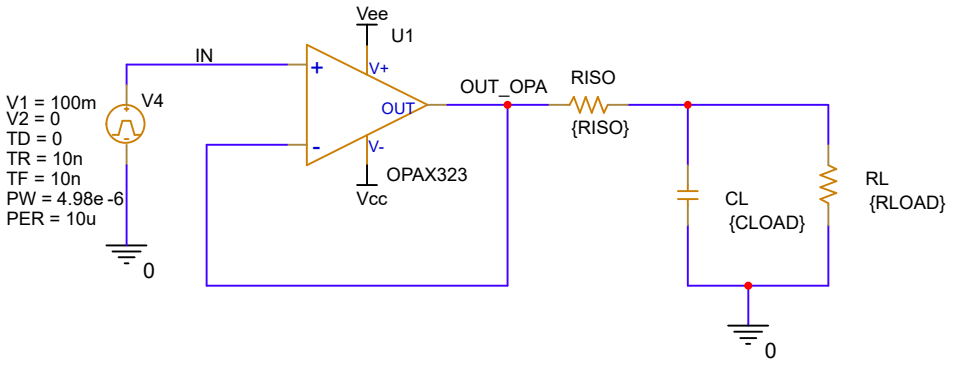

Figure 3. *Riso compensation scheme.*

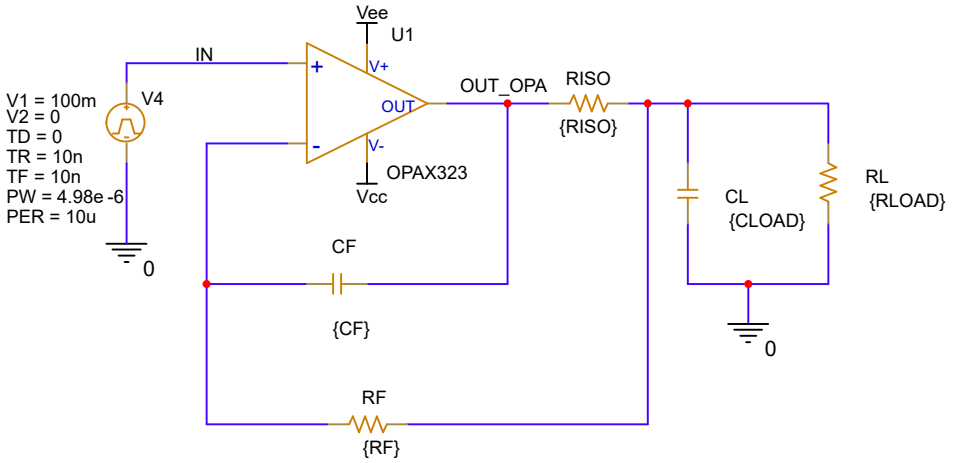

Figure 4. *Riso dual feedback scheme.*

Riso is the simplest method for isolating the phase lag introduced by the load capacitance. It involves placing a resistor between the feedback loop and the load capacitor. One drawback, however, is decreased DC accuracy when the output has a load current. The amount of DC error will be the value of the isolation resistor multiplied by the output current.

The Riso dual feedback compensation scheme overcomes this DC inaccuracy. The circuit enables a high-frequency path through the feedback capacitor to stabilize the feedback loop and a DC path that allows the op amp to compensate for the I × R drop over the isolation resistor. You can find these values either mathematically or through simulation by trying different values of Riso and seeing where there is stable operation.

Let's try an approach that uses mathematical analysis with simulated results.

The two main components for accurate modeling of amplifier loop stability are the open-loop gain and open-loop output impedance. TI's standard op-amp macromodel, the Green-Williams-Lis (GWL) model, accurately characterizes these parameters for all op amps released after 2016. Many of the more popular op amps, such as the **LM2904** and its newer version, the **LM2904B**, also have GWL macromodels created for them. The library file for the SPICE macromodels includes a header that details what parameters are accurately reflected in the SPICE model. If the open-loop gain and open-loop output impedance are modeled, it is likely that the stability of the model will reflect the silicon's performance.

Ensuring the accuracy of the SPICE model enables you to analyze the loop stability of your circuit and mathematically calculate the best value for Riso. The value of Riso that ensures 45 degrees of phase margin should create a zero in the feedback loop at the intersection point of the feedback factor (1/beta) and the amplifier open-loop gain. For extra assurance, setting the zero where the open-loop gain is 20dB, you can see the maximum positive phase shift from the zero in the feedback loop.

Compensation	Formula
Large capacitive load	
R_{ISO} (minimum)	$R_{iso} = \frac{1}{2\ \pi\ f_{AOL\ Loaded\ =\ 0dB}\ C_{LOAD}}$
R_{ISO}	$R_{iso} = \frac{1}{2\ \pi\ f_{AOL\ Loaded\ =\ 20dB}\ C_{LOAD}}$
R_{ISO} plus dual feedback	$R_F \geq R_{ISO}\ \ 100$ $\frac{5 \times R_{iso} \times C_L}{R_F} \leq C_F \leq \frac{10 \times R_{iso} \times C_L}{R_F}$

Table 1. *Formulas for calculating isolation resistor value and feedback components for Riso dual feedback.*

Part of the power of PSpice for TI is you can set up, archive, and share simulations and equations for later schematics. Since the evaluation for Riso and Riso dual feedback are formulaic and easily repeatable, you can leverage these template projects to eliminate the need to remember the formulas to calculate Riso or the Rf/Cf for the Riso dual feedback circuit across four common op-amp circuits. Simply download the PSpice for TI project, drop in the op amp you want to analyze, enter the parameters that complete the specific circuit that needs stabilizing, and run the simulation to find the appropriate value of Riso that you need. These projects can also compensate circuits that are unstable from capacitance on the inverting terminal, or those with very large feedback resistors.

Circuit Type	PSpice for TI Project
Buffer Amplifier	**https://www.ti.com/lit/zip/sbomcj2**
Inverting Amplifier	**https://www.ti.com/lit/zip/sbomcj0**
Non-inverting Amplifier	**https://www.ti.com/lit/zip/sbomci9**
Difference Amplifier	**https://www.ti.com/lit/zip/sbomcj1**

The drop-in solution

There is also a solution when you don't want extra compensation circuitry, or it's not feasible to add it. TI's **OPA994** device family has a special compensation structure that is stable across capacitive loads, which is possible because the bandwidth of the device changes when the output sees different capacitive loads. Keeping the bandwidth constantly lower than the pole introduced by the output impedance and capacitive load will maintain the stability of the amplifier, regardless of what capacitor you place on the output. **Figure 5** illustrates the phase margin for different values of load capacitance with no external compensation resistor, taken from the **OPA994** data sheet.

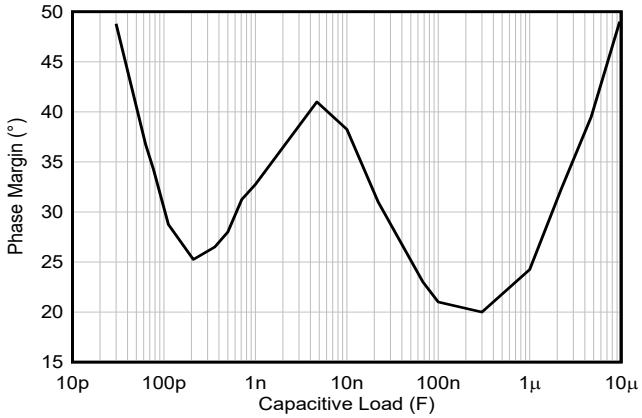

Figure 5. *Phase margin over various capacitive loads in unity gain.*

Every design decision comes with a cost in addition to a benefit, and the **OPA994** device family is no different. A more complex design results in a larger device, which can be more costly than simpler devices. Additionally, this means that the device cannot fit into TI's smallest packages, such as the 0.64mm^2 extra-small outline no-lead (X2SON) package. This design is currently only available in a bipolar amplifier, so if you require the low-input bias current of a complementary metal-oxide semiconductor (CMOS), this device may have too high of an input bias current.

There are many benefits associated with a bipolar amplifier, including lower noise and more bandwidth, for less quiescent current than CMOS devices. The full trade-off of bipolar vs. CMOS can be weighed on a circuit-by-circuit basis [**1**]. Overall, the **OPA994** can in many cases serve as a drop-in solution for stability.

Conclusion

In the initial design stage, the main question is how much phase margin is sufficient for reliable performance over process variation and temperature. If the phase margin of the initial implementation is not sufficient, multiple compensation schemes are available to increase the phase margin to an acceptable level. These solutions are given through pre-configured, easy-to-use projects in PSpice for TI. Finally, if there is a project already in production that does encounter a stability issue, use the drop-in solution proposed.

References

1. **Trade-Offs Between CMOS, JFET, and Bipolar Input Stage Technology** – Marek Lis

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