EVM User's Guide: UCC35131EVM-118

UCC35131-Q1 Evaluation Module for Automotive and Industrial Bias Supply Applications

Description

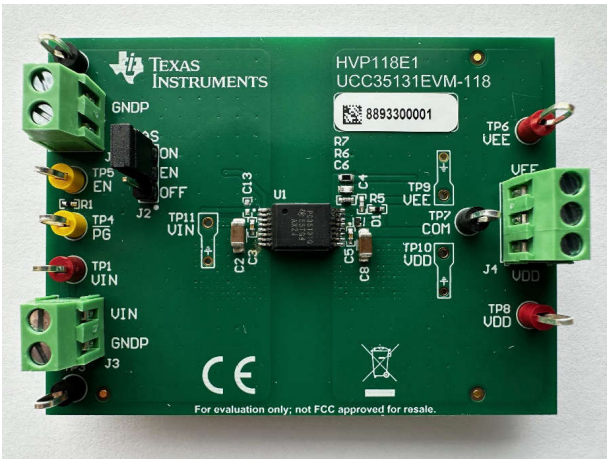
This evaluation module (EVM) allows designers to quickly and efficiently evaluate the UCC35131-Q1 for use in automotive or industrial applications requiring gate driver, IC bias power as high as 2W and meeting up to 5kV$_{RMS}$ isolation. The EVM demonstrates the small size, high power density, voltage regulation accuracy and robust set of protection features necessary for providing reliable bias power to SiC and IGBT gate drivers.

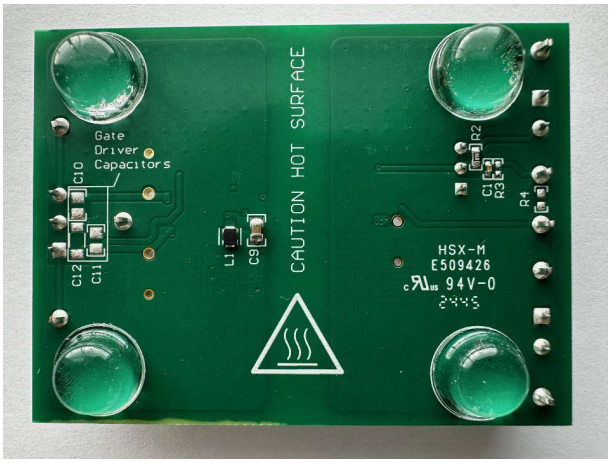
Features

- Wide input voltage range: 5.5V ≤ VIN ≤ 20V
- High power density
- >5kV$_{RMS}$ isolation
- Open drain/power good (PG) signal
- Integrated protections: undervoltage lockout (UVLO), overvoltage lockout (OVLO), short-circuit, overvoltage protection (OVP), undervoltage protection (UVP), and thermal shutdown
- ENA pin for logic enable, ON/OFF control
- AEC-Q100 qualified for automotive applications: -40°C ≤ T_A ≤ 125°C

Applications

- Hybrid, electric and power train systems (EV/HEV)
  - Inverter and motor control
  - On-board (OBC) and wireless charger
  - DC/DC converters
- Energy Infrastructure
  - DC fast charging power module
  - DC charging (pile) station
  - String inverter
- Industrial automation
  - Off-highway vehicle electric drive
- Power delivery
  - Rack and server power





1 Evaluation Module Overview

1.1 Introduction

The UCC35131-Q1 is a high efficiency, low-emissions, 5kV$_{RMS}$ isolated DC-DC converter capable of delivering 2W of power. Since the UCC35131-Q1 provides isolated power in an integrated package, this allows systems to reduce cost and size by removing the need for separate isolated power supplies. The UCC35131-Q1 delivers class-leading power density and highest efficiency while removing the need for bulky external transformers or power modules commonly used in existing designs. This integration allows for minimal printed circuit board (PCB) area as well as decreased height profile.

1.2 U1: Solder Reflow

When performing solder rework by hand, the recommended solder profile used in manufacturing is often not easily followed on the lab bench. Please exercise appropriate ESD material handling precautions and use caution when soldering, especially with forced air solder equipment. For IC removal, use only just enough hot air focused at the pins while gently lifting upward on the IC package body so that as soon as the solder begins to reflow, the IC is lifted off the PCB. Recommend to set the hot air temperature to no more the 250°C with minimal forced air. For IC install by hand, recommend to hand solder with solder iron if possible, otherwise, follow similar guidance if hot air must be used.

1.3 Kit Contents

Table 1-1. EVM Kit Contents

Designator	Description	Quantity
PCB1/HVP118E1	UCC35131EVM-118	1

1.4 Specification

V_{IN} = 12V, V_{DD}-COM = 15V, V_{EE}-COM = -5V, T_A = 25°C (unless otherwise noted).

Parameter		Test Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
V_{IN}	Input voltage range	$P_{VDD-COM}$ = 2W	10.8	12	13.2	V
		$P_{VDD-COM}$ = 1.6W	8	12	20	V
		$P_{VDD-COM}$ = 0.5W	5.5		8	V
V_{IN_ON}	Input voltage on		4		4.5	V
V_{IN_OFF}	Input voltage off		3.8		4.28	V
OUTPUT CHARACTERISTICS						
V_{DD}-COM	DC full load set-point	10.8V < V_{IN} < 13.2V, I_{VDD} = 133mA		15		V
I_{VDD}	V_{DD} load current range	10.8V < V_{IN} < 13.2V	0		133	mA
P_{MAX}	Maximum output power	10.8V < V_{IN} < 13.2V, I_{VDD} = 133mA			2	W
V_{EE}-COM	DC full load set-point			-5		V

1.5 Device Information

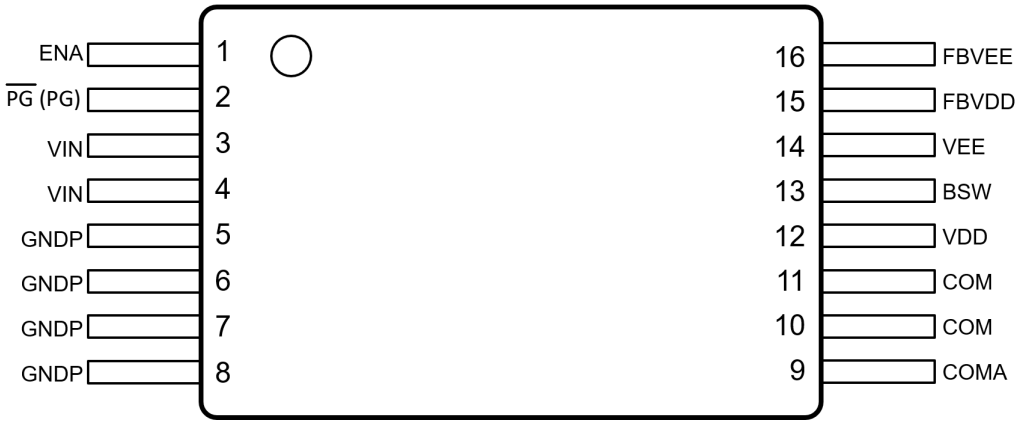


Figure 1-1. DHA Package, 16-Pin SSOP (Top View)

Table 1-2. Pin Configuration and Functions

Pin		Type (1)	Description
Name	No.		
ENA	1	I	Enable pin. Forcing ENA LOW disables the device. Pull HIGH to enable normal device functionality. 5.5V recommended maximum. Can be used to program input UVLO with a resistor divider from VIN.
PG(PG)	2	O	Power-Good open-drain output pin. Remains active when $V_{VIN\_UVLOP} \le V_{VIN} \le V_{VIN\_OVLOP}$; $V_{VDD\_UVP} \le V_{FBVDD} \le V_{VDD\_OVP}$; $V_{VEE\_UVP} \le V_{FBVEE} \le V_{VEE\_OVP}$; $T_{J\_Primary} \le T_{SHUT\_P\_R}$; and $T_{J\_secondary} \le T_{SHUT\_S\_R}$. Connect a decoupling capacitor in 0402 body size for by-passing the high frequency noise. It must be next to the Power-Good pin on the same side of the PCB as the IC.
VIN	3,4	P	Primary input voltage. Connect a 10µF and a parallel 0.1µF ceramic capacitor from VIN to GNDP. The 0.1µF ceramic capacitor is for by-passing the high frequency noise and must be next to the VIN and GNDP pins
GNDP	5, 6, 7, 8	G	Primary-side ground connection for VIN. Place several vias to copper pours for thermal relief. See PCB Layout Example section for more details.
COMA	9	G	Secondary-side analog sense reference connection for the noise sensitive analog feedback input FBVDD, and FBVEE. Connect the low-side FBVDD feedback resistor and high frequency decoupling filter capacitors close to the COMA pin and respective feedback pin FBVDD. Connect to secondary-side gate drive voltage reference, COM. Use a single point connection and place the high frequency decoupling ceramic capacitor close to the COMA pin.
COM	10, 11	G	Secondary ground. Connect to Source of power switch.
VDD	12	P	Secondary-side isolated output voltage from transformer. Connect a 10µF and a parallel 0.1µF ceramic capacitor from VDD to COM. The 0.1µF ceramic capacitor is for bypassing high frequency noise and must be next to the VDD and COM pins.
BSW	13	P	Internal buck-boost converter switch pin. Connect an inductor from this point to COM. Recommend a 3.3µH to 10µH chip inductor.
VEE	14	P	Secondary-side isolated output voltage for negative rail. Connect a 2.2µF ceramic capacitor from VEE to COM for bypassing high frequency noise.
FBVDD	15	I	Feedback (VDD – COM) output voltage sense pin and to adjust the output (VDD – COM) voltage. Connect a resistor divider from VDD to COM so that the midpoint is connected to FBVDD. The equivalent FBVDD voltage is regulated at 2.5V with the internal hysteresis control across isolation. Adding a 470pF ceramic capacitor for high frequency decoupling in parallel with the low-side feedback resistor is needed. The 470pF ceramic capacitor for high frequency bypass must be next to the FBVDD and COMA pins on top layer or back layer connected with vias.
FBVEE	16	I	Feedback (COM – VEE) output voltage sense pin used to adjust the output (COM – VEE) voltage. Connect one feedback resistor to VEE to program the (COM – VEE) voltage from 2V and 8V. Connect a 10pF ceramic capacitor from FBVEE to COMA for bypassing high frequency noise. The 10pF ceramic capacitor must be next to the FBVEE pin on top layer or back layer connected with vias.

(1) TYPE: P=Power, PG=Primary Ground, SG=Secondary Return, SGA=Secondary Return Analog, I=Input, O=Output

2 Hardware

WARNING

- Caution Hot Surface. Contact may cause burns. U1 package surface can reach temperatures of 45°C above ambient. Do not touch!
- If you are not trained in proper safety, handling and testing power electronics, please do not test this EVM

2.1 Power Requirements

2.2 Recommended Test Equipment

1. V_{BIAS}: DC power supply1: 5V, 10mA
2. V_{IN}: DC power supply2: 20V, 500mA
3. I_{VDD}: Electronic load (set to constant resistance) or fixed resistor: 15V, 133mA
4. I_{VEE}: Electronic load (set to constant resistance) or fixed resistor: 5V, 65mA
5. (3) DVMs measuring DC voltage <30V
6. (3) DVMs measuring DC current <200mA on I_{VDD}, I_{VEE}, <500mA on I_{VIN}
7. Oscilloscope: 4-channel, 500MHz or better, voltage probes, current probes
8. Minimum wire gauge 20AWG to 22AWG or better
9. Thermal camera (optional) or thermocouple to measure U1 case temperature

2.3 External Connections for Easy Evaluation

The UCC35131EVM-118 utilizes screw terminals for quickly connecting to V_{IN}, VDD and VEE. Connecting the appropriate ammeters and voltmeters, as shown in Figure 2-1, allows accurate EVM efficiency measurements to be made.

Connecting test equipment:

1. Move shunt jumper, SH-J1 into the J2, 1-2, EN OFF position. This makes sure that the EVM cannot start while test equipment is being connected.
2. Connect a +5V DC bias power supply J1:1-2 (+3.3V to +5V). Set the power supply to 0V. The +5V supply at J1 serves as the pullup bias for /PG and ENA. Turn off/disable the +5V DC Bias power supply.
3. Connect the V_{IN} DC power supply capable of 5V < V_{IN} < 20V, 500mA at J3:1-2 (V_{IN}). Adjust the power supply to 12V, and set the current limit to 1A. Turn off/disable the V_{IN} power supply.
4. Connect a variable load between J4:1 (VDD) and J4:2 (COM). If using an electronic load, set to constant resistance (CR), 450Ω (~500mW). Leave the load disabled until the EVM is powered.
5. Connect a second load between J4:2 (COM) and J4:3 (VEE). If using an electronic load, set to constant resistance (CR), 2.5kΩ (~10mW). Leave the load disabled until the EVM is powered. Since the required load is small, a through-hole, 500mW, load resistor can be connected between J4:2-3.
6. Some electronic loads are not able to regulate/stabilize CC when setting in the low mA range. Monitor the input current and load currents by inserting ammeters as shown in Figure 2-1. A current probe can be used with the oscilloscope to verify the stability of the DC current being regulated by an electronic load.

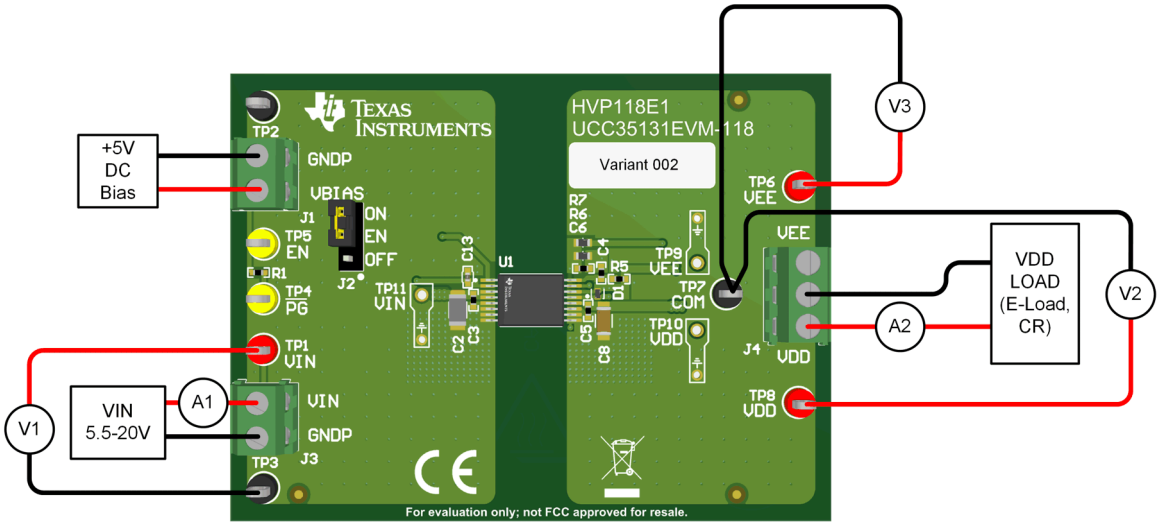


Figure 2-1. Typical Efficiency Measurement Setup

Power on for start-up:

1. Verify V_{IN} and +5V DC bias power supplies are off-disabled and no voltage is applied to the UUT
2. Move shorting jumper, SH-J1, into the J2:2-3, EN ON position. NOTE: removing the shorting jumper, SH-J1 also results in EN ON.
3. Turn on the V_{IN} DC power supply. Verify 12V is present at TP1-to-TP3
4. Verify the loads on VDD and VEE are disabled
5. Turn on the +5V DC bias power supply. EVM is now enabled with VDD and VEE in regulation under no load condition.
6. Verify +15V present on VDD-COM, and -5V present on VEE-COM
7. Enable the load on VDD, enable the load on VEE
8. The UCC35131-Q1 is now regulating VDD and VEE and processing ~0.5W of isolated output power
9. Vary V_{IN} between 5.5V < V_{IN} < 20V, vary I_{VDD} between 0mA < I_{VDD} < 133mA, Vary I_{VEE} between 0mA<I_{VEE}<150mA. Max power capability is reduced from 2W for VIN<12V, VIN>18V. If max power is exceeded, the EVM shuts down. In this case, remove the loads from VDD and VEE, restart VIN (or toggle EN) and verify EVM return to normal operation before slowly increasing VDD and/or VEE loads.
10. Insert oscilloscope probes into TP9, TP10 and TP11 for measuring VEE, VDD and V_{IN} startup, steady state and AC ripple voltage

Power off for shutdown:

1. Move shorting jumper SH-J1 into the J2:1-2, EN OFF position
2. Turn off +5V, DC bias power supply
3. Disable I_{VDD} load
4. Disable I_{VEE} load
5. Turn off V_{IN} power supply

2.4 Test Points

Table 2-1 describes the various EVM test points, allowing easy access for connecting oscilloscope probes, DVM test leads and wire connections to lab test equipment as outlined in Section 2.2. Pay attention to maintain separation between the primary side, GNDP and secondary side, COM. Primary-side test points are not to be referenced to COM through improper test equipment insertion. Likewise, secondary-side test points are not to be referenced to GNDP through improper test equipment insertion.

Table 2-1. Input, Output, Test Point (I/O/TP) Description

Pin	I/O/TP	Color	Description	Min	Typ	Max	Unit
J1	I	Green	V_{BIAS}, EN and /PG bias	3	V_{BIAS}	5	V
SH-J1	I	Black	J2 shorting jumper		0		V
J2:1-2	I	Black	EN, off		0		V
J2:2-3	I	Black	EN, on (SH-J1 removed is EN, on)		V_{BIAS}		V
J3	I	Green	V_{IN}, primary input voltage	5	12	20	V
J4:1-2	O	Green	Secondary VDD-to-COM	0		18	V
J4:2-3	O	Green	Secondary VEE-to-COM	-5		0	V
TP1	TP	Red	V_{IN}, positive probe point	5	12	20	V
TP2	TP	Black	GNDP, shared primary GND test point		0		V
TP3	TP	Black	GNDP, shared primary GND test point		0		V
TP4	TP	Yellow	/PG, power good test point		V_{BIAS}		V
TP5	TP	Yellow	EN, enable test point		V_{BIAS}		V
TP6	TP	Red	VEE, secondary VEE test point	-5		0	V
TP7	TP	Black	COM, secondary side reference		0		V
TP8	TP	Red	VDD, secondary VDD test point	0		18	V
TP9	TP	PCB	VEE-to-COM, secondary VDD scope probe point	-5		0	V
TP10	TP	PCB	VDD-to-COM, secondary VDD scope probe point	0		18	V
TP11	TP	PCB	V_{IN}-to-GNDP scope probe point	5	12	20	V

2.5 Oscilloscope Probes: Probing the EVM

Using TP9-11 oscilloscope probe PCB test points: The UCC35131-Q1 is a high frequency DC-DC module that requires careful measurement for accurately capturing transient events and measuring high frequency, AC ripple voltage. Remove the "witch hat" probe tip cover and ground lead from the scope probe. If scope probe ground springs are not available, wrap a piece of 22 AWG bare wire around the scope probe ground ring or use a fitted ground spring and insert the probe tip and ground into the EVM as shown in Figure 2-2.

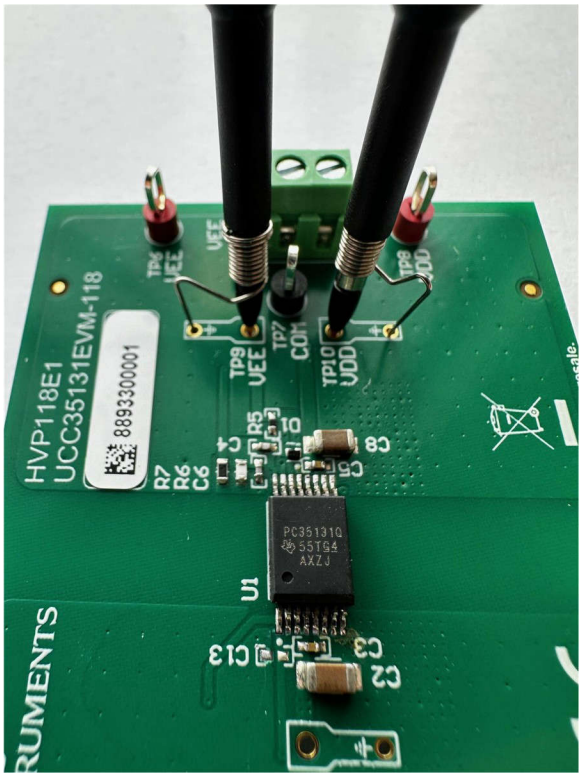


Figure 2-2. PCB Scope Probe Test Points

The EVM output nomenclature (VDD, VEE, COM) corresponds to what is commonly used when referring to isolated gate driver ICs. As shown in Figure 3-1, TP4 (COM) is the midpoint reference intended to connect to the COM pin of the isolated gate driver IC. When the UCC35131-Q1 is used to bias a gate driver IC, VDD (VDD-COM) and VEE (VEE-COM) are referred to with respect to COM.

3 Hardware Design Files

3.1 Schematics

Figure 3-1 shows the EVM electrical schematic.

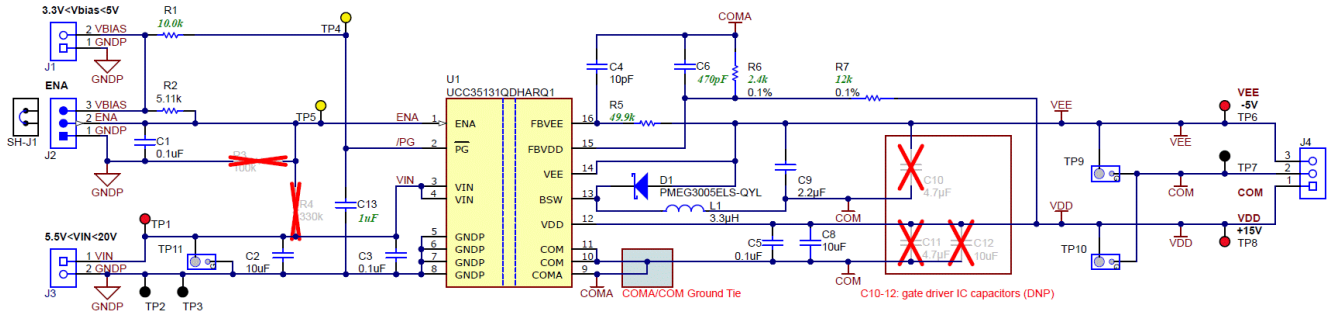


Figure 3-1. UCC35131EVM-118 Schematic

3.2 PCB Layouts

The UCC35131EVM-118 is designed using a four-layer, FR4, PCB, fabricated with 2-ounce copper on all four layers. The EVM, PCB demonstrates the important use of ground planes and tented stitching vias for shielding and improving EMI performance. For higher density PCBs such as automotive traction inverters, the PCB can include several additional signal layers but similar design methodology can be applied as best as possible.

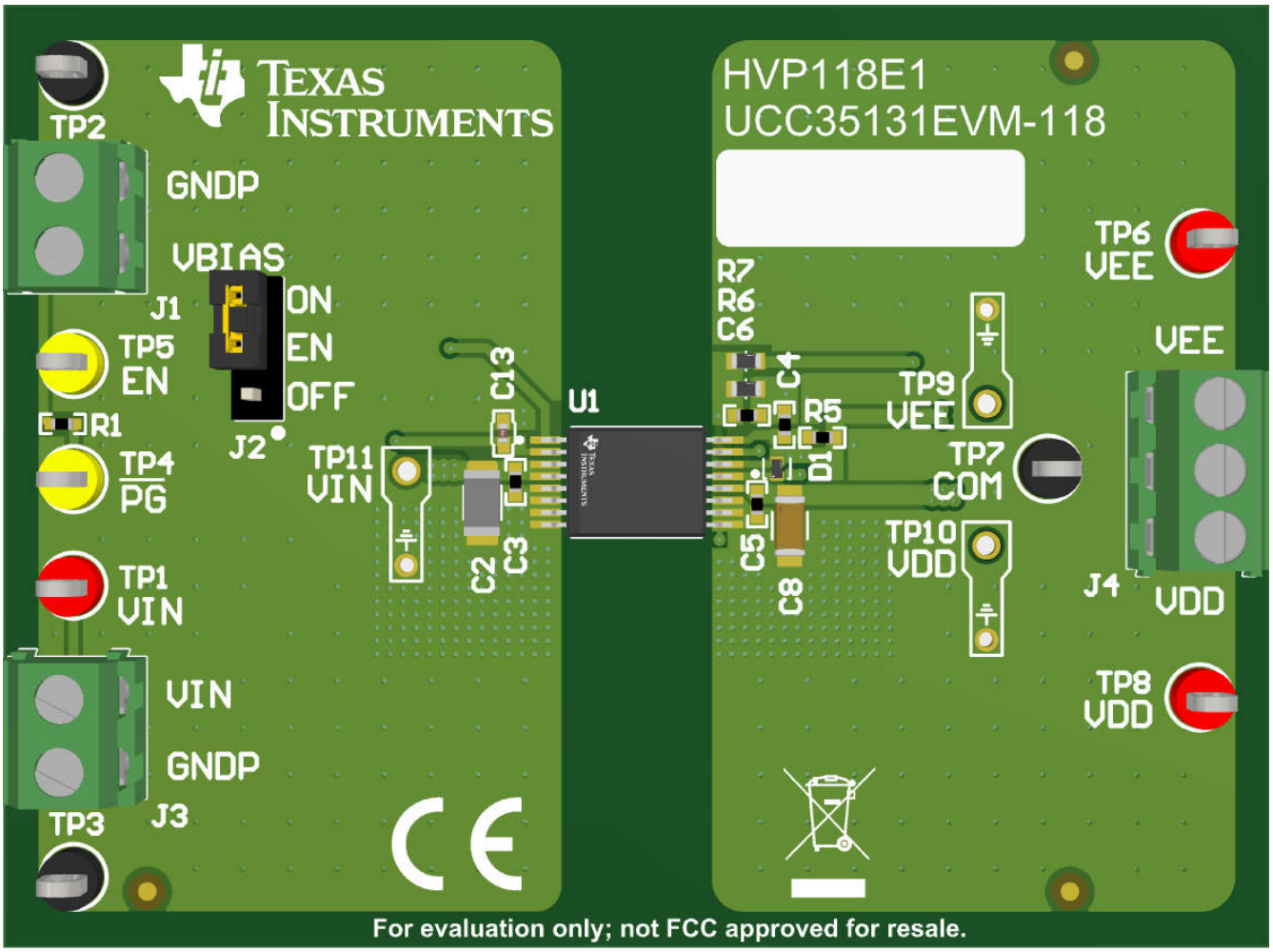


Figure 3-2. Fully Assembled 3D Top View

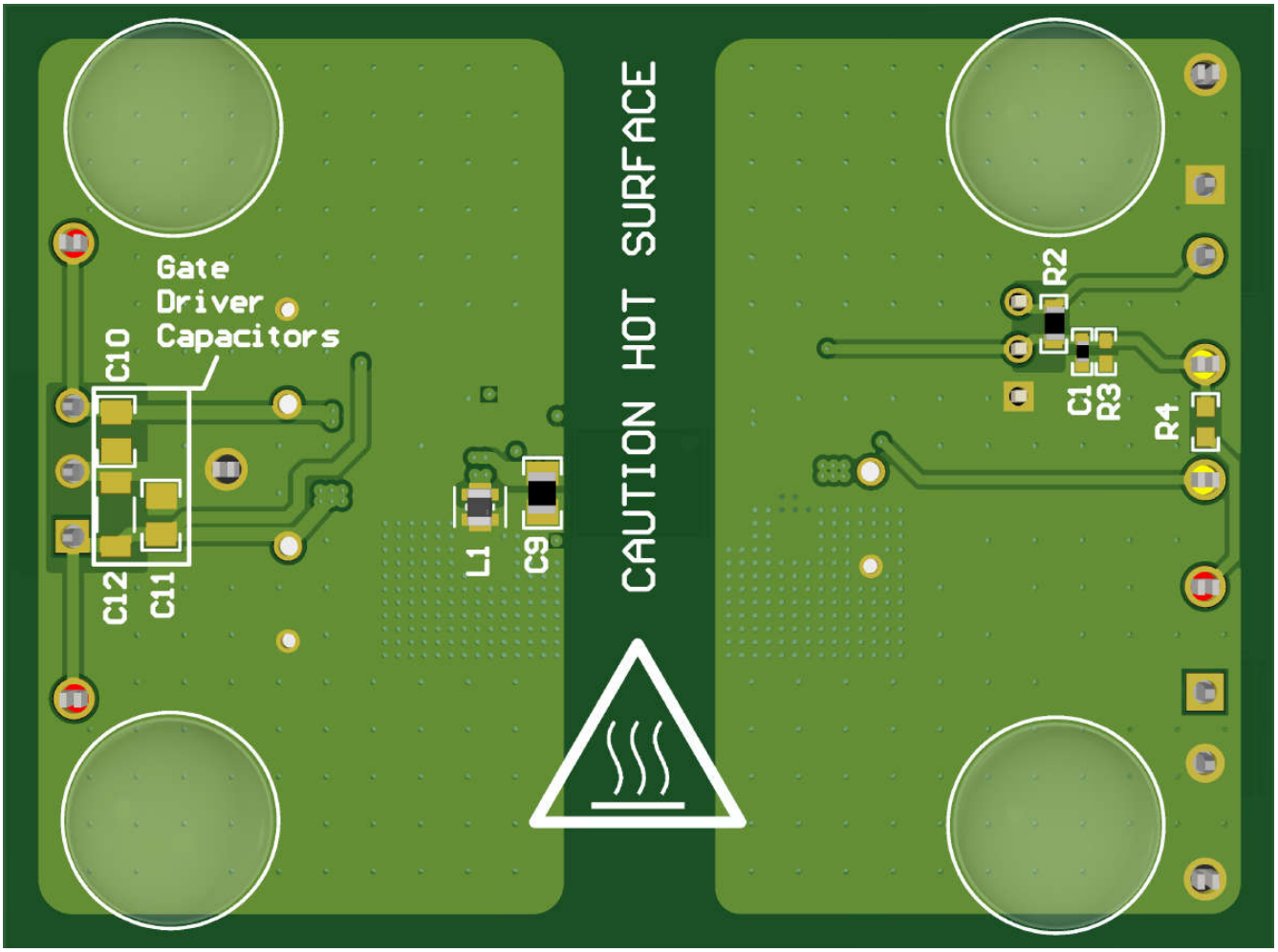


Figure 3-3. Fully Assembled 3D Bottom View

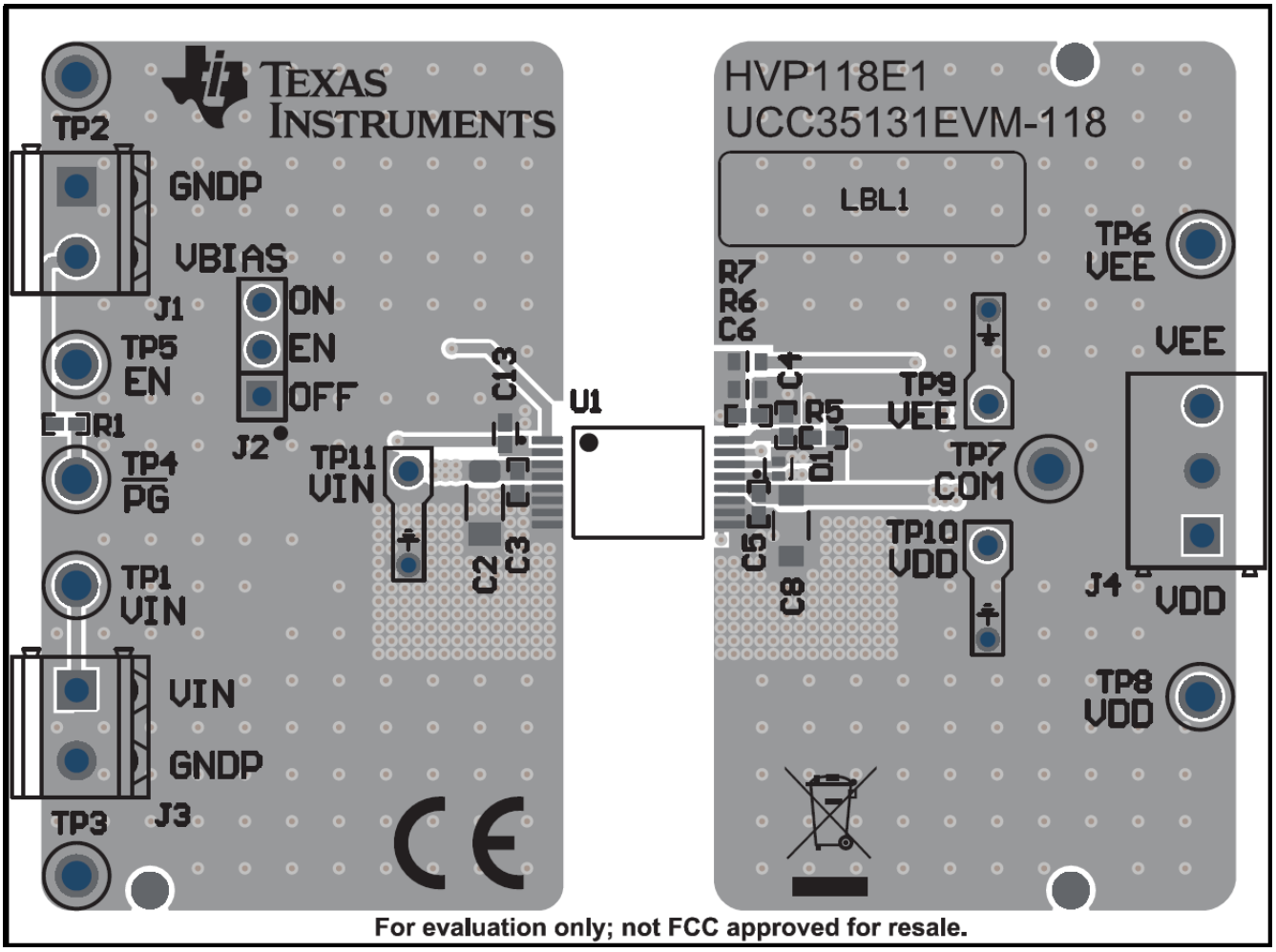


Figure 3-4. PCB Top Layer, Assembly

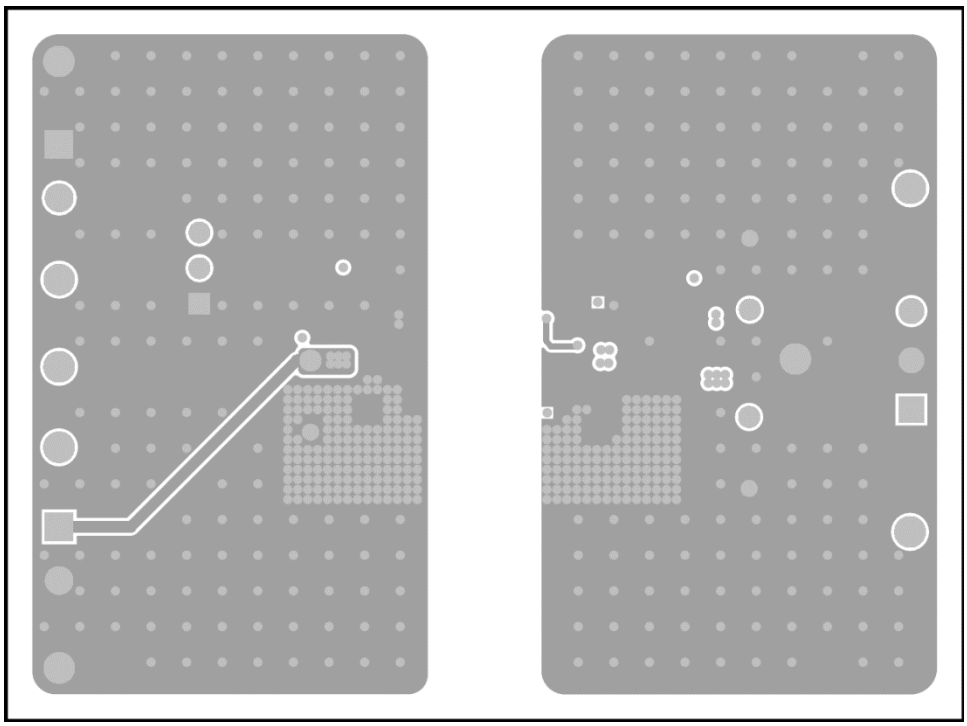


Figure 3-5. Ground Layer 2

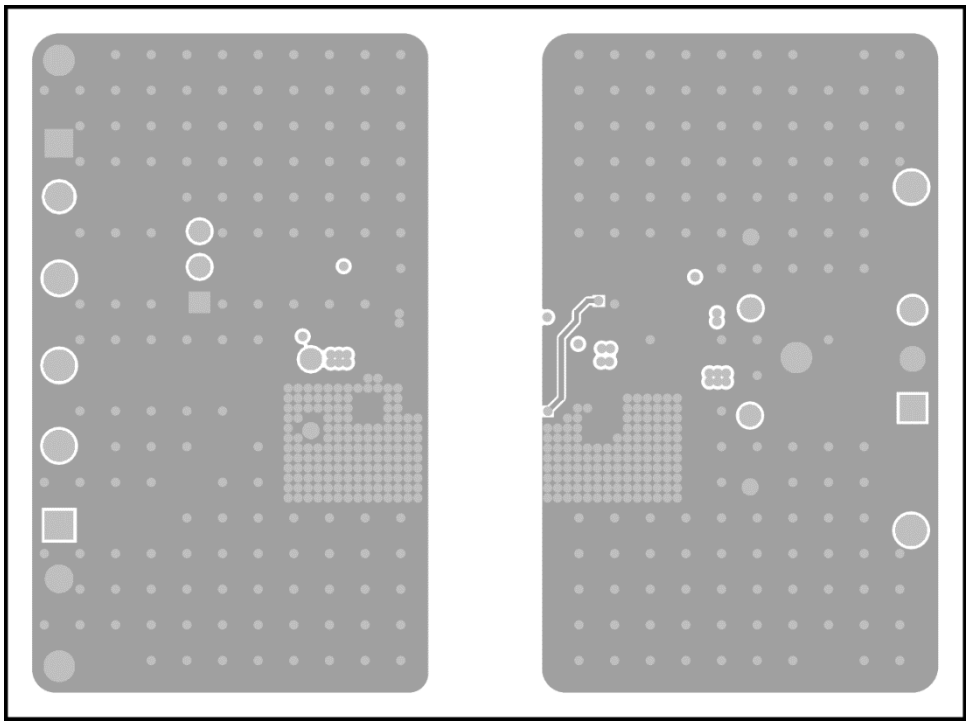


Figure 3-6. Ground Layer 3

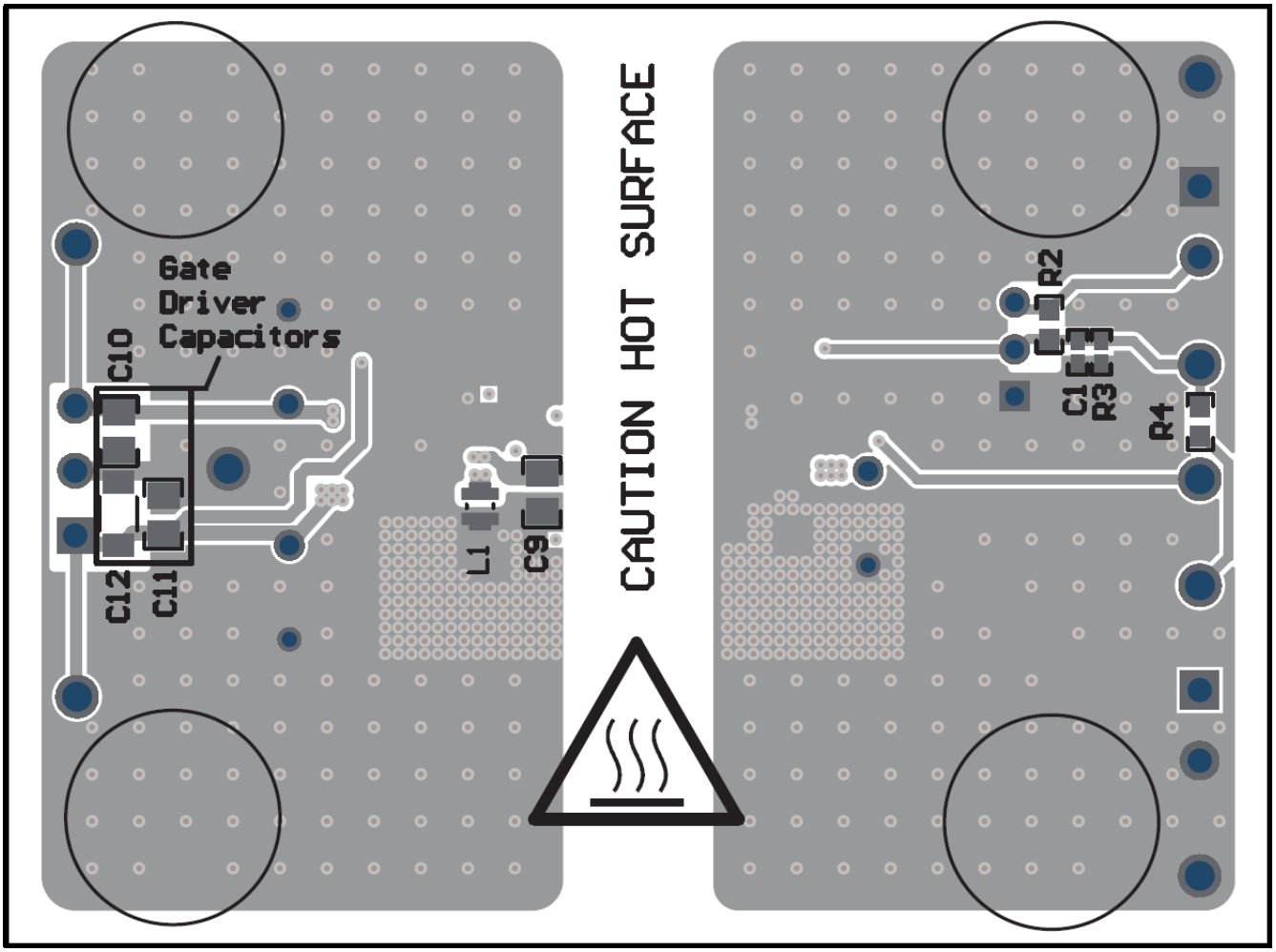


Figure 3-7. PCB Bottom Layer, Assembly (Mirrored View)

3.3 PCB Layout Guidelines

The UCC35131-Q1 integrated isolated power design simplifies system design and reduces board area usage. Follow these guidelines for proper PCB layout to achieve optimum performance. A minimum of 4-layer PCB layer stack using 2-ounce copper on external layers is recommended to accomplish a good thermal PCB design. The recommendation is to not route signal tracks or place components directly beneath the UCC35131-Q1.

1. Input capacitors between VIN pin and GNDP pin:
   a. Place the 0.1µF high frequency bypass capacitor (C3) as close as possible to pins 3, 4 (VIN) and pins 5–8 (GNDP) and on the same side of the PCB as the IC. 0402 ceramic SMD or smaller is a desired size for optimal placement. The self-resonant frequency in a range between 10MHz to 30MHz is best to offer low impedance decoupling for the switching frequency noise of the internal isolated convertor. Do not place any vias between the bypass capacitor and the IC pins so as to force the high frequency current through the capacitor.
   b. Place the bulk VIN capacitor(s) (C2) as close as possible and parallel to the 0.1µF high frequency bypass capacitor (C3) and on the same side of the PCB as the IC as shown in Figure 3-8.
2. /PG decoupling capacitor: The /PG decoupling capacitor should be placed close to pin 2 (/PG) and on the same side of the PCB as the UCC35131-Q1. Refer to C13 placement shown in Figure 3-8.
3. Output capacitors between VDD pin and COM pin:
   a. Place the 0.1µF high frequency bypass capacitor (C5) as close as possible to pin 12 (VDD) and pins 10, 11 (COM) and on the same side of the PCB as the IC. 0402 ceramic SMD or smaller is a desired size for placement. The self-resonant frequency in a range between 10MHz to 30MHz is best to offer low impedance decoupling for the switching frequency noise of the internal isolated convertor. Do not place any vias between the bypass capacitor and the IC pins so as to force the high frequency current through the capacitor.
   b. Place the bulk VDD-COM capacitor (C8) as close as possible and parallel to the 0.1µF high frequency bypass capacitor (C5) and on the same side of the PCB as the IC as shown in Figure 3-8.
4. Output capacitors between VEE pin and COM pin:
   a. Place the 2.2µF high frequency bypass capacitor (C9) as close as possible to VEE and COM pins. The self-resonant frequency in 3MHz to 4MHz is best to offer low impedance decoupling for the switching frequency noise of the buck-boost converter with the 3.3uH inductor (L1) selection. Putting the capacitor on the different side of PCB and using vias to connect is possible, to reduce the switching loop between the capacitor and the internal low-side MOSFET of the VEE buck-boost converter. In addition, putting the capacitor on different side also simplifies the decoupling capacitor placement of VDD pin and COM pin. An example of bottom side PCB placement of C9 and L1 is shown in Figure 3-12.
5. Feedback:
   a. COMA must be isolated through all PCB layers, from the COM plane. Use one via to make a direct connection to the low-side resistor and filter capacitor from FBVDD pin, same as the low-side filter capacitor from FBVEE pin.
   b. Place the RFBVDD feedback resistors (R6 and R7) and the decoupling ceramic capacitor (C6) close to the IC.
   c. The top-side feedback resistor must be placed next to the low-side resistor with a short, direct connection between both resistors and single connection to FBVDD pin. The top connection to sense the regulated rail (VDD-COM) must be routed and connected at the VDD bias capacitor remote location near the gate driver pins for best accuracy and best transient response.
   d. The VEE feedback resistor (R5) must be placed with the decoupling ceramic capacitor (C4) next to FBVEE (pin 15); while the connection to sense the regulated rail (COM-VEE) must be routed and connected at the COM bias capacitor remote location near the gate driver pins for best accuracy and best transient response.
   e. When using the dual output mode, the buck-boost inductor (L1) and a 2.2uF decoupling ceramic capacitor (C9) must be populated. These can be place on the opposite side of the IC or on the same layer as IC.
   f. A layout example is shown in Figure 3-9, where L2 (yellow) is routed on layer 2 and L3 (green) is routed on layer 3.

6. Thermal vias: The UCC35131-Q1 internal transformer makes a direct connection to the lead frame. It is therefore critical to provide adequate space and proper heatsinking designed into the PCB as outlined in the steps below.
   a. TI recommends to connect the VIN, GNDP, VDD, and COM pins to internal ground or power planes through multiple vias. Alternatively, make the polygons connected to these pins as wide as possible.
   b. Use multiple thermal vias connecting PCB top side GNDP copper to bottom side GNDP copper. If possible, the recommendation to use 2-ounce copper on external top and bottom PCB layers.
   c. Use multiple thermal vias connecting PCB top side VEE copper to bottom side VEE copper. If possible, the recommendation is to use 2-ounce copper on external top and bottom PCB layers.
   d. Thermal vias connecting top and bottom copper can also connect to internal copper layers for further improved heat extraction.
   e. Thermal vias should be similar to pattern shown below but apply as many as the copper area allows. TI recommends to use thermal via with 30mil diameter, 12mil hole size.
   f. A layout example is shown in Figure 3-10. For cases where less copper area is available, use as many thermal vias as the design permits, placed close to pins 5-8 (primary) and 9-11 (secondary).
7. Creepage clearance: To maintain the full creepage, clearance and voltage isolation ratings specified in the data sheet, avoid routing signal traces or placing components directly under the UCC35131-Q1. Maintain the clearance width highlighted in red, throughout the entire defined isolation barrier. Keep-out clearance for basic isolation can be 50% less than the reinforced isolation requirement (8.2mm). Using 8.2mm provides additional margin. A layout example is shown in Figure 3-11.
8. Gate driver output capacitors: CVDD_GD (C11 and C12) and CVEE_GD (C10) are reference designators referred to in the UCC35131-Q1 Excel Calculator Tool. C11 and C12 are the capacitors between VDD-COM and C10 is the capacitor between COM-VEE. C10-12 are capacitors required by the gate driver IC.
   a. CVDD_GD and CVEE_GD must be placed next to the gate driver IC for best decoupling and gate driver switching performance.
   b. For best voltage regulation, the feedback trace from VEE (FBVEE) and VDD (FBVDD) must be as direct as possible so that the voltage feedback is being sensed directly at the VDD and VEE capacitors near the gate driver IC.

3.4 PCB Layout Example

The PCB layout example, highlighted in the following figures, is based on the EVM schematic shown in Figure 3-1 and PCB layer images shown in Figure 3-4 to Figure 3-7.

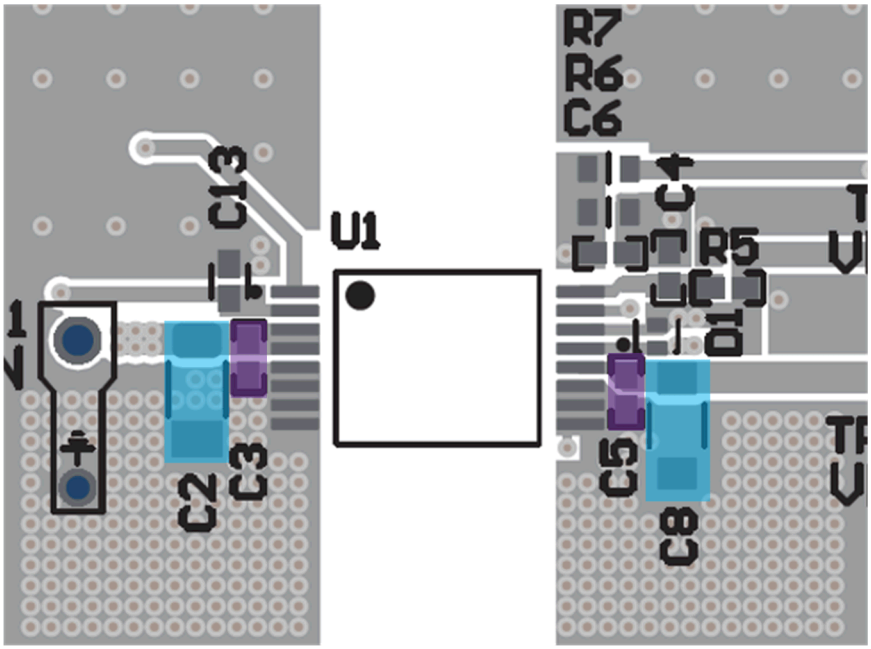


Figure 3-8. VIN (C2, C3) and VDD (C5, C8) Capacitors

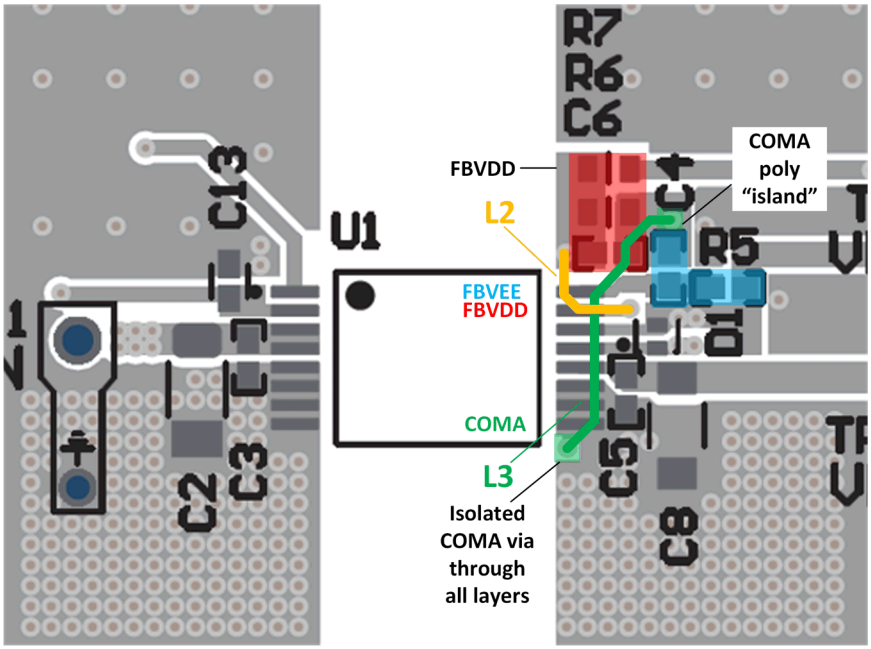


Figure 3-9. FBVDD (R6-7, C6), FBVEE (R5, C4), COMA Routing

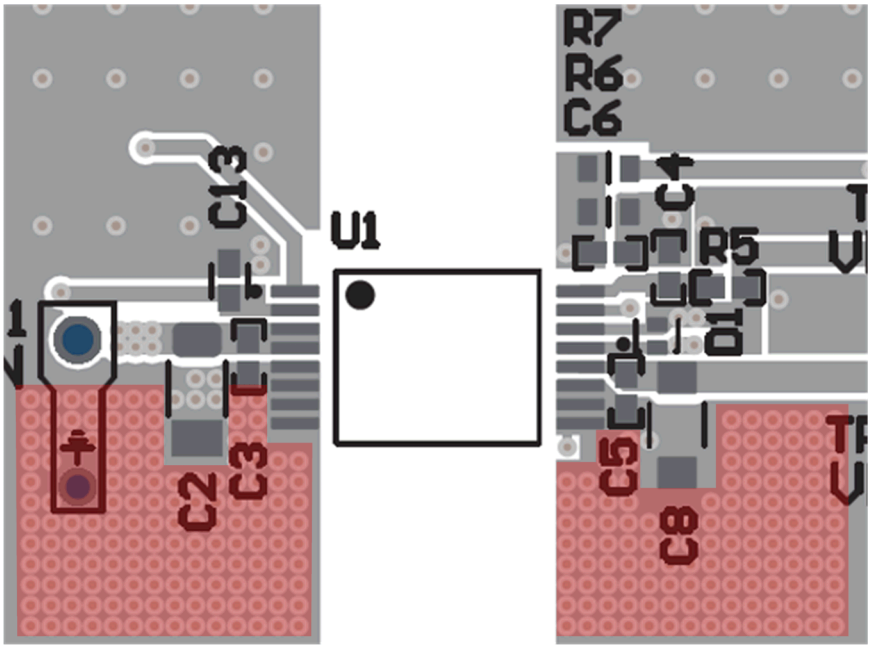


Figure 3-10. Thermal Vias

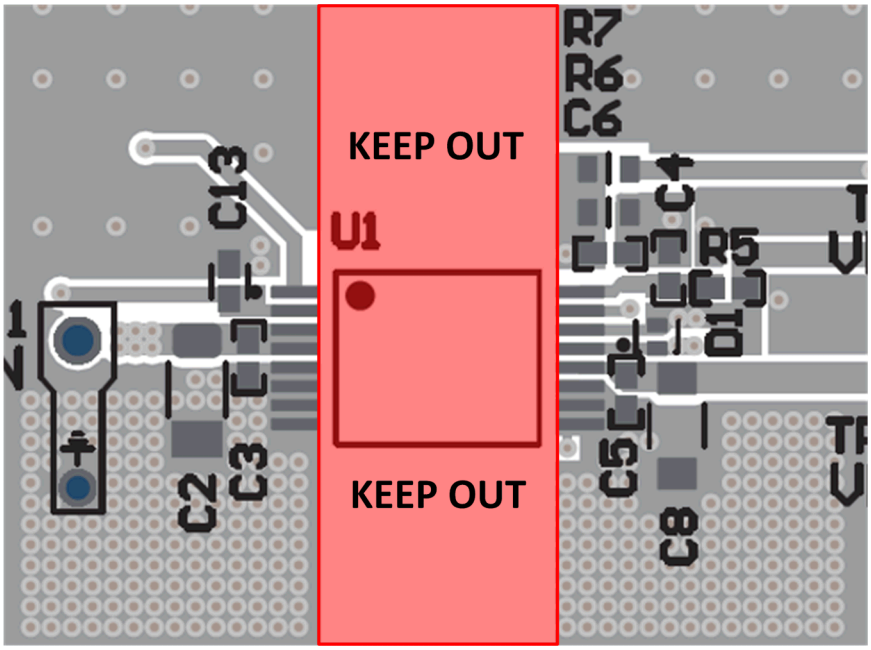


Figure 3-11. Isolation Keep Out Region

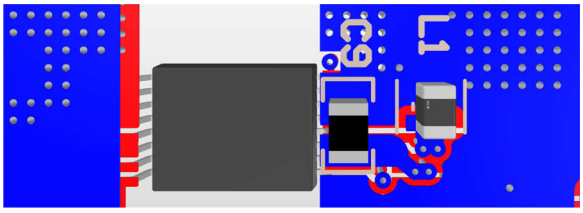


Figure 3-12. Bottom Side, Buck Boost, VEE LC Placement and Routing

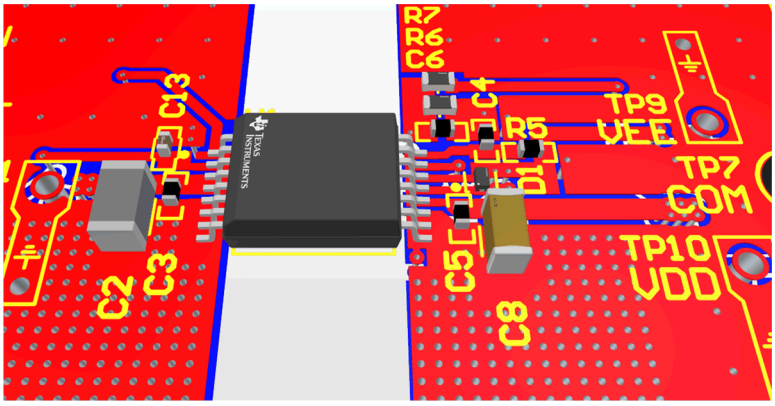


Figure 3-13. Top Side, Component Placement and Routing

3.5 Bill of Materials (BOM)

Table 3-1. Bill of Materials

Ref Des	Qty	Description	Part Number	Mfr
PCB1	1	Printed Circuit Board	HVP118	Any
C1, C3, C5	3	CAP, CERM, 0.1µF, 50V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	GCM155R71H104KE02D	MuRata
C2	1	CAP, CERM, 10µF, 35V, +/- 10%, X7R, AEC-Q200 Grade 1, 1206_190	CGA5L1X7R1V106K160AC	TDK
C4	1	CAP, CERM, 10pF, 50V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0402	CGA2B2C0G1H100D050BA	TDK
C6	1	CAP, CERM, 470pF, 50V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	CGA2B2X7R1H471K050BA	TDK
C8	1	CAP, CERM, 10µF, 25V, +/- 20%, X7R, AEC-Q200 Grade 1, 1206	CGA5L1X7R1E106M160AC	TDK
C9	1	CAP, CERM, 2.2µF, 16V, +/- 10%, X7R, 0805	C2012X7R1C225K125AB	TDK
C13	1	1µF ±20% 10V Ceramic Capacitor X7R 0402 (1005 Metric)	KAM05CR71A105MH	KYOCERA AVX
D1	1	Diode, 30V, 500mA, Surface Mount, DFN1006BD-2	PMEG3005ELS-QYL	Nexperia
H1, H2, H3, H4	4	Bumpon, Hemisphere, 0.44 X 0.20, Clear	SJ-5303 (CLEAR)	3M
J1, J3	2	Terminal Block, 2x1, 3.81mm, 24-16 AWG, 10A, 300VAC, TH	691214310002	Wurth Elektronik
J2	1	Header, 100mil, 3x1, Tin, TH	PEC03SAAN	Sullins
J4	1	Terminal Block, 3.5mm, 3x1, Tin, TH	691214110003	Wurth Elektronik
L1	1	3.3µH Shielded Drum Core, Wirewound Inductor 870mA 279mΩ	74404020033	Wurth Elektronik
L1-ALT	0	Inductor Power Shielded Wirewound 3.3uH 20% 100KHz Ferrite 0.88A 0.3Ω DCR T/R	NRV2010T3R3MGF	Taiyo Yuden
R1	1	RES, 10.0kΩ, 1%, 0.2 W, AEC-Q200 Grade 0, 0402	ERJPA2F1002X	Panasonic
R2	1	RES, 5.11kΩ, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW06035K11FKEA	Vishay-Dale
R5	1	RES, 49.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	ERJ-2RKF4992X	Panasonic
R6	1	2.4kΩ ±0.1% 0.1W, 0.1W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thin Film	ERA-3AEB242V	Panasonic
R7	1	12kΩ ±0.1% 0.1W, 0.1W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thin Film	ERA-3AEB123V	Panasonic
SH-J1	1	Shunt, 100mil, Gold plated, Black	SNT-100-BK-G	Samtec
TP1, TP6, TP8	3	Test Point, Multipurpose, Red, TH	5010	Keystone Electronics
TP2, TP3, TP7	3	Test Point, Multipurpose, Black, TH	5011	Keystone Electronics
TP4, TP5	2	Test Point, Multipurpose, Yellow, TH	5014	Keystone Electronics
U1	1	Automotive 2W, 12V-Vin, 25V-Vout, High Efficiency, High-Density, >5 kV_{RMS}, Isolated DC-DC Module	UCC35131QDHARQ1	Texas Instruments
C10, C11	0	CAP, CERM, 4.7µF, 35V, +/- 10%, X7R, AEC-Q200 Grade 1, 0805	CGA4J1X7R1V475K125AC	TDK
C12	0	CAP, CERM, 10µF, 35V, +/- 10%, X7R, AEC-Q200 Grade 1, 1206_190	CGA5L1X7R1V106K160AC	TDK
R3	0	RES, 100kΩ, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	ERJ-2GEJ104X	Panasonic
R4	0	RES, 330kΩ, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	ERJ-3EKF3303V	Panasonic

Trademarks

All trademarks are the property of their respective owners.

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2025) to Revision A (November 2025)	Page
• Updated Pin Configuration and Functions table	3
• Updated schematic	8
• Updated Bill of Materials	17

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025