

Technical White Paper

Measuring Output Noise for Ultra-Low Noise LDOs



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ABSTRACT

This technical white paper provides an outline for measuring noise for a low dropout regulator (LDO). This document also provides a solution for measuring noise for ultra-low noise LDOs. Current LDOs can have output noise levels substantially below the sensitivity for the vast spectrum analyzers available on the market. This document discusses the noise measurement basics of LDOs and options for measuring extremely, low-noise LDOs. The proposed solution is not *solely* limited to noise measurements intended for LDOs, the option can be used in many other types of measurement or sensing applications.

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1 Introduction to LDO Noise and Noise Measurement

1.1 LDO Noise and LDO Noise Representation

Noise that occurs in any electrical system as a purely physical phenomena can be defined as any undesirable voltage or current signal that interferes, distorts, or combines with the input or output of that system. Even if all external (extrinsic) noise sources are eliminated from coupling into a system (as the noise definition suggests), an internal (intrinsic) noise generates within the system. This intrinsic noise is present on the system output, and often, this intrinsic noise must be considered and measured. A simple system (device) like the LDO generates internal noise, which can be measured on the output. The noise of the LDO is a key specification in the datasheet, usually expressed over a frequency bandwidth (BW) of 10Hz–100kHz (typical). Further details on LDO noise can be found in the [References](#) [1] section. Graphs in the datasheet are often used to express the output noise of the LDO. [Figure 1-1](#) shows the output noise for a typical LDO.

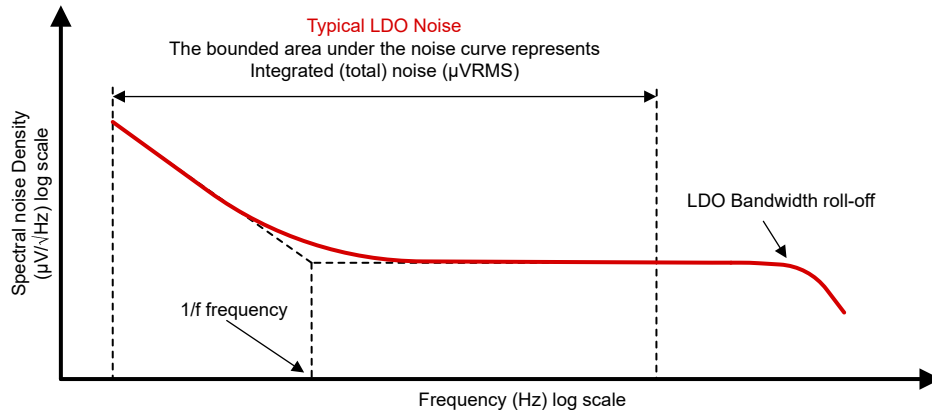


Figure 1-1. Typical Noise Graph for an LDO

Any point on the noise curve is recognized as the spectral noise density of the LDO at that frequency. At low frequency, the noise of the LDO is dominated by flicker noise, then the noise rolls-off at the 1/f frequency to a lower noise level—thermal noise—then the curve of the LDO noise rolls-off due to the BW of the LDO rolling-off. The total noise, or RMS, is an additional metric reported in the electrical characteristics table for the LDO, accompanied by the specific frequency BW. This RMS noise is simply the accumulated, integrated, spectral-noise density under the noise curve over a specific BW, typically 10Hz–100kHz in units of μVRMS .

1.2 Measuring LDO Noise Using a Spectrum Analyzer

A spectrum analyzer with a frequency BW wider than the BW of the LDO is usually used to measure the noise of the LDO. Similar to the LDO, the spectrum analyzer has internal noise referred to as the analyzer noise floor (sensitivity). The noise floor (technically called the displayed average noise level–DANL) of the analyzer is a key specification in the analyzer datasheet over the frequency BW of the analyzer. Measuring and notating the noise floor of the analyzer is critical before making any noise measurement, as explained in the [References](#) [2] section.

To measure the noise floor for any analyzer, simply run frequency sweeps with the lowest setting of resolution bandwidth (RBW) available for the analyzer at multiple averages across the desired noise measurement BW. The measured noise curve (noise floor) is the lowest noise the analyzer can resolve over that BW. By knowing this noise level, a determination can be made regarding using such an analyzer to measure the noise of the LDO (DUT noise).

To maintain a noise measurement accuracy greater than 95% for the BW operation of the LDO, the noise curve of the LDO must be 10dB higher than the noise floor curve of the analyzer, as shown in [Figure 1-2](#).

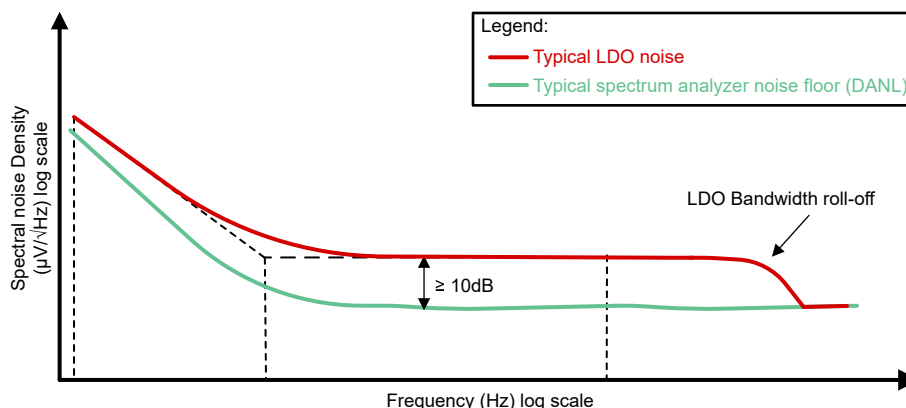


Figure 1-2. Typical LDO Noise Versus Typical Spectrum Analyzer Noise Floor

This 10dB (or 3.16V/V) of gain between the analyzer and the LDO noise achieves the 95% accuracy by combining the curves as two uncorrelated noise sources. If one source (the LDO) is 3.16 (V/V) higher than the other source (the analyzer), then the resulting total noise is more than 95% dominated by the higher source, as demonstrated in [Equation 1](#):

$$\begin{aligned} \text{Total Noise} &= \sqrt{(3.16)^2 + (1)^2} = 3.31; \\ \text{Measurement Accuracy} &= 100\% - \frac{(3.31 - 3.16)}{3.31} \times 100\% = 95.5\% \end{aligned} \quad (1)$$

The choice for 95% accuracy is reasonable for any noise measurement of an LDO, given the random nature of noise phenomena. A margin that is lower than 10dB results in a measurement that is less accurate at the BW roll-off of the LDO, as is obvious in [Figure 1-2](#). When the LDO noise (red curve) in [Figure 1-2](#) approaches the spectral analyzer noise floor (green curve), the noise measurement becomes incorrect and significantly dominated by the spectral analyzer noise. This flat noise is not the noise of the LDO, but rather, a combination of noise from the LDO and analyzer significantly dominated by the noise floor of the analyzer.

The internal circuitry of the analyzer can contribute to the measured DUT noise, however, the contributed noise is at or near the absolute minimum value of noise—174dBm/Hz. This extremely low noise level is the thermal noise level (power); the noise levels of the analyzer and LDO (DUT) are examined in detail in the next sections.

[Figure 1-3](#) shows the noise curve for an ultra-low noise LDO, which is more than 10dB lower than the noise floor of a typical spectrum analyzer. So, the question is—how can this ultra-low noise LDO be measured?

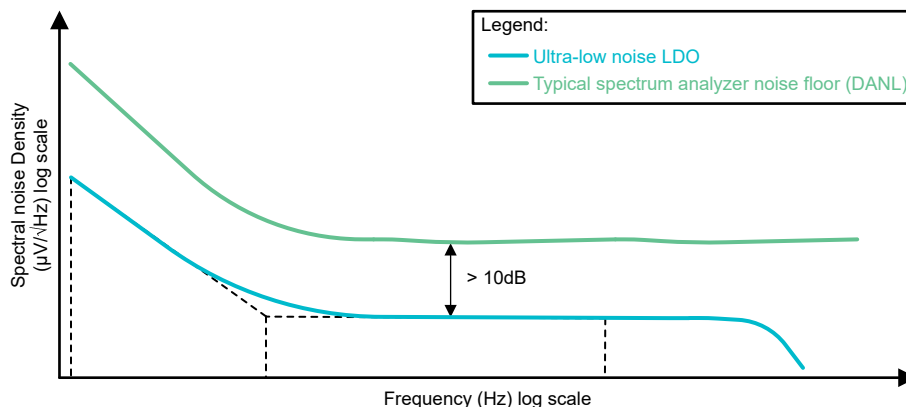


Figure 1-3. Ultra-Low Noise of the LDO Versus the Noise Floor of a Typical Spectrum Analyzer

The solution is relatively simple—an amplifier that can gain-up the noise of the LDO to 10dB (or higher) above the noise floor of the analyzer so we can measure the LDO noise. Few spectrum analyzers have a built-in preamplifier for these types of low-noise signals, but preamplifiers are often gain-limited to less than 40dB and the BW for those preamplifiers often starts at 1kHz or higher.

But what if more gain is necessary and the measurement must start at a lower frequency?

The next section discusses the design requirements for a higher gain amplifier with a BW of 10Hz–10MHz.

2 Solution for Measuring an Ultra-Low Noise LDO (Noise Amplifier Requirements)

Note

Before diving into the design details of the noise amplifier, take time to consider how the noise of the amplifier combines with the noise of the LDO and analyzer, as discussed earlier.

Since the noise of the analyzer is already higher than the noise of the LDO by a significant margin (as shown in [Figure 1-3](#)), the noise of the LDO and the amplifier can be safely considered first. Once the noise of the required amplifier is determined, then we can consider the necessary amplifier gain second.

2.1 Estimating the Maximum Noise for the Amplifier

The starting point for the design of the amplifier is the output noise of the LDO, the DUT. Recent advancements in silicon process technology enable Texas Instruments to deliver an ultra-low noise LDOs. A spectral noise density of 1.3–1.1nV/Hz at 1kHz, and 1nV/Hz (or lower) at 10kHz, can be identified by examining the noise levels of such LDOs. These noise levels are comparable to noise levels offered by *current* top performing operation amplifier (op-amp) devices. Working back from these levels (using the 10dB margin discussed earlier) an amplifier with input reference noise levels of $\approx 350\text{pV/Hz}$ and 250pV/Hz at 1kHz and 10kHz, respectively, is necessary, as the 10dB margin suggests. These noise levels equate to noise levels for a transistor (not taking into considering the required BW measurement, which is from 10Hz up to 10MHz for a typical LDO).

Fortunately, similar—and possibly lower—noise levels are achievable by stacking parallel op-amp stages, as discussed in the [References](#) [3] section. Therefore, select an op-amp with the lowest noise available to achieve a lower equivalent input voltage (EIVN) and equivalent input current noise (EICN), respectively. The selected op-amp must have a wide enough BW to accommodate the required gain over the noise measurement BW.

Texas Instruments offers plenty of low-noise op-amps. This design requires the lowest amount of noise and the widest amount of BW to accommodate the requirements of the design. Therefore, an op-amp with a noise level of 700pV/Hz to 950pV/Hz at 1kHz is a good potential candidate. Another required feature of the amplifier design is that the op-amp must have a very low 1/f noise level at 1kHz.

Using the parallel op-amp technique (discussed in the [References](#) [3] section) and an op-amp with roughly 800pV/Hz of noise results in roughly ten parallel stages, as shown in the [Equation 2](#):

$$\text{Number of stages } \left(N \right) = \left(\frac{800 \left(\frac{\text{pV}}{\text{Hz}} \right)}{250 \left(\frac{\text{pV}}{\text{Hz}} \right)} \right)^2 = 10.24 \quad (2)$$

The results from simulation and prototyping found that ten stages maintains a margin of more than 10dB against parasitic and components tolerance without significantly complicating the circuit design of the amplifier.

2.2 Estimating the Amplifier Needed Gain

This section returns to the required gain for the amplifier design. If the DANL is examined for a typical spectrum analyzer (BW over 1kHz–100kHz), a typical DANL is found to be close to -120dBm/Hz (224nV/Hz), a noise of 10dB or higher results in approximately -110dBm/Hz or 708nV/Hz . Using this level, along with a noise of approximately 1nV/Hz for the LDO, you achieve a gain of approximately 708(V/V).

$$\text{The roughly estimated amplifier gain} = 20 \times \log(708) = 57\text{dB} \quad (3)$$

This estimate is a rough estimate for the minimum gain value for our design. This minimum gain value is much higher than the 40dB of gain that only a few analyzers offer with a preamplifier.

Figure 2-1 shows the proposed amplifier circuit.

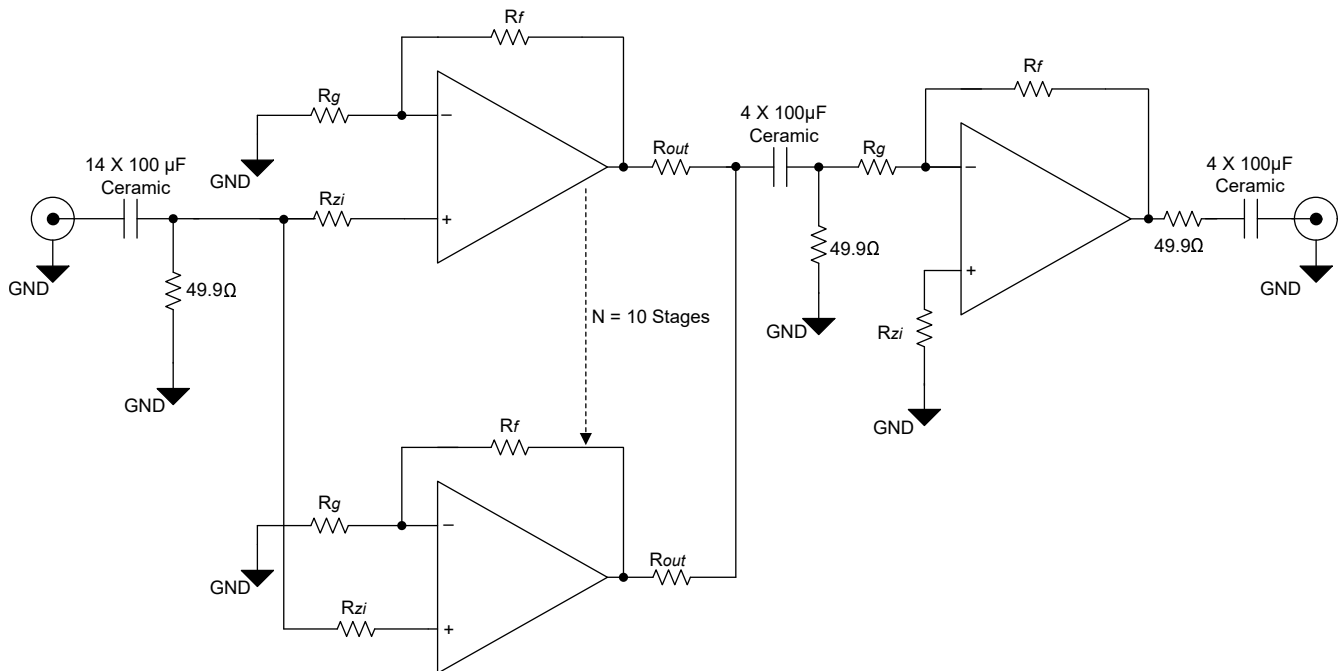


Figure 2-1. The Proposed Amplifier Circuit

To maintain a flat gain response over the BW measurement of 10Hz–10MHz, the total necessary amplifier gain (of roughly 70dB, adjusted above the minimum value of 57dB) is carried out by two series of stages. The first stage, which is strictly in a non-inverting configuration, carries most of the gain to quickly raise the noise of the LDO (DUT) to a higher level. The second stage, which is in an inverting configuration, is used to fine-tune the total gain of the amplifier.

2.3 Selecting the Amplifier Circuit Feedback Resistor Values

The proposed amplifier circuit mentioned in the previous section utilizes the same op-amp device across the series and parallel stages for performance, design simplicity, and design cost savings. To leverage the ultra-low noise performance of the op-amp, very small feedback resistor values must be used.

Examine the noise analysis shown in Figure 2-2 for a non-inverting op-amp device.

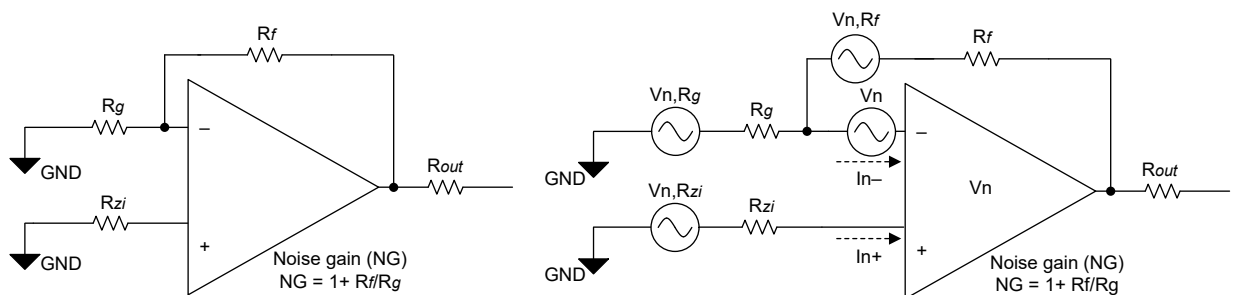


Figure 2-2. Noise Analysis for a Non-Inverting Op-Amp Device

V_n : Represents the op-amp voltage noise.

V_n, R_x : The voltage noise generated by each resistor in the circuit. This voltage noise can be calculated using Equation 4:

$$V_n, R_x = \sqrt{4KTR} \quad (4)$$

where K is Boltzmann constant = 1.380649×10^{-23} (1/K°), K is the temperature in Kelvin.

$I_{n\pm}$: Represents the thermal noise generated by the op-amp currents flowing in either input resistor.

Equation 5 can be used to calculate the noise of the op-amp input currents.

$$I_{n\pm} = (I_{n\pm})^2 \times R_x^2 \quad (5)$$

Using the non-inverting op-amp noise calculation from the [References](#) [4] section, you get the input referred noise (RTI) using Equation 6:

$$\text{Referred to input Noise (RTI)} = \sqrt{(V_n)^2 + 4KTR_{zi} + 4KTR_g \left[\frac{R_f}{R_f + R_g} \right]^2 + (I_{n+} \times R_{zi})^2 + \left(I_{n-} \times \left[\frac{R_g \times R_f}{R_g + R_f} \right] \right)^2 + 4KTR_f \left[\frac{R_f}{R_g + R_f} \right]^2} \quad (6)$$

If the thermal noise equation for a resistor ([Equation 4](#)) is used to draw a plot with resistance on the x-axis and noise on the y-axis, the outcome is shown in [Figure 2-3](#).

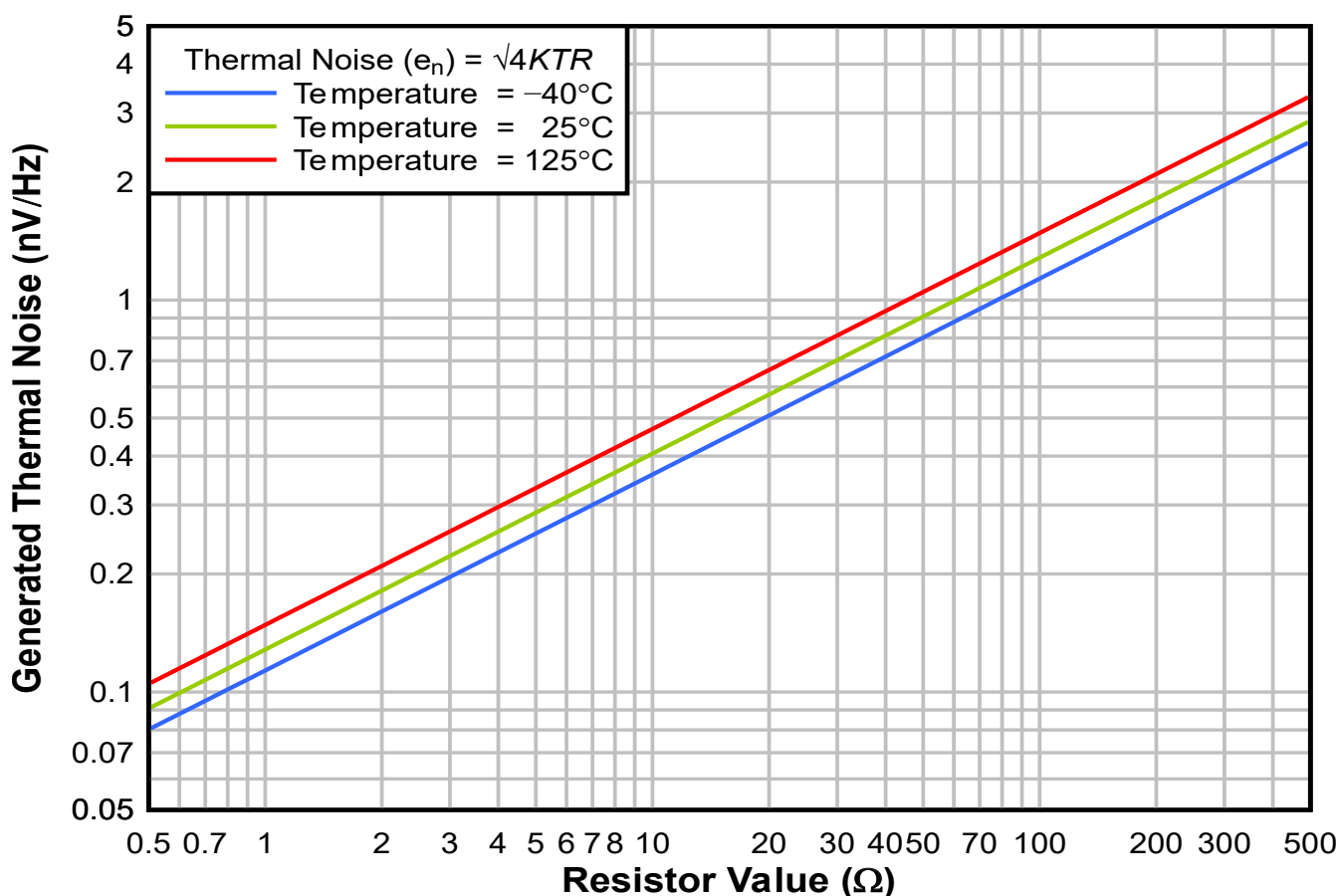


Figure 2-3. Thermal Noise for a Resistor

Figure 2-3 shows that a 50Ω resistor, sitting at room temperature, generates thermal noise that equals the noise of a $900\text{pV}/\text{Hz}$ op-amp at 1kHz . In this amplifier design, selecting very small values for the feedback resistors is critical since these type of resistors generate thermal noise that can exceed the noise for the selected op-amp. By examining Equation 6, recognize that the resistor values of R_{z_i} , R_g , and R_f can contribute significant noise when the values are large values compared to the noise of the op-amp. Selecting resistor values that make the noise of the op-amp the dominate noise source in Equation 6 is required for this particular design to work. The R_{z_i} and R_g values of the resistors can have the same small value to balance the input currents of the op-amp, thus maintaining a minimum output offset voltage. The R_f value of the resistor can be relatively large to accommodate the significant gain for the first parallel stage as this stage carries most of the total gain of the amplifier circuit. Thin film resistors are preferred for this amplifier circuit as these resistors offer better stability, while maintaining lower noise, compared to thick film resistors.

The values of the feedback resistors for the second series stage are not that critical since the amplified signal (noise) is already higher than the noise of both the op-amp and the resistor. The package sizes for all the above mentioned resistors must be maintained to a small package size to reduce the parasitic capacitance beneath them.

2.4 The Amplifier Input/Output DC Blocking Filters

High-pass filters that block DC at the input of the amplifier, at the second series stage input, and at the input of the analyzer are used to eliminate any DC offset from creeping into the amplified noise signal. The input filter has a 3Hz cutoff frequency to enable a flat enough noise measurement from such low frequency if necessary. The remaining filters have 10Hz cutoff frequencies, as required by the BW noise measurement of the LDO.

Tantalum capacitors are preferred for the filters blocking DC to the input of the amplifier, however, ceramic capacitors can be used despite the piezoelectric nature of these capacitors. In this design, ceramic capacitors are used since these capacitors maintain a neutral polarity attribute and have characteristically low ESR and ESL. This enables the use of the amplifier for both positive and negative LDOs. Placing the amplifier circuit in a vibration free, and RF immune, test enclosure can eliminate the adverse piezoelectric nature of such capacitors.

2.5 Verifying the Designed Amplifier Performance

Measuring the RTO noise and then calculating the RTI noise of the amplifier circuit is easy by knowing the NG. Figure 2-4 shows the measured amplifier versus the simulated RTO noise, RTI noise, and the measured noise floor of the HP4395A spectrum analyzer.

Note

Any spectrum analyzer with a noise floor lower than the RTO noise of the amplifier can be used with the proposed amplifier design.

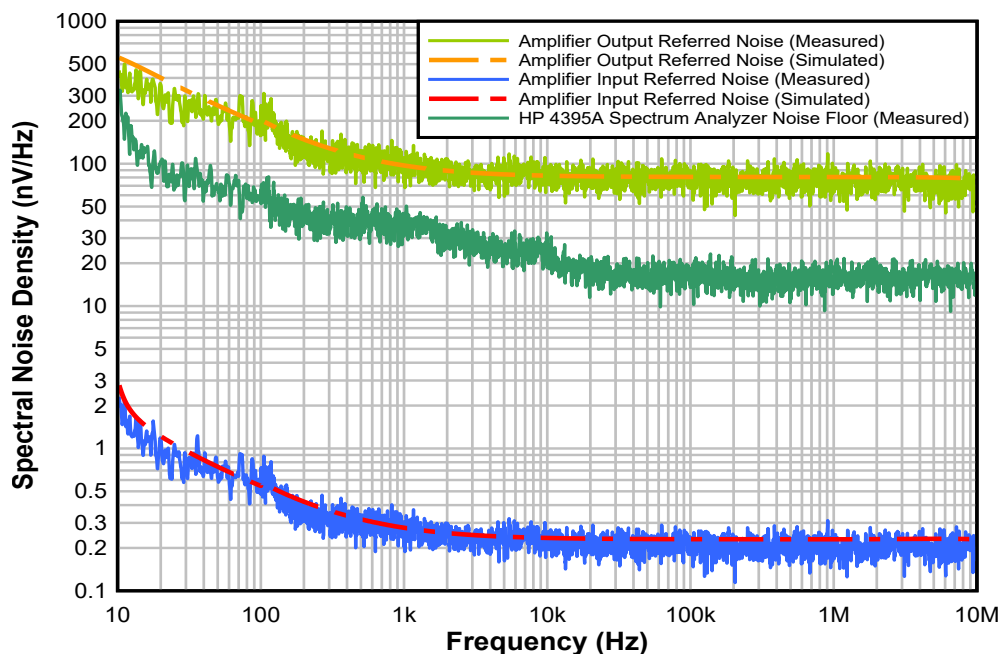


Figure 2-4. The Measured Amplifier Versus the Simulated RTO and RTI Noise

In Figure 2-4, the measured RTO noise curve of the amplifier matches the simulated RTO noise very well. The measured RTO noise of the amplifier is also 10dB above the measured noise floor of the spectrum analyzer (as required), which achieves a measurement accuracy of greater than 95%.

Similarly, the calculated RTI of the amplifier, from dividing the measured RTO noise by the NG, matches the simulated RTI noise well. The measured amplifier RTI noise is acting as the new (improved) noise floor for the LDO noise measurement.

Before making noise measurements of the LDO (DUT), TI recommends verifying another measurement to confirm the amplifier performance. A flat white noise generator like the NC6105A was used to generate a 10nV/Hz (-147dBm) flat noise across a BW of 10Hz–10MHz, then that noise was measured using this design. This very low-noise level is slightly lower than the noise floor of the HP4395A. Figure 2-5 shows the measured flat noise of 10nV/Hz.

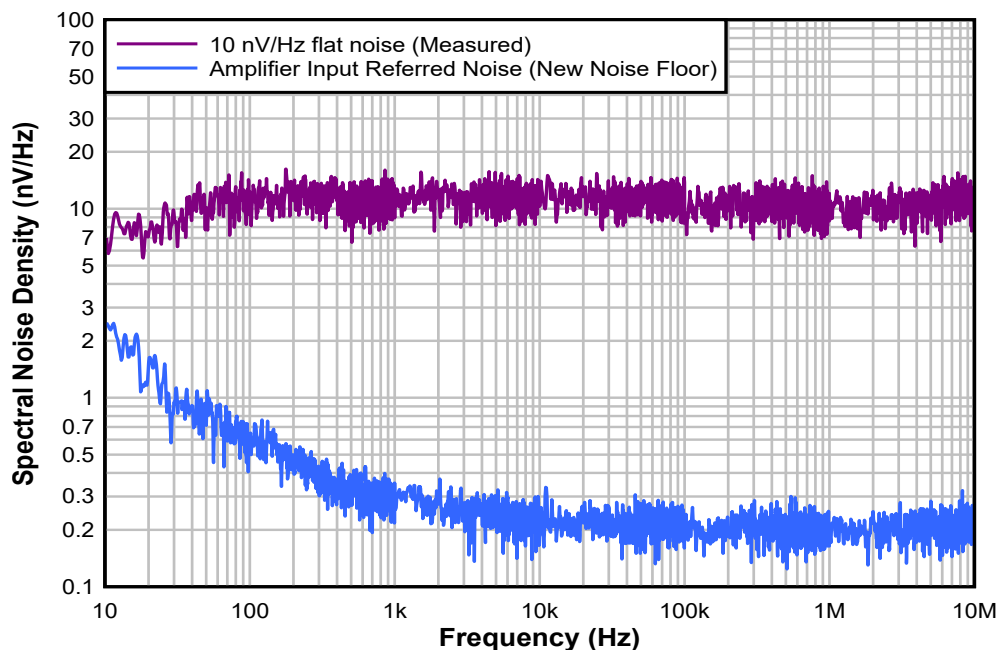


Figure 2-5. Measured Flat Noise of 10nV/Hz Across a BW of 10Hz–10MHz

A lower noise level can be measured using this amplifier (as low as 1nV/Hz and potentially 0.9nV/Hz), however, the input noise to the amplifier is lower than the noise of the actual amplifier (op-amp 1/f noise), below 1kHz, as shown in [Figure 2-6](#).

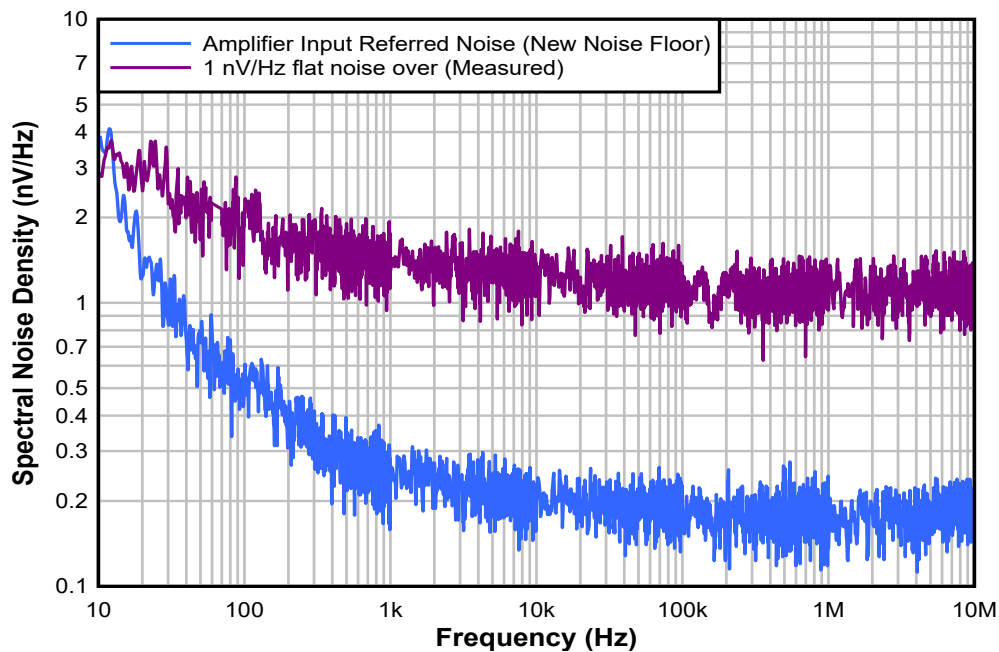


Figure 2-6. Measured Flat Noise of 1nV/Hz Across a BW of 1kHz–10MHz

3 Conclusion

This technical white paper discussed the noise measurement basics of LDOs while using a spectrum analyzer. The document also discussed the requirements to design an extremely low-noise amplifier circuit necessary for measuring the noise of an ultra-low noise LDO. The designed amplifier circuit benefits from the parallel op-amp technique discussed in the [References](#) [3] section to lower the input referred noise of the amplifier. This significant reduction in the input noise makes this amplifier design a vital tool for amplifying tiny signals within the BW of 3Hz–10MHz. Additionally, to improve the noise floor measurement for any spectrum analyzer, the amplifier circuit can also be used to improve the noise floor measurement of any network analyzer.

The use of a ceramic capacitor as a filter for blocking DC enables the amplifier to work with noise (tiny signals) that has a positive or negative offset voltage.

4 References

1. Texas Instruments, [LDO Noise Demystified](#), application report.
2. Keysight Technologies, [Understanding Noise and Sensitivity in Spectrum Analyzers](#), white paper, Keysight Technologies website (2000–2025), viewed 21 October 20025.
3. G. Scandurra, G. Cannatà, G. Giusi and C. Ciofi, 2013. [Configurable Low Noise Amplifier for Voltage Noise Measurements](#), *2013 22nd International Conference on Noise and Fluctuations (ICNF)*, Montpellier, France, 2013, pp. 1–4, doi: 10.1109/ICNF.2013.6578999.
4. Texas Instruments, [Noise Analysis in Operational Amplifier Circuits Application Report](#), application note.

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