Application Note

Active Current Sharing: Advanced Current Distribution Feature From TI's Smart eFuses

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ABSTRACT

eFuses are integrated power path protection devices which are increasingly being adopted to replace discrete front-end protection circuits in various applications, offering a compact and efficient design. eFuses cater to a wide range of currents up to 60A and voltages up to 80V. However, certain applications, such as servers and communication equipment, require significantly higher currents, often in the range of several tens to hundred of amperes. To address these demands, system designers frequently consider paralleling eFuses to scale the system for higher current requirements and improve thermal management. However, current distribution among parallel connected eFuses remains a challenge which leads to false system shutdown or reliability concerns. This application note introduces the Active Current Sharing (ACS) feature of TI eFuses and describes design and performance advantages using examples of four eFuses supporting a 80A load current and six eFuses supporting 100A load current.

Table of Contents

List of Figures

List of Tables

Trademarks

1 Introduction

Artificial intelligence (AI) advancements has led to an unprecedented surge in power and current consumption in AI-powered processors and servers. As AI models grow increasingly complex, requiring massive computational resources, power demands have skyrocketed. Modern AI processors, such as graphics processing units (GPUs) and tensor processing units (TPUs), consume significantly more power than the predecessors. AI-driven data centers and servers have seen a staggering increase in power consumption, with some estimates suggesting a 20-30% rise in energy usage over the past few years. This trend poses significant challenges for data center operators who must balance computational performance with energy efficiency, heat management, and environmental sustainability. To mitigate these concerns, researchers are exploring remarkable designs, including advanced cooling systems, low-power chip designs, and novel memory architectures, to make sure that AI's transformative potential is realized without compromising the planet's resources.

Figure 1-1 illustrates a 48V rack server architecture and a power distribution design commonly employed in data centers and server rooms to efficiently supply power to servers and other equipment. This architecture has gained widespread adoption due to the ability to minimize energy losses, maximize power density, and optimize overall system efficiency. TI's high-current eFuse family of devices, TPS1685, TPS1689, TPS25984, TPS25985, provide input power path protection to devices such as inrush current management, input under-voltage, input over-voltage, power up into output short, over-current, output hot-short, and so forth. eFuses are placed in between the PSU and the power stages of voltage regulator modules (VRMs) and other end loads.

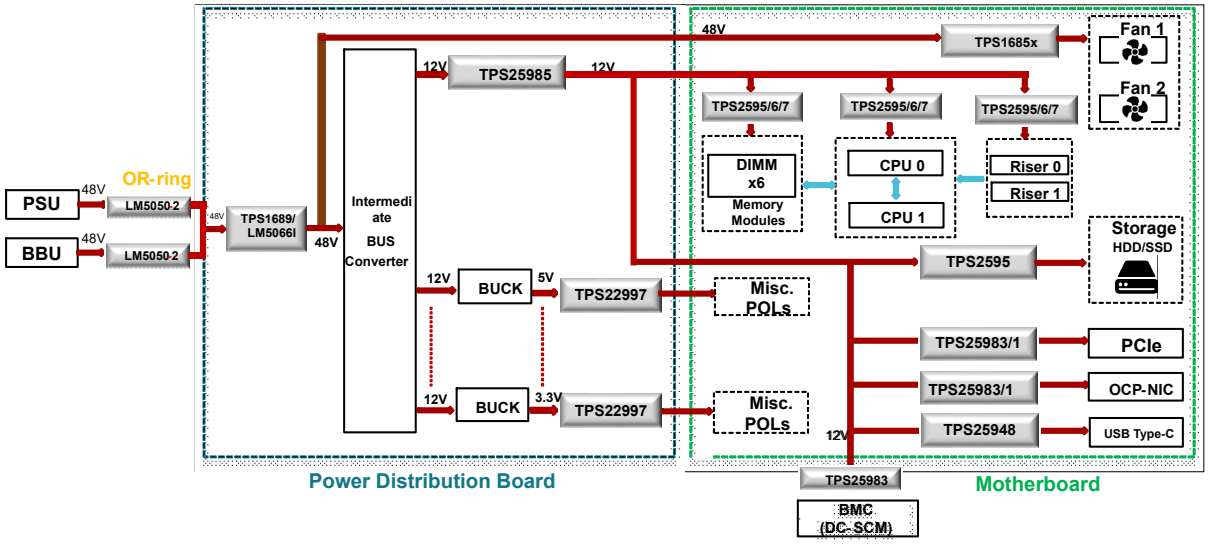

Figure 1-1. 48V Rack Server Architecture

2 Challenges for Stackable and Parallel Operation of eFuse

In this application, TPS1685 is considered for parallel operation. When eFuses are operated in a parallel configuration, current balancing among eFuses is a major challenge. A successful parallel operation makes sure of equal current balancing among the parallel-connected devices both under steady-state . Figure 2-1 shows the number of *N* eFuse devices connected in parallel configuration. The input and the output terminals are connected together.

Conventional stackable eFuses operate independently, each with a predefined trip threshold calculated by dividing the system's total threshold by the number of eFuses as shown in Equation 1. This decentralized approach means each eFuse is unaware of the status or actions of another eFuse.

$$I_{threshold} = \frac{I_{total}}{N} \quad (1)$$

In a setup, where the eFuses are exactly matched in specifications and the PCB trace resistance in each eFuse path is exactly equal, this design works well and trips exactly at the target system threshold. However, when the eFuses have mismatch in Rdson and the comparator thresholds or reference voltages along with PCB trace resistance mismatch, the eFuses with individual over current threshold can trip at different thresholds. The ones with lower Rds(on), path resistance and threshold trips sooner, even when the total system load current is below the over current threshold. This has an effect of lowering the total system over current threshold, which causes false tripping during normal operation.

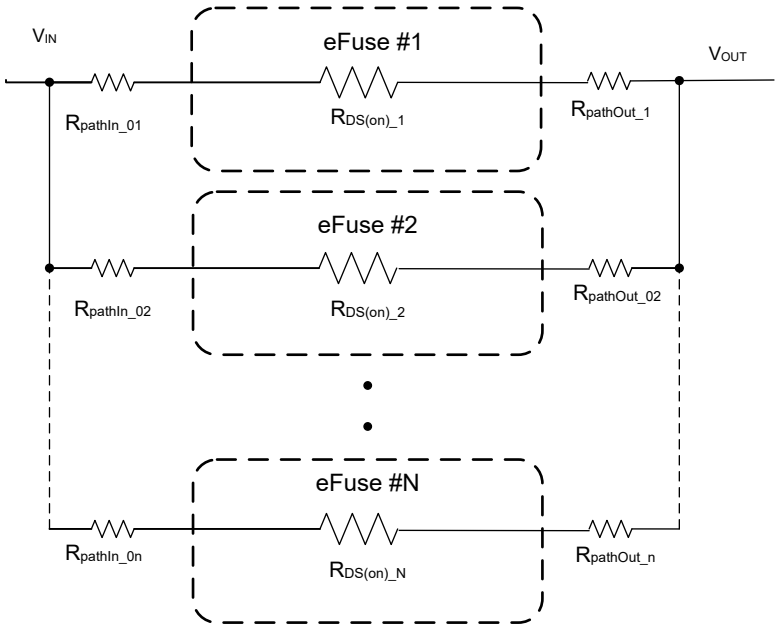

Figure 2-1. Number of *N* eFuse Devices Connected in Parallel Configuration

3 Techniques for Current Distribution in eFuse

In this section, different current distribution techniques are described with a system example to evaluate the system performance, long term reliability and effective current distribution.

Table 3-1 shows a system example of 58V voltage rail application with four TPS1685 eFuses connected in parallel to support 80A load current. Different path impedance is introduced in each eFuse path to create a realistic mismatch in $R_{DS(on)}$ and path impedance because of mismatch in trace length.

Table 3-1. Design Parameter

Design Parameter	Example Value
Input voltage range (VIN)	58V
Maximum DC load current (IOUT (max))	80A
Number of eFuse in parallel	4
Maximum output capacitance (CLOAD)	3mF
$R_{DS(on)}$	3.65mΩ
Path impedance_1	0Ω
Path impedance_2	0.5mΩ
Path impedance_3	0.5mΩ
Path impedance_4	1mΩ
Ambient temperature	25°C

3.1 Parallel Operation with Individual eFuse Over Current Limit

Figure 3-1 shows four eFuses with 20A individual over current threshold connected in parallel to share 80A load current in a 58V server voltage rail. During steady-state operation, the current sharing is decided by the $R_{DS(on)}$ mismatch among the parallel-connected eFuse devices. The device that has the lowest drain to source resistance ($R_{DS(on)\_min}$) shares the highest current (IMAX) than the rest of the devices. Realistic path impedances are introduced as shown in Table 3-1 to show the current distribution in eFuse.

Current through each eFuse can be calculated by using Equation 2.

$$I_{eFuse\_N} = I_S \times \frac{R_{Total\ system}}{R_N} \quad (2)$$

Table 3-2. Current Distribution in Four eFuses Connected in Parallel

eFuse	Effective Resistance (RDS_ON+path Resistance)	Current Distribution
eFuse_1	3.65mΩ	22.57A
eFuse_2	4.15mΩ	19.85A
eFuse_3	4.15mΩ	19.85A
eFuse_4	4.65mΩ	17.72A

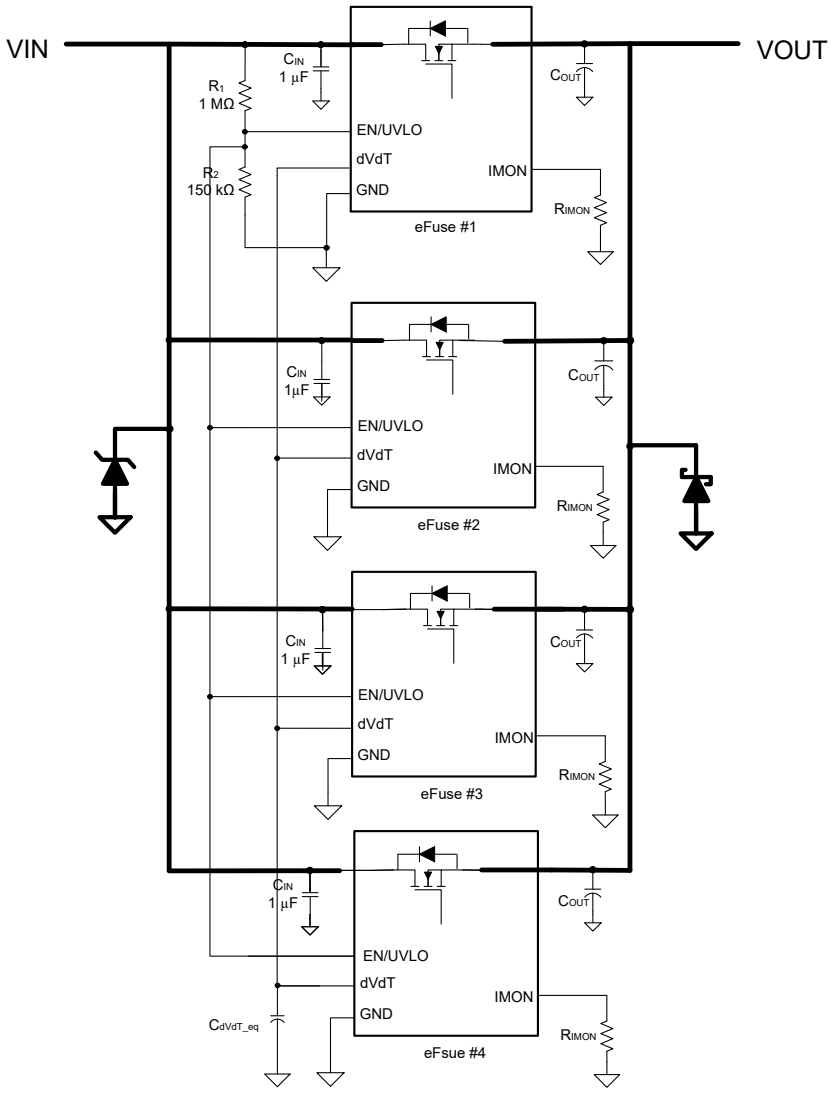

Figure 3-1. eFuse Devices Connected in Parallel with Individual Over Current Limit to Support 80A Load Current

As per effective resistance and current distribution shown in Table 3-2, eFuse_1 can be seen taking more than 20A current which trips the first eFuse, and subsequently trips the other connected eFuses in parallel. Hence, system gets shutdown much below 80A.

Limitations

To mitigate eFuse inaccuracy, system designers must choose between:

1. **Overdesigning the Power Supply (PSU)**

   Increasing the system trip threshold to accommodate potential eFuse errors results in an oversized power supply unit (PSU), leading to wasted resources, higher production costs, increased power consumption, reduced system efficiency and the need for additional components such as more eFuses in parallel to make sure of safe operation.
2. **Limiting System Performance**

   Capping the load below the system trip threshold to prevent false tripping. Artificially limiting system capabilities to accommodate eFuse inaccuracy which leads to lower system throughput and inferior performance.

3.2 Parallel Operation with Total System Over Current Limit

To avoid the problem stated in Section 3.1, TI's eFuse devices use a new method for overcurrent protection. These eFuses devices rely on the total system current instead of individual device current. All the IMON pins are tied together to R_{IMON_eq} to set the total system current as shown in Figure 3-2. This eliminates the problem of lowering of the overcurrent threshold due to mismatches between the devices and paths.

Keeping the system trip threshold higher than the system maximum current avoids unwanted eFuse tripping. However, current distribution through eFuse is unequal as shown in Table 3-2. eFuse_1 continues carrying higher current than the eFuse operating current.

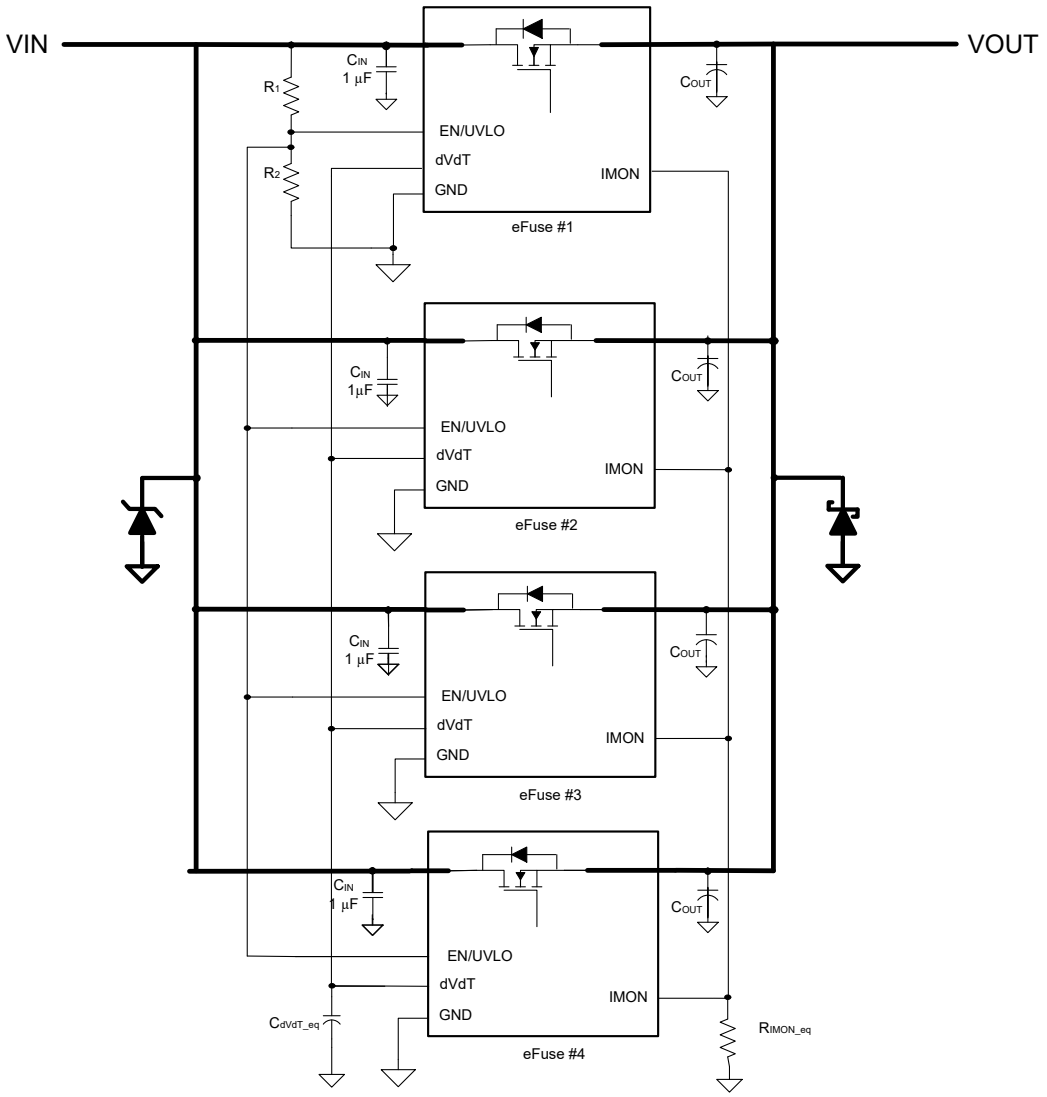

Figure 3-2. eFuse Devices Connected in Parallel with Common Over Current Limit to Support 80A Load Current

To evaluate the performance, load current is increased in steps of 2A as shown in Figure 3-3. Due to mismatch in path resistance, eFuses can be seen carrying unequal current distribution. In Figure 3-3, currents through each eFuses are kept higher so device does not go into ACS.

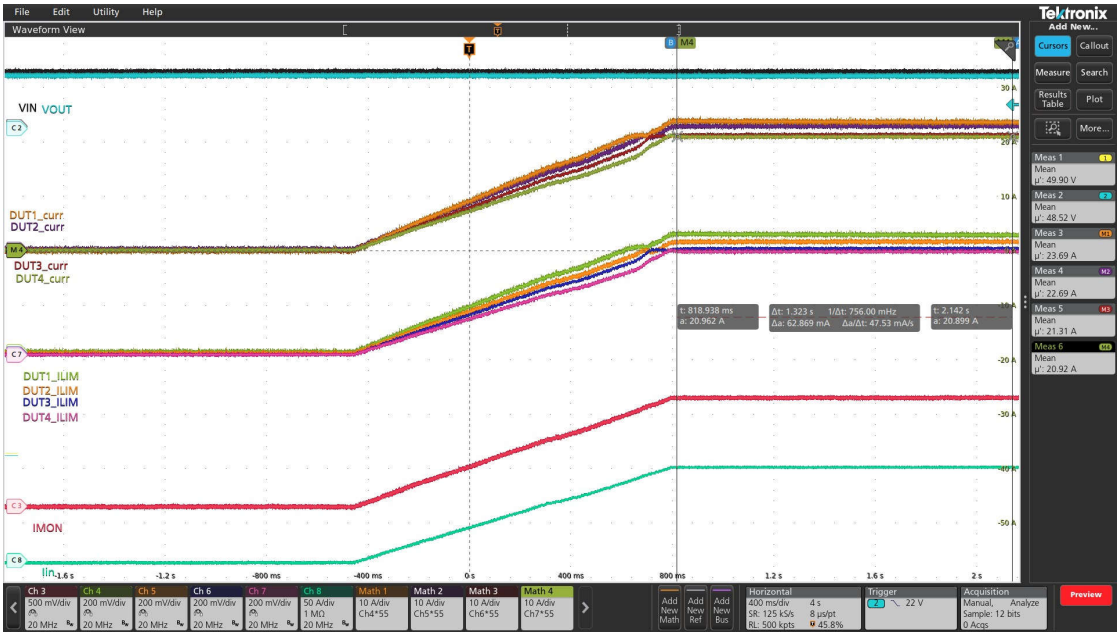

Figure 3-3. Current Sharing Among Four eFuses Without ACS

Note

TPS1685 ACS is described in Section 3.3, and can be disabled by keeping the ACS threshold much higher than individual current rating of eFuse. TPS1685 design calculator can be used to determine the R_{ILIM} value.

Limitations

Unequal Current Sharing Among eFuses

When eFuse devices are operating at the max rated current, unequal current distribution among individual eFuses lead to varying stress levels. With those eFuse devices carrying higher currents face increased thermal and electrical stress. This can cause premature failure, overheating, and degradation, potentially exceeding rated currents in PCB traces or vias. As a result, system reliability is reduced, maintenance costs increase, and potential system downtime occurs, ultimately shortening the PCB's lifespan.

3.3 Parallel Operation with Active Current Sharing (ACS)

To solve the problem stated in Section 3.2, TI eFuses implement ACS, which is triggered when the current crosses a certain threshold. The active current sharing loop works by regulating the Rdson of the FETs. The eFuse carrying higher current increases the Rdson slightly to reduce current and allow other devices in the chain to take higher current, thus achieving redistribution or balancing of the current.

Setting ACS threshold low can increase the overall resistance in the path, which increases the power loss or self-heating unnecessarily at lower currents. At the same time, this does not yield any benefit in terms of long-term reliability.

The active current sharing threshold needs to be set at the maximum rated DC current for each device. The best choice is to set this close to the overcurrent protection threshold of each device. Note, that this is the overcurrent threshold which is not affected by the mismatches. This makes sure that once the system load current start approaching the max DC current, the active current sharing kicks in. This is particularly helpful from a long-term reliability perspective if the system is operating in this region for extended periods of time. Once the load current increases further beyond this point (during load transients or faults), the active current sharing loop is deactivated and the device relies on the overcurrent protection circuit (with blanking timer) instead.

Current threshold where the device goes into active current sharing depends upon VREF and RILIM value. TPS1685 design calculator can be used to determine R_{IREF} , V_{IREF} and R_{ILIM} value.

Equation 3 is used to determine RILIM resistance based on ACS threshold.

$$R_{ILIM} = \frac{1.1 \times V_{IREF}}{3 \times G_{ILIM} \times I_{LIM(ACS)}} \quad (3)$$

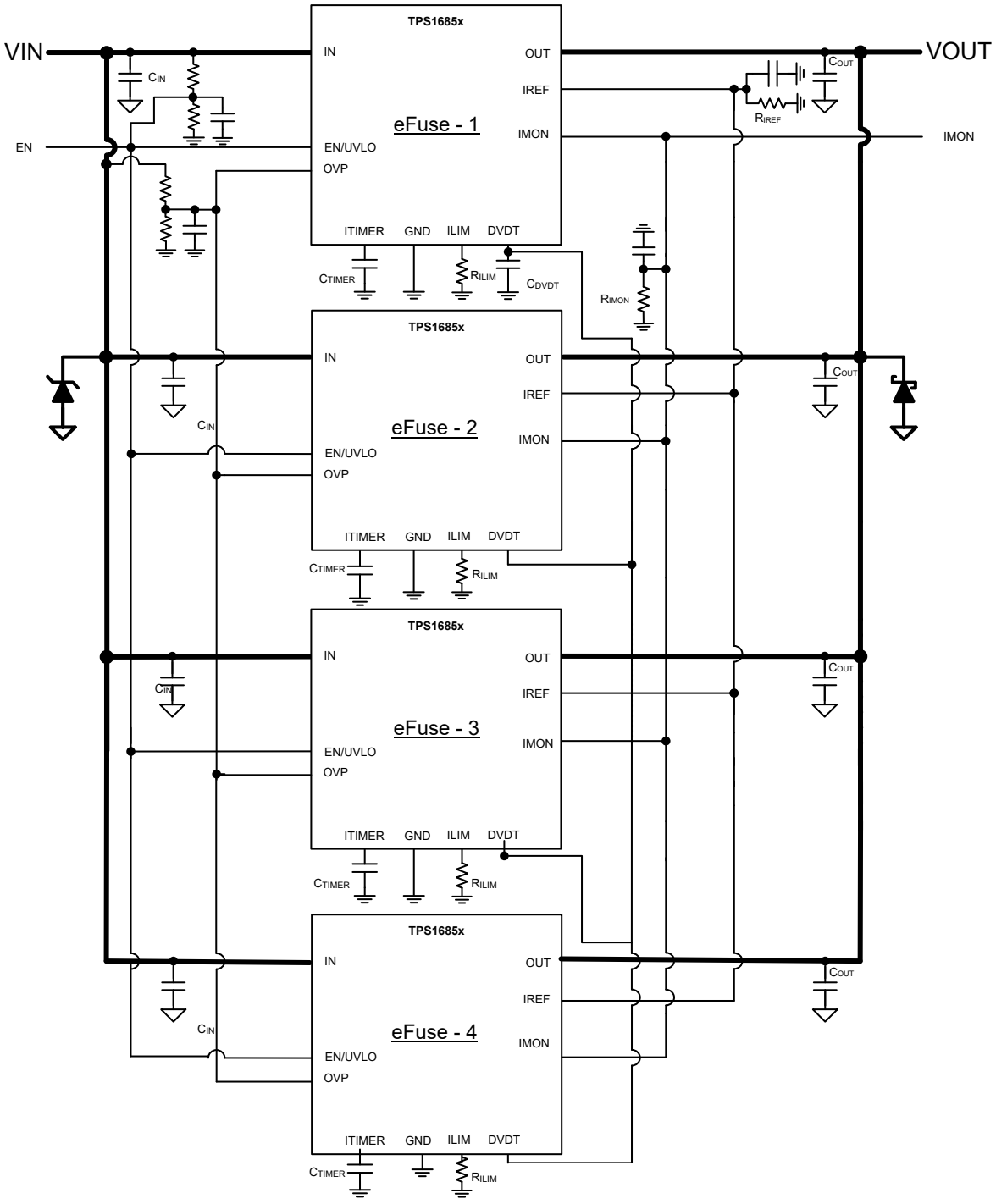

Figure 3-4. eFuse Devices Connected in Parallel with Common Over Current Limit and ACS to Support 80A Load Current

To evaluate the performance, load current is increased in steps of 2A as shown in Figure 3-5. Due to mismatch in path resistance, eFuses can be seen carrying unequal current distribution initially during the current step. Current through individual eFuse can be seen converging together with ACS.

This waveform is taken with system parameters as discussed in Table 3-1.

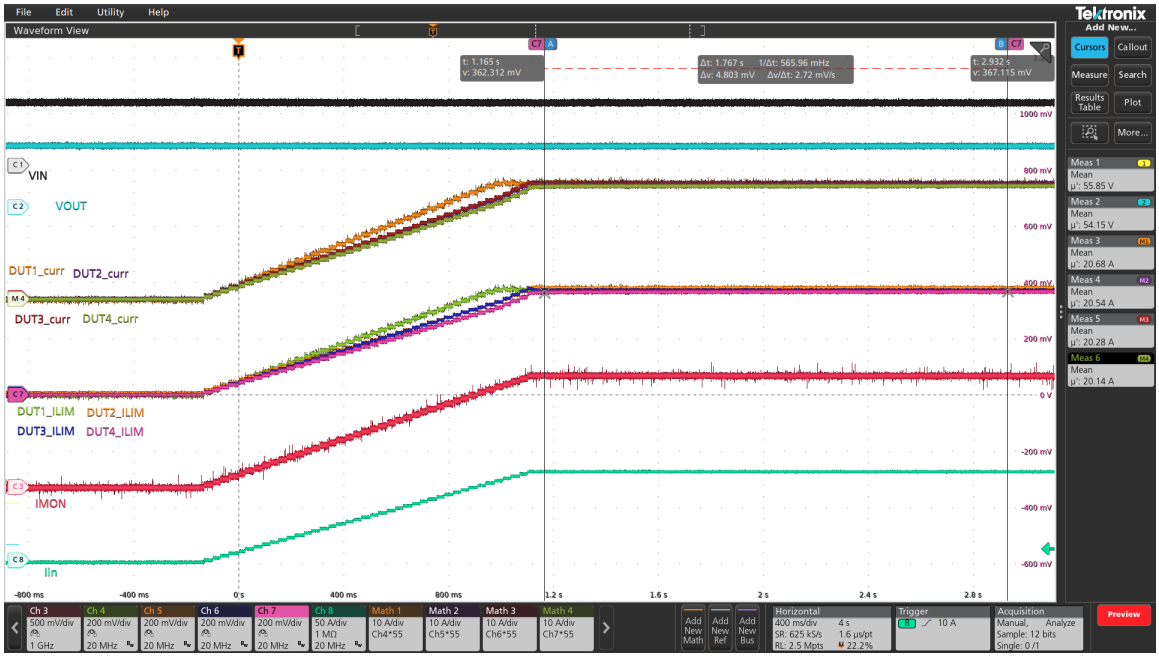

Figure 3-5. Current Sharing Among Four TPS1685 eFuses with ACS

The TPS1685x implements a proprietary current balancing mechanism during start-up, which allows multiple TPS1685x devices connected in parallel to share the inrush current and distribute the thermal stress across all the devices. This feature helps to complete a successful start-up with all the devices and avoid a scenario where some of the eFuses hit thermal shutdown prematurely. This increases the inrush current capability of the parallel chain. The improved inrush performance helps to support very large load capacitors on high current platforms without compromising the inrush time or system reliability.

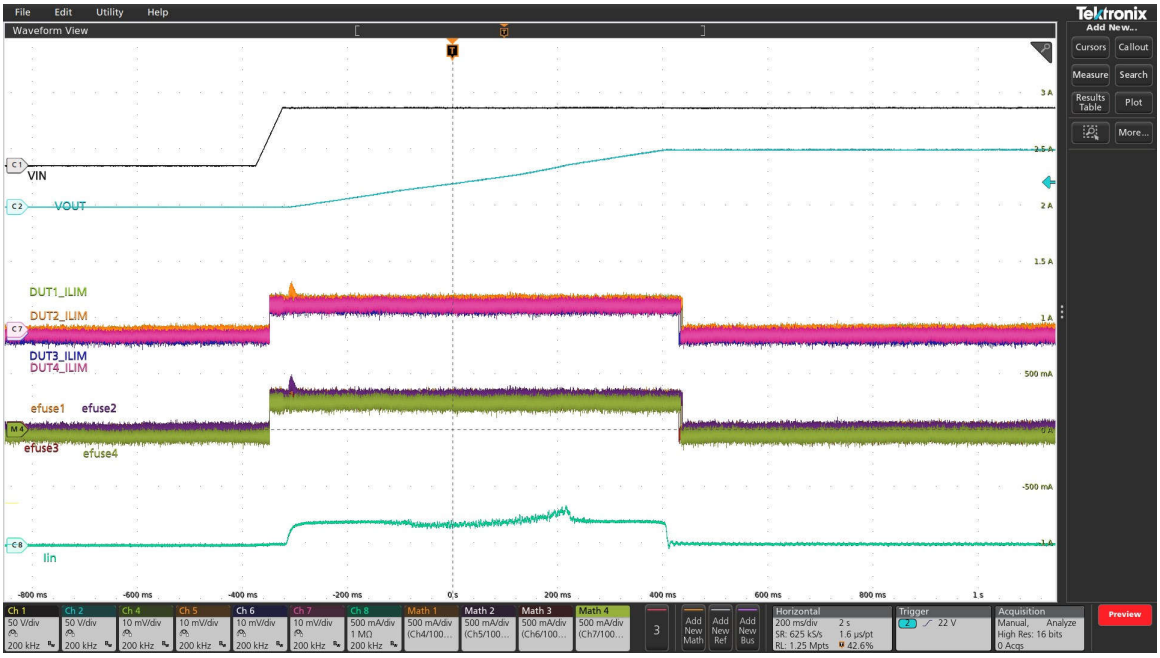

Figure 3-6. Current Distribution Among Four TPS1685 eFuses During Start-up

Current Distribution in Six eFuse Devices in Parallel with ACS

This example discusses six TPS1685 eFuses connected in parallel with a 100A system current requirement. From the TPS1685x 9V–80V, 3.65mΩ, 20A Stackable Integrated Hotswap (eFuse) With Accurate and Fast Current Monitor data sheet, the typical $R_{DS(on)}$ is 3mΩ and can be as high as 6mΩ. Table 3-3 shows an example of $R_{DS(on)}$ variation among six eFuses devices connected in parallel with max system current of 100A . Current distribution among eFuses can be seen in Table 3-3 . eFuse_1 current can be as high as 23.07A, which is 15% higher than the recommended operating current of eFuse.

ACS (Active Current Sharing) adjusts the $R_{DS(on)}$ of the high current devices to evenly distribute current. The ACS threshold for this current can be set using TPS1685 design calculator. The following are the individual eFuse currents if ACS is enabled and the ACS threshold of the devices are set to 20A. Table 3-4 shows the RDS(on) variation and current distribution with ACS. There is no change in RDS(on) of eFuse_2, eFuse_3, eFuse_4 , eFuse_5 and eFuse_6, while RDS(on) of eFuse_1 is increased by 30% to make the current distribution more uniform. With ACS, current on eFuse_1 is reduced from 23.07A to 18.57A and stress is redistributed evenly and eFuse_1 life time is improved by around 2x (can be computed by using Black's equation). This results in 2x effective system lifetime improvement, considering the first point of failure decides the system reliability.

Table 3-3. Current Distribution Among Six TPS1685 eFuses with $R_{DS(on)}$ Variation

eFuse_N	eFuse_1	eFuse_2	eFuse_3	eFuse_4	eFuse_5	eFuse_6
$R_{DS(on)}$	0.0035Ω	0.0055Ω	0.005Ω	0.0045Ω	0.006Ω	0.0055Ω
Max current	**23.07A**	14.7A	16.15A	17.9A	13.46A	14.7A

Table 3-4. Current Distribution Among Six TPS1685 eFuses with $R_{DS(on)}$ Correction Through ACS

eFuse_N	eFuse_1	eFuse_2	eFuse_3	eFuse_4	eFuse_5	eFuse_6
$R_{DS(on)}$	0.00455Ω	0.0055Ω	0.005Ω	0.0045Ω	0.006Ω	0.0055Ω
Max current	**18.75A**	14.7A	15.5A	17.06A	14.2A	15.5A

4 Summary

Parallel eFuse configuration also helps system designers do better thermal management as the power loss is spread across multiple devices. In this application note, four TPS1685 devices and six TPS1685 devices parallel operations with Active Current Sharing (ACS) are described to meet 80A and 100A current distribution and protection. However, the approach can be easily extended for other current levels.

5 References

1. Texas Instruments, Achieve 20A Circuit Protection and Space Efficiency Using Paralleled eFuses, application report
2. Texas Instruments, TPS1685x 9V–80V, 3.65mΩ, 20A Stackable Integrated Hotswap (eFuse) With Accurate and Fast Current Monitor, data sheet
3. Texas Instruments, TPS25985x 4.5V – 16V, 0.59mΩ, 80A Stackable eFuse with Accurate and Fast Current Monitor, data sheet

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