Application Note

Boost Behaviors When Vout Drops Below Vin: Start-up and Output Short Protection

Travis Wang, Shelly Xie

ABSTRACT

The boost converter is capable of producing a DC output voltage higher than the input voltage. For common nonsynchronous boost converters, there is a risk that when the output voltage is below input during start-up or output short conditions, the high-side diode can always be forward biased and the current can be out of control.

To overcome these drawbacks of the nonsynchronous boost converters, TI applies multiple control strategies and topologies to limit the inductor current under start-up or output short conditions. This application note introduces different ways to achieve soft start-up and output short current limit.

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1 Introduction

For common nonsynchronous boost converters, the load (Vout) is connected to the input port through the high-side diode and the inductor when output voltage drops below the input, causing a big current spike through the device. Figure 1-1 depicts the device behavior when Vout drops below Vin.

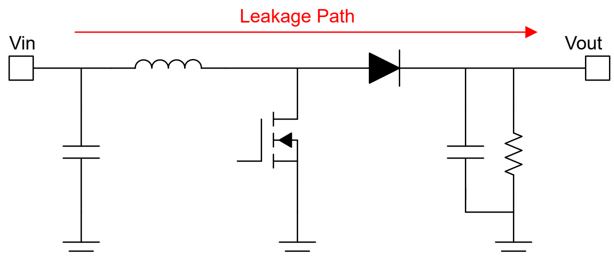

Figure 1-1. Common Nonsynchronous Boost Converter

Obviously, the network of Figure 1-1 does not allow control over inductor current. For the start-up process, the moment Vin is connected, the diode becomes forward biased, and there is a big inrush current into the output capacitor. For output short situations, Vin is shorted to GND through the leakage path, causing damage over the whole system.

To suppress this inrush current and achieve smooth current control under a Vin > Vout condition, TI applies multiple control strategies and topologies to limit the inductor current under start-up or output short conditions. This application note introduces behaviors of TI synchronous boost, which, with the application of switchable body diode or extra Isolated Field-Effect Transistor (ISO FET), is capable of controlling current when Vin > Vout during start-up and output short situation.

2 Start-up

2.1 Body Diode Pass

Similar to nonsynchronous boost converters, some older generations of synchronous devices like the TPS61088 cannot block the leakage path when Vin > Vout due to the body diode of the high-side switch.

The network in Figure 2-1 does not allow control over inductor current, in the same manner as nonsynchronous devices.

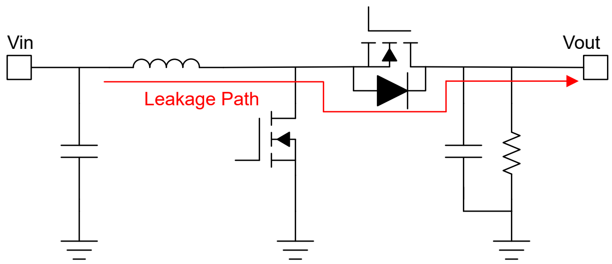

Figure 2-1. Body Diode Leakage Path

Taking a start-up situation as an example, when Vin is applied and the diode starts to conduct, Equation 1 expresses the state:

$$\begin{cases} L\frac{di_L}{dt} = -i_L \times DCR - V_o - V_D + V_{in} \\ C\frac{V_o}{dt} = i_L - i_o \end{cases} \tag{1}$$

For power supply or converter inputs, the slew rate of Vin is limited by the input capacitor and the input capability. Inrush current has a time constant far smaller than Vin rise time, so the system can be regarded as a ramp response as shown in Equation 2.

$$V_{in} = a \times t \tag{2}$$

Equation 3 shows the inductor current during this period.

$$i_L = \frac{at\left(DCR + R_o\right) - a\left(L - C_oR_o^2\right)}{\left(DCR + R_o\right)^2} + \frac{e^{-\frac{t\sigma_2}{2C_oLR_o}}\left(\cosh\left(\sigma_3\right) - \frac{C_oLR_o\sinh\left(\sigma_3\right)\left(\frac{DCRaC_o^2R_o^3 + 2aC_oLR_o^2 - aL^2}{\sigma_1} + \frac{\sigma_2}{2C_oLR_o}\right)}{\sigma_4}\right)\sigma_1}{C_oLR_o\left(DCR + R_o\right)^2} \tag{3}$$

where

- $$\sigma_1 = C_oL^2R_oa - C_o^2LR_o^3a \tag{4}$$
- $$\sigma_2 = L + C_oDCRR_o \tag{5}$$
- $$\sigma_3 = \frac{t\sigma_4}{C_oLR_o} \tag{6}$$
- $$\sigma_4 = \sqrt{\frac{C_o^2DCR^2R_o^2}{4} - \frac{C_oDCRLR_o}{2} - C_oLR_o^2 + \frac{L^2}{4}} \tag{7}$$

The design assumes an inductor with 1µH inductance and 25mΩ DC resistance (DCR). The Vin slew rate measures 20µs/V and output capacitance measures 88µF. Equation 8 calculates the current.

$$i_L = 3.10e^{-7.42 \times 10^5 t} - 3.10e^{-9.62 \times 10^3 t}\cos\left(7.55 \times 10^4 t\right) + 27.09e^{-9.62 \times 10^3 t}\sin\left(7.55 \times 10^4 t\right) + 4 \times 10^{-10} \quad (8)$$

That worst case happens when t = 30μs. The current spike can reach 7.43A. Figure 2-2 shows the waveform.

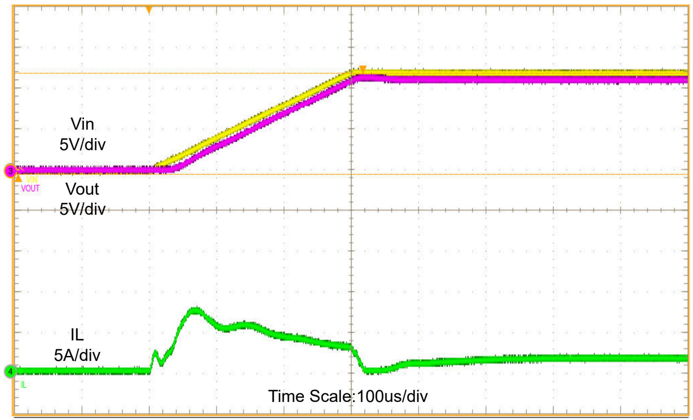

Figure 2-2. TPS61088 Inrush Current

According to the previous analysis ,a smaller C_{out} and a slower slew rate of V_{in} suppresses the inrush peak current. Assuming other conditions remains unchanged as Figure 2-2, the relationship between I_{Lpeak} with V_{in} slew rate and output capacitance is given by Figure 2-3.

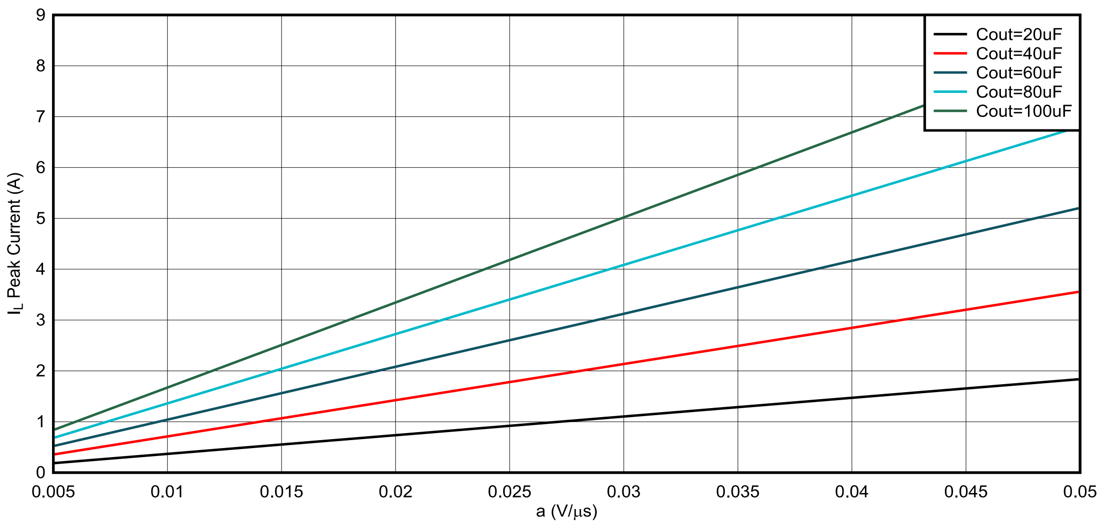

Figure 2-3. I_{Lpeak} With a and C_{out}

For battery input connected by a physical switch, the input capacitor, internal resistor of the battery and resistance of the physical contact point need to be taken into consideration.

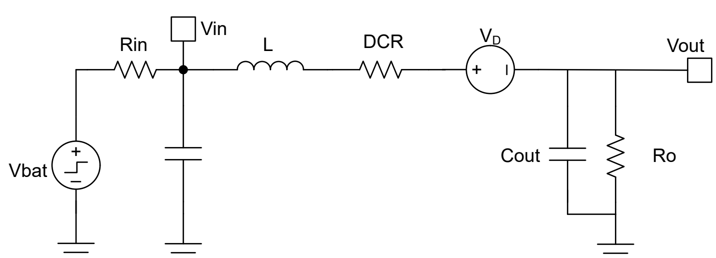

Figure 2-4. Battery Connect Equivalent Circuit

In Figure 2-4, the internal resistor of the battery and resistance of the physical contact point are depicted as R_{in}, while Vbat represents the open voltage of the battery. The diode forward voltage remains a small constant value and does not affect the inrush current. Neglecting VD, the equation of state can be expressed as Equation 9.

$$\begin{cases} L\frac{di_L}{dt} = V_{in} - i_L \times DCR - V_o \\ C_{in}\frac{dV_{in}}{dt} = (V_{bat} - V_{in})/R_{in} - i_L \\ C_o\frac{dV_o}{dt} = i_L - V_o/R_o \end{cases} \tag{9}$$

The inductor current during this period yields Equation 10.

$$i_L = \frac{V_{bat}}{DCR + R_{in} + R_o} - \frac{LV_{bat}\sigma 1}{DCR + R_{in} + R_o} + \frac{C_oR_o{}^2V_{bat}\sigma 1}{DCR + R_{in} + R_o} - \frac{C_{in}LR_{in}V_{bat}\sigma 2}{DCR + R_{in} + R_o} - \frac{C_oLR_oV_{bat}\sigma 2}{DCR + R_{in} + R_o} - \frac{C_{in}DCRR_{in}V_{bat}\sigma 1}{DCR + R_{in} + R_o} - \frac{C_{in}R_{in}R_oV_{bat}\sigma 1}{DCR + R_{in} + R_o} - \frac{C_{in}C_oLR_{in}R_oV_{bat}\sigma 3}{DCR + R_{in} + R_o} - \frac{C_{in}C_oDCRR_{in}R_oV_{bat}\sigma 2}{DCR + R_{in} + R_o} \tag{10}$$

where

- $$\sigma_1 = \sum_{n = 0 \text{ to } 3} e^{tz(n)}/\sigma_{4(n)} \tag{11}$$
- $$\sigma_2 = \sum_{n = 0 \text{ to } 3} z_{(n)}e^{tz(n)}/\sigma_{4(n)} \tag{12}$$
- $$\sigma_3 = \sum_{n = 0 \text{ to } 3} z_{(n)}^2e^{tz(n)}/\sigma_{4(n)} \tag{13}$$
- $$\sigma_{4(n)} = L + C_{in}DCRR_{in} + C_oDCRR_o + C_{in}R_{in}R_o + C_oR_{in}R_o + 2C_{in}LR_{in}z_{(n)} + 2C_oLR_oz_{(n)} + 2C_{in}C_oDCRR_{in}R_oz_{(n)} + 3C_{in}C_oLR_{in}R_oz_{(n)}{}^2 \tag{14}$$

  where $z_{(1)}$,$z_{(2)}$,$z_{(3)}$ are the roots of:

  – $$\left(C_{in}C_oLR_{in}R_o\right)z^3 + \left(C_{in}C_oDCRR_{in}R_o + C_oLR_o + C_{in}LR_{in}\right)z^2 + \left(C_oR_{in}R_o + C_{in}R_{in}R_o + C_oDCRR_o + C_{in}DCRR_{in} + L\right)z + R_o + R_{in} + DCR = 0 \tag{15}$$

The system assumes an inductor with 2µH inductance (including parasitic inductance) and 8mΩ DCR. The battery provides 4V open voltage (typical single lithium battery application). Input capacitance measures 44µF. R_o remains open, and R_{in} measures 30mΩ. Output capacitance comprises 4 × 22µF. Inrush current reaches peak value before Vout rises. The DC-bias effect requires no calculation. Equation 16 provides the inductor current.

$$i_L = 3.10e^{-7.42 \times 10^5t} - 3.10e^{-9.62 \times 10^3t}\cos\left(7.55 \times 10^4t\right) + 27.09e^{-9.62 \times 10^3t}\sin\left(7.55 \times 10^4t\right) + 4 \times 10^{-10} \tag{16}$$

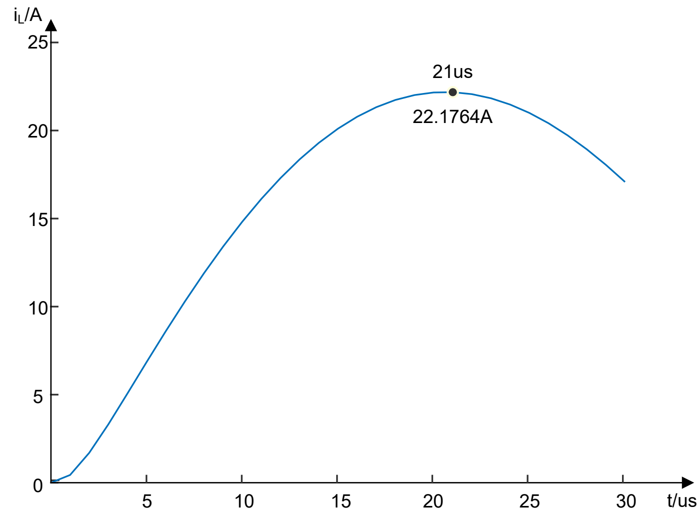

Figure 2-5. Calculated Inductor Current

Figure 2-5 depicts the calculated i_L. The inductor current reaches peak when t = 21μs. The current spike can reach 22.176A. Figure 2-6 shows the actual waveform.

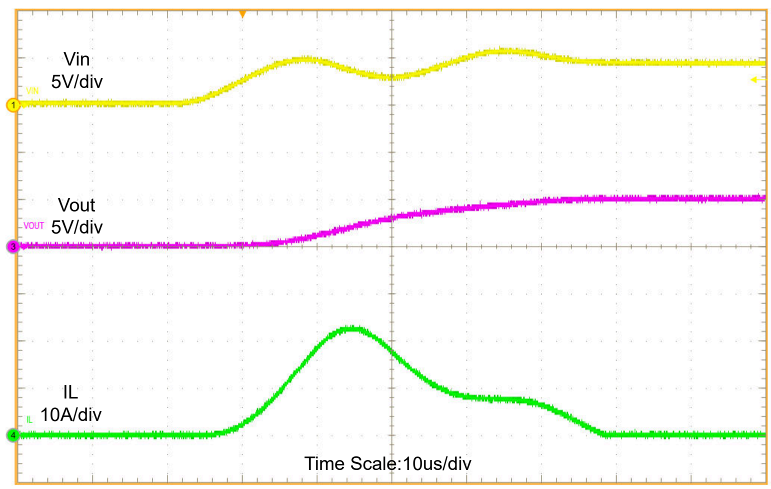

Figure 2-6. Inrush Current Waveform

Previous analysis reveals that larger L and smaller C_{out} suppress peak current. Assuming other conditions remain the same as Figure 2-5, Figure 2-7 depicts the relationship between I_{Lpeak} with inductance and output capacitance.

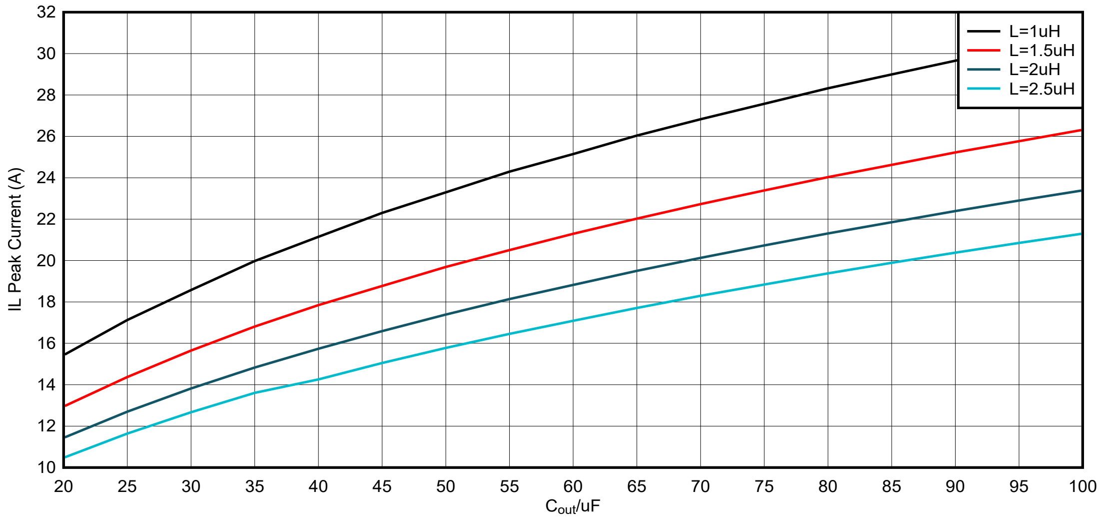

Figure 2-7. I_{Lpeak} With L and C_{out}

After Vout reaches Vin, the device can start-up using boost mode. Figure 2-8 shows the start-up waveform. As EN becomes high, the device reference voltage starts ramping up until reaching the target. With appropriate control loop, the output voltage follows the reference value and ramps up to the target.

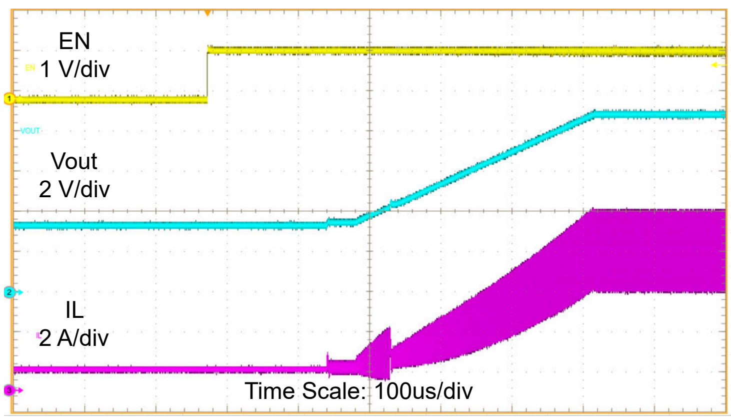

Figure 2-8. TPS61088 Start-Up Waveform

2.2 Pre-Charge

Named the *pre-charge phase*, some boost devices use the saturation characteristic of the high-side MOSFET to charge the output capacitor continuously before Vout reaches Vin. Taking TPS61022 as an example, the device has an internal switch on the high-side MOSFET. This switch allows the MOSFET to change the body diode direction and block inrush current when Vin > Vout.

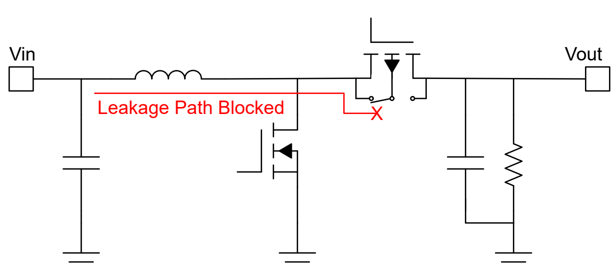

Figure 2-9. Switchable Body Diode on TPS61022

When entering pre-charge phase, the low-side switch shuts off while the high-side MOSFET enters saturation region. The source switches to SW during this process. A saturated MOSFET functions as a current source whose current the gate voltage controls. Therefore, the output capacitor charges with limited current. Figure 2-10 depicts the device behavior of TPS61022 during start-up.

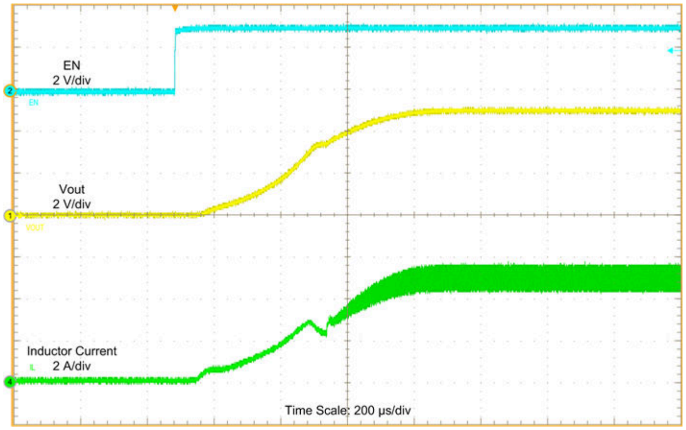

Figure 2-10. TPS61022 Start-Up Waveforms

After the output voltage reaches the input voltage, TPS61022 enters boost start-up mode. The device starts switching and the output voltage ramps up until reaching the target.

2.3 Down Mode

The TPS61299 differs from the TPS61022 pre-charge method. The TPS61299 applies a switching charge method called down mode to charge the output when output voltage drops below the input. Current control requires creating a voltage higher than input so that volt-second balance can be implemented.

TPS61299 serves as a typical example of PMOS down mode. Like pre-charge devices such as TPS61022, TPS61299 switches the source to the SW pin to block the previously mentioned inrush current. Figure 2-11 depicts the down mode behavior of TPS61299.

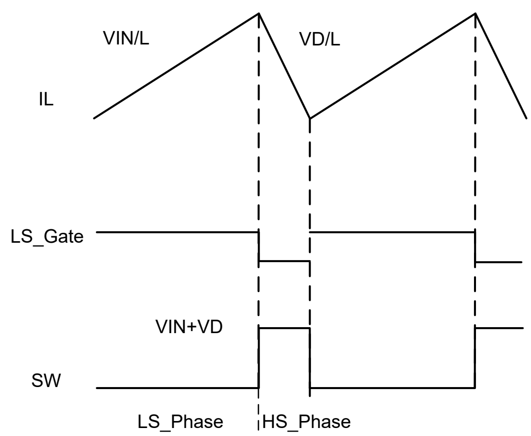

Figure 2-11. TPS61299 Down Mode Behavior

Similar to the boost mode switching process, a down mode switching cycle divides into a low-side phase and a high-side phase. During the low-side phase, the low-side switch turns on and inductor current rises with slope VIN/L. Then during the high-side phase, the low-side switch turns off while the high-side switch connects the gate to the input. As shown in Figure 2-12, inductor current charges the gate capacitor and raises the voltage on the SW pin.

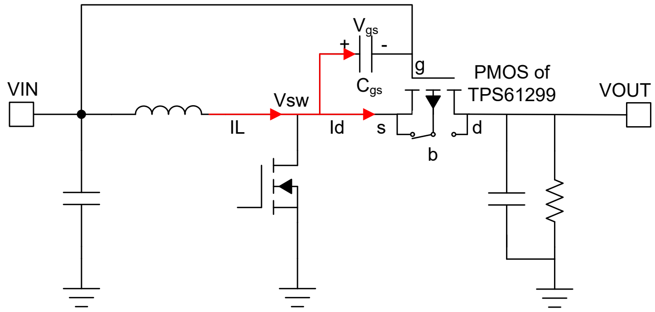

Figure 2-12. High-Side Phase of Down Mode

As V_{gs} rises, the high-side enters the saturation region and charges the output capacitor with Id. Current Ig continues charging Cg and raising Vsw until Id matches IL. At this point, Equation 17 gives the voltage on the SW pin.

$$\mathrm{Vsw} = \mathrm{V_{gs}} + \mathrm{V_{in}} \tag{17}$$

With this SW voltage higher than Vin, volt-second balance can be implemented and the device can be controlled the same way as boost mode. Figure 2-13 shows the TPS61299 start-up waveform.

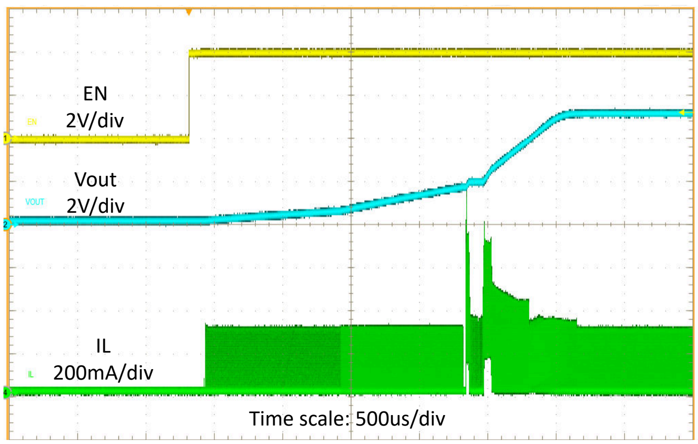

Figure 2-13. TPS61299 Start-Up Waveform

Down mode devices overcome the drawback of pre-charge in low Vin start-up capability. For pre-charge devices, the V_{gs} of the high-side switch receives supply from and cannot exceed the input voltage. If the input voltage lacks sufficient level for the switch to form a channel, the device cannot start-up. However, with Vgs charged by inductor current instead of input current, down mode devices can boot up with much lower input voltage. This makes down mode devices better for low-Vin products.

Also, for high-current devices that use NMOS as the high-side switch, pre-charge cannot be applied. For an NMOS upper switch, the gate voltage must exceed the input voltage to get the interface inverted. Without switching, the bootstrap capacitor cannot be charged and the gate voltage becomes impossible to provide.

However, compared with pre-charge devices, down mode devices have worse efficiency. Power loss for down mode is given by Equation 18 and power loss for pre-charge is given by Equation 19. Obviously, down mode devices suffer from more loss than pre-charge devices due to higher voltage across the high-side MOSFET.

$$\mathrm{P_{loss}} = \left(\mathrm{V_{gs}} + \mathrm{V_{in}} - \mathrm{V_o}\right)\mathrm{I_o} \tag{18}$$

$$\mathrm{P_{loss}} = (\mathrm{V_{in}} - \mathrm{V_o})\mathrm{I_o} \tag{19}$$

3 Output Short Protection

Another Vin > Vout situation happens when output shorts or suffers from voltage drop when current limit activates. Some devices can stay in start-up procedure continuously when Vout stays below Vin. These devices restart instantly when the short circuit releases. Other parts shut down and try rebooting intermittently until successful (called hiccup operation). This chapter introduces output short protection strategies used on TI synchronous boost devices.

3.1 Continuous Reboot

3.1.1 Continuous Reboot by Pre-charge

TPS61022 behaves the same way as start-up during output short situations. After Vin drops below Vout, the device stops switching and enters pre-charge mode where current limitation occurs.

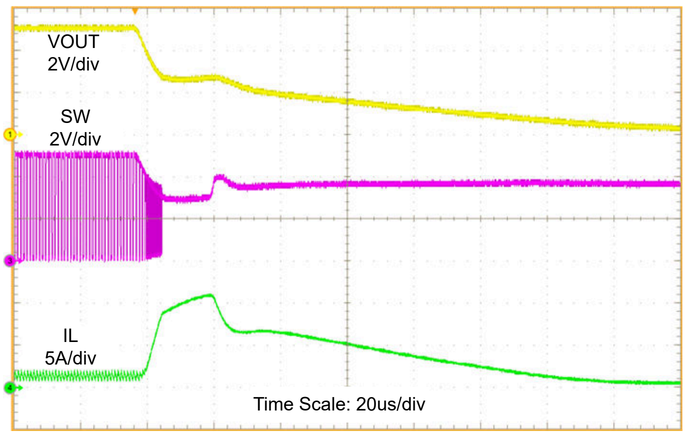

Figure 3-1. TPS61022 Into Short-Circuit Waveform

The device continuously maintains pre-charge until the short circuit is released and the device is able to reboot.

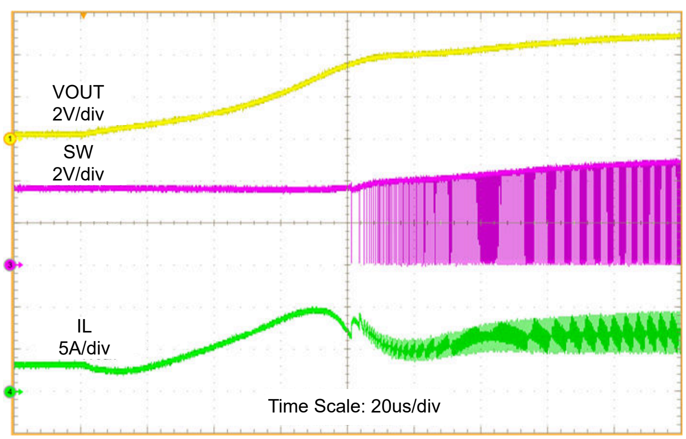

Figure 3-2. TPS61022 Short-Circuit Release Waveform

3.1.2 Continuous Reboot by Down Mode

TI boost devices with down-mode start-up multiplex the start-up strategy during output short conditions (TPS61299). Whenever output voltage drops below the input, the device enters down mode. I_{LIMIT} limits the inductor current until Vout drops below 0.5V. After that, the soft start-up current limit applies and clamps the current peak to 350mA. Figure 3-3 show the output short behavior.

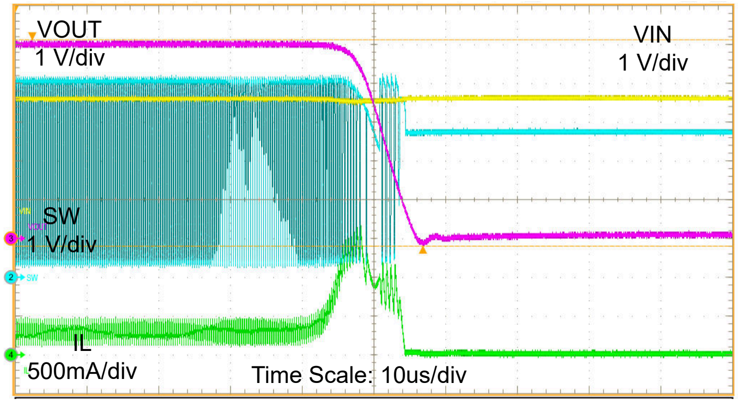

Figure 3-3. TPS61299 Into Short-Circuit Waveform

The device stays in down-mode start-up procedure until the short circuit releases and the device can start up.

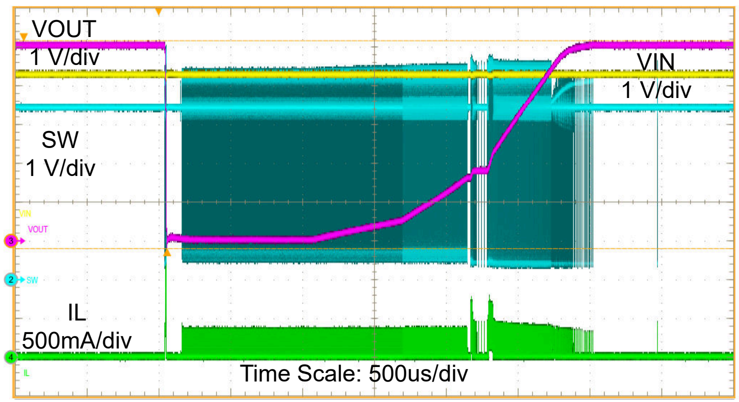

Figure 3-4. TPS61299 Short-Circuit Release Waveform

3.2 Hiccup Reboot

Different from current limit methods like pre-charge or down mode, some devices like TPS61253A or TPS61378 apply an SCP strategy named hiccup. This strategy aims to shut down the device when an output short situation is detected and reboot intermittently until the short circuit releases.

3.2.1 Hiccup Reboot by Pre-charge

TPS51253A applies a pre-charge hiccup strategy for short-circuit protection. When Vout drops below Vin, the high-side switch connect the gate to Vin and the body diode direction is switched to block the inrush current. The V_{sw} can rise above Vin and IL can drop until reaching zero. After the shut-down session, the device can try pre-charge rebooting for 1ms with 1A current limit. The rebooting attempt can be repeated every 20ms until output short is released and the device is able to boot up. Figure 3-5 shows the output short behavior.

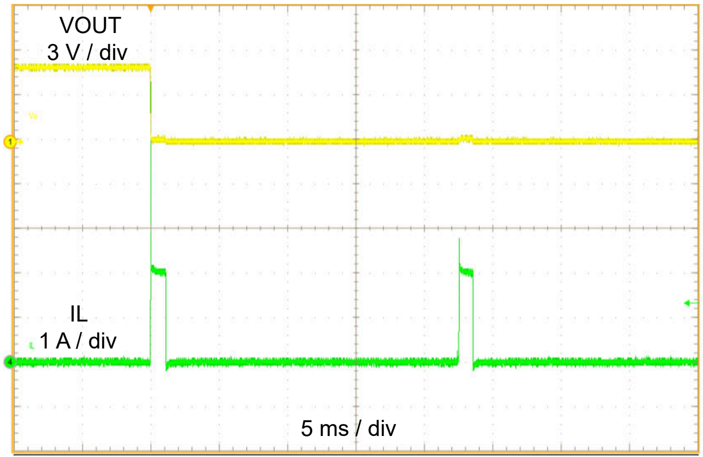

Figure 3-5. TPS61253A Short-Circuit Waveform

3.2.2 Hiccup Reboot by Down Mode

Similar to TPS61253A, TPS61378 also shuts down when an output short occurs. After the shutdown session, the device tries down-mode rebooting for 1.8ms. The rebooting attempt can repeat every 67ms until output short releases and the device can boot up. Figure 3-6 shows the output short behavior.

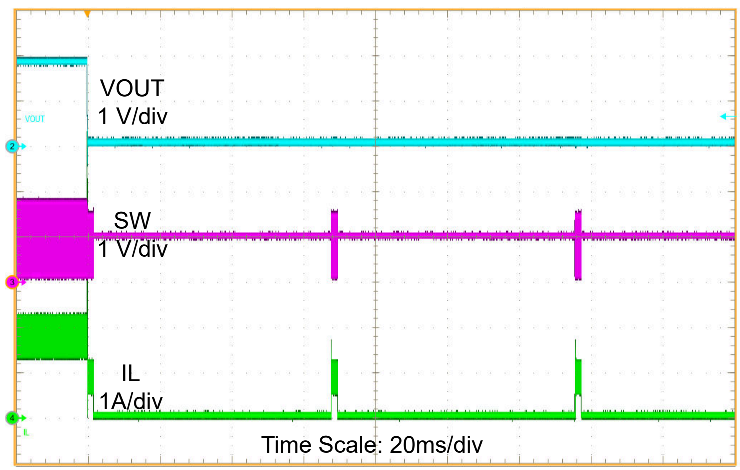

Figure 3-6. TPS61378 Short-Circuit Waveform

Compared to continuous rebooting devices, hiccup devices have lower rebooting frequency and therefore offer lower average loss and better thermal performance.

3.3 Boost Converter Short-Circuit Protection Behavior Summary

Table 3-1 compares performances between three short-circuit protection behaviors.

Table 3-1. Comparison Between Pre-charge, Down Mode, and Hiccup

	Reboot After Release	Power Loss
Pre-charge	Instantly	$$V_{in}I_{SCP} \quad (20)$$
Down mode	Instantly	$$(V_{GS} + V_{in})I_{SCP} \quad (21)$$
Hiccup	< t_{wait}(20ms to 80ms)	$$\frac{V_{in}I_{SCP}t_{reboot}}{t_{wait}} \quad (22)$$

In conclusion, devices that require fast recovery when the short circuit releases can use pre-charge or down-mode devices. Applications that prioritize temperature rise under output short conditions benefit from hiccup mode, which provides lower power loss.

4 Boost Converter Start-Up Behavior Summary

Table 4-1 compares performances of the three start up behaviors.

Table 4-1. Comparison Between Hard Start-Up, Pre-charge, and Down Mode

	Voltage Drop	Power Loss	Output Short Restart
Hard start-up	NA	NA	NA
Pre-charge	Controlled	$$(V_{in} - V_o)I_o \quad (23)$$	Controlled
Down mode	Controlled	$$(V_{GS} + V_{in} - V_o)I_o \quad (24)$$	Controlled

In conclusion, low-cost devices with large current capability that do not prioritize inrush current can use hard start-up. Devices that require frequent rebooting and prioritize power loss during start-up benefit from pre-charge, which shows better efficiency. Applications that use AA batteries as the input benefit from down-mode devices, which provide clear advantages in minimum start-up voltage.

5 References

1. Texas Instruments, *TPS61088 10-A Fully-Integrated Synchronous Boost Converter Datasheet*
2. Texas Instruments, *TPS61022 8-A Boost Converter with 0.5-V Ultra-low Input Voltage Datasheet*
3. Texas Instruments, *TPS61299 95-nA Quiescent Current, 5.5-V Boost Converter with Input Current Limit and Fast Transient Performance Datasheet*
4. Texas Instruments, *TPS61253A, TPS61253E 3.8-MHz, 5-V, 4-A Boost Converter in 1.2-mm × 1.3-mm WCSP Datasheet*
5. Texas Instruments, *TPS61378-Q1 25-μA Quiescent Current Synchronous Boost Converter with Load Disconnect Datasheet*