Technical White Paper

A Comprehensive Analysis of Different Short-Circuit Protection Methods for SiC MOSFETs

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ABSTRACT

SiC MOSFETs emerged as a common choice for high voltage switches in electric vehicle systems. In high-voltage and high-power designs using SiC MOSFETs, it is important to detect any fault that can lead to DC-link short circuits and thermal hazards. To facilitate a quick disconnection from the HV battery and improve protection against thermal risks, this technical white paper examines three short-circuit detection strategies for SiC MOSFETs: shunt-based detection, desaturation method, and hall-effect current sensor-based detection. Measurement results are presented to compare these three different methods in terms of response time, accuracy, cost, and so forth. Advantages and limitations of each approach are analyzed and insights for fault management are provided.

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1 Introduction

1.1 Difference Between SiC and IGBT

Due to the increasing demand for battery electric vehicles (BEVs), high-voltage DC/DC converters and on-board chargers (OBCs) are gaining increased importance[1–4]. Lately, 800V BEVs are rapidly entering the market which allows for fast charging [5]. Silicon carbide (SiC) metal-oxide semiconductor field-effect transistors (MOSFETs) have several advantages over silicon (Si) insulated gate bipolar transistors (IGBTs). The most important advantages include higher thermal conductivity, faster switching speed, higher junction temperature and higher blocking voltage [6]. Therefore, utilization of SiC MOSFET in automotive systems is growing rapidly.

However, the use of SiC MOSFET poses new challenges. The differences between SiC MOSFET and IGBT in dealing with short-circuit scenarios are mainly reflected in the following two aspects. [7]

- Smaller chip size of SiC MOSFET compared to IGBT
  - The SiC MOSFET die has lower thermal dissipation capability. During short circuit conditions, the surge current generates a significant amount of joule heating and the die can be destroyed in a short period of time without enough capability to dissipate the heat.
- Difference in operating region during normal ON operation
  - IGBT typically works in the saturation region during the normal ON state. When a short circuit happens, the collector current I_C increases and goes through a sharp transition from the saturation region to the active region. The collector current gets self-limited and becomes independent of V_{CE}.
  - SiC MOSFET works in the linear region during normal ON operation and SiC MOSFET has a larger linear region. During a short circuit event, the transition from the linear region to saturation region happens significantly higher. The drain current keeps increasing along with the increasing V_{DS}. The device is destroyed before reaching the transition point.

These characteristics lead to the fact that SiC MOSFETs in HV DC/DC converters and OBCs need faster and reliable short-circuit protection measures to meet the high safety standards in automotive. The challenges particularly lie in the speed of detection and disconnection of the short-circuit event to prevent damage of the system [8]. The system short circuit protection (SCP) response time is defined to verify reliable short circuit protection.

1.2 System SCP Response Time Requirement

From the occurrence of the short circuit event to achieving a safe state of the system, several processes are experienced as explained below:

- The current reaches the SCP threshold**.** The time usually depends on the type of short circuit event, the inductance on the current path, the margin of the SCP threshold, and so forth.
- The current sensor reports SCP signal**.** The time usually depends on the response time of current sensor, which is critical and is elaborated on in this document.
- The SCP signal is transmitted to the gate driver. This time mainly depends on the components in the SCP signal path, which is closely related to the customer high-level architecture design.
- V_{GS} starts to decrease. The time of this part mainly depends on the typical propagation delay of the gate driver.
- The system enters to a safe state. The time mainly depends on the shutdown feature of the gate driver, the turn-off resistance, SiC MOSFET characteristic parameters, inductance in the main circuit, and so on.

The total system SCP response time is defined as the sum of the above response time, which is the final requirement from SiC MOSFET. The comparison among different designs mainly lie in the selection of current sensors, and other parts remain the same.

1.3 Different SCP Locations

Short-circuits in power semiconductor devices are categorized into three types [9, 10]. In case of a short-circuit type 1 (SCT 1), the short circuit is already present in the system and a MOSFET actively switches on in this short circuit. On the contrary, a short-circuit type 2 (SCT 2) occurs while the MOSFET is already switched on. In case of a short-circuit type 3 (SCT 3), the short circuit happens while the body diode of the MOSFET is in the freewheeling state.

Figure 1-1, Figure 1-2, Figure 1-3 shows the current path of three types of short circuit scenarios. The current path indicates where the current sensor is placed to detect the short circuit fault. By comparing three types of short circuits, placing the current sensor on HV BUS- was found to be the best position, as this can cover all three different cases.

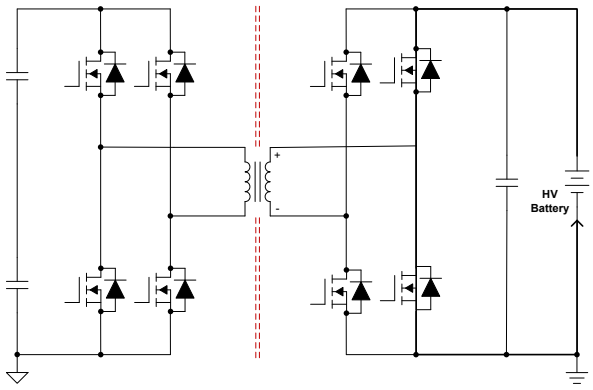

Figure 1-1. Short Circuit Scenario 1

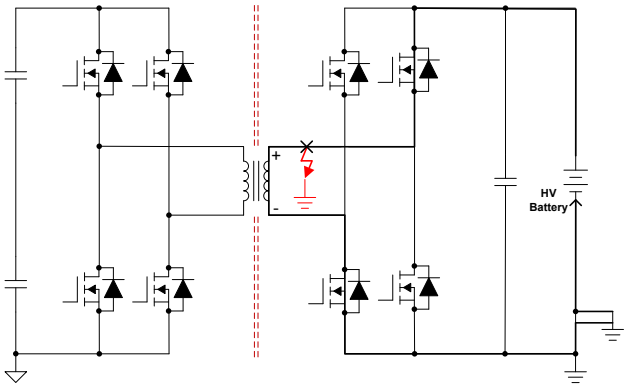

Figure 1-2. Short Circuit Scenario 2

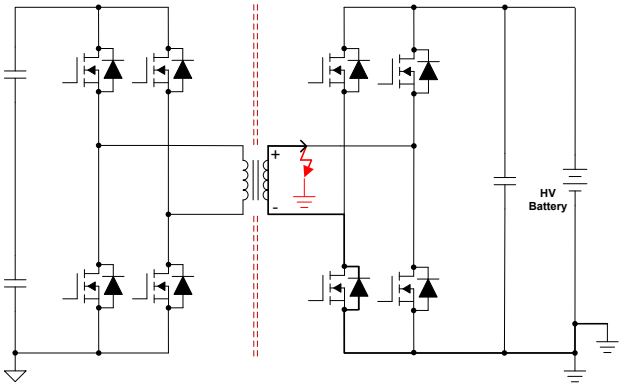

Figure 1-3. Short Circuit Scenario 3

Several methods for short-circuit detection are described in the literature. One possibility is to measure the drain source voltage of the MOSFETs to determine over currents [11]. Another possibility is to measure the short-circuit current directly with various sensors to detect faults [12, 13]. Monitoring the dc-link voltage to detect faults in sufficient time is another option [14].

This document focuses on the SCT 1 for comparing and analyzing state of the art short-circuit protection methods for SiC MOSFETs. First, the principle of the short-circuit detection for SiC MOSFET are analyzed. Second, three protection methods are described and verified with measurements in detail. Finally, the performance of all three methods is compared based on important parameters.

2 Short-Circuit Mechanism

To analyze the mechanisms of an SCT 1, the half-bridge model is shown in Figure 2-1. The two SiC MOSFETs S_{HS} and S_{LS} are controlled by a gate driver unit (GDU), respectively. Furthermore, two capacitors provide energy for the converter: the capacitance C_C provides the needed energy for the current commutation between the two SiC MOSFETs S_{HS} and S_{LS}, while the capacitance C_B is used as bulk filter at the output of the converter. The inductances $L_{\sigma,C}$ and $L_{\sigma,B}$ represent the sum of parasitic inductances of capacitors, MOSFETs and PCB traces. A common circuit breaker S_B connects the high-voltage battery U_{batt} to various power electronic devices.

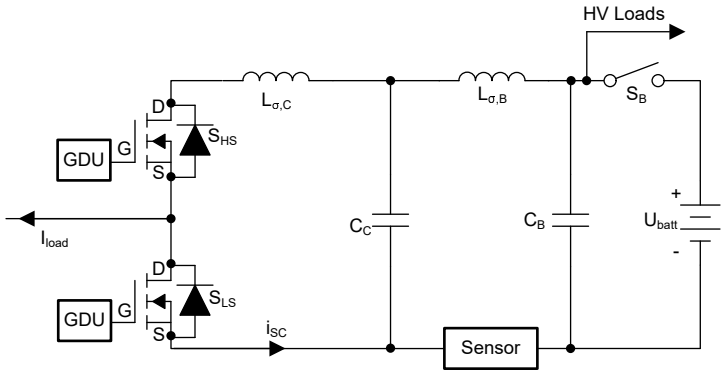

Figure 2-1. Simplified Schematic to Analyze an SCT 1

In the event of a short circuit, it is crucial to isolate the fault to avoid further damage, such as fire hazards. Using the breaker S_B to disconnect the fault disrupts the operation of other functioning devices connected to the battery. One idea is to incorporate an additional mechanical or electronic fuse in each converter; however, this approach increases costs, which is not great in the price-sensitive automotive application. Consequently, there is a pressing need for a reliable and cost-effective short-circuit protection scheme to prevent thermal incidents.

Two of the short-circuit detection methods utilize an additional current sensor. As discussed in the Section 1.3, the current sensor is placed between the two capacitors C_C and C_B.

For the measurement, two SiC MOSFETs S_{HS} and S_{LS} form the half-bridge topology. The drain and source pins of the MOSFET S_{LS} are soldered together to make sure a low impedance short circuit to simulate SCT 1 on MOSFET S_{HS}. At time t_0, the GDU of MOSFET S_{HS} gets the turn-on command and the gate-source voltage of high-side SiC MOSFETs u_{GS} starts to increase.

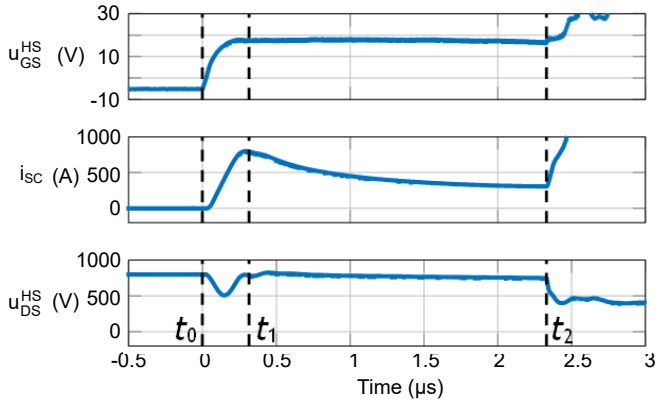

Figure 2-2. Waveforms of a Failing MOSFET During an SCT 1

The current slope di_{SC}/dt is dependent on various parameters such as stray inductances and capacitances of the SiC MOSFETs [16]. The current i_{SC} reaches the peak at the time t_1 and decreases afterwords. The decreasing current can be explained due to the self-heating of the SiC MOSFET die, caused by losses and therefore increasing drain-source resistance [16].

Even though the current continues to decrease, more and more energy is dissipated in the SiC MOSFET as the drain-source voltage of high-side SiC MOSFETs u_{DS} stays high. Hence, the MOSFET keeps continuously increasing the temperature. At time t_2, the SiC MOSFET reaches the critical junction temperature and gets damaged in a low impedance state. As the current i_{SC} is not limited by the drain-source resistance anymore, i_{SC} starts to increase again. From now on, the short circuit cannot be isolated by the MOSFETs and as long as the battery provides energy, this short circuit is a potential risk of fire and smoke hazards. Therefore, there is a need for short-circuit protection to prevent damage to the MOSFETs. Current sensing methods such as shunt-based detection and hall-effect sensor- based detection, along with the voltage sensing method like the desaturation method, are selected as protection methods for analysis.

3 Short Circuit Detection Methods

Three short circuit detection methods considering different factors like cost and response time (less than 2µs [15]) are explained in more detail.

3.1 Shunt-Based Method

Shunt-based sensing scheme is one of the simple methods to monitor the short circuit scenarios. The sensing circuit consists of a high precision resistor and isolated comparator. A shunt resistor R_S is employed to measure the current flowing between the bulk capacitance C_B and commutation capacitance C_C. The simplified circuit for shunt-based method is shown in Figure 3-1.

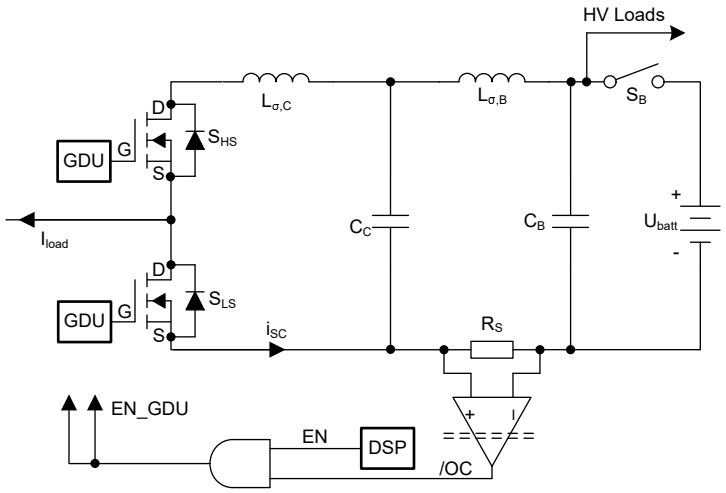

Figure 3-1. Simplified Circuit for Shunt-Based Detection

The current flowing through the shunt resistor creates a voltage drop across the shunt resistor:

$$u_{RS} = i_{SC} \times R_S + L_{SH} \times \frac{di_{SC}}{dt} \quad (1)$$

where L_{SH} being the parasitic inductance of the shunt [17].

Care must be taken in the design to minimize the parasitic inductance to avoid false fault detection during normal operation. The voltage u_{RS} across the shunt resistor is monitored by the programmable and isolated comparator AMC23C12-Q1. As soon as the voltage u_{RS} reaches the defined trigger voltage, the output of the comparator is used to disable the gate driver and turn off the MOSFET.

The AMC23C12-Q1 provides an open-drain output with optional latching function. The output is actively pulled low when |VIN| exceeds the threshold value defined by the voltage on the REF pin, as shown in Figure 3-2.

The open-drain output is diode-connected to the VDD2 supply, meaning that the output cannot be pulled more than 500mV above the VDD2 supply before significant current begins to flow into the OUT pin. In particular, the open-drain output is clamped to one diode voltage above ground if VDD2 is at the GND2 level.

On a system level, the CMTI performance of an open-drain signal line depends on the value of the pullup resistor. During a common-mode transient event with a high slew rate (high d_V/d_t), the open-drain signal line can be pulled low due to parasitic capacitive coupling between the high-side and the low-side of the printed circuit board (PCB). The AMC23C12-Q1 has been characterized with a relatively weak pullup resistor value of 10kΩ to verify that the specified CMTI performance is met in a typical application with a 4.7kΩ or lower pullup resistor.

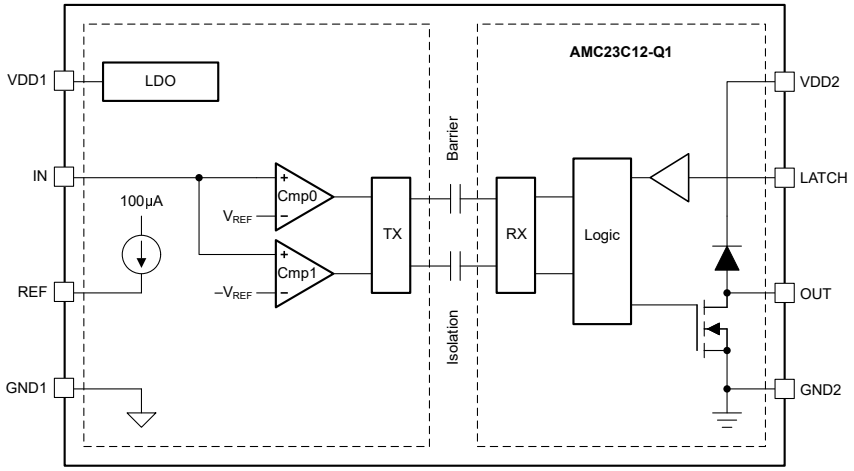

Figure 3-2. Block Diagram of AMC23C12-Q1

3.2 Desaturation-Based Method

The DESAT protection has been widely used for short circuit protection of IGBTs. This circuit indirectly measures the drain-source voltage of the MOSFET during the on-state to detect short circuits. Figure 3-3 illustrates the simplified circuit.

The DESAT protection circuit consists of a resistor blanking capacitor, and a diode. When the device turns on, a current source charges the blanking capacitor and the diode is conducted. During normal operation, the capacitor voltage is clamped at the forward voltage of the device. When short circuit happens, the capacitor voltage is quickly charged to the threshold voltage which triggers the device shutdown.

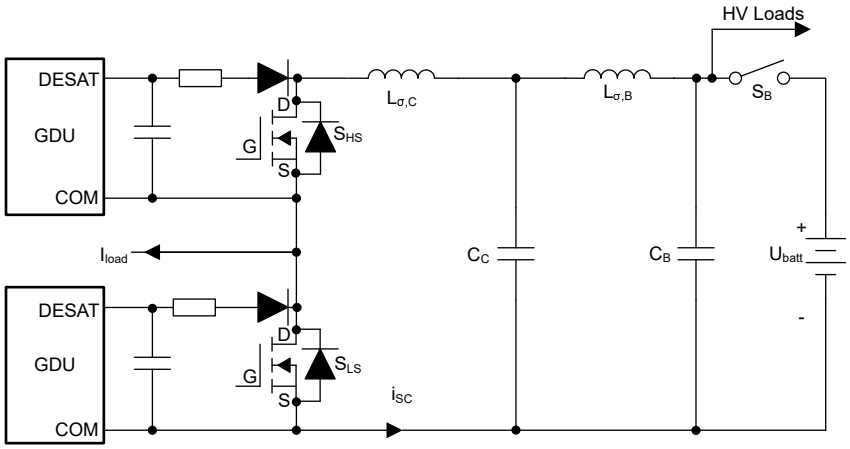

Figure 3-3. Simplified Circuit for Desat-Based Detection

As shown in Figure 3-4, to make sure that the switching transients do not interfere with the desaturation detection, the current i_{desat} and the capacitor C_{desat} need to be carefully chosen to define a proper blanking time t_{blk}. To increase the current i_{desat} and decrease the reaction time, the diode D_2 with the forward voltage u_{D2} and the resistor R_2 are implemented. Neglecting the time that is needed to block the diode D_1, the blanking time t_{blk} can be estimated with

$$t_{blk} = -C_{desat} \times R_2 \times \ln\left(1 - \frac{9.15V}{U_{dd} - u_{D2} + i_{int} \times R_2}\right) \quad (2)$$

where U_{dd} is the supply voltage of the gate driver.

In case of a fault detection, the gate driver initiates a soft turn-off pulling a constant current of 400mA out of the MOSFET gate to verify low overshoots in the drain-source voltage.

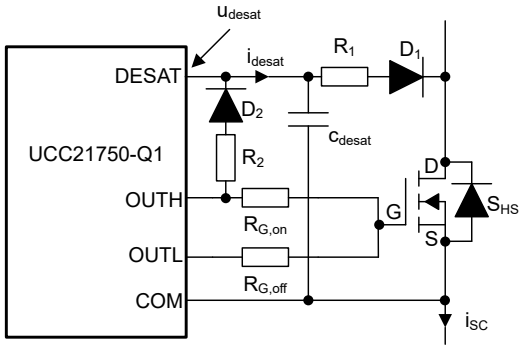

Figure 3-4. Operation Principle of Desaturation Protection

3.3 Hall-Effect Sensor-Based Method

Hall-effect sensors are popular in OBC and DCDC applications to sense the current, and can also be used to detect the short-circuit current i_{SC}. The hall-effect sensor detects short-circuit currents by sensing the magnetic field generated by current flowing through the sensing element [18]. Figure 3-5 shows the simplified circuit for hall-effect sensor-based method.

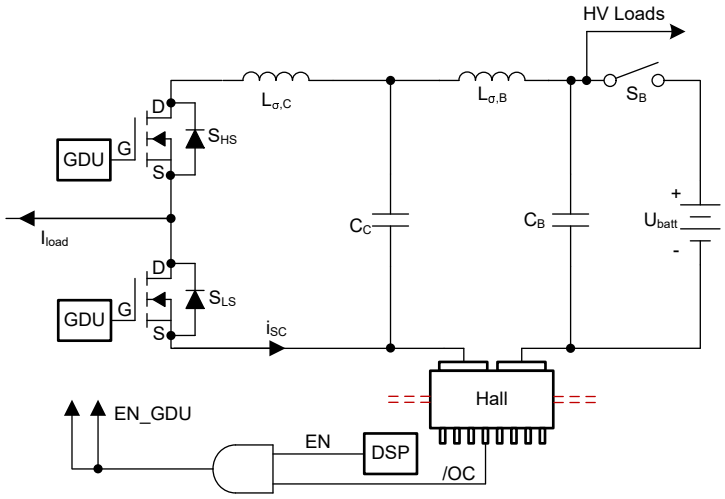

Figure 3-5. Simplified Circuit for Hall-Based Detection

As hall-effect based current sensor, a TMCS1126-Q1 with integrated comparator is used. The Short circuit Detection (OCD) circuit provides a comparator output that can be used to trigger a warning or system shutdown to prevent damage from excessive current flow caused by short circuits, motor stalls, or other system conditions. This digital response can be configured on both bidirectional and unidirectional devices to trip anywhere between half and over twice the analog measurement range.

The trigger threshold is set using external passive elements. Similar to the shunt-based design, the sensor is placed between the two capacitors C_C and C_B. As soon as the current i_{SC} reaches the defined threshold current set in the hall-effect sensor, the over-current output pin is used to disable the gate driver and turn-off the SiC MOSFET.

4 Test Setup

Figure 4-1 shows the hardware test setup. Two SiC MOSFET in a HU3PAK package with a typical on state resistance of R_{DS} = 25mΩ are used for the measurements. The drain and source pins of the MOSFET S_{LS} are soldered together to maintain a low impedance short circuit. The MOSFET S_{HS} is controlled by a UCC21750-Q1 gate driver and the gate-driver signal is generated by the control PCB using a LAUNCHXL- F280025C launchpad. All three discussed short-circuit detection circuits are implemented on the PCB. For the DC-link capacitor, a total of C_B = 20µF film capacitors are used. Multilayer ceramic chip capacitors (MLCCs) are used for the commutation capacitance C_C = 100nF (unless otherwise specified) to provide a low inductive commutation path. All the short-circuit detection methods are set to a trigger threshold of 100A. The measurement results of each detection method are analyzed in the following. Only one method is active during each measurement, while the other two methods are deactivated or removed.

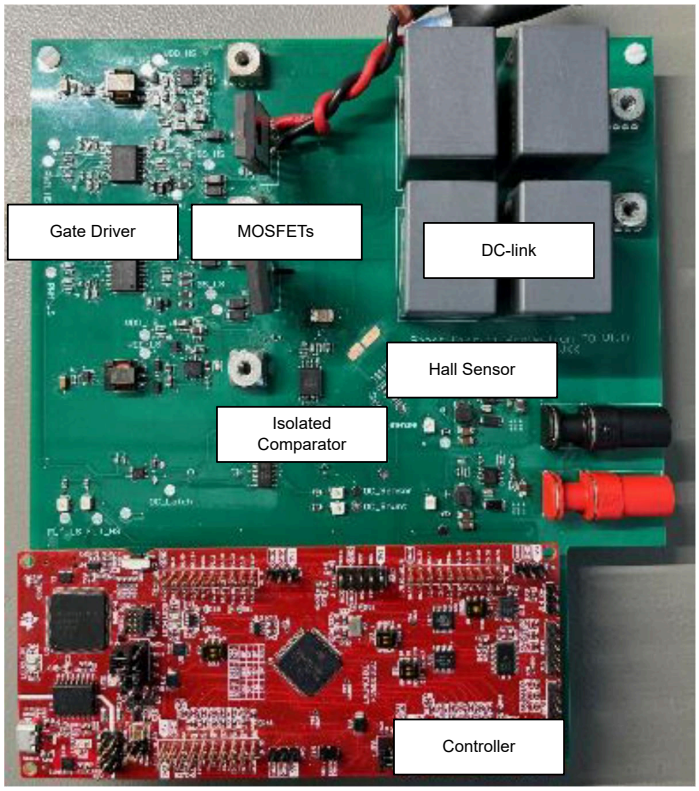

Figure 4-1. Hardware Setup for Short Circuit Measurements

5 Measurement Results

In this section, the measurement results of each short-circuit detection method are discussed. Additionally, further measurements using the shunt-detection method are conducted. This analysis aims to provide a better understanding of the SiC MOSFET's behavior during a short-circuit.

5.1 Shunt Based Measurements

The shunt-based protection triggers the enable pin of the gate driver. As soon as this enable pin goes low, the gate driver turns off the SiC MOSFET via the turn-off resistance $R_{G,OFF}$.

As the turn-off event is a hard turn-off, the drain-source voltage of the high-side SiC MOSFETs u_{DS} has an overshoot during the switching event that can damage the SiC MOSFET. Under normal operating conditions, that overshoot depends on the stray inductance $L_{\sigma,C}$, the slope of the SiC MOSFET current di_{SC}/dt and the commutation capacitance C_C [19] However, due to the large current present in the event of a short circuit, the overshoot in the drain-source voltage in the event of a fault also depends on the stray inductance $L_{\sigma,B}$, as the commutation capacitance C_C can no longer provide enough energy to limit the overshoot.

The influence of different commutation capacitors C_C during an SCT 1 with a DC-link voltage U_{batt} = 400V is shown in Figure 5-1. For these measurements, a turn-off gate resistance $R_{G,OFF}$ = 80Ω is used. While different commutation capacitors C_C show only a minor effect on the current i_{SC}, the capacitance has an impact on the drain-source voltage of the high-side SiC MOSFETs u_{DS}. Using a capacitance C_C = 10 nF, the u_{DS} voltage reaches 1230V, which is a potential hazard for the 1200V SiC MOSFET.

Increasing the capacitance C_C to 20nF, the voltage peak is reduced to 840V. However, increasing that capacitance further to C_C = 300nF, no significant reduction in the voltage overshoot is observed. This can be explained by the fact, that a commutation capacitance $C_C \geq$ 200nF is sufficient to provide the energy stored in the inductance $L_{\sigma,C}$ in case of a short-circuit current.

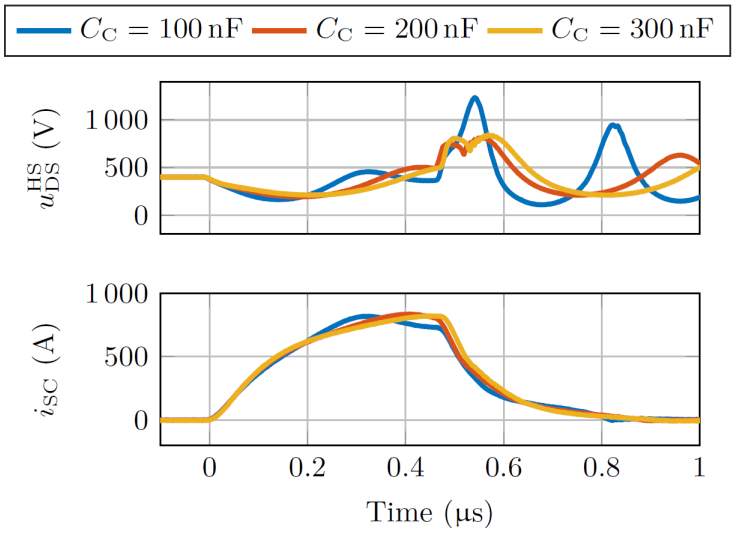

Figure 5-1. Influence of Different Commutation Capacitors C_C on Switching Transients During SCT 1

The choice of the value for the capacitance C_C is a trade-off between cost and performance. The voltage overshoot should not be overly constrained, because the SiC MOSFET is capable of dissipating a limited amount of energy during an avalanche event. In all other discussed measurements, the commutation capacitance is chosen to C_C = 100nF.

To verify a safe turn-off with a capacitance C_C = 100nF, the turn-off resistor $R_{G,off}$ needs to be increased to decrease the voltage overshoot. Figure 5-2 shows measurement results for different turn-off gate resistances $R_{G,off}$ with a DC-link voltage U_{batt} = 400V. The measured short-circuit current shows only slight changes in the short-circuit current i_{SC}, while the drain-source voltage u_{DS} differs significantly.

Using a resistance $R_{G,off}$ = 8Ω, the voltage peak reaches 1230V. Increasing the resistance to $R_{G,off}$ = 20Ω, the voltage overshoot is decreased to 1000V. With a resistance $R_{G,off}$ = 35Ω, the drain-source voltage reaches only 860V as maximum.

Although a larger gate resistor can reduce the voltage overshoot, this increases the turn-off losses in normal operation. Therefore, the choice of the turn-off resistance is a trade-off between losses and overshoot.

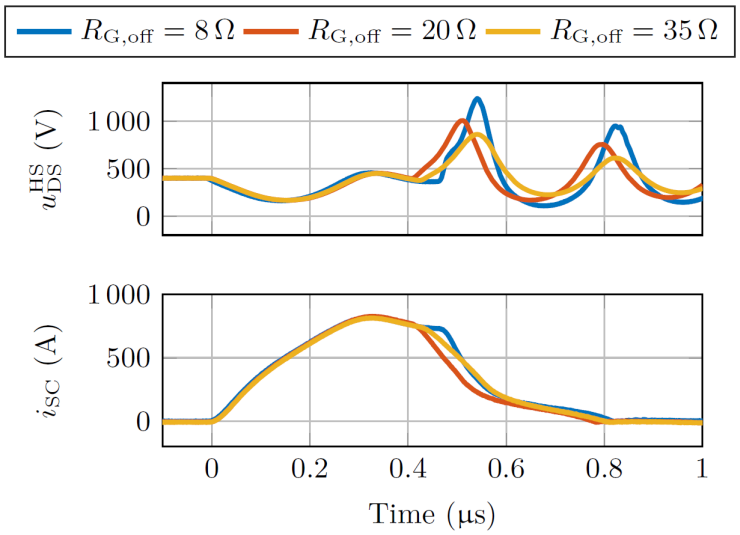

Figure 5-2. Influence of Different Turn-Off Resistors $R_{G,off}$ on Switching Transients During SCT 1

Figure 5-3 shows the waveforms of an SCT 1 with a DC-link voltage U_{batt} = 800V and a turn-off gate resistor $R_{G,off}$ = 35Ω. At time 0ns, the gate-source voltage u_{GS} reaches the threshold voltage of the MOSFET and the current i_{SC} starts to rise. The fault signal u_{shunt} starts to decrease significantly at time 200ns, indicating a fault. The gate-source voltage u_{GS} starts to decrease at time 380ns, starting to turn-off the SiC MOSFET . The drain-source voltage u_{DS} reaches its maximum of 1190V at 48ns.

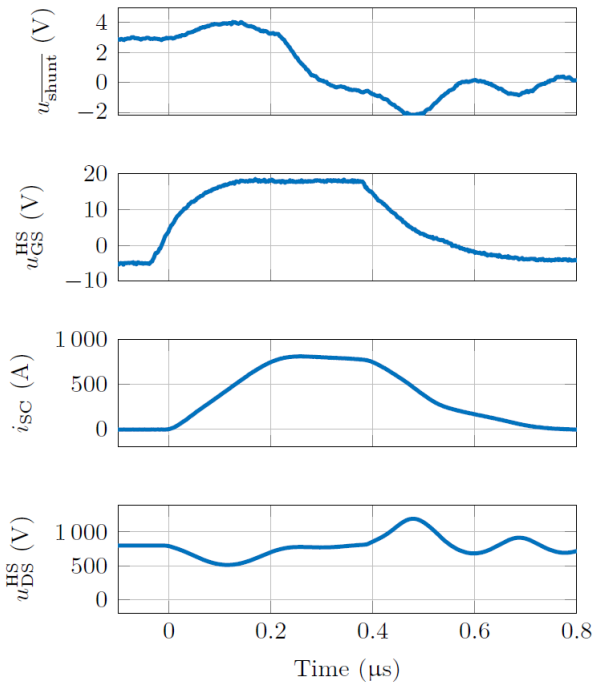

Figure 5-3. Waveforms for Shunt-Based Method With $R_{G,off}$ = 35Ω

5.2 Desaturation-Based Measurements

This section discusses the measurement results using the integrated desaturation detection of the gate driver UCC21750-Q1. Table 5-1 lists the crucial values of the components, resulting in a theoretical blanking time of t_{blk} = 1µs.

Table 5-1. Component Overview of Desaturation Setup

Part	Value
R_2	30kΩ
u_{D2}	0.3V
C_{desat}	100pF

Figure 5-4 shows the measurement results using the desaturation method. As soon as the gate-source voltage u_{GS} reaches the threshold voltage of the SiC MOSFET at time 0ns, the current i_{SC} starts to rise. At the same time, the voltage u_{desat} starts to increase reaching the maximum at 1600ns, indicating an overcurrent for the gate driver. After the detection, the gate driver starts to slowly turn-off the SiC MOSFET. Due to the soft turn-off event, the drain-source voltage overshoot only reaches 940V at 1700ns.

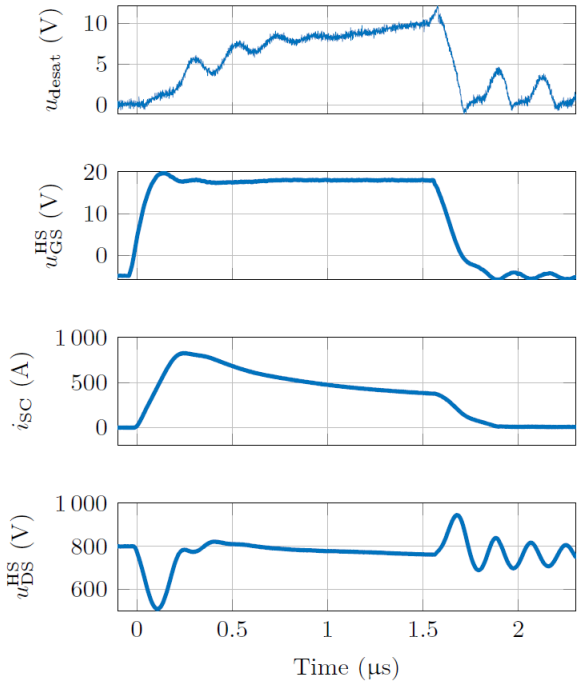

Figure 5-4. Waveforms for Desaturation-Based Method With Soft Turn Off

5.3 Hall-Effect-Sensor Measurements

For the hall-effect-based measurements, the turn-on gate resistance $R_{G,on}$ needs to be modified to detect the short-circuit event. In the meantime, the slew rate of the current can be decreased by increasing turn-on resistance $R_{G,on}$.

Therefore, in these measurements, the resistance $R_{G,on}$ is increased from 15Ω to 25Ω. In Figure 5-5, the measurement results using the hall-sensor-based short-circuit detection is shown. At time 0ns, the gate-source voltage u_{GS} reaches the threshold voltage of the SiC MOSFET and the current i_{SC} starts to rise. The fault signal u_{hall} decreases rapidly at time 700ns, disabling the gate driver. At time 830ns, the gate-source voltage u_{GS} starts to decrease, turning off the MOSFET S_{HS} safely. The overshoot in the drain-source voltage u_{DS} reaches 1090V at the maximum.

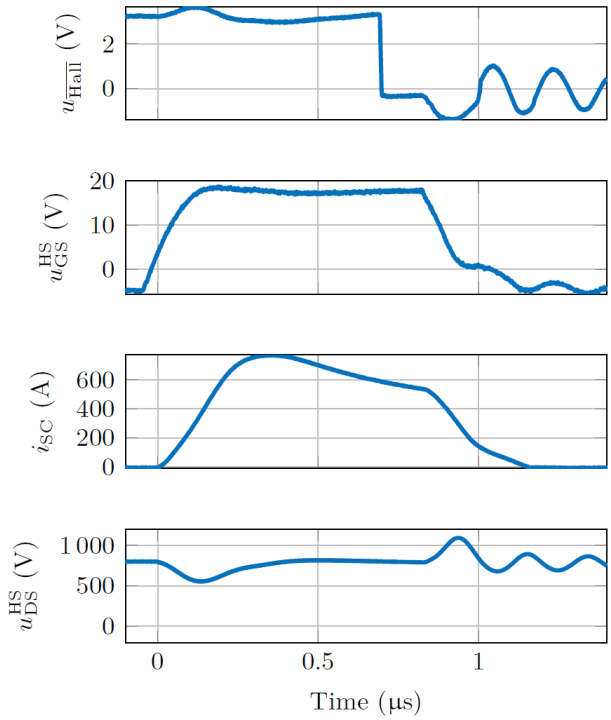

Figure 5-5. Waveforms for Hall-Based Method With $R_{G,off}$ = 35Ω

5.4 Performance Comparison

All three analyzed short-circuit protection methods are able to turn-off the SiC MOSFET under a SCT 1 condition safely. However, there are differences between the presented designs.

Table 5-2 lists a comparison of short-circuit protection methods. Among the evaluated methods, the shunt-based design stands out in terms of response time and accuracy. However, the limitation of this method is the highest overshoot of the drain-source voltage in the hard turn-off event. This issue can be mitigated by optimizing the PCB layout to minimize the stray inductance, allowing the SiC MOSFETs to operate at higher turn-off speeds without excessive overshoots in the drain-source voltage.

The Hall-effect sensor-based method meets the typical requirements for response time and accuracy, and it has lower power loss compared with shunt-based solution. However, basically hall-effect sensor is more susceptible in case of high di_{SC}/dt during short-circuit events, which makes the PCB layout critical.

The desaturation-based protection incorporates a soft turn-off feature, which helps to gradually switch off the short-circuit current, significantly reducing the drain-source voltage overshoot. This relaxes the PCB design constraints which allows for higher stray inductance circuits, and also allows SiC MOSFETs to operate at maximum switching speed, minimizing energy losses during normal operation. However, the main limitation of the desaturation method is the relatively longer response time during SCT 1 faults. Design optimizations are necessary to lower this response time to maintain a safe turn-off in case of a short-circuit event.

Table 5-2. Comparison of Analyzed Short-Circuit Detection Methods

Parameter	Shunt	Hall Effect	Desaturation+ Soft Turn-Off
Response time	380ns	820ns	1.55µs
Accuracy	±3.4%	±10%	Not applicable
Losses at 20A	0.4W	0.28W	Negligible
Overshoot	1190V	1090V	940V

In summary, these three options have their own benefits and limitation in different aspects.

- Response time. Shunt-based method has the shortest response time, while other two methods can also meet the typical response time requirement.
- Accuracy. Shunt-based method has the highest accuracy on overcurrent threshold.
- Power loss. The shunt-based method and Hall-effect-based method add additional losses to the system, while the additional losses using the desaturation-based method are negligible.
- Voltage overshoot. The desaturation-based method has the lowest overshoot because of its soft turn-off feature.
- PCB layout. The implementation of the current sensors influences the stray inductances of the commutation cell, while the impact of the desaturation implementation is negligible, as this does not need to be inserted in the current path.
- Cost. Gate drivers with desaturation protection and soft turn-off functionality are generally more expensive than standard gate drivers used in alternative methods.

Therefore, these three solutions are suitable for different scenarios, depending on the customer's requirement. Shunt-based method is particularly suitable for situations that require high response speed and accuracy. Hall-effect-based method is particularly suitable for situations that require lower losses and also current values for redundant software protection. Desaturation-based method is particularly good for situations that require lower voltage overshoot and easy PCB layout.

6 Conclusion

This technical white paper delivers a comprehensive analysis of three protection methods: Shunt-based detection, desaturation method and hall-effect-based detection for addressing short circuit scenarios in high voltage SiC MOSFETs. The shunt-based method offers the fastest response and lowest cost for low-inductance circuits. The desaturation detection is comparatively costly and slower response time of the examined methods but has lower overshoot as advantage. Hall sensors, while a cost-effective option, comes with a extra effort to manage high di_{SC}/dt scenarios. Balancing of different factors like PCB layout optimization, component selection, and application-specific requirements are key to enhance SiC MOSFET reliability in HEV/EV systems.

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7 References

1. H. Wouters and W. Martinez, “Bidirectional onboard chargers for electric vehicles: State-of-the-art and future trends,” IEEE Transactions on Power Electronics, vol. 39, no. 1, pp. 693–716, Jan. 2024. DOI: 10.1109/tpel.2023.3319996.
2. B. Shi, A. I. Ramones, Y. Liu, H. Wang, Y. Li, et al., “A review of silicon carbide MOSFETs in electrified vehicles: Application, challenges, and future development,” IET Power Electronics, vol. 16, no. 12, pp. 2103–2120, May 2023. DOI: 10.1049/pel2. 12524.
3. E. Chemali, M. Preindl, P. Malysz, and A. Emadi, “Electrochemical and electrostatic energy storage and management systems for electric drive vehicles: State-of-the-art review and future trends,” IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 3, pp. 1117–1134, 2016. DOI: 10.1109/jestpe.2016.2566583.
4. J. Serrano, “Imagining the future of the internal combustion engine for ground transport in the current context,” Applied Sciences, vol. 7, no. 10, p. 1001, Sep. 2017. DOI: 10.3390/app7101001.
5. S. Dutta and J. Bauman, “An overview of 800 V passenger electric vehicle onboard chargers: Challenges, topologies, and control,” IEEE Access, vol. 12, pp. 105 850–105 864, 2024. DOI: 10.1109/access.2024.3435463.
6. M. Zhang, H. Li, Z. Yang, S. Zhao, X. Wang, and L. Ding, “Analysis of SiC MOSFETs short-circuit behavior in half bridge configuration during shoot through event,” in 2023 IEEE Energy Conversion Congress and Exposition (ECCE), IEEE, Oct. 2023, pp. 5350–5358. DOI: 10.1109/ecce53617. 2023.10362468.
7. H. Qin, H. Hu, W. Huang, Y. Mo, and W. Chen, “An improved desaturation short-circuit protection method for SiC power modules,” Energy Reports, vol. 8, pp. 1383–1390, Apr. 2022. DOI: 10.1016/j. egyr.2021.11.274.
8. M. Zhang, H. Li, Z. Yang, S. Zhao, X. Wang, and L. Ding, “Short circuit protection of silicon carbide MOSFETs: Challenges, methods, and prospects,” IEEE Transactions on Power Electronics, vol. 39, no. 10, pp. 13 081–13 095, Oct. 2024. DOI: 10. 1109/tpel.2024.3430897.
9. M. Cui, J. Li, Y. Du, and Z. Zhao, “Behavior of SiC MOSFET under short-circuit during the on-state,” IOP Conference Series: Materials Science and Engineering, vol. 439, p. 022 026, Nov. 2018. DOI: 10.1088/1757-899x/439/2/022026.
10. J. Lutz and T. Basler, “Short-circuit ruggedness of high-voltage IGBTs,” in 2012 28th International Conference on Microelectronics Proceedings, IEEE, May 2012, pp. 243–250. DOI: 10. 1109/miel.2012.6222845.
11. Z. Wang, X. Shi, Y. Xue, L. M. Tolbert, F. Wang, and B. J. Blalock, “Design and performance evaluation of overcurrent protection schemes for silicon carbide (sic) power mosfets,” IEEE Transactions on Industrial Electronics, vol. 61, no. 10, pp. 5570– 5581, Oct. 2014. DOI: 10.1109/tie.2013.2297304.
12. J.-A. Lee, D. H. Sim, and B. K. Lee, “Short-circuit protection for SiC MOSFET based on PCB-type rogowski current sensor: Design guidelines, practical solutions, and performance validation,” IEEE Transactions on Power Electronics, vol. 39, no. 3, pp. 3580–3589, Mar. 2024. DOI: 10.1109/tpel. 2023.3339724.
13. C. Xiao, L. Zhao, T. Asada, W. Odendaal, and J. van Wyk, “An overview of integratable current sensor technologies,” in 38th IAS Annual Meeting on Conference Record of the Industry Applications Conference, 2003., ser. IAS-03, vol. 2, IEEE, 2003, pp. 1251–1258. DOI: 10.1109/ias.2003. 1257710.
14. M. Laumen, C. L¨udecke, and R. W. De Doncker, “Ultra-fast short-circuit detection for SiC MOSFETs using dc-link voltage monitoring,” in 2020 IEEE 11th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), IEEE, Sep. 2020, pp. 547–553. DOI: 10.1109/pedg48541.2020.9244367.
15. D. Xing, B. Hu, M. Kang, Y. Zhang, S. Nayak, et al., “1200-v sic mosfet short-circuit ruggedness evaluation and methods to improve withstand time,” IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 10, no. 5, pp. 5059–5069, Oct. 2022. DOI: 10.1109/jestpe.2022.3144995.
16. B. Kakarla, T. Ziemann, R. Stark, P. Natzke, and U. Grossner, “Short circuit ruggedness of new generation 1.2 kv sic mosfets,” in 2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), IEEE, Oct. 2018, pp. 118– 124. DOI: 10.1109/wipda.2018.8569077.
17. J. Ferreira,W. Cronje, andW. Relihan, “Integration of high frequency current shunts in power electronic circuits,” in PESC ‘92 Record. 23rd Annual IEEE Power Electronics Specialists Conference, IEEE, 1992, pp. 1284–1290. DOI: 10.1109/pesc. 1992.254728.
18. M. Crescentini, S. F. Syeda, and G. P. Gibiino, “Hall-effect current sensors: Principles of operation and implementation techniques,” IEEE Sensors Journal, vol. 22, no. 11, pp. 10 137–10 151, Jun. 2022. DOI: 10.1109/jsen.2021.3119766.

19. N. Fritz, G. Engelmann, A. Stippich, C. L¨udecke, D. A. Philipps, and R. W. De Doncker, “Toward an in-depth understanding of the commutation processes in a SiC MOSFET switching cell including parasitic elements,” IEEE Transactions on Industry Applications, vol. 56, no. 4, pp. 4089–4101, Jul. 2020. DOI: 10.1109/tia.2020.2995331.
20. V. K. Krishnappa, C. Luedecke, J. Riedel and J. Fu, "Comparison of Short-Circuit Detection and Protection Methods for Silicon Carbide MOSFETs in EV Applications," PCIM Conference 2025; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nürnberg, Germany, 2025, pp. 1085-1092, doi: 10.30420/566541141.

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