Developer's Guide

TPS92520-Q1 Frame Definitions and Code Examples

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Table of Contents

Description

This document serves as a quick reference for Software or Firmware Engineers tasked with establishing and maintaining communications with the TPS92520-Q1 device. This document provides you with real code examples written in the C programming language designed to accelerate the learning curve required to effectively manipulate the various registers found in TPS92520-Q1 devices. All data sheet references are from the *TPS92520-Q1 4.5-V to 65-V Dual 1.6-A Synchronous Buck LED Driver with SPI Control Data Sheet*.

1 Build an SPI Transmission Frame

Create a valid frame based on address and data with parity.

```
Uint16 assembleSPICmd_520(Uint16 write, Uint16 address, Uint8 data)
{
    Uint16 assembledCmd = 0; // Build this to shift through parity calculation
    Uint16 parity = 0;       // Parity bit calculated here
    Uint16 packet = 0;       // This will be what we send

    if(write)
    {
        assembledCmd |= 0x8000;  // Set CMD = 1
    }

    assembledCmd |= (((address << 9) & 0x7E00) | (Uint16)(data & 0x00FF));
    packet = assembledCmd;

    // Calculate parity
    while(assembledCmd > 0)
    {
        // Count the number of 1s in the LSb
        if(assembledCmd & 0x0001)
        {
            parity++;
        }
        // Shift right
        assembledCmd >>= 1;
    }

    // If the LSb is a 0 (even # of 1s), we need to add the odd parity bit
    if(!(parity & 0x0001))
    {
        packet |= (1 << 8);
    }

    return(packet);
}
```

The following image illustrates the command frame section of the *TPS92520-Q1 4.5-V to 65-V Dual 1.6-A Synchronous Buck LED Driver with SPI Control Data Sheet*:

7.5.2 Command Frame

The command frames are the only defined frame-format that are sent from master to slave on MOSI. A command frame can be either a read command or a write command. A command frame consists of a CMD bit, six bits of ADDRESS, a PARITY bit (odd parity), and eight bits of DATA. Figure 39 shows the format of the command frame. The bit sequence is as follows:

1. The COMMAND bit (CMD). CMD = 1 means the transfer is a write command; CMD = 0 means it is a read command.
2. Six bits of ADDRESS (A5:A0)
3. The PARITY bit (PAR). This bit is set by the following equation: PARITY = XNOR(CMD, A5..A0, D7..D0).
4. Eight bits of DATA (D7..D0). For read commands, set the DATA bits to zero.

Both the read and the write command follow the command frame format.

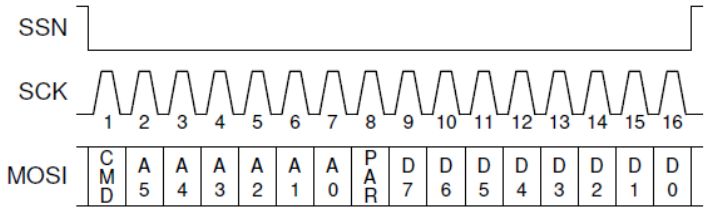

Figure 39. Command Frame Format

2 Response Frame

The command response frames are defined in the following portions of the *TPS92520-Q1 4.5-V to 65-V Dual 1.6-A Synchronous Buck LED Driver with SPI Control Data Sheet*.

The following image illustrates the response frame section of the data sheet:

7.5.3 Response Frame

There are three possible response frame formats: read response, write response, and write error/POR. These formats are further described in *Write Response Frame Format* through *Write Error/POR Frame Format*.

7.5.3.1 Read Response Frame Format

The read response has the following format:

1. The SPI Error bit (SPE)
2. Five reserved bits (always '11000')
3. The Power-Cycled bit (PC)
4. The Thermal Warning bit (TW)
5. Eight bits of DATA (D7..D0) (only valid if SPE = 0)

Figure 40 shows the read response format. The frame is sent out by the TPS92520-Q1 following a read command.

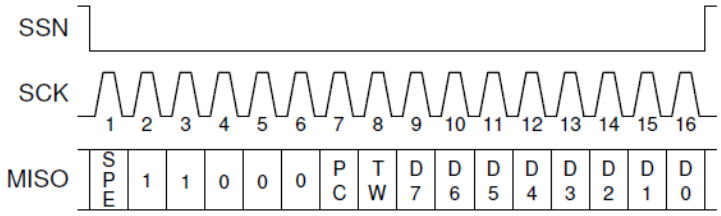

Figure 40. Read Response Frame Format

Command frame below is SPI MOSI and the response is found in SPI MISO below it. In this example the return (MISO) has a status byte of 0x60 with a data byte of 0x37. The result is a calculated value for VIN of approximately 14.

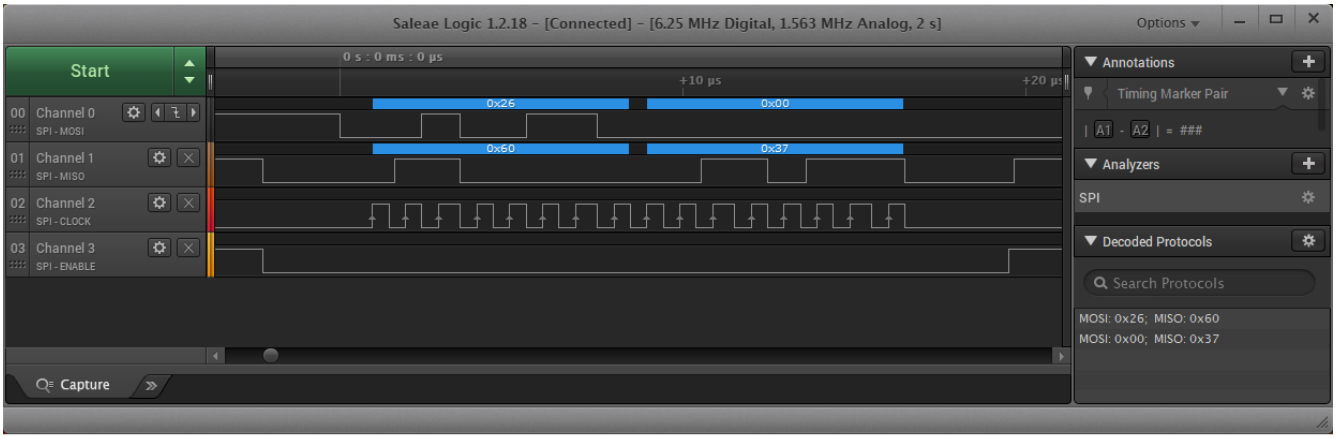

Figure 2-1. Example Read Register 0x13 CH1VIN ADC Measurement

The following image shows the write response frame format, write error/POR frame format SPI error sections from the data sheet:

7.5.3.2 Write Response Frame Format

The write response frame has the following format:

1. The SPI Error bit (SPE)
2. The COMMAND bit (CMD)
3. Six bits of ADDRESS (A5..A0)
4. Eight bits of DATA read from the destination register (D7..D0)

Figure 41 shows the write response format. This frame is sent out following a write command if the previously received frame was a write command and no SPI error occurred during that frame.

The data bits in the write response are read back from the destination register that was just written. There is no need to issue a read command and evaluate the read response in order to check that the destination register was written correctly.

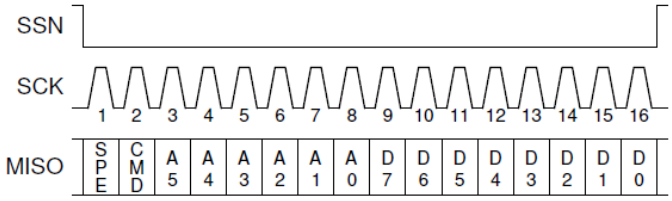

Figure 41. Write Response Frame Format

7.5.3.3 Write Error/POR Frame Format

The write error/POR frame is simply a '1' in the MSB followed by all zeroes (see Figure 42). This frame is sent out by the TPS92520-Q1 internal digital block during the first SPI transfer following power-on reset, or following a write command with a SPI Error.

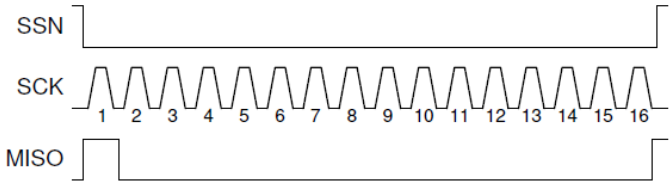

Figure 42. Write Error/POR Frame Format

7.5.4 SPI Error

The TPS92520-Q1 device records a SPI Error if any of the following conditions occur:

1. The SPI command has a non-integer multiple of 16 SCK pulses.
2. Any of the DATA bits during a read command are non-zero.
3. There is a parity error in the previously received command.

If any of these conditions are true, the TPS92520-Q1 sets the SPE bit high in the next response frame. A write command with a SPI error does not write to the register begin addressed. Similarly, a read command does not clear any active fault bits if the command has a SPI error. Additionally, if a read response has SPE = 1, the read data bits are invalid and must be disregarded.

Command frame below is SPI MOSI and the response is found in SPI MISO below it. In this example the return (MISO) has a status byte of 0x40 with a data byte of 0x00.

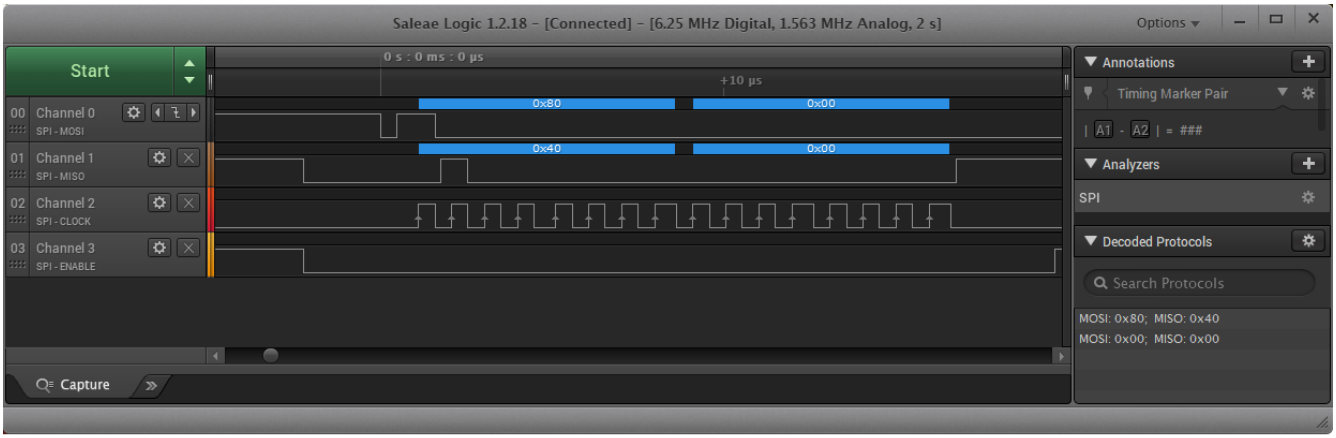

Figure 2-2. Example Write Register 0x00 SYSCFG1 to 0x00

3 Initialization

Note

The standalone communication watchdog timer is enabled by default. The 520 device will timeout after approximately 1.67 seconds without communication taking place on the 520 SPI bus putting the device in standalone mode.

Initialize the 520 device at power up with no watchdog before the default device timeout of approximately 1.67 seconds.

1. Read register 0x05 to clear the PC (Power Cycle) bit (D2).
   a. SPI Transmission Frame: assembleSPICmd_520(0, 0x05, 0x00);
2. Write byte 0x00 to register 0x00 to set bit D4 to 0, disabling the watchdog.
   a. SPI Transmission Frame: assembleSPICmd_520(1, 0x00, 0x00);

Initialize the 520 device at power up with no watchdog after the device has had a standalone communication timeout and is in standalone mode. To place the 520 device into load mode write a 0xC3 byte to register 0x2E to the 520 device.

1. Write byte 0xC3 to register 0x2E. With the device in load mode the watchdog timer will timeout after the time specified in register 0x02 has been exceeded 3 consecutive times. Complete step 2 before the watchdog timeout occurs or the device will go into limp home mode.
   a. SPI Transmission Frame: assembleSPICmd_520(1, 0x2E, 0xc3);
2. Write byte 0x00 to register 0x00 to set bit D4 to 0, disabling the watchdog.
   a. SPI Transmission Frame: assembleSPICmd_520(1, 0x00, 0x00);

Initialize the 520 device at power up with no watchdog after the device had a standalone communication timeout and is in standalone mode. To place the 520 device into detect mode write a 0xD4 byte to register 0x2E to the 520 device

1. Read register 0x05 to clear the PC (Power Cycle) bit (D2).
   a. SPI Transmission Frame: assembleSPICmd_520(0, 0x05, 0x00);
2. Write byte 0xD4 to register 0x2E, this will set the device communications timeout to approximately 1.67 seconds. Complete step 3 before the communications timeout occurs or the device will go into standalone mode.
   a. SPI Transmission Frame: assembleSPICmd_520(1, 0x2E, 0xD4);
3. Write byte 0x00 to register 0x00 to set bit D4 to 0, disabling the watchdog.
   a. SPI Transmission Frame: assembleSPICmd_520(1, 0x00, 0x00);

Initialize the 520 device at power up (Power On Reset) with watchdog. The following steps must be completed before the standalone communications timer times out in the default timeout time of approximately 1.67 seconds. After timeout the 520 device will go into standalone mode. To re-start the initialization process after timeout and return the 520 device to detect mode you must cycle the power or write a 0xD4 byte to register 0x2E to the 520 device.

1. Read register 0x05 to clear the PC (Power Cycle) bit (D2).
   a. SPI Transmission Frame: assembleSPICmd_520(0, 0x05, 0x00);
2. To change the default watchdog timeout value of approximately 1.67 seconds modify register 0x02 contents to select the desired watchdog timeout period otherwise continue to step 3.
   a. SPI Transmission Frame: assembleSPICmd_520(1, 0x02, 0xXX);

3. Repeatedly write or read a register within the specified period in step 2 in order to avoid triggering a watchdog timer time out event. Note that the 520 device will go into Limp Home mode after the watchdog timer has timed out 3 consecutive times.
4. For more information, see the *TPS92520-Q1 4.5-V to 65-V Dual 1.6-A Synchronous Buck LED Driver with SPI Control Data Sheet*.

The next image illustrates the following sections from the data sheet:

- Write Response Frame Format
- Write Error/POR Frame Format
- SPI Error

7.5.3.2 Write Response Frame Format

The write response frame has the following format:

1. The SPI Error bit (SPE)
2. The COMMAND bit (CMD)
3. Six bits of ADDRESS (A5..A0)
4. Eight bits of DATA read from the destination register (D7..D0)

Figure 41 shows the write response format. This frame is sent out following a write command if the previously received frame was a write command and no SPI error occurred during that frame.

The data bits in the write response are read back from the destination register that was just written. There is no need to issue a read command and evaluate the read response in order to check that the destination register was written correctly.

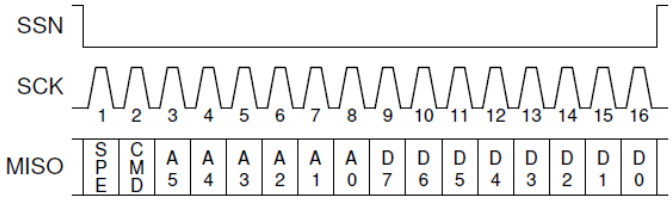

Figure 41. Write Response Frame Format

7.5.3.3 Write Error/POR Frame Format

The write error/POR frame is simply a '1' in the MSB followed by all zeroes (see Figure 42). This frame is sent out by the TPS92520-Q1 internal digital block during the first SPI transfer following power-on reset, or following a write command with a SPI Error.

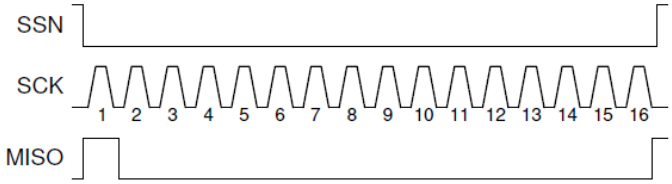

Figure 42. Write Error/POR Frame Format

7.5.4 SPI Error

The TPS92520-Q1 device records a SPI Error if any of the following conditions occur:

1. The SPI command has a non-integer multiple of 16 SCK pulses.
2. Any of the DATA bits during a read command are non-zero.
3. There is a parity error in the previously received command.

If any of these conditions are true, the TPS92520-Q1 sets the SPE bit high in the next response frame. A write command with a SPI error does not write to the register begin addressed. Similarly, a read command does not clear any active fault bits if the command has a SPI error. Additionally, if a read response has SPE = 1, the read data bits are invalid and must be disregarded.

The following image shows the functional modes illustration from the data sheet.

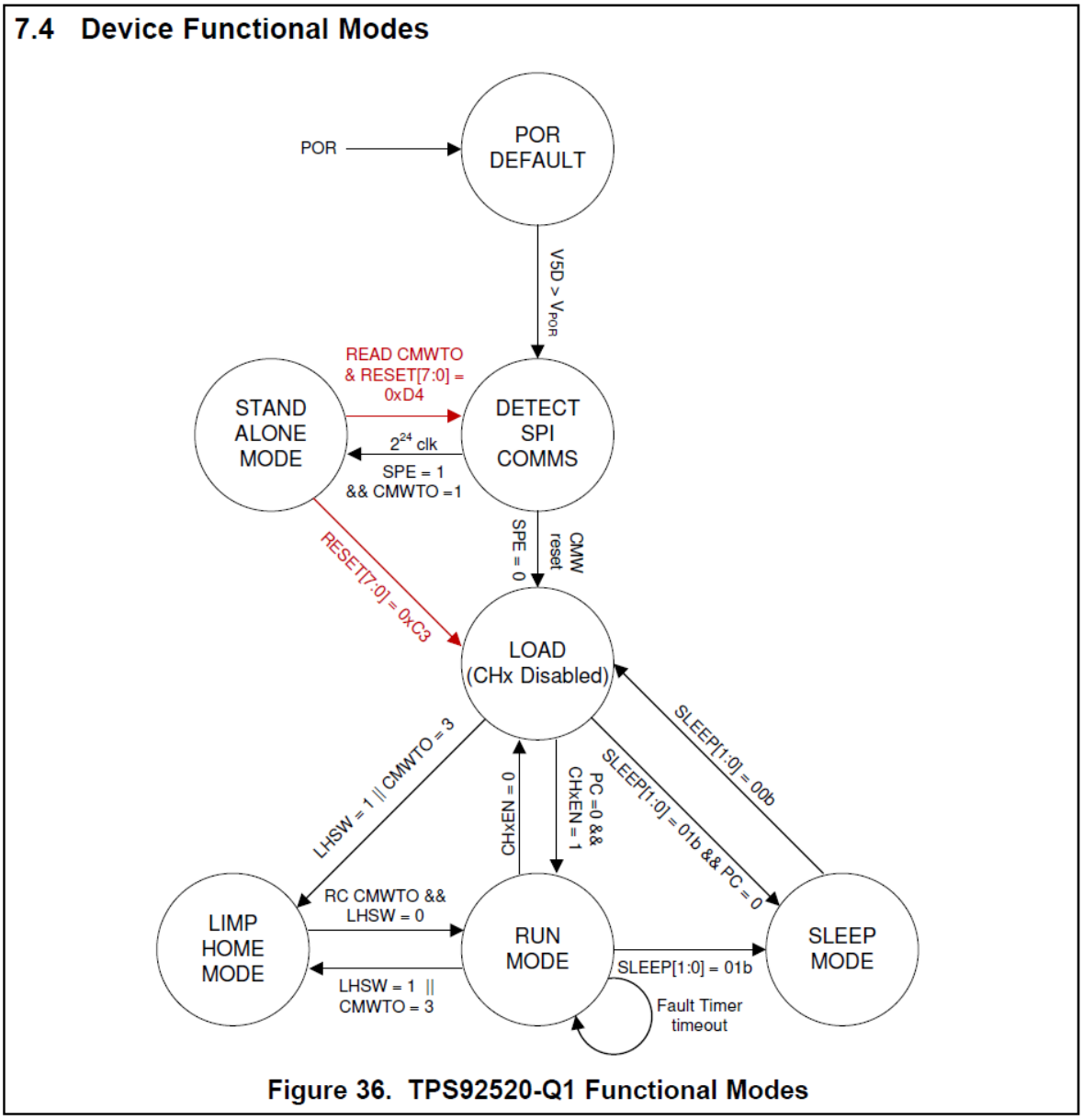

Figure 36. TPS92520-Q1 Functional Modes

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