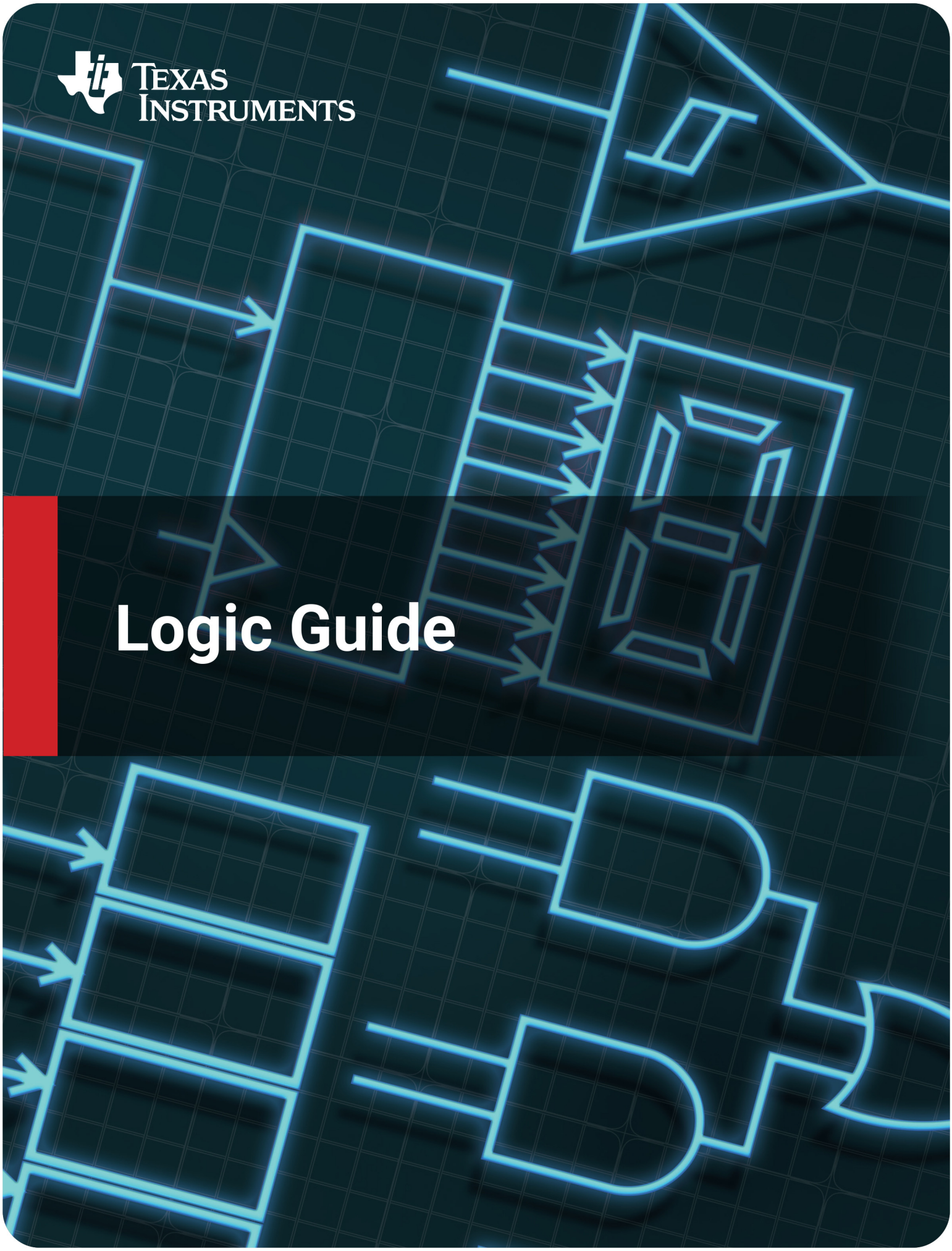
Texas Instruments
Logic Guide

Application Note

Logic Guide

Emrys Maier

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Trademarks

1 Introduction

As electronic systems become increasingly complex, designers face growing challenges in achieving excellent performance, power efficiency, and cost-effectiveness. As the world leader in logic, Texas Instruments (TI) provides a comprehensive portfolio of logic functions and technologies designed to address these demands. Our portfolio is built around advanced complementary metal-oxide semiconductor (CMOS) families – including HC, HCS, LVC, AUP, AHC(T), AC(T), and LV-A – offering an excellent balance of performance, power, and price for a wide range of applications.

We are committed to supporting our customers throughout the entire product lifecycle. While actively innovating with leading-edge CMOS technologies, we also understand the need to support existing designs utilizing mature logic families such as LS. Although older technologies like TTL, F, S, AS, ALS, and CD4000 remain available for specific requirements, our primary focus is on providing the latest CMOS technologies that enable smaller, faster, and more power-efficient designs.

Finding the right logic component can be challenging. If you are looking for a TI replacement product for an existing competitor part, please utilize our online cross-reference tool.

For a quick overview of our entire logic product offering, please visit our online logic landing page online logic landing page.

Today's applications demand greater functionality, smaller size, and lower power consumption. TI's goal is to help designers easily find the best logic technology or function, with a focus on delivering benchmark performance, reliability, and worldwide support. Our commitment to innovation and customer support makes TI a trusted partner for logic products, from leading-edge to mature technologies.

For technical support and to connect with the TI community, please post to the Engineer to Engineer (E2E) forums.

The E2E forums also host in-depth Frequently Asked Questions (FAQ) pages for logic and a separate page for FAQs on TPLD products FAQs on TPLD products.

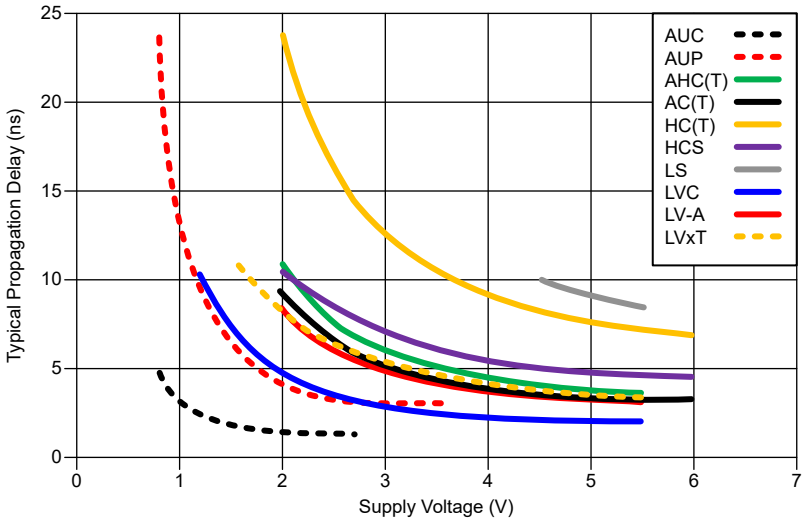


Figure 1-1. Logic Family General Speed Comparison

2 Logic Overview

2.1 Logic Family Quick Reference

Logic devices are separated by technology primarily by the logic family name. Figure 2-1 contains a quick reference for comparison of logic family performance metrics. See <section not done yet> for a listing of functions available in each family.

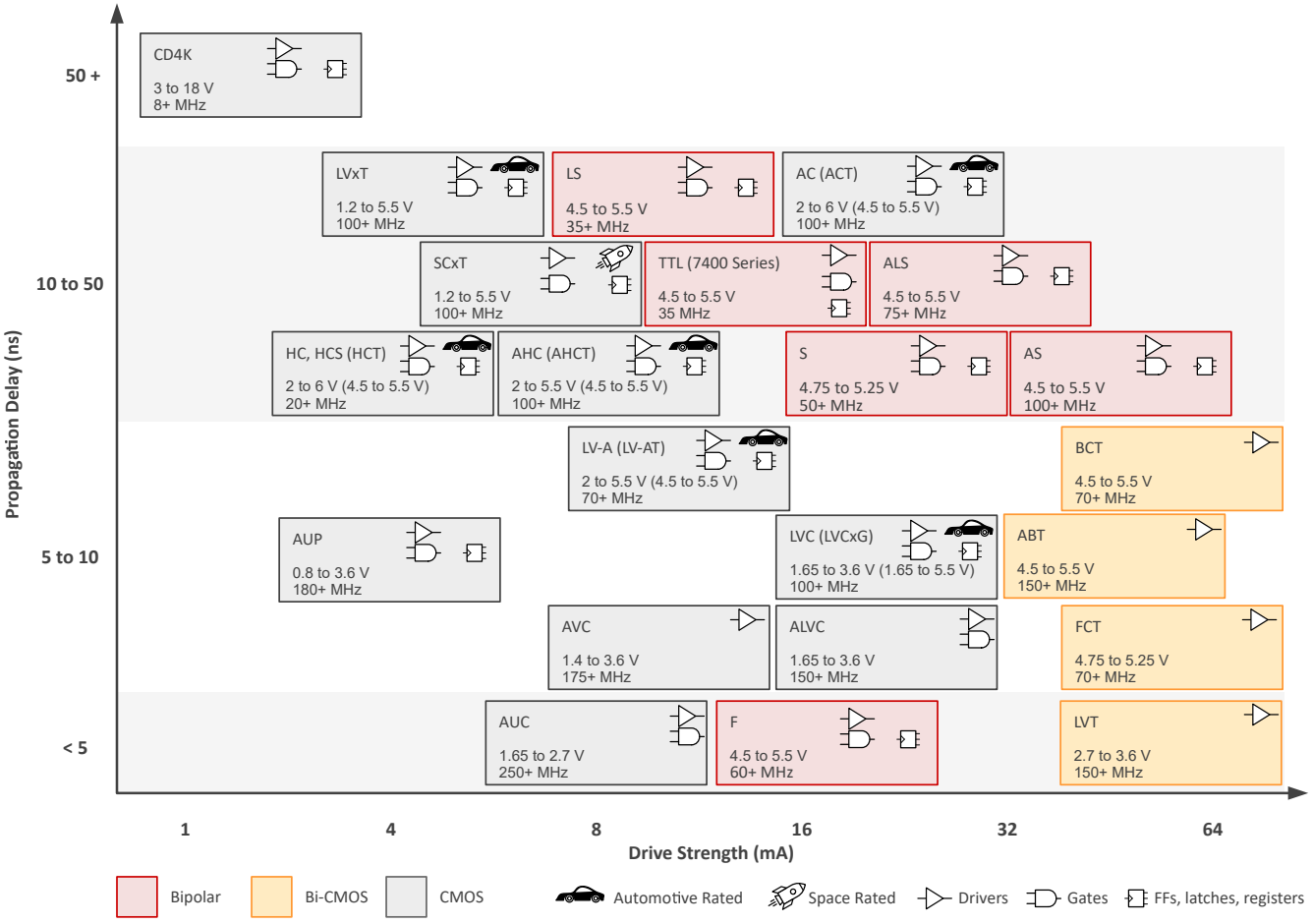


Figure 2-1. Logic Family Comparison Chart

2.2 Comparison of Switching Standards

The following figures provide a comprehensive comparison of different I/O standards for logic devices. Figure 2-2 illustrates the evolution of 5V I/O standards, from traditional TTL devices to advanced CMOS and Schmitt-trigger input devices, highlighting the differences in voltage thresholds and output levels.

Figure 2-3 provides a detailed comparison of multiple voltage standards, including 5V, 3.3V, 2.5V, 1.8V, 1.2V, and 0.8V, enabling easy evaluation and selection of the most appropriate I/O standard for a given application. The graphics show the minimum switching levels (V_{IH} and V_{IL}) for normal operation, as well as the approximate switching threshold (V_t) and output levels (V_{OH} and V_{OL}) for each supply voltage (V_{CC}) specified, enabling designers to make informed decisions about logic device selection.

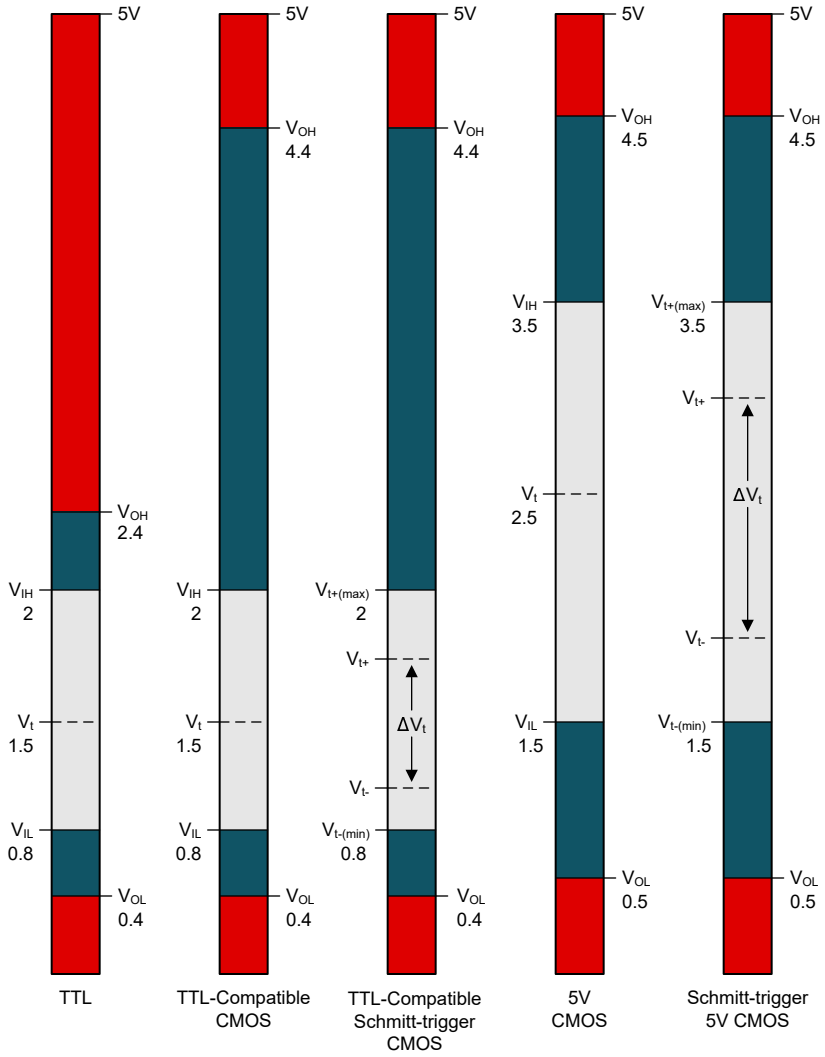


Figure 2-2. 5V Logic I/O Standards

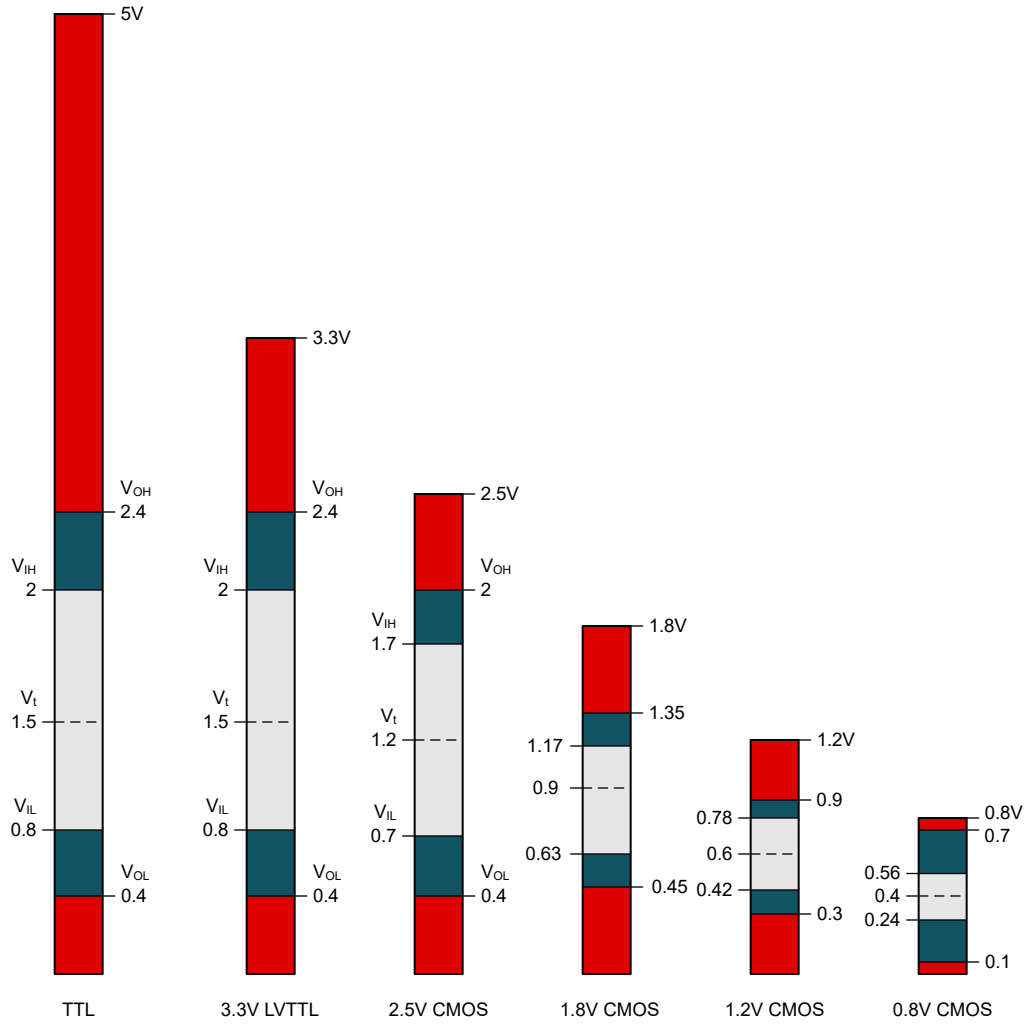


Figure 2-3. CMOS Logic I/O Standards

2.3 Automotive Logic

The Automotive Engineering Council (AEC) established the AEC-Q100 qualification standard for automotive-rated products, with contributions from semiconductor manufacturers like Texas Instruments (TI). This standard establishes a high level of component performance in harsh automotive environments. TI's automotive logic products, marked with a "Q1" in the part number, meet this stringent standard for reliability and performance in demanding automotive applications. Our portfolio offers a range of functions, providing designers with flexibility to maximize designs for specific applications and enable advanced automotive features. Products are available in various packages, including industry-standard and compact, small-form-factor options, allowing for efficient board layout and reduced footprint.

TI is dedicated to providing exceptional support to automotive customers. Industry-leading lead times and tightly controlled manufacturing processes support requirements for low defect rates. Rigorous design-flow checks promote long-term reliability, contributing to confidence in system performance and durability.

With a proven track record of supply continuity since 1964, and automotive-grade products since 1984, TI provides automotive customers with the assurance of a stable supply and reliable performance throughout the lifetime of vehicles.

Key Features

- AEC-Q100 Qualified Portfolio
- Broad portfolio with over 200 automotive qualified products
- Variety of package offerings to meet system needs from standard SOIC and TSSOP to the latest X2SON and X2QFN options
- Our vast network of production sites provides best-in-class lead times to our customers
- Excellent quality control checks are geared to achieve zero-DPPM requirements for automotive OEMs
- TI's design-flow checks provide long-term reliability expectations
- TI has a solid track record of supply continuity with products dating back to 1964 that are still available today

Common AEC-Q100 Qualification Tests

- Test group A: Accelerated environment stress test
  - A2 - Biased HAST (JESD22-A101/JESD22-A110)
  - A3 - Unbiased HAST (JESD22-A102/JESD22-A118)
  - A4 - Temperature cycle and post temp cycle bond pull (JESD22-A104, MIL-STD883 method 2011)
  - A6 - High temp storage bake (JESD22-A103)
- Test group B: Accelerated lifetime simulation test
  - B1 - High temperature operating life (JESD22-A108)
  - B2 - Early life failure rate (AEC Q100-008)
- Test group C: Package assembly integrity tests
  - C1 - Wire bond shear (AEC Q100-001)
  - C2 - Wire bond pull (MIL-STD883 method 2011)
  - C3 - Solderability (JEDEC J-STD-002)
  - C4 - Physical Dimensions (JESD22-B100 and B108)
  - C5 - Solder ball shear (AEC Q100-010)
- Test group D: Die fabrication reliability tests
  - D1 - Electromigration
  - D2 - Time dependent dielectric breakdown
  - D3 - Hot carrier injection
  - D4 - Bias temperature instability
  - D5 - Stress migration
- Test group E: Electrical verification
  - E2 - Electrostatic discharge (ESD) human body model (HBM) (AEC Q100-002)
  - E3 - Electrostatic discharge (ESD) charged device model (CDM) (AEC Q100-011)
  - E4 - Latch-up (AEC Q100-004)
  - E5 - Electrical distributions (AEC Q100-009)
- Visit Quality, reliability & packaging data download website for product specific details.

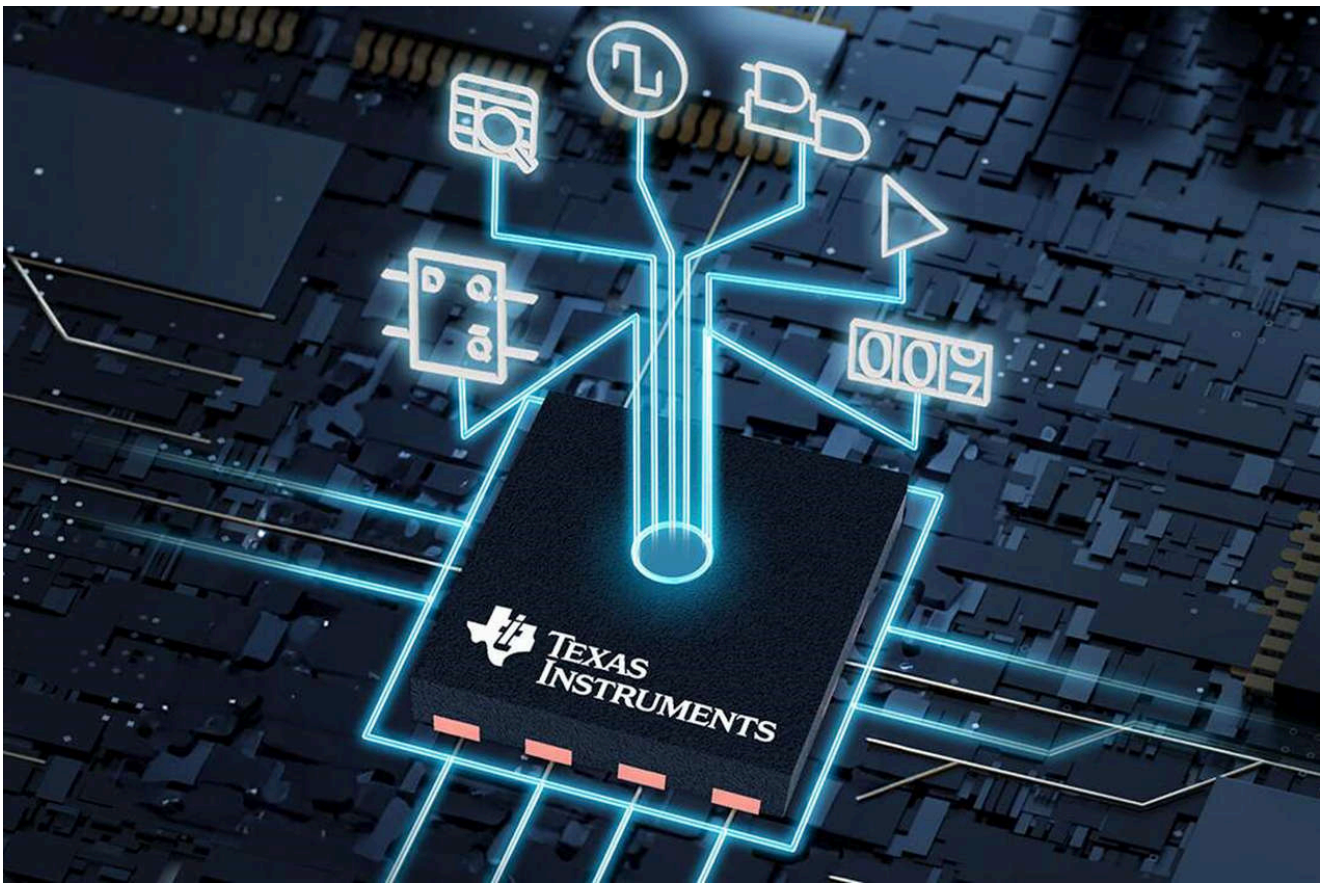
2.4 Ongoing Packaging Investment

TI continues to invest in the future of standard logic products with the latest VSSOP (DGS), SOT-23-THN (DYY), and X2QFN (DTX) packages.

VSSOP and SOT-23-THN packages provide 0.5mm pitch for maximum space savings while also maximizing manufacturability.

TI is not only investing in the standard logic space, but also in popular little logic functions. TI has released the newest and smallest next generation X2SON package (a.k.a. X2QFN) for 5-pin and 6-pin devices. The 5-pin DPW package is just 0.8 × 0.8 × 0.4 mm (0.5-mm pitch), whereas the 6-pin DTB package is only 0.8 × 1.0 × 0.4 mm (0.4-mm pitch)

2.5 TI's Programmable Logic Devices: TPLD



Texas Instruments proudly introduced the TPLD line of programmable logic devices in 2024, marking a new era for our logic portfolio. While TI has had the broadest portfolio of logic available on the market for some time, there are still niche logic requirements that come up for our customers, and TPLD products provide a fast and easy method to fill those gaps in our portfolio. Whether you need a 3-input NAND gate with one inverted input or a complex logic function, TPLD has you covered.

Table 2-1.

Key Features	Packaging Options
• Wide supply voltage range of 1.71 to 5.5V • I/Os are highly configurable with integrated pull-up and pull-down resistors, selectable input modes (Schmitt-trigger, low voltage threshold, standard), and selectable output modes (single/double drive strength, open-drain, 3-state) • Internal blocks are almost infinitely configurable using the connection mux • InterConnect Studio (ICS) provides GUI-based schematic hardware development • The TPLD programmer interfaces ICS to each EVM for rapid prototyping • Pre-configured devices can be ordered direct from TI	• SOT-5X3 (DRL; 8) • X2QFN (RWB; 12) • VSSOP (DGS; 10, 20) • UQFN (RJY; 20)

2.6 Function Table

Table 2-2. Function Offered by Family

Family[1]	Buffers & Inverters	Transceivers	Logic Gates	Configurable Gates	Flip-flops & Latches	Shift Registers	Digital Mux & Demux	Counters
AC	🚗	🚗	🚗	🚗	🚗	🚗	🚗	✓
ACT	🚗	🚗	🚗	🚗	🚗	🚗	🚗	✓
AHC	🚗	🚗	🚗		🚗	🚗	🚗	
AHCT	🚗	🚗	🚗		🚗	🚗	🚗	
ALVC	✓	✓	✓					
AUC	✓	✓	✓	✓	✓			
AUP	✓		🚗	✓	✓			
AUPxT	✓		✓	✓				
AVC	✓	✓			✓			
HC	🚗	✓	🚗		🚗	🚗	🚗	🚗
HCS	🚗	🚗	🚗		🚗	🚗	🚗	
HCT	🚗	✓	✓		🚗	🚗	✓	✓
LV-A	🚗	🚗	✓		🚗	🚗	🚗	🚗
LVxT	🚗	🚗	🚗	🚗	🚗	🚗	🚗	
LVC	🚗	✓	🚗	🚗	🚗	🚗	🚗	
LVT	🚗	🚗			🚗			

(1) ✓ = Commercial 🚗 = Commercial and Automotive (AEC-Q100)

3 Logic Families

3.1 Legacy Logic

Legacy Family Comparison

Texas Instruments continues to support a variety of legacy logic families to support those customers and products that have not yet updated to the latest and greatest technologies. This table provides a brief summary for comparison of our legacy logic family offerings.

Table 3-1.

Family Name	Example GPN	Recommended Replacement Family	Typical Supply Voltage (V)	Typical Static Supply Current (mA)	Switching Standard	Defining Features	Intro Year
Transistor-Transistor Logic (TTL)	SN7400	AHCT ACT HCT	5	12	TTL	First commercial integrated transistor-transistor logic	1966
Complimentary Metal-Oxide Semiconductor (CMOS) logic	CD4011B	AHC AC HC	3 to 18	0.001	CMOS	First CMOS logic family, originally introduced by RCA	1968
Schottky TTL	SN74S00	AHCT ACT HCT	5	20	TTL	Schottky diodes used to improve switching speeds	1969
Low-power Schottky TTL	SN74LS00	AHCT ACT HCT	5	2.4	TTL	Lower power version of the S family	1971
Fast Schottky TTL	SN74F00	AHCT ACT	5	6.8	TTL	Originally from Fairchild, included "miller-killer" circuit to improve low-to-high transition times	1978
Advanced low-power Schottky TTL	SN74ALS08	AHCT ACT HCT	5	1.5	TTL	Same technology as the AS family, but with reduced speed to improve power consumption	1980
Advanced Schottky TTL	SN74AS00	AHCT ACT	5	10.8	TTL	Improved version of the F logic family, producing the best speed to power ratio (Propagation Delay Product, PDP) available in any bipolar logic family	1982
Bipolar-CMOS (BiCMOS) logic	SN74BCT245	LVT ACT	5	57	TTL	High drive (+64/-15mA) bus buffers and transceivers, 5ns typical delay	1986
Fast CMOS	CY74FCT245T	LVT ACT	5	0.0001	TTL	High drive (+64/-32mA) bus buffers and transceivers, 3ns typical delay	1988
Advanced BiCMOS	SN74ABT245B	LVT ACT	5	30	TTL	High drive (+64/-32mA) bus buffers and transceivers, 2ns typical delay	1991

3.2 AC(T): Advanced CMOS

The AC family is TI's high-drive CMOS logic family supporting over 90MHz operation at 5V with up to 24mA of continuous current per output channel. The AC family contains a full complement of logic gates and registers while also supporting wide bus communications with higher channel count bus drivers. The ACT family has the same high speed and high drive capabilities of the AC family while providing TTL-compatible I/Os when operating from a 5V supply.

Key Features	Packaging Options
• Ultra-wide operating voltage from 1.5 to 6V • 90MHz+ capable (5V V_{CC}) • High drive outputs support 75mA bursts for up to 2ms • Positive input clamp diodes provide over-voltage protection • See all available logic gates here • See all available drivers here • See all available flip-flops, latches, and registers here	• PDIP (N; 14, 16, 20) • SOIC (D, DW; 14, 16, 20, 24, 28) • SOP (NS; 14, 16, 20) • SSOP (DB, DL; 14, 20, 48, 56) • TSSOP (PW; 14, 16, 20) • VQFN (RKS; 20) • VSSOP (DGS; 20) • WQFN (BQA, BQB; 14, 16)

Applications

- Solar energy
- Industrial automation
- Single and multi-axis servo drives
- Energy storage systems
- Hybrid and electric vehicle (HEV/EV) on-board charge (OBC)
- Retail automation
- Automotive electronics and lighting
- High performance computing
- Advanced driver assistance systems (ADAS)

3.3 AHC(T): Advanced High-Speed CMOS

The AHC family provides a natural migration for high speed CMOS (HC) users who need more speed for low-power, and low-drive applications. Unlike many other advanced logic families, AHC does not have the drawbacks that come with higher speed, e.g., higher signal noise and power consumption. The AHC logic family consists of gates, registers, and bus functions that feature higher performance than the HC product family at comparable cost. The AHCT family has the same high speed and low noise capabilities of the AHC family while providing TTL-compatible I/Os when operating from a 5V supply.

Key Features	Packaging Options
• Low noise without characteristic overshoot or undershoot • 115MHz+ capable (5V V_{CC}) • Inputs are over-voltage tolerant to 5V independent of V_{CC} • See all available logic gates here • See all available drivers here • See all available flip-flops, latches, and registers here	• PDIP (N; 14, 16, 20) • SOIC (D, DW; 14, 16, 20) • SOP (NS; 14, 16, 20) • SOT-23 (DBV; 5) • SOT-5X3 (DRL; 5) • SOT-SC70 (DCK; 5) • SSOP (DB, DL; 14, 16, 20, 48) • TSSOP (PW, DGG; 14, 16, 20, 48) • TVSOP (DGV; 14, 16, 20, 48) • VQFN (RGY, RKS; 14, 16, 20) • VSSOP (DGS; 20) • WQFN (BQA, BQB; 14, 16) • X2SON (DTX; 5)

Applications

- Hybrid and electric vehicle powertrain systems
- Automotive body electronics and lighting
- Broadband fixed line optical and copper
- Server motherboards
- Network switches and routers
- Advanced driver assistance systems (ADAS)
- Industrial automation

3.4 ALVC: Advanced Low-Voltage CMOS

While the ALVC family does include some logic gates, the family is primarily optimized for high speed communication bus applications, including up to 24-channel devices with bus hold and added damping resistors to enable wide-bus commuication systems.

Key Features	Packaging Options
• 8, 16, and 24 channel bus drivers, latches, and registers • Bus-hold option eliminates requirement for external pull-up or pull-down resistors • Damping resistors option improves impedance matching to 50Ω transmission lines for better signal integrity • Specified at 3.3V, 2.5V, and 1.8V supply • 150MHz+ capable (2.5 to 3.3V V_{CC}) • See all available logic gates here • See all available drivers here • See all available flip-flops, latches, and registers here	• SOIC (D, DW; 14, 20) • SOP (NS; 14, 20) • SSOP (DL; 48, 56) • TSSOP (PW, DGG; 14, 20, 48, 56, 64) • TVSOP (DGV, DBB; 14, 20, 48, 56, 80) • VQFN (RGY; 14, 20)

Applications

- Network switches and routers
- Industrial automation: PLC, DCS, PAC
- Power inverters
- Solar energy
- Server motherboards
- Medical imaging
- Hospital patient care
- Flat screen TV
- Scientific instrumentation

3.5 AUC: Advanced Ultra Low Voltage CMOS

The AUC family of logic is the fastest operating 1.8V family, utilizing multi-stage 50Ω impedance matching outputs that provide excellent signal integrity while switching faster than any other logic family. If you need high speed logic while operating at 1.8V, the AUC family is the best option.

Key Features	Packaging Options
• 1.8V optimized performance driving 50Ω microstrip directly • Typical delays under 1ns • V_{CC} specified at 2.5V, 1.8V, and 1.2V • 3.6V input tolerance • Specified for partial power down applications • See all available logic gates here • See all available drivers here	• SOT-23 (DBV, 5, 6) • SC-70 (DCK, 5, 6) • SOT-553 (DRL, 5, 6) • VQFN (RGY, 14, 20) • WCSP (YZP, 5, 6) • TSSOP (DGG, 48) • TVSOP (DGV, 48)

Applications

- PC and notebooks
- Data center and enterprise computing
- Mobile phones
- Gaming
- Wired networking
- Medical and healthcare

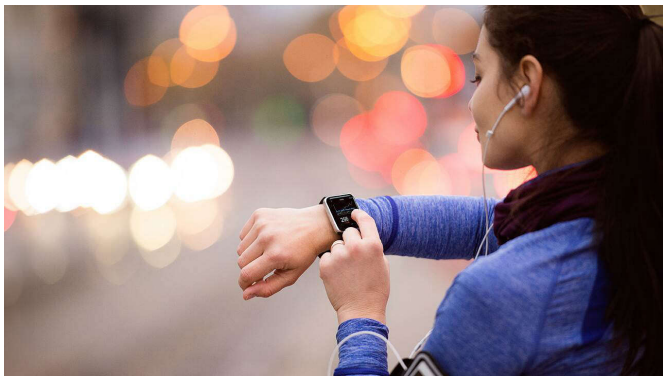
3.6 AUP: Advanced Ultra-Low Power

Designed to help extend battery life in portable applications, TI's AUP family of logic makes logic virtually unnoticeable in low voltage battery-powered system designs. The power savings include both static and active state power consumption, with over 90% savings over common CMOS families such as LVC.

Key Features	Packaging Options
• Ultra-low static power consumption (500nA MAX at 25°C) • Ultra-low dynamic power consumption (2.5pF typical C_{pd}) • 250MHz+ capable (3.3V V_{CC}) • Supports supply operation down to 0.8V • Input hysteresis (150mV typical at 3.3V V_{CC}) allows slow signal transitions and better noise immunity at the input • Partial power down support prevents back-drive • See all available logic gates here • See all available drivers here • See all available flip-flops, latches, and registers here	• SOT-23 (DBV; 5, 6) • SC-70 (DCK; 5, 6) • SOT-5X3 (DRL; 5, 6) • SSOP (DCT; 8) • UQFN (RSE; 8) • USON (DRY; 6) • VSSOP (DCU; 8) • X2SON (DPW, DSF; 5, 6) • WCSP (YFP, YZP; 4, 5, 6, 8)

Applications

- Wearables
- Mobile phone
- Tablet computer
- Digital and video cameras
- Digital photo frames
- Notebook PC
- Wireless LAN



3.7 AVC: Advanced Very-Low-Voltage CMOS

The AVC logic family is targeted at high speed wide-bus applications with several unique features to enhance communication capabilities.

Key Features

- Under 2ns max t_{pd} at 2.5V
- DOC™ (Dynamic Output Control) circuit dynamically changes output impedance, resulting in noise reduction without speed degradation
- Dynamic drive capability is equivalent to standard outputs with I_{OH} and I_{OL} of ±24mA at 2.5V
- 3.3V I/O tolerance
- Specified from 1.2 to 3.6V supply; optimized for 1.8V, 2.5V, or 3.3V
- Partial-power-down support prevents back-powering
- See all available drivers here
- See all available flip-flops, latches, and registers here

Packaging Options

- TSSOP (DGG; 48, 56, 64)
- TVSOP (DGV; 48, 56)

Applications

- High-performance workstations
- PCs
- Networking servers
- Telecommunication equipment

3.8 HC(T): High-Speed CMOS

The HC family was designed to provide improved switching speed and lower power consumption compared to earlier bipolar logic families. The HCT family has the same capabilities of the HC family while providing TTL-compatible I/Os when operating from a 5V supply for systems that still use some TTL devices. The HC and HCT familes are a staple of digital logic design, providing balanced performance and one of the broadest function sets available today.

Key Features	Packaging Options
• Optimized for 5V operation; capable of operation from 2V to 6V • Positive and negative clamp diodes on all I/O pins • Low power CMOS design • Balanced output drive • See all available logic gates here • See all available drivers here • See all available flip-flops, latches, and registers here	• PDIP (N; 14, 16, 20) • SOIC (D, DW; 14, 16, 20) • SOP (NS; 14, 16, 20) • SOT-23 (DBV; 5) • SOT-5X3 (DRL; 5) • SOT-SC70 (DCK; 5) • SSOP (DB, DL; 14, 16, 20, 48) • TSSOP (PW, DGG; 14, 16, 20, 48) • TVSOP (DGV; 14, 16, 20, 48) • VQFN (RGY, RKS; 14, 16, 20) • VSSOP (DGS; 20) • WQFN (BQA, BQB; 14, 16) • X2SON (DTX; 5)

Applications

- Hybrid and electric vehicle powertrain systems
- Engine management
- Residential air conditioner
- Automation in HVAC systems
- Major applicances
- Infotainment and digital cluster
- Industrial automation

3.9 HCS: High-Speed CMOS with Schmitt-trigger inputs

The HCS family was designed as an expansion to the HC family portfolio, maintaining compatibility with existing HC devices while integrating Schmitt-trigger inputs into every logic function. There are many benefits to Schmitt-trigger inputs including: greater tolerance to slow inputs, improved noise margins, and reduced power consumption.

Key Features	Packaging Options
• Schmitt-trigger inputs for all functions • Expanded catalog temperature range: -55°C to 125°C • Optimized for 5V operation; capable of operation from 2V to 6V • Positive and negative clamp diodes on all I/O pins • Low power CMOS design • Balanced output drive • See all available logic gates here • See all available drivers here • See all available flip-flops, latches, and registers here	• SOIC (D; 14, 16) • SOT-23-THN (DYY; 14, 16) • TSSOP (PW; 14, 16, 20) • VQFN (RKS; 20) • VSSOP (DGS; 20) • WQFN (BQA, BQB; 14, 16)

Applications

- Hybrid and electric vehicle powertrain systems
- Engine management
- Residential air conditioner
- Automation in HVAC systems
- Major applicances
- Infotainment and digital cluster
- Industrial automation

3.10 LV-A(T): Low Voltage

The LV-A logic family was designed to support 2.5, 3.3, and 5V with similar signal performance characteristics to the high drive AC family while providing power consumption and drive strength numbers similar to the HC family. The LV-AT family provides TTL-compatible inputs while operating with a 5V supply.

Key Features	Packaging Options
• Schmitt-trigger inputs for all functions • Expanded catalog temperature range: -55°C to 125°C • Optimized for 5V operation; capable of operation from 2V to 6V • Positive and negative clamp diodes on all I/O pins • Low power CMOS design • Balanced output drive • See all available logic gates here • See all available drivers here • See all available flip-flops, latches, and registers here	• PDIP (N, 20) • SOIC (D, DW; 14, 16, 20) • SOP (NS; 14, 16, 20) • TSSOP (PW; 14, 16, 20) • TVSOP (DGV; 14, 16, 20) • VQFN (RGY, RKS; 14, 16, 20) • VSSOP (DGS; 20) • WQFN (BQA, BQB; 14, 16)

Applications

- Portable electronics
- Buffer memory address registers
- Bidirectional bus drivers
- I/O ports

3.11 LVxT: Low-Voltage CMOS Single Supply Translating Logic

The LVxT family combines common logic functions with a very flexible input voltage range to support a wide variety of up- and down-translation applications. Built to match most closely to the AHC family for performance, the LVxT family provides a simple way to interface different logic levels to a single supply system.

Key Features

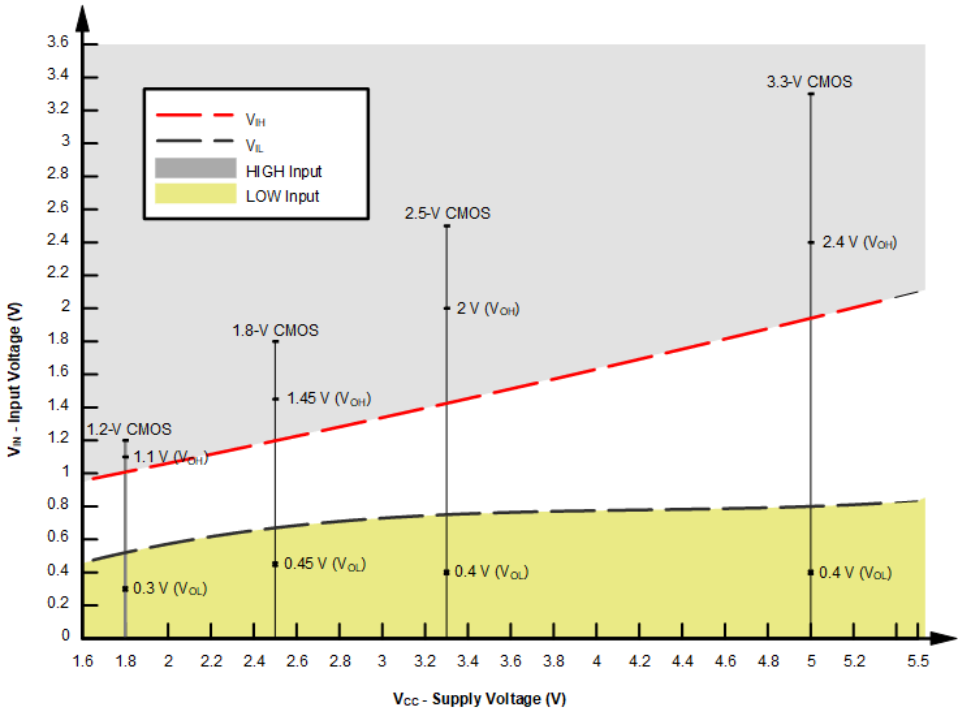
- Wide operating range of 1.65V to 5.5V
- Up translation:
  - 1.2V to 1.8V
  - 1.5V to 2.5V
  - 1.8V to 3.3V
  - 3.3V to 5.0V
- Down translation:
  - 5.0V, 3.3V, 2.5V to 1.8V
  - 5.0V, 3.3V to 2.5V
  - 5.0V to 3.3V
- See all available logic gates here
- See all available drivers here
- See all available flip-flops, latches, and registers here

Packaging Options

- SOT-23 (DBV; 5)
- SC-70 (DCK; 5)
- TSSOP (PW; 14, 16)
- X2SON (DPW, DSF; 5, 6)
- WQFN (BQA, BQB; 14, 16)

Applications

- Computing
- Wearables
- Personal Electronics
- Automotive and industrial
- Notebook



3.12 LVC: Low-Voltage CMOS

With over 130 functions available in a wide variety of packages, the LVC logic family is by far the largest and most diverse family of logic available today. The LVC family has been called the "swiss army knife" of logic, supporting almost any general logic requirement. Without a doubt the LVC family of logic contains a diverse function set for any system designer.

Key Features	Packaging Options
• Big logic (14+ pins) supports 1.65 to 3.6V operation • Little logic (4 to 8 pins) supports 1.65 to 5.5V operation • Over-voltage tolerant inputs support 5V signals independent of V_{CC} • Partial power down support prevents back-powering • Partial power down support prevents back-drive • See all available logic gates here • See all available drivers here • See all available flip-flops, latches, and registers here	• DSBGA (YFP, YZT, YZV, YZP; 4, 5, 6, 8) • JRBGA (ZQL; 56) • NFBGA (NMJ; 96) • PDIP (P, N; 8, 20) • SOIC (D, DW; 14, 16, 20, 24) • SOP (NS; 14, 16, 20) • SOT-23 (DBV; 5, 6) • SOT-5X3 (DRL; 5, 6) • SOT-SC70 (DCK; 5, 6) • SSOP (DCT, DB, DBQ, DL; 8, 14, 16, 20, 24, 48, 56) • TSSOP (PW, DGG; 14, 16, 20, 24, 48, 56) • TVSOP (DGV; 14, 16, 20, 24, 48, 56) • UQFN (RSE, RSV; 8, 16) • USON (DPK, DRY; 5, 6) • VQFN (RGY; 14, 16, 20) • VSSOP (DCU; 8) • WQFN (BQA, BQB; 14, 16) • X1QFN (RWP; 20) • X2SON (DPW, DSF, DQE; 5, 6, 8)

Applications

- Portable electronics
- Telecommunications equipment
- Networking servers
- Routing, clock buffering, and muxing
- Personal computing

3.13 LVT: Low-Voltage BiCMOS Technology

The LVT logic family was designed in a submicron BiCMOS process to be the successor to the ABT family with 90% improved static power consumption, live insertion support, and mixed-mode voltage operation.

Key Features	Packaging Options
• Over-voltage tolerant inputs support 5.5V independent of supply voltage • Supply voltage range from 2.7V to 3.6V • Power-up 3-state and partial power down support for live insertion applications • Rail-to-rail output drive for CMOS compatibility • Fast operation with t_{pd} < 5ns • See all available drivers here	• SOIC (D, DW; 14, 20, 24) • SOP (NS; 14, 20, 24) • SSOP (DB; 14, 20, 24) • TSSOP (PW, DGG; 14, 20, 24, 48, 56, 64) • TVSOP (DGV; 14, 20, 48) • VQFN (RGY; 14, 20)

Applications

- Computing
- Wearables
- Personal electronics
- Automotive and industrial

4 Appendix A: Logic Packages

Note: Pictures are not to scale

Table 4-1. 5-8 Pin Packages

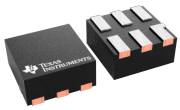
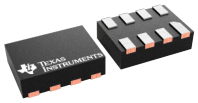
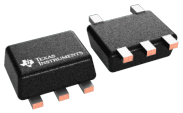
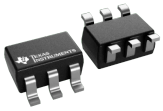
Pin Count	5	6	8
X2SON Pitch: 0.48 mm, 0.35 mm	0.8 × 0.8 mm (0.48 mm)  **DPW 5**	1.0 × 1.0 mm (0.35 mm)  **DSF 6**	1.4 × 1.0 mm (0.35 mm)  **DQE 8**
VSSOP Pitch: 0.5 mm			2.3 × 2.0 mm  **DCU 8**
SOT-5X3 Pitch: 0.5 mm	1.6 × 1.2 mm  **DRL 5**	1.6 × 1.2 mm  **DRL 6**	
USON Pitch: 0.5 mm		1.45 × 1.0 mm  **DRY 6**	
SOT-SC70 Pitch: 0.65 mm	2.0 mm × 1.25 mm  **DCK 5**	2.0 mm × 1.25 mm  **DCK 6**	
SSOP Pitch: 0.65 mm			2.95 × 2.8 mm  **DCT 8**
SOT-23 Pitch: 0.95 mm	2.9 × 1.6 mm  **DBV 5**	2.9 × 1.6 mm  **DBV 6**	

Table 4-2. 14-24 Pin Packages

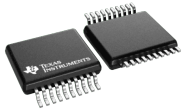
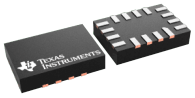
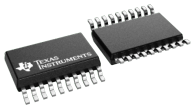
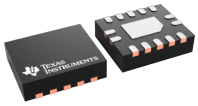
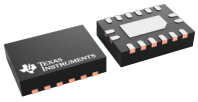
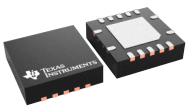
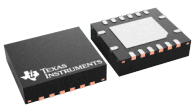
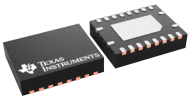
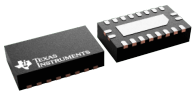
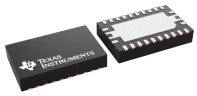
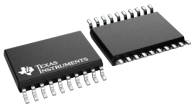
Pin Count	14	16	20	24
TVSOP Pitch: 0.4 mm	3.6 × 4.4 mm  **DGV 14**	3.6 × 4.4 mm  **DGV 16**	5.0 × 4.4 mm  **DGV 20**	5.0 × 4.4 mm  **DGV 24**
UQFN Pitch: 0.4 mm		2.6 × 1.8 mm  **RSV 16**		
VSSOP Pitch: 0.5 mm			8.1 × 3.0 mm  **DGS 20**	
SOT-23-THN Pitch: 0.5 mm	4.2 × 2.0 mm  **DYY 14**	4.2 × 2.0 mm  **DYY 16**		
WQFN Pitch: 0.5 mm	 **BQA 14** 3.0 × 2.5 mm	 **BQB 16** 3.0 × 2.5 mm		
VQFN Pitch: 0.5 mm	3.5 × 3.5 mm  **RGY 14**	4.0 × 3.5 mm  **RGY 16**	4.5 × 3.5 mm  **RGY 20** 4.5 × 2.5 mm  **RKS 20**	5.5 × 3.5 mm  **RGY 24** 5.5 × 3.5 mm  **RHL 24**

Table 4-2. 14-24 Pin Packages (continued)

Pin Count	14	16	20	24
SSOP Pitch: 0.65 mm	6.2 × 5.3 mm  **DB 14**	6.2 × 5.3 mm  **DB 16**	7.2 × 5.3 mm  **DB 20**	8.2 × 5.3 mm  **DB 24**
TSSOP Pitch: 0.65 mm	 **PW 14** 5.0 × 4.4 mm	 **PW 16** 5.0 × 4.4 mm	 **PW 20** 6.5 × 4.4 mm	 **PW 24** 7.8 × 4.4 mm
SOIC Pitch: 1.27 mm	8.65 × 3.91 mm  **D 14**	9.9 × 3.91 mm  **D 16** 10.3 × 7.5 mm  **DW 16**	12.8 × 7.5 mm  **DW 20**	15.4 × 7.5 mm  **DW 24**
SOP Pitch: 1.27 mm	10.3 × 5.3 mm  **NS 14**	10.3 × 5.3 mm  **NS 16**	12.6 × 5.3 mm  **NS 20**	15.0 × 5.3 mm  **NS 24**

5 Appendix B: Competitor Family Cross Reference

The following tables show corresponding family names for other major semiconductor manufacturers. TI also provides an online cross reference tool that can be accessed from:

Table 5-1. CMOS Logic Family Cross Reference

TI	Nexperia	Onsemi	Toshiba	Diodes
AC		AC	AC	
AHC	AHC		SH, WH, VHC	AHC
ALVC	ALVC	ALVC		
AUC		NL17SV, NL27WZ	TC7SA	
AUP	AUP	AUP, NC7SP		AUP
AVC		NC7SV, NC7WV		AVC
CD4K	HEF	MC14K		
HC	HC	HC, VHC	W, HC	HC
HCS	HCS			
LV-A	LV			LV-A
LVC	LVC	LCX, VCX, NC7SZ, NC7WZ	SZ, LCX	LVC

Table 5-2. TTL and TTL-Compatible CMOS Logic Family Cross Reference

TI	Nexperia	Onsemi	Toshiba	Diodes
ABT	ABT			
ACT		ACT	ACT	AHCT
AHCT	AHCT		SET, VHCT	HCT
HCT	HCT	HCT, VHCT, NC7ST	HCT	LVT
LVT		LVT		
LVxT	LVxT			

6 Appendix C: Logic Part Number Naming Conventions

The majority of products in logic follow a consistent naming format that can help you quickly find or identify products.

The inclusion of an option does not necessarily indicate that the option is available or implemented. Not all combinations and exceptions are listed.

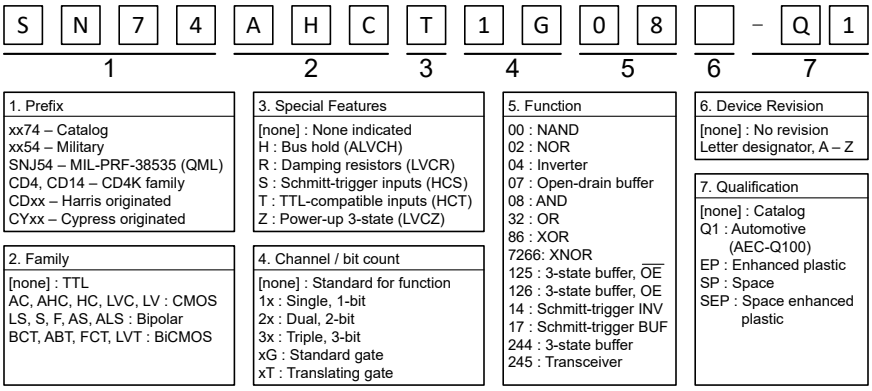


Figure 6-1. Generic Part Number (GPN) naming convention for general purpose logic devices

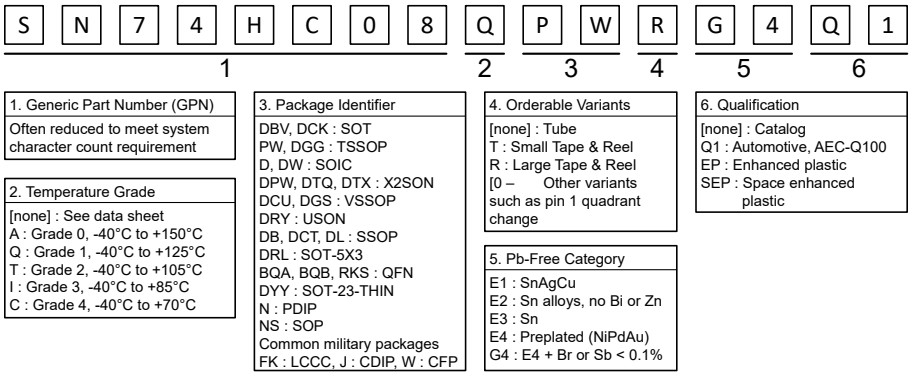


Figure 6-2. Orderable Part Number (OPN) naming convention for general purpose logic devices

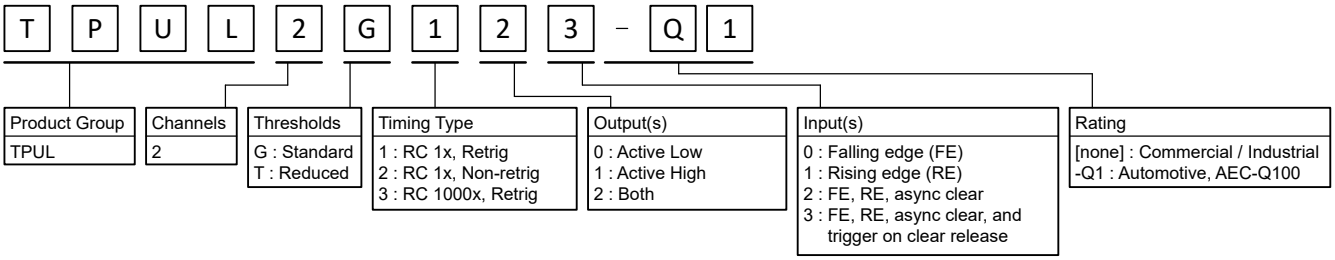


Figure 6-3. GPN naming convention for the TPUL family of logic devices

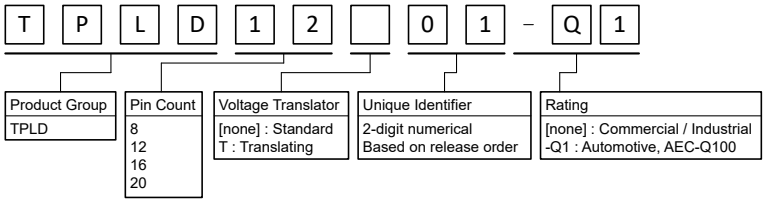


Figure 6-4. GPN naming convention for the TPLD family of programmable logic devices

7 Appendix D: Standard Logic Functions

Logic functions are typically indicated by a code in the part number. The below list provides a quick reference for commonly used functions. Open-collector and open-drain outputs are both listed as "open-drain" for brevity.

Configurable Logic

- TPLD
  - Programmable logic devices, learn more here
  - See TPLD naming conventions for device nomenclature
- 57, 58, 97, 98, 99: Pin configurable logic gates
  - See Utilizing Configurable Logic in System Design for details

Gates

- 00: 2-input NAND gates
  - 01: Open-drain
  - 03: Open-drain (alternate pinout)
  - 10: 3-Input
  - 20: 4-Input
  - 30: 8-Input
  - 38: Open-drain
- 02: 2-Input NOR gates
  - 27: 3-Input
  - 33: Open-drain
- 04: NOT gates (inverters)
  - 05: Open-drain
  - 06: Open-drain
  - 14: Schmitt-trigger
- 08: AND gates
  - 09: Open-drain
  - 11: 3-input
  - 21: 4-input
  - 7001: Schmitt-trigger input
- 32: OR gates
  - 7032: Schmitt-trigger
- 86: 2-Input XOR gates
- 7266: 2-Input XNOR gates
  - 266: open-drain

Flip-Flops, Latches, and Registers

- 74: D-type flip-flops with preset and clear
  - 72: Negative-edge triggered
  - 273: Octal DFFs with shared clock and clear
  - 374: Octal DFFs with shared clock and 3-state outputs
  - 573: 374 function with flow-through pinout
- 112: JK flip-flop, edge triggered
  - 107: Negative edge triggered
  - 109: Level triggered
- 373: D-type latches with shared latch enable and 3-state outputs
  - 573: Flow-through pinout
- 161: 4-Bit counter, synchronous and presettable, asynchronous clear
  - 163: Synchronous clear
- 164: 8-Bit parallel-out shift register
- 165: 8-Bit parallel-in shift register
  - 166: Clear instead of inverted output
- 595: 8-Bit parallel-out shift register with output registers and 3-state outputs

  - 594: Output register clear instead of 3-state outputs
  - 596: Open-drain outputs
- 299: 8-I/O universal shift register
- 193: 4-Bit up/down counter, synchronous
- 393: 4-bit ripple counter
- 4020: 14-Bit counter
- 4040: 12-Bit counter
- 4060: 14-Bit counter with oscillator

Buffers, Drivers, and Transceivers

- 07: Open-drain
- 17: Schmitt-trigger
- 34: Standard logic buffer
- 125: 3-State outputs
  - 126: 3-State outputs, active-high output enable
- 244: Bus buffers, banks of four with 3-state outputs
  - 240: Inverted outputs
  - 241: One active-low output enable and one active-high output enable
  - 540: 240 with flow-through pinout
  - 541: Flow-through pinout
  - 7541: 541 with open-drain outputs
  - 8541: 541 with Schmitt-trigger inputs
- 245: Transceivers (selectable direction buffers, A to B or B to A)

Specialty Logic

- 123: Monostable multivibrator (one-shot), retriggerable
  - 221: Monostable multivibrator (one-shot), non-retriggerable
  - See TPUL naming conventions for updated monostable multivibrator function numbering
- 4046: Digital PLL
- 684: 8-Bit magnitude comparator with equal and greater outputs
  - 682: Input pull-up resistors
  - 688: Only equal output

8 Revision History

Changes from Revision AB (June 2017) to Revision AC (November 2025)	Page
• Changed format from marketing white paper to application note	2

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