

Application Note

AFE7920 PLL Alarm at High Temperature and Design



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ABSTRACT

This report introduces the cause and design when the AFE7920 PLL alarm occurs at a specific temperature. Since the AFE7920 is a complex IC that integrates various digital and analog blocks, effectively identifying and resolving the cause when an alarm occurs is one of the most important factors. While there are various reasons why a PLL alarm can occur, this application report demonstrates the basic operating principles of the PLL and explains why the PLL unlock phenomenon occurs only at a specific temperature.

Table of Contents

1 Introduction.....	2
2 Issue Phenomenon and Observations.....	3
3 Introduction to Phase Locked Loop (PLL).....	3
4 Design.....	4
5 Summary.....	5
6 References.....	5

1 Introduction

The AFE79xx is a family of high performance, wide bandwidth multichannel transceivers, integrating four RF sampling transmitter chains, four RF sampling receiver chains, and up to two RF sampling digitizing auxiliary chains (feedback paths). The high dynamic range of the transmitter and receiver chains allows the device to generate and receive 3G, 4G, and 5G signals from wireless base stations, while the wide bandwidth capability of the AFE79xx devices is designed for multiband 4G and 5G base stations. Each receiver chain includes a 25dB range DSA (Digital Step Attenuator), followed by a 3GSPS ADC (analog-to-digital converter). Each receiver channel has an analog peak power detector and various digital power detectors to assist an external or internal autonomous automatic gain controller, and RF overload detectors for device reliability protection. The single or dual digital down converters (DDC) provide up to 600MHz of combined signal BW.

Figure 1-1 shows the AFE7920/AFE7921 functional block diagram including the PLL block. The AFE79xx has an internal PLL with four separate VCOs to generate the clock at the DAC sample rate. For operation, the FREF frequency and size that conform to the specification must be input as a differential signal to the CLKIN +/- pin.

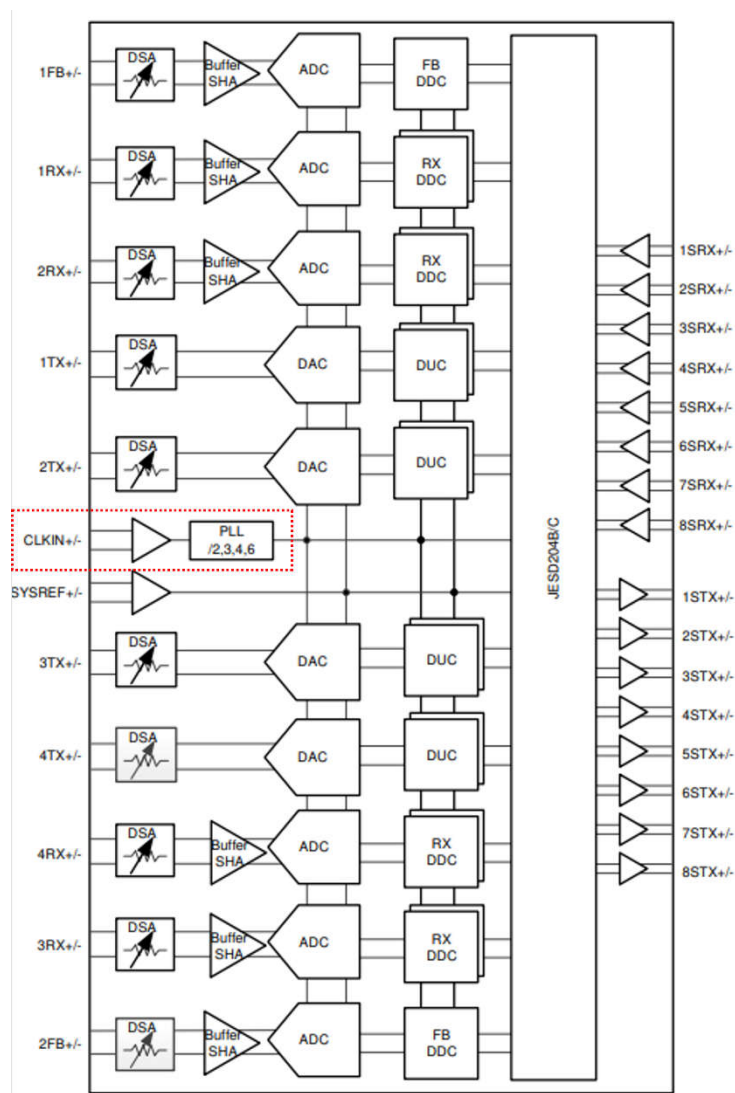


Figure 1-1. AFE792x Functional Block Diagram

2 Issue Phenomenon and Observations

Issue Phenomenon

AFE7920 alarm pin triggered during system operation and PLL alarm was masked when detail alarm register checked. AFE7920 has an internal temperature sensor to monitor the internal temperature of the device. When reading the temperature of the AFE, the read through temperature sensor was 110°C in the failure temperature condition.

Observations in Debug

PLL lock status was read back which showed that the PLL_LOCK is OK but PLL_LOCK_LOST_STICKY was triggered, implying that lock was lost momentarily, thereby triggering the PLL alarm disturbed the FB data path of the AFE7920, causing the FB overpower issue. Further, PLL V_{ctrl} was brought onto the Aux ADC, inside AFE, and was measured to be the edge of high V_{ctrl} range. The limits on V_{ctrl} for the PLL to remain in lock are from 0.2V to 1.55V.

3 Introduction to Phase Locked Loop (PLL)

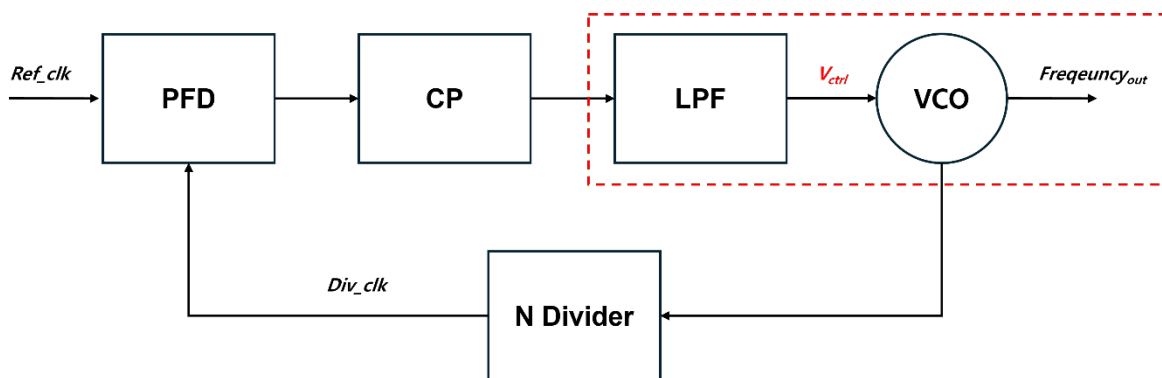


Figure 3-1. Generic Block Diagram of AFE PLL

A phase-locked loop (PLL) consists of a phase frequency detector (PFD), a charge pump (CP), a low-pass filter (LPF), a voltage-controlled oscillator (VCO), and an N divider. The problematic part of this issue is the range of V_{ctrl} that comes from the LPF output and is connected to the VCO input.

To verify the lock across temperature during calibration the V_{ctrl} voltage has to be set to a reference target voltage (V_{ref}). This V_{ref} is a voltage that scales linearly with temperature and is trimmed on ATE. V_{ref} is a reference voltage while V_{ctrl} is the tuning voltage for VCO of PLL. During the initial PLL calibration step at bring up, the cap bank in VCO is adjusted such that the VCO outputs desired frequency when $V_{ctrl} = V_{ref}$. Offsetting by 200mV in the V_{ref} offsets V_{ctrl} by 200mV. Offsetting V_{ref} is only a functional fix to make sure that the PLL locks across temperature and does not affect the performance of the AFE.

4 Design

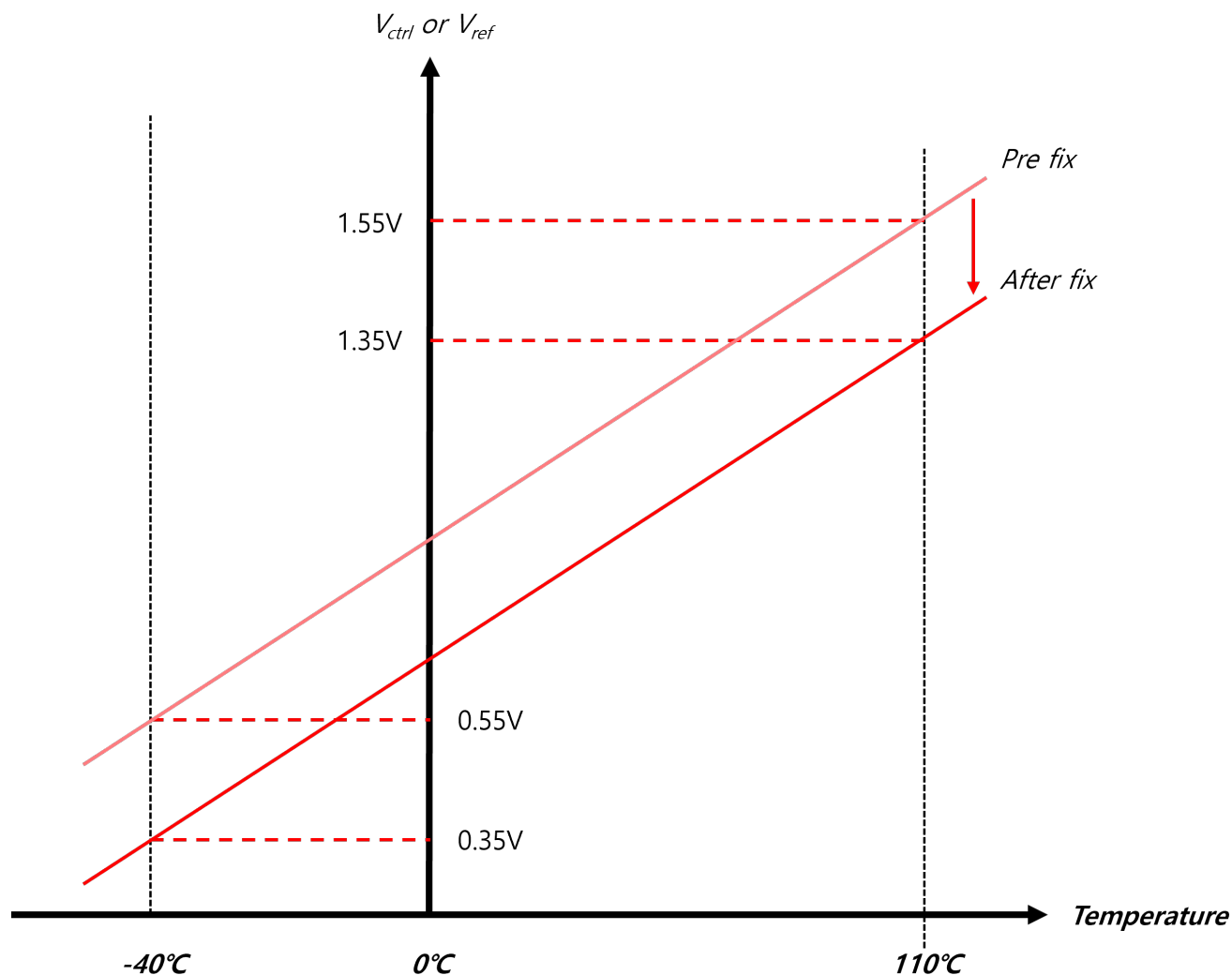


Figure 4-1. Graph Illustrating A Fix

V_{ctrl} of measured value from the customer is therefore marginally close to a higher limit, resulting in a momentary PLL unlock. A better margin on at hot temperature is required. Offsetting □ by approximately 200mV is suggested as a fix.

V_{ctrl} can range from (lower limit at cold temp of -40°C while higher at hot temperatures at 125°C):

- Before fix: 0.55V to 1.55V
- After fix: 0.35V to 1.35V

This makes sure that V_{ctrl} operates with robust margin at both hot and cold corners of temperature.

5 Summary

The previous bring up was modified with the suggested fix and was delivered as an updated one. The customer confirmed that the updated bring up ran successfully multiple times with no issue at hot temperature. This fix can be applied across programs which verifies a more robust operation of the device. This fix has also been incorporated into the software library of the AFE. Checking Pll Vctrl was only a debug step. Checking for PLL LOCK status inside PLL lock detector of AFE is sufficient to monitor the state of PLL. The suggest fix can be applied to all the programs. Customer does not need to check PLL Vctrl voltage for each program. The fix is a configuration level change for more robust operation.

6 References

- Texas Instruments, [AFE79xx Quad-Channel RF Transceiver With Feedback Path](#), data sheet.
- Texas Instruments, [AFE79xx Evaluation Module](#), user's guide.
- Texas Instruments, [Fractional/Integer-N PLL Basics](#), technical brief.

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