Application Note

DP83826 to DP83826A Hardware Rollover Document

David Liu

ABSTRACT

Texas Instruments offers a variety of Ethernet PHY transceivers which provide designs to multiple end equipment use cases. This application note references the differences between two of the PHYs within the 10/100Mbps portfolio (DP83826x[(1)] and DP83826Ax[(2)]) and how an existing design using DP83826x can be converted to use DP83826Ax.

- DP83826x refers to DP83826E and DP83826I.
- DP83826Ax refers to DP83826AI.

Table of Contents

Trademarks

1 Introduction

The DP83826x and DP83826Ax are a single-port physical layer transceivers compliant to IEEE802.3 10BASE-Te and 100BASE-TX standards. The DP83826x and DP83826Ax are designed to meet stringent industrial field bus application requirements and offers very low latency, deterministic variation in latency (across reset, power cycle), fixed phase between XI and TX_CLK, low power, and configuration using hardware bootstraps to achieve fast link up.

The devices support the standard MII and RMII (Leader mode and Follower mode) for direct connection to the media access controller (MAC). The device dedicated CLKOUT pin can be used to clock other modules on the system. In addition, the PWRDN pin controls the DP83826x and DP83826Ax link up from power-on-reset (POR) and helps with the design of asynchronous power-up of the DP83826x and DP83826Ax and host system-on-a-chip (SoC) or field-programmable-gate-array (FPGA) controller. The device operates from a single 3.3V power supply and has an integrated LDO to provide voltage rails required for internal blocks.

The device allows I/O voltage interfaces of 3.3V or 1.8V, which in turn enables the DP83826x and DP83826Ax to operate as a single-supply PHY when I/O voltage is 3.3V and a dual-supply PHY when I/O voltage is 1.8V. Automatic supply configuration within the DP83826x and DP83826Ax allows for any combination of VDDIO supply without the need for additional configuration settings. The DP83826x and DP83826Ax uses mixed-signal processing to perform equalization, data recovery, and error correction to achieve robust operation over a CAT5e twisted-pair cable.

2 Difference Between DP83826x and DP83826Ax

2.1 Fast Link-Drop (FLD) Strap Configuration

The DP83826x and DP83826Ax supports an enhanced link-drop mechanism, also called fast link-drop (FLD), which shortens the observation window for determining a link. There are multiple ways of determining the link status, which can be enabled or disabled based on user preference.

2.1.1 Basic Mode

In DP83826x BASIC mode, fast link-drop is enabled by default. Fast link-drop is enabled for RX Error and Signal and Energy Loss Count.

In DP83826Ax BASIC mode, fast link-drop is still enabled by default. Additional FLD mechanisms in BASIC mode can be determined by Strap11 as shown in Table 2-1.

Table 2-1. DP83826Ax Basic Mode FLD Configuration

Strap Configuration	RX Error Count	MLT3 Error Count	Low SNR Threshold	Signal and Energy Loss	Descrambler Link Loss
Strap 11 = Low (default)	Enabled	Enabled	Disabled	Enabled	Disabled
Strap 11 = High	Disabled	Disabled			

For both DP83826x/DP83826Ax, additional configuration can be programmed using the Control Register 3 (CR3, register address 0x000B). Bits[3:0] and bit[10] allow for various FLD conditions to be enabled.

2.1.2 Enhanced Mode

Table 2-2 and Figure 2-1 list the DP83826x FLD detection mode configuration. Note when Strap7 = High, Strap1 = High/Low, and Strap 8 = High/Low, the MLT3 Error Count is disabled.

Table 2-2. DP83826x FLD Detection Modes by Bootstrap Configuration

Strap Configuration	RX Error Count	MLT3 Error Count	Low SNR Threshold	Signal/Energy Loss	Descrambler Link Loss
(Default) Strap7 = LOW Strap1 = X Strap8 = X	Disabled	Disabled	Disabled	Disabled	Disabled
Strap7 = HIGH Strap1 = HIGH Strap8 = LOW	Enabled		Enabled	Enabled	Enabled
Strap7 = HIGH Strap1 = LOW Strap8 = LOW	Enabled		Disabled	Enabled	Disabled
Strap7 = HIGH Strap1 = LOW Strap8 = HIGH	Enabled		Disabled	Disabled	Disabled

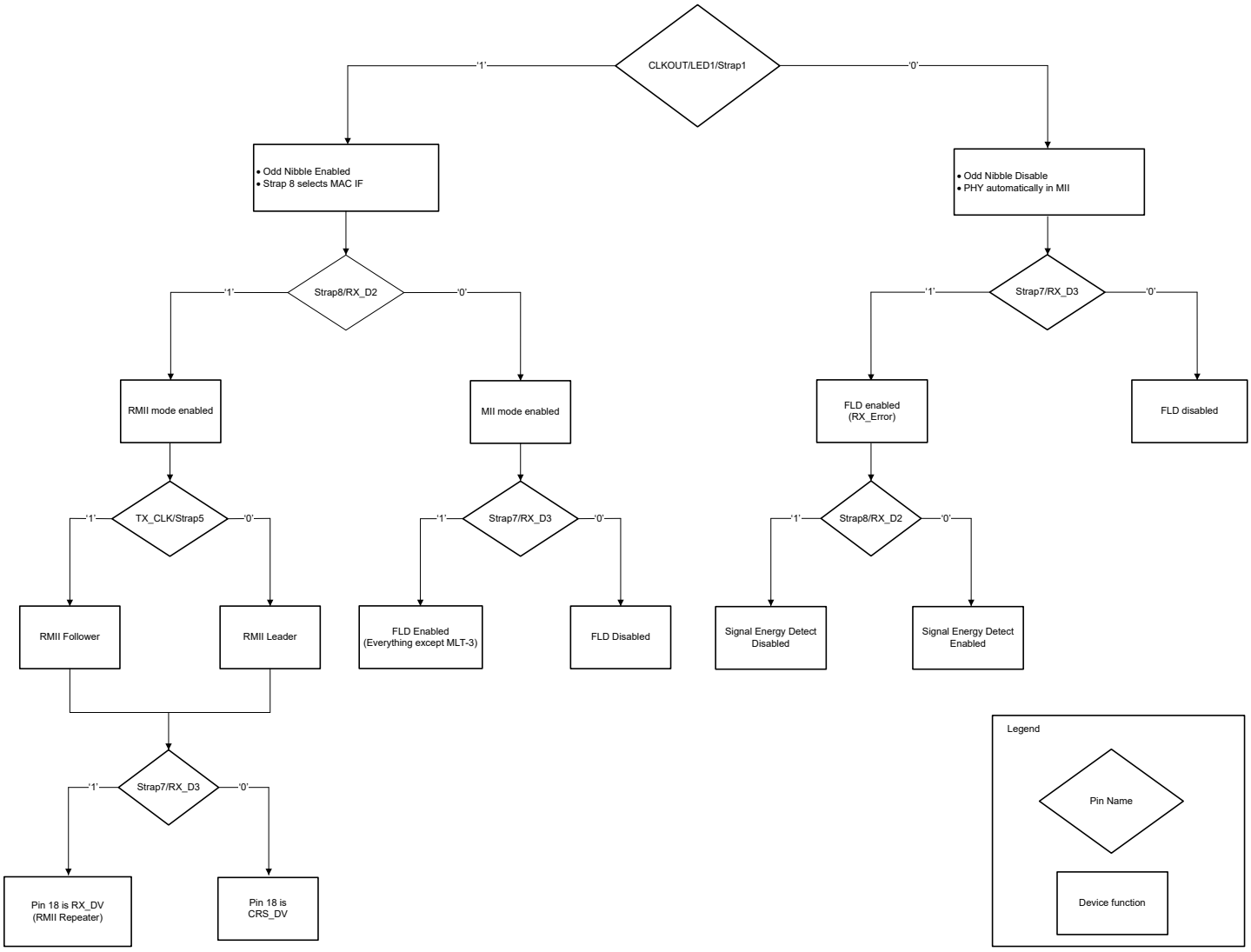

Figure 2-1. DP83826x Bootstrap Configurations Flowchart

Table 2-3 and Figure 2-2 list the DP83826Ax FLD Detection Mode configuration. Note under the same strap configuration, the MLT3 Error Count is enabled. For DP83826x and DP83826Ax, the RX error count is enabled in both cases. With the RX Error being a superset of MLT-3 Error, the superset is triggered before MLT-3 error. So even though there is a configuration difference in the MLT-3 error count, there is no behavioral difference between DP83826x and DP83826Ax.

Table 2-3. DP83826Ax FLD Detection Modes by BootStrap Configuration

FLD Strap Option	Strap Configuration	RX Error Count[1]	MLT3 Error Count	Low SNR Threshold	Signal/Energy Loss[1] [2]	Descrambler Link Loss
1	Strap1 = X Strap8 = X Strap11 = X	Disabled	Disabled	Disabled	Disabled	Disabled
2	Strap7 = HIGH Strap1 = HIGH Strap8 = LOW Strap11 = LOW	Enabled	Enabled	Enabled	Enabled	Enabled
3 [3]	Strap7 = HIGH Strap1= LOW Strap8= LOW Strap11 = LOW	Enabled	Enabled	Disabled	Enabled	Disabled
4[3]	Strap7 = HIGH Strap1 = LOW Strap8 = HIGH Strap11 = LOW	Enabled	Enabled	Disabled	Disabled	Disabled
5[3]	Strap7 = HIGH Strap1 = LOW Strap8 = HIGH Strap11 = HIGH	Disabled	Disabled	Disabled	Enabled	Disabled
6	Strap7 = HIGH Strap1 = HIGH Strap8 = LOW Strap11 = HIGH	Disabled	Disabled	Enabled	Enabled	Enabled

(1) Enabling RX_ERROR count and Signal/Engery Loss provides robust FLD operation
(2) Enabling signal and energy loss provides best immunity performance
(3) Recommended FLD enabled strap setting

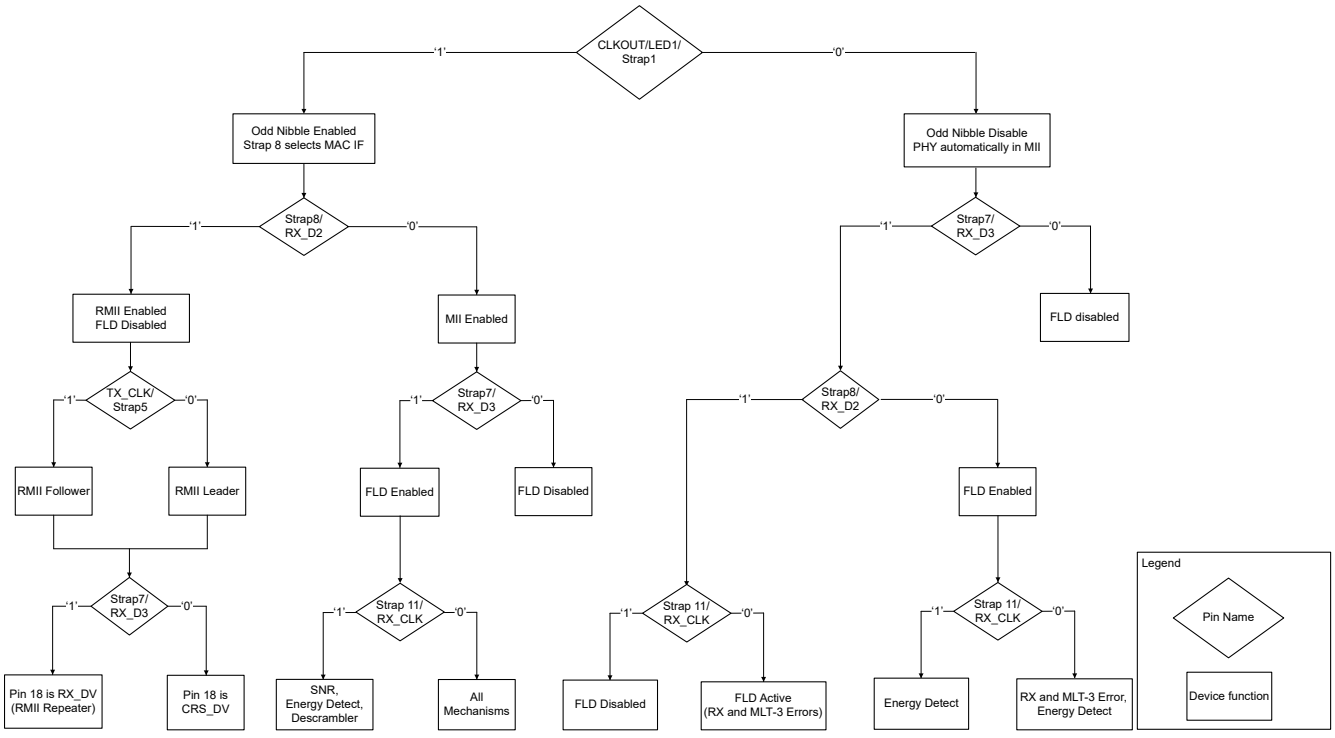

Figure 2-2. DP83826Ax Bootstrap Configuration Flowchart

For best EMC performance, TI recommends enabling the signal and energy loss FLD mode.

For both DP83826x and DP83826Ax, additional configuration can be programmed using the Control Register 3 (CR3, register address 0x000B). Bits[3:0] and bit[10] allow for various FLD conditions to be enabled.

2.2 EMC Performance

DP83826Ax offers significant EMC performance boost over DP83826x in both the basic and the enhanced mode. Table 2-4 lists the DP83826x and DP83826Ax performance difference. To enable better EMC performance, strap 11 must be pulled high regardless of mode in DP83826Ax.

The EMI/EMC compliance testings are done on DP83826AEVM. Please see section 4 of the *DP83826AEVM User's Guide* for detailed EMI test results.

Table 2-4. DP83826x and DP83826Ax EMC Performance Comparison

Test	Standard	Test Level	DP83826x	DP83826Ax
ESD	IEC 61000 4-2	+/-4kV Contact (RJ-45) +/-15kV Air (on cable)	+/- 4kV Criteria A +/- 8kV Criteria B	+/- 8kV Criteria A
Surge	IEC 61000-4-5	+/-2kV: line to line +/-4kV: line to GND	Criteria B	Criteria A
Radiated Immunity	IEC 61000-4-6	10V/m (150kHz - 80MHz)	Criteria A at 3Vrms Criteria B at 10Vrms	Criteria A at 10Vrms

Criteria A: No link drop of packet error and loss during the EMC testing.

Criteria B: Link drop is allowed, but PHY must recover the link without reset.

3 Summary

DP83826x and DP83826Ax are similar 10/100 Mbps PHYs which can be used in similar applications. This document notes the similarities and differences between the devices from an implementation perspective.

4 References

1. Texas Instruments, *DP83826 Deterministic, Low-Latency, Low-Power, 10/100Mbps, Industrial Ethernet PHY*, data sheet.
2. Texas Instruments, *DP83826Ax Deterministic, Low-Latency, Low-Power, 10/100Mbps, Industrial Ethernet PHY*, data sheet.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265