Application Report

Optimizing Network Switch Designs with Common Logic Use Cases

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ABSTRACT

Network switches (switches for wireless and wired infrastructure) integrate numerous subsystems together that are dedicated to high data throughput communication critical to the next-generation of internet, cloud, and 5G solutions. Though the switches differ in bandwidth and external interfaces, they share similar digital interfacing challenges; such as differing voltage domains between management CPUs and switch-fabric ASICS as well as a lack of GPIO pins for either LED control or communication QSFP module signals. All of the use cases shown in the *Block Diagram* and *Logic and Translation Use Cases* sections of this document are commonly seen in Network Switch designs.

Logic gates, voltage translators, and other logic devices are utilized for many purposes throughout modern electronic systems. This document provides example solutions for common design challenges that can be solved using logic and translation. Not all of the solutions here appear in every system; all solutions shown, however, are commonly used and effective.

There are dozens of logic families available from Texas Instruments, and it can be difficult to select the right one for the application. Network switches can very in size and in complexity, but the key design parameters remain the same making it easier to identify an appropriate family for this application. Refer to *Recommended Logic and Translation Families for Network Switches* in this document for help finding the right logic family for your use case.

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Trademarks

1 Block Diagram

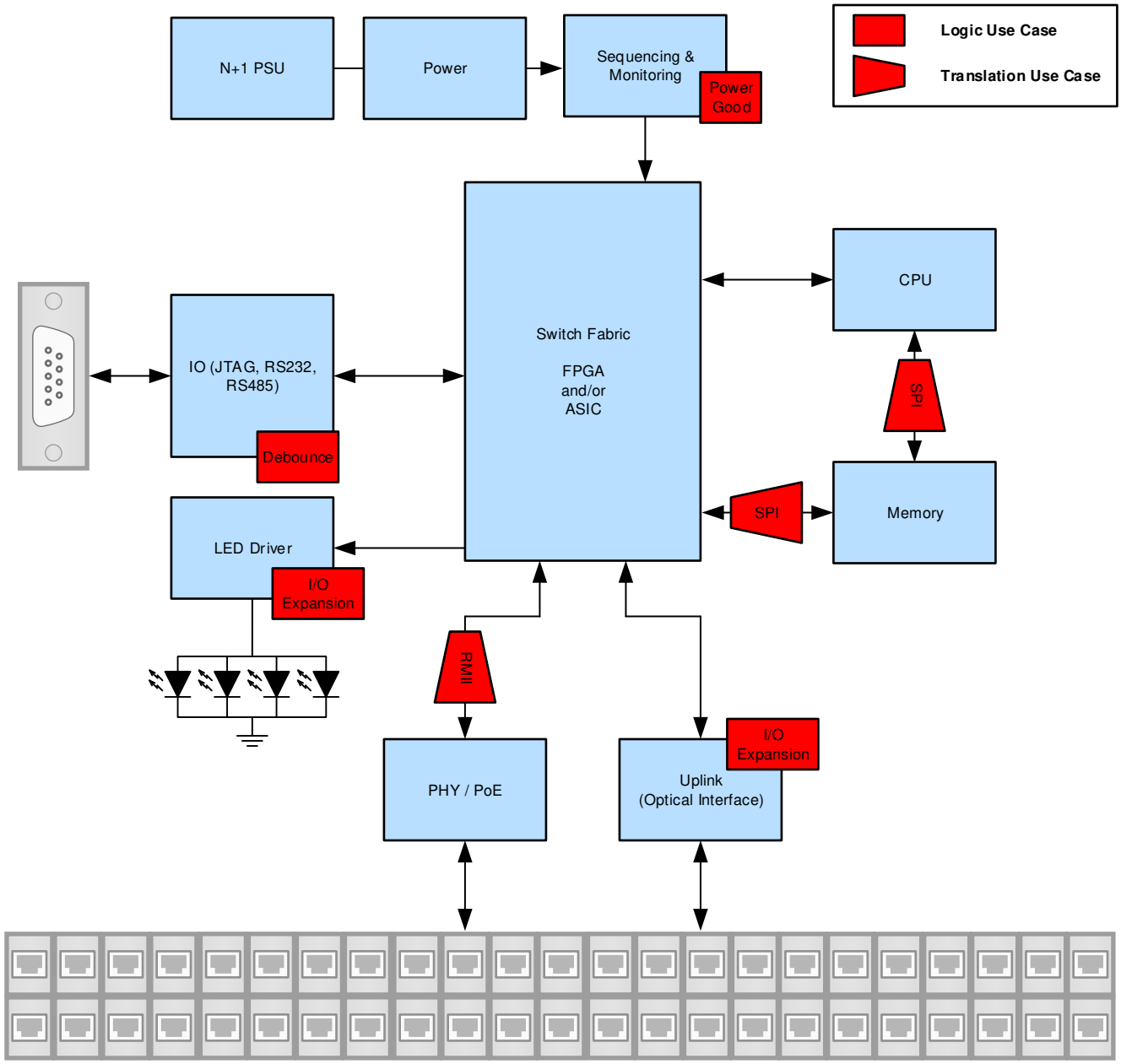

Figure 1-1. Simplified Block Diagram for Campus and Branch Switches

There are two primary types of Network switches, Campus and Branch as well as Data Center switches. Both of these types of switches have similar design architecture so the highlighted use cases apply to both. A simplified Campus and Branch system block diagram is used to illustrate the logic and translation use cases for the purpose of this report. See the interactive online End Equipment Reference Diagram *Campus and Branch switches* and *Data Center switches* for a more complete view.

2 Optimizing System Controller I/O Usage

A network switch with 24 channels typically will have 48 or more low-current LEDs to display channel status such as established connections and data transfer. The issue with this is the number of GPIOs required to control all these LEDs. To avoid increased costs of using FPGAs or ASICS containing more I/Os, a common solution is to offload the LED driving and control to 8-bit shift registers. This reduces the 48 required GPIOs to just 3 while also increasing drive strength in most cases. Shift-registers, such as the SN74HC595, can be cascaded together to provide as many outputs as needed in the system.

For network switches that contain optical interfaces, the benefits of using a shift register can be applied to the Small Form-factor Pluggable (SFP) or Quad Small Form-factor Pluggable (QSFP) interface. Many QSFP ports will have 4 system management pins, two for input signals and two for output signals. These signals include: a reset signal for module, a module selection/enable signal, a module present signal, and an interrupt signal. The number of GPIOs needed to manage these ports can quickly get cumbersome for more complex network switches containing several of these optical interfaces. Figure 2-1 illustrates the shift register use case for a system with four QSFP ports.

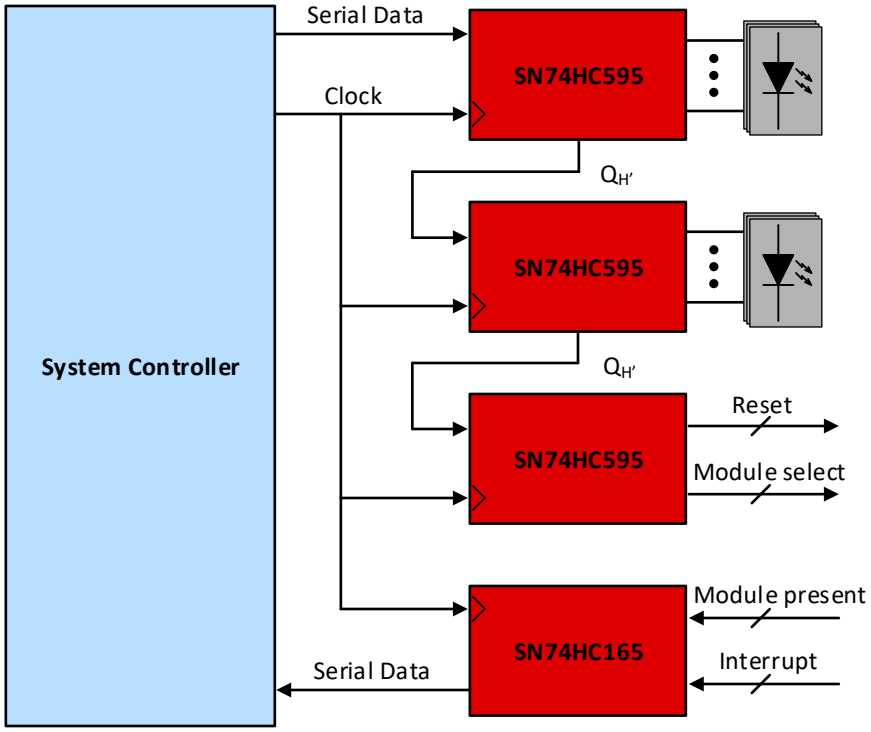

Figure 2-1. I/O Expansion for Network Switch Optical Interface

The SN74HC595, a serial-in parallel-out shift register, is cascaded together resulting in twenty-four outputs to control sixteen status LEDs and 8 QSFP module management signals. The SN74HC165, a parallel-in serial-out shift register, takes the 8 signals coming from the QSFP module and outputs the data serially to the system controller. Having all shift registers share a common clock signal will allow for the system controller to perform all of this while only using a total of five GPIOs.

3 Logic and Translation Use Cases

3.1 Logic Use Cases

3.1.1 Combine Power Good Signals

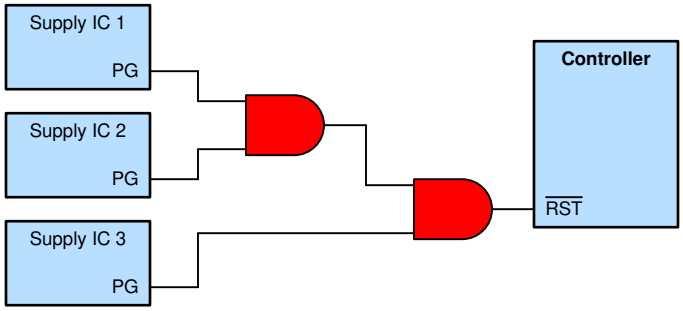

Figure 3-1. Using Logic to Combine Multiple Power-Good Signals

- Add system indicators without software or system controller interaction
- Drive low current indicator LEDs (1 mA to 25 mA) with most logic gates
- Add configurability using logic functions
- See the Logic Minute video *Combining Power Good Signals* for more information about this use case
- See *online parametric search tool* to find the right AND gate

3.1.2 Debounce Switches and Buttons

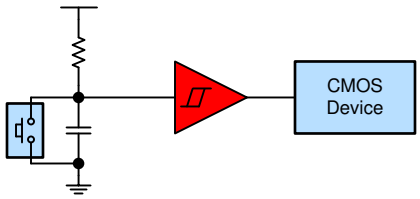

Figure 3-2. Using Logic to Prevent Multiple Triggers of a CMOS Input Due to Switch Bounce

- Prevents multiple triggers of CMOS inputs due to switch bounce
- Works when the system controller is asleep
- Works without a system controller
- Reduces controller code complexity, no software debounce required
- See the Logic Minute video *Debounce a Switch* for more information about this use case
- See *online parametric search tool* to find the right Schmitt-trigger buffer

3.1.3 Increase Number of Controller Inputs

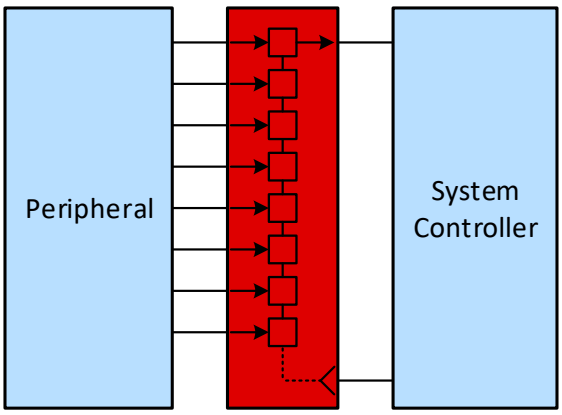

Figure 3-3. Using Shift-register to Serialize Parallel Data and Conserve Controller I/O's

- Input 8 bits of parallel data to the System Controller with as few as two I/Os
- Daisy chain shift registers to produce large numbers of inputs
- Input up to 180 Mbps of serial data with a parallel-in serial-out shift register
- See *online parametric search tool* to find the right Shift Register

3.1.4 Increase Number of Controller Outputs

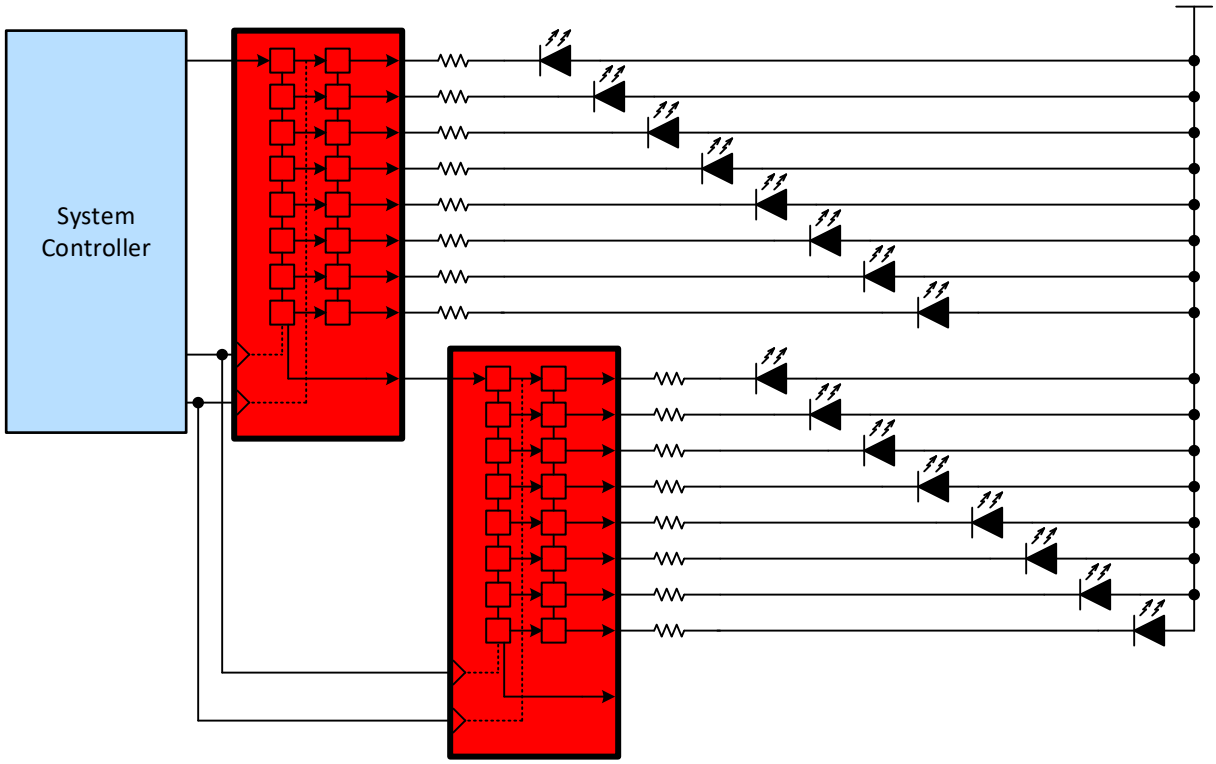

Figure 3-4. Using Two Shift Registers to Control 16 LEDs with Three Signals (Data, Shift Clock, and Output Register Clock)

- Turn as few as two outputs into 8 outputs with one serial-in parallel-out shift register
- Daisy chain shift registers to produce large numbers of outputs
- Drive low-current (< 8 mA) LEDs directly
- See *online parametric search tool* to find the right Shift Register

3.2 Voltage Translation Use Cases

3.2.1 SPI Communication

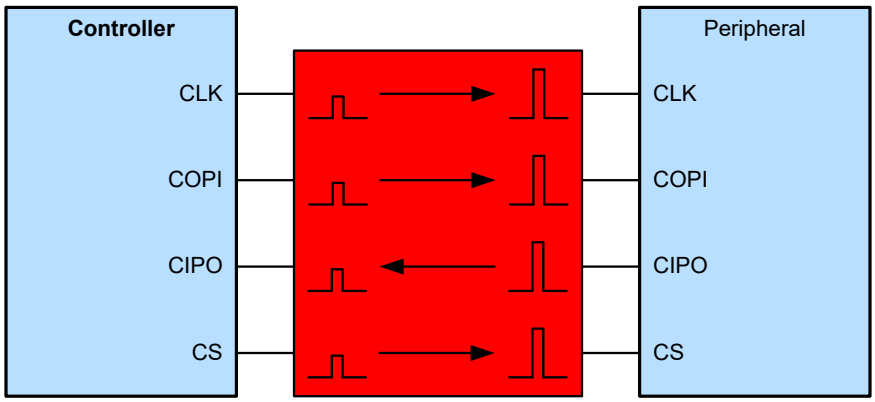

Figure 3-5. Using Voltage Translation with a SPI-Communication Bus

- Enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Improve data rates over discrete translation solutions
- Provide protection from disconnected peripherals
- See *online parametric search tool* to find the right voltage level translator

3.2.2 RMII Communication

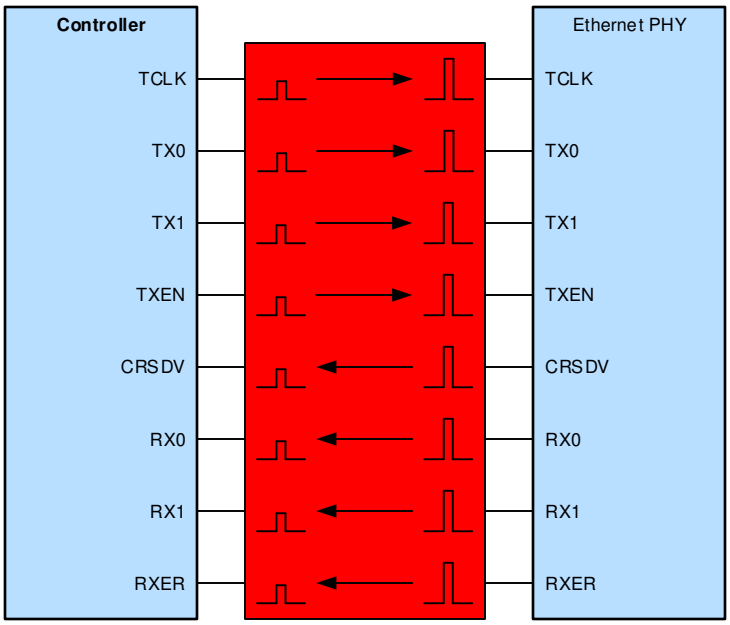

Figure 3-6. Using Voltage Translation with a RMII Communication Bus

- Enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Improve data rates over discrete translation solutions to support RMII interface speed of 100 Mbps
- Protect downstream devices during power down with V_{CC} isolation
- See *online parametric search tool* to find the right voltage level translator

4 Recommended Logic and Translation Families for Network Switches

4.1 AXC: Advanced eXtremely Low-Voltage CMOS Translation

Key Features

- Up and down translation across 0.65 V to 3.6 V
- Designed with glitch suppression circuitry to improve power sequencing performance
- Maximum quiescent current (I_{CCA} + I_{CCB}) as low as 6 µA (85°C maximum) and 14 µA (125°C maximum)
- Up to 500-Mbps support when translating from 1.8 V to 3.3 V
- V_{CC} Isolation feature – if either V_{CC} input is below 100 mV, all I/Os outputs are disabled and become high impedance
- I_{off} supports partial-power-down mode operation
- Operating temperature: –40°C to +125°C
- Packaging options: SC70, SM8, SON, SOT-23, SOT, UQFN, US8, and X2SON

See *online parametric search tool* to find the right AXC family voltage level translation devices.

4.2 LVC: Low-Voltage CMOS Logic and Translation

Key Features: SN74**LVC**xxxx

- Huge portfolio of logic functions
- LVC: 4+ channels per package
- Over-voltage tolerant inputs allow unidirectional down-translation with any function
- High-drive outputs (up to 32 mA)
- Up to 250-Mbps operation
- I_{off} supports partial-power-down mode operation
- Packaging options: SOIC, TSSOP, VQFN, SOP, and SSOP

Key Features: SN74**LVCxG**xxxx

- Put 1, 2, or 3 channels of any logic function right where you need them
- Configurable gates available ('57, '58, '97, '98, and '99 functions)
- Over-voltage tolerant inputs allow unidirectional down-translation with any gate or buffer
- High-drive outputs (up to 32 mA)
- Up to 250-Mbps operation
- I_{off} supports partial-power-down mode operation
- Packaging options: SOT-23, SC70, X2SON, SOT-5X3, SON, and DSBGA

Key Features: SN74**LVCxT**xxxx

- LVCxT: Up and Down Translation Across 1.65 V to 5.5 V
- 1, 2, 8, or 16 channels per device
- High-drive outputs (up to 32 mA)
- Up to 250-Mbps operation
- I_{off} supports partial-power-down mode operation

See *online parametric search tool* to find the right LVC family logic and voltage level translation devices.

4.3 HC: High-speed CMOS Logic

Key Features:

- Huge portfolio of logic functions
- 4+ channels per package
- Inputs and output include positive and negative clamp diodes
- Wide voltage operating range of 2 V to 6 V
- Up to 140-Mbps operation
- Packaging options: PDIP, SO, SOIC, SSOP, and TSSOP

See *online parametric search tool* to find the right HC family voltage level translation devices.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2020) to Revision A (April 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated the *Using Voltage Translation with a SPI-Communication Bus* figure for inclusive SPI terminology	5

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