Functional Safety Information

TPS7A53-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the TPS7A53-Q1 (VQFN and VQFNP packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

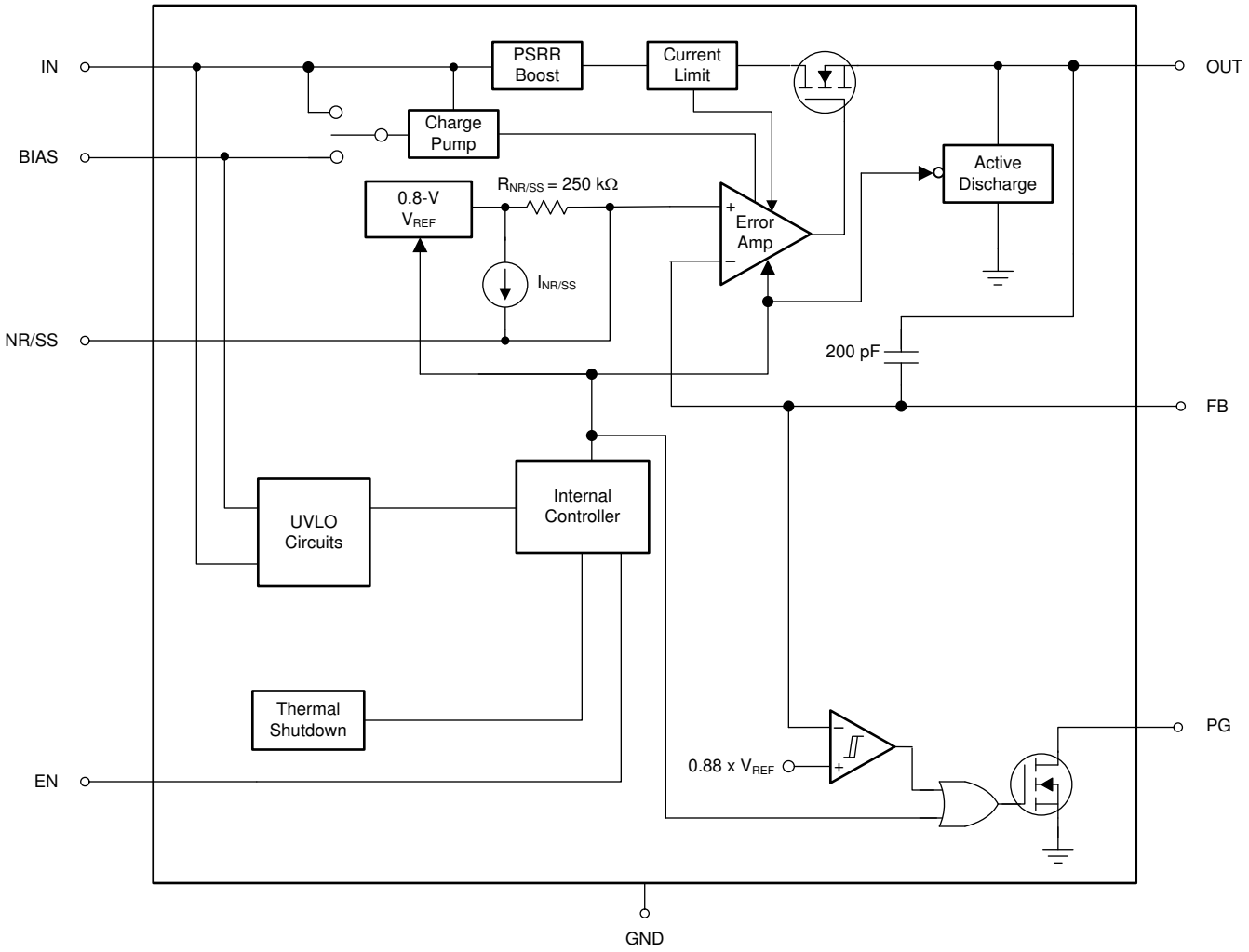

Figure 1-1. Functional Block Diagram

The TPS7A53-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 VQFN Package

This section provides functional safety failure in time (FIT) rates for the VQFN package of the TPS7A53-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	16
Die FIT rate	6
Package FIT rate	10

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 1000 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 VQFNP Package

This section provides functional safety failure in time (FIT) rates for the VQFNP package of the TPS7A53-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	18
Die FIT rate	6
Package FIT rate	12

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 1000 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS7A53-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT high (following VIN)	15
VOUT not in specification (voltage or timing)	60
VOUT low (no output)	15
PG false trigger (fails to trigger)	5
Short circuit any two pins	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS7A53-Q1 (VQFN and VQFNP packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6.)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to supply (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

4.1 VQFN Package

Figure 4-1 shows the TPS7A53-Q1 pin diagram for the VQFN package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7A53-Q1 data sheet.

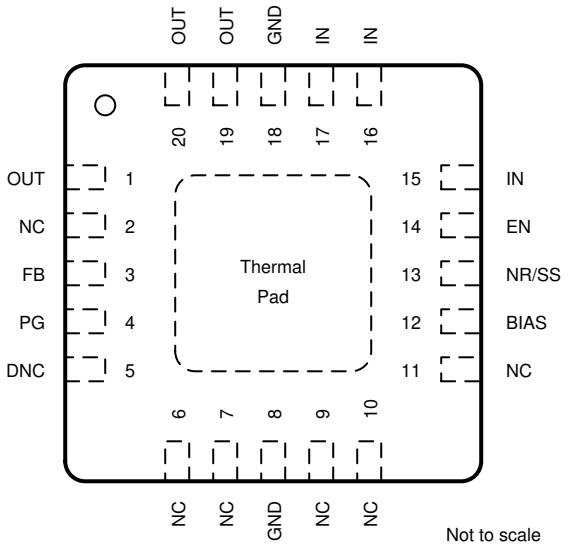

Figure 4-1. Pin Diagram (VQFN Package)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B
NC	2	No effect. Normal operation.	D
FB	3	Output voltage is the input voltage minus the dropout voltage because the error amplifier drives the pass transistor gate to the rail.	B
PG	4	PG always indicates that the output is not at the target level.	B
DNC	5	No effect. Normal operation.	D
NC	6	No effect. Normal operation.	D
NC	7	No effect. Normal operation.	D
GND	8	No effect. Normal operation.	D
NC	9	No effect. Normal operation.	D
NC	10	No effect. Normal operation.	D
NC	11	No effect. Normal operation.	D
BIAS	12	VBIAS does not provide biasing, any benefits associated with using a separate VBIAS are no longer present.	C
NR/SS	13	The internal reference cannot start. The device cannot turn on.	B
EN	14	The device is disabled, resulting in no output voltage.	B
IN	15	There is no power to the device, resulting in no output voltage.	B
IN	16	There is no power to the device, resulting in no output voltage.	B
IN	17	There is no power to the device, resulting in no output voltage.	B
GND	18	No effect. Normal operation.	D
OUT	19	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B
OUT	20	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Device parasitics are increased and transient performance is degraded.	C
NC	2	No effect. Normal operation.	D
FB	3	The error amplifier input is not connected. Output voltage is indeterminate.	B
PG	4	PG functionality is lost.	B
DNC	5	No effect. Normal operation.	D
NC	6	No effect. Normal operation.	D
NC	7	No effect. Normal operation.	D
GND	8	Device biasing has no current path. The device is not operational and does not regulate.	B
NC	9	No effect. Normal operation.	D
NC	10	No effect. Normal operation.	D
NC	11	No effect. Normal operation.	D
BIAS	12	VBIAS does not provide biasing, any benefits associated with using a separate VBIAS are no longer present.	C
NR/SS	13	The device starts up with default timing. Any noise-reduction benefits are lost.	C
EN	14	The enable circuit is in an unknown state. The device can be enabled or disabled.	B
IN	15	Device parasitics are increased and transient performance is degraded.	C
IN	16	Device parasitics are increased and transient performance is degraded.	C
IN	17	Device parasitics are increased and transient performance is degraded.	C
GND	18	The charge pump has no current path. The device regulates but performance is degraded.	C
OUT	19	Device parasitics are increased and transient performance is degraded.	C
OUT	20	Device parasitics are increased and transient performance is degraded.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	NC (pin 2)	No effect. Normal operation.	D
NC	2	FB (pin 3)	No effect. Normal operation.	D
FB	3	PG (pin 4)	PG functionality is lost. The output voltage set by the feedback resistors is incorrect.	B
PG	4	DNC (pin 5)	The low-dropout regulator (LDO) can possibly not work properly because the PG signal can create errors during LDO start-up.	B
DNC	5	NC (pin 6)	No effect. Normal operation.	D
NC	6	NC (pin 7)	No effect. Normal operation.	D
NC	7	GND (pin 8)	No effect. Normal operation.	D
GND	8	NC (pin 9)	No effect. Normal operation.	D
NC	9	NC (pin 10)	No effect. Normal operation.	D
NC	10	NC (pin 11)	No effect. Normal operation.	D
NC	11	BIAS (pin 12)	No effect. Normal operation.	D
BIAS	12	NR/SS (pin 13)	VBIAS can potentially violate the absolute maximum rating on the NR/SS pin and cause damage. If this condition is not met, the internal reference cannot get to the target voltage and the output voltage is incorrect.	A
NR/SS	13	EN (pin 14)	The output voltage is incorrect.	B
EN	14	IN (pin 15)	The device is always enabled when the input is powered.	B
IN	15	IN (pin 16)	No effect. Normal operation.	D
IN	16	IN (pin 17)	No effect. Normal operation.	D
IN	17	GND (pin 18)	No power to the device, resulting in no output voltage.	B
GND	18	OUT (pin 19)	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B
OUT	19	OUT (pin 20)	No effect. Normal operation.	D
OUT	20	OUT (pin 1)	No effect. Normal operation.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible.	B
NC	2	No effect. Normal operation.	D
FB	3	The FB absolute maximum rating (3.6 V max) can be violated, damaging the device. If VIN < 3.6 V and if there is any loading on the device, the output is approximately 0 V. If there is no load on the device, the output is equal to VIN.	A
PG	4	PG functionality is lost.	B
DNC	5	The LDO can possibly not work properly because the input signal can create errors during LDO start-up.	B
NC	6	No effect. Normal operation.	D
NC	7	No effect. Normal operation.	D
GND	8	No output voltage. System performance depends on the upstream current limiting.	B
NC	9	No effect. Normal operation.	D
NC	10	No effect. Normal operation.	D
NC	11	No effect. Normal operation.	D
BIAS	12	Any benefits of using a separate supply for VBIAS are lost. If VIN is shorted to VBIAS, the supplies can destroy each other.	C
NR/SS	13	The absolute maximum rating for the NR/SS pin can be violated, damaging the pin. If the absolute maximum rating is not violated, the output voltage is equal to the input voltage minus the dropout voltage.	A
EN	14	The device is always enabled when the input is powered.	B
IN	15	No effect. Normal operation.	D
IN	16	No effect. Normal operation.	D
IN	17	No effect. Normal operation.	D
GND	18	No output voltage. System performance depends on the upstream current limiting.	B
OUT	19	Regulation is not possible.	B
OUT	20	Regulation is not possible.	B

4.2 VQFNP Package

Figure 4-2 shows the TPS7A53-Q1 pin diagram for the VQFNP package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7A53-Q1 data sheet.

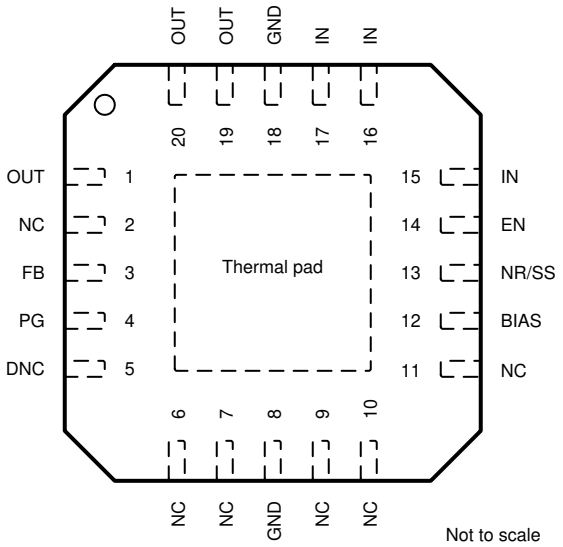

Figure 4-2. Pin Diagram (VQFNP Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B
NC	2	No effect. Normal operation.	D
FB	3	Output voltage is the input voltage minus the dropout voltage because the error amplifier drives the pass transistor gate to the rail.	B
PG	4	PG always indicates that the output is not at the target level.	B
DNC	5	No effect. Normal operation.	D
NC	6	No effect. Normal operation.	D
NC	7	No effect. Normal operation.	D
GND	8	No effect. Normal operation.	D
NC	9	No effect. Normal operation.	D
NC	10	No effect. Normal operation.	D
NC	11	No effect. Normal operation.	D
BIAS	12	VBIAS does not provide biasing, any benefits associated with using a separate VBIAS are no longer present.	C
NR/SS	13	The internal reference cannot start. The device cannot turn on.	B
EN	14	The device is disabled, resulting in no output voltage.	B
IN	15	There is no power to the device, resulting in no output voltage.	B
IN	16	There is no power to the device, resulting in no output voltage.	B
IN	17	There is no power to the device, resulting in no output voltage.	B
GND	18	No effect. Normal operation.	D
OUT	19	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B
OUT	20	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Device parasitics are increased and transient performance is degraded.	C
NC	2	No effect. Normal operation.	D
FB	3	The error amplifier input is not connected. Output voltage is indeterminate.	B
PG	4	PG functionality is lost.	B
DNC	5	No effect. Normal operation.	D
NC	6	No effect. Normal operation.	D
NC	7	No effect. Normal operation.	D
GND	8	Device biasing has no current path. The device is not operational and does not regulate.	B
NC	9	No effect. Normal operation.	D
NC	10	No effect. Normal operation.	D
NC	11	No effect. Normal operation.	D
BIAS	12	VBIAS does not provide biasing, any benefits associated with using a separate VBIAS are no longer present.	C
NR/SS	13	The device starts up with default timing. Any noise-reduction benefits are lost.	C
EN	14	The enable circuit is in an unknown state. The device can be enabled or disabled.	B
IN	15	Device parasitics are increased and transient performance is degraded.	C
IN	16	Device parasitics are increased and transient performance is degraded.	C
IN	17	Device parasitics are increased and transient performance is degraded.	C
GND	18	The charge pump has no current path. The device regulates but performance is degraded.	C
OUT	19	Device parasitics are increased and transient performance is degraded.	C
OUT	20	Device parasitics are increased and transient performance is degraded.	C

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	NC (pin 2)	No effect. Normal operation.	D
NC	2	FB (pin 3)	No effect. Normal operation.	D
FB	3	PG (pin 4)	PG functionality is lost. The output voltage set by the feedback resistors is incorrect.	B
PG	4	DNC (pin 5)	The low-dropout regulator (LDO) can possibly not work properly because the PG signal can create errors during LDO start-up.	B
DNC	5	NC (pin 6)	No effect. Normal operation.	D
NC	6	NC (pin 7)	No effect. Normal operation.	D
NC	7	GND (pin 8)	No effect. Normal operation.	D
GND	8	NC (pin 9)	No effect. Normal operation.	D
NC	9	NC (pin 10)	No effect. Normal operation.	D
NC	10	NC (pin 11)	No effect. Normal operation.	D
NC	11	BIAS (pin 12)	No effect. Normal operation.	D
BIAS	12	NR/SS (pin 13)	VBIAS can potentially violate the absolute maximum rating on the NR/SS pin and cause damage. If this condition is not met, the internal reference cannot get to the target voltage and the output voltage is incorrect.	A
NR/SS	13	EN (pin 14)	The output voltage is incorrect.	B
EN	14	IN (pin 15)	The device is always enabled when the input is powered.	B
IN	15	IN (pin 16)	No effect. Normal operation.	D
IN	16	IN (pin 17)	No effect. Normal operation.	D
IN	17	GND (pin 18)	No power to the device, resulting in no output voltage.	B
GND	18	OUT (pin 19)	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B
OUT	19	OUT (pin 20)	No effect. Normal operation.	D
OUT	20	OUT (pin 1)	No effect. Normal operation.	D

Table 4-9. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible.	B
NC	2	No effect. Normal operation.	D
FB	3	The FB absolute maximum rating (3.6 V max) can be violated, damaging the device. If VIN < 3.6 V and if there is any loading on the device, the output is approximately 0 V. If there is no load on the device, the output is equal to VIN.	A
PG	4	PG functionality is lost.	B
DNC	5	The LDO can possibly not work properly because the input signal can create errors during LDO start-up.	B
NC	6	No effect. Normal operation.	D
NC	7	No effect. Normal operation.	D
GND	8	No output voltage. System performance depends on the upstream current limiting.	B
NC	9	No effect. Normal operation.	D
NC	10	No effect. Normal operation.	D
NC	11	No effect. Normal operation.	D
BIAS	12	Any benefits of using a separate supply for VBIAS are lost. If VIN is shorted to VBIAS, the supplies can destroy each other.	C
NR/SS	13	The absolute maximum rating for the NR/SS pin can be violated, damaging the pin. If the absolute maximum rating is not violated, the output voltage is equal to the input voltage minus the dropout voltage.	A
EN	14	The device is always enabled when the input is powered.	B
IN	15	No effect. Normal operation.	D
IN	16	No effect. Normal operation.	D
IN	17	No effect. Normal operation.	D
GND	18	No output voltage. System performance depends on the upstream current limiting.	B
OUT	19	Regulation is not possible.	B
OUT	20	Regulation is not possible.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2019) to Revision A (December 2022)	Page
• Changed document to comply with latest standards and add missing sections	2

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