EVM User's Guide: ADC3663 ADC3662 ADC3661

ADC36xx Evaluation Module

Description

The ADC36xx evaluation module (EVM) is designed to evaluate the ADC36xx family of high-speed analog-to-digital converters (ADCs) including the ADC3663, ADC3664 and ADC3683, all which have a serial low-voltage differential signaling (LVDS) interface.

Get Started

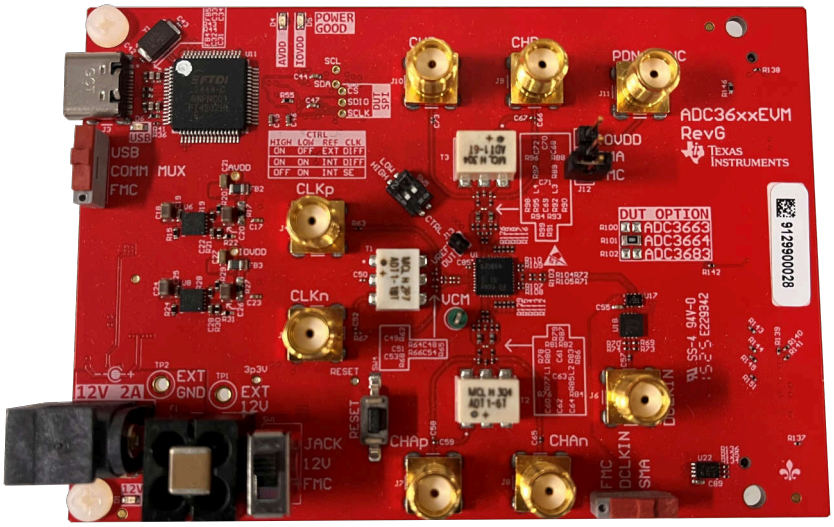
1. Order the ADC3663EVM, ADC3664EVM, or ADC3683EVM
2. Download the latest revision of the data sheet
3. Download the latest software
4. Download the comprehensive reference design files from the tools page of the EVM

Features

- Single-ended and differential options for AC-coupled analog input with onboard balun
- Single-ended and differential options for sampling clocking input
- Powered with an external 12V connection and onboard power regulation
- Flexible switch controlled ADC configuring thru USB-C connection or FMC connector
- FMC connector to interface with TI data capture card or third-party FPGA development kit

Applications

- Software defined radio
- Communications infrastructure
- Spectrum analyzer
- Medical and healthcare
- Control systems



ADC36xxEVM

1 Evaluation Module Overview

1.1 Introduction

The ADC36xxEVM is an evaluation board used to evaluate the ADC36xx family of analog-to-digital converters (ADC) from Texas Instruments. The ADC36xx uses a serial LVDS interface to output the digital data. The ADC36xx can be operated in 'oversampling + decimating' mode using the internal decimation filter in order to improve the dynamic range.

By default, the EVM is configured to receive external inputs for the sampling clock and analog input via AC-coupled transformer (balun) inputs. The transformer performs the single-ended to differential conversion, and provides a low noise/distortion passive input.

This user’s guide describes the characteristics, operation, and use of the ADC36xx evaluation module (EVM). This user's guide also discusses how to set up and configure the software and hardware.

1.2 Kit Contents

The following equipment is included in the EVM evaluation kit:

Table 1-1. Included equipment

Item	Description	Quantity
ADC36xxEVM	PCB	1
DC Jack Power Cable	Cable	1
USB-C Cable	Cable	1
JTAG Dongle & Micro USB Cable	PCB and Cable	1

1.3 Device Information

There are three variants of the ADC36xxEVM which cover the devices in this family with LVDS output interfaces: the ADC3683EVM, the ADC3664EVM, and the ADC3663EVM.

The following is a list of the devices that these EVM variants can be used to evaluate:

Table 1-2. Devices evaluated using the ADC3683EVM

ADC3683EVM			
Device	**Number of Channels**	**Resolution**	**Max Sample Rate**
ADC3683	2	18	65MHz
ADC3682	2	18	25MHz
ADC3681	2	18	10MHz
ADC3583	1	18	65MHz
ADC3582	1	18	25MHz
ADC3581	1	18	10MHz

Table 1-3. Devices evaluated using the ADC3664EVM

ADC3664EVM			
Device	**Number of Channels**	**Resolution**	**Max Sample Rate**
ADC3664	2	14	125MHz
ADC3564	1	14	125MHz

Table 1-4. Devices evaluated using the ADC3663EVM

ADC3663EVM			
Device	**Number of Channels**	**Resolution**	**Max Sample Rate**
ADC3663	2	16	65MHz
ADC3662	2	16	25MHz
ADC3661	2	16	10MHz
ADC3563	1	16	65MHz
ADC3562	1	16	25MHz
ADC3561	1	16	10MHz

2 Hardware

This section details the required hardware tools and connections necessary to effectively use the ADC36xxEVM, which covers the ADC3663, ADC3664 and ADC3683 variant EVMs

2.1 Required Hardware

The following equipment is **not** included in the EVM evaluation kit, but is **required** for evaluation of this EVM:

- TSWDC155EVM data capture board and related items
- Three low-noise signal generators for the analog input, sample clock, and DCLKIN signals. (These signal generators must share the same reference frequency)
- Two bandpass filters for your desired sample clock frequency and analog input frequency.
- One power supply capable of supplying 12V, 1A
- PC running Microsoft® Windows® 10 or 11.

TI recommends the following low phase noise signal generators for analog inputs and clocking inputs:

- Rohde & Schwarz SMA100A
- Rohde & Schwarz SMA100B
- Keysight E8257D
- Hewlett Packard HP8644B
- Rohde & Schwarz SMHU
- Or other equivalents

A bandpass filter is required for all signal generators in order to remove spurious components and/or noise. The DCLKIN input does not require a bandpass filter. If bandpass filters are not used, then the true performance of the ADC may not be clearly seen, and will be limited by the performance of the signal generators used.

The bandpass filter used is recommended to have:

- Greater than or equal to 60-dB harmonic attenuation
- Less than or equal to 10% bandwidth
- Greater than 18-dBm power
- Less than 5-dB insertion loss

2.2 Hardware Setup

1. Connect the ADC36xxEVM to the TSWDC155EVM via the FMC connectors.
2. Connect the USB-C connector to J3 on the ADC36xxEVM to your PC using the included USB-C Cable.
3. Connect the USB-C connector to J8 on the TSWDC155EVM to your PC using the included USB C cable.
4. Connect the Micro USB Cable to the JTAG dongle and connect the JTAG dongle to the JTAG header J7 on the TSWDC155EVM. Then connect the Micro USB Cable to your PC.
5. Ensure jumper J2 on the TSWDC155EVM is installed across pins 1-2 to power the board through the USB-C connector

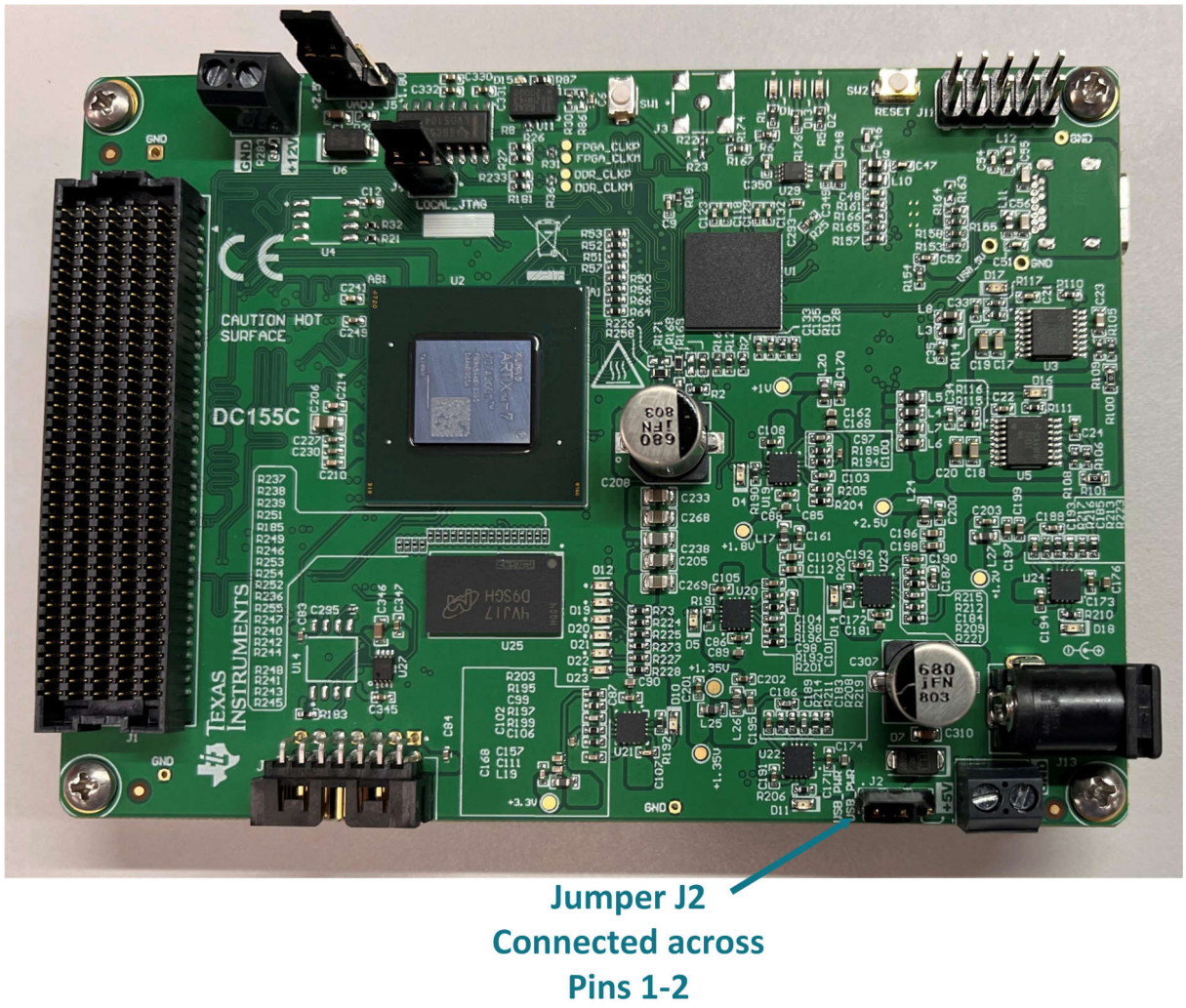


Figure 2-1. TSWDC155EVM Jumper J2

6. Ensure the following Switches and Jumpers are in the following configurations on the ADC3664EVM:
   a. Ensure the 12V Power Switch (SW1) is switched to Jack.
   b. Ensure the Comms Mux switch (SW2) is switched to USB.
   c. Ensure the DCLKIN switch (SW3) is switched to SMA.
   d. Ensure the both switches on the VREF CTRL Switch bank (SW5) are switched to ON.
   e. Ensure the VREF Jumper (J13) is populated.
   f. Ensure the PDN/SYNC Jumper (J12) is not connected.

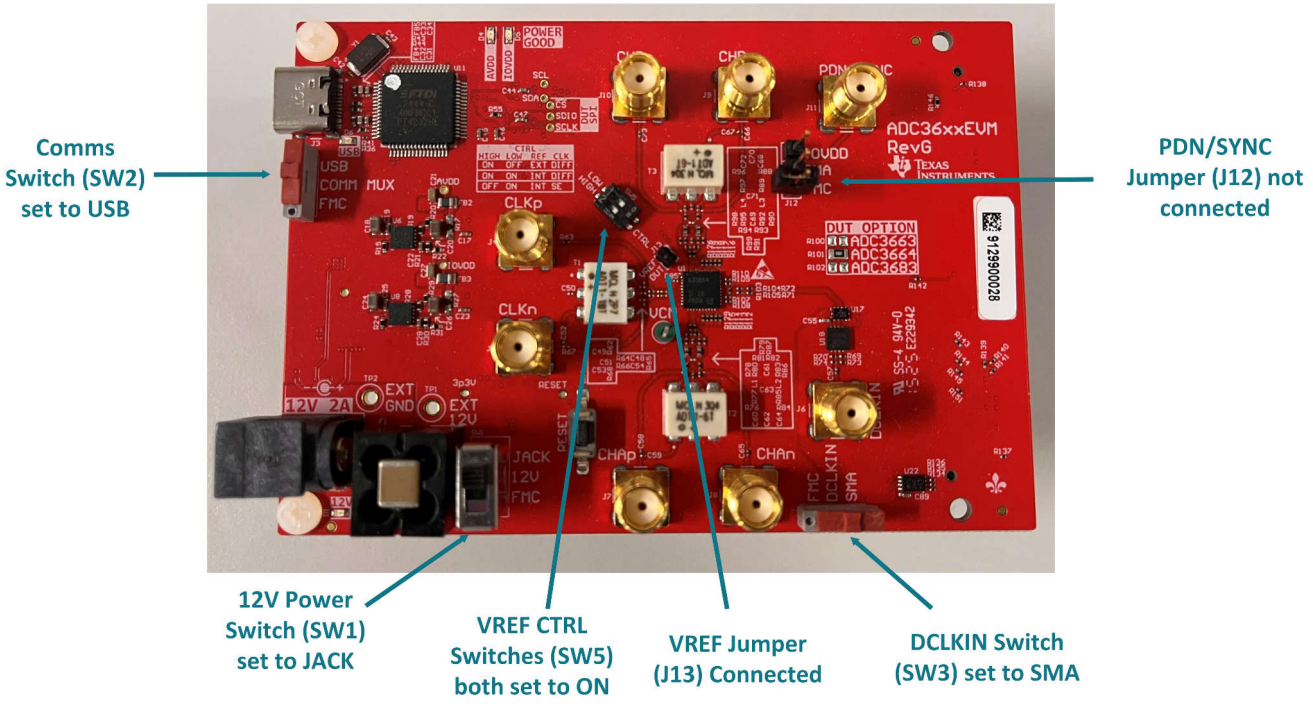


Figure 2-2. ADC36xxEVM Switches and Jumpers

3 Software

This section details the required software tools and applications necessary to effectively use the ADC36xxEVM, which covers the ADC3663, ADC3664 and ADC3683 varient EVMs.

3.1 Required Software

Below is a list of required software to evaluate the ADC36xxEVM:

- ADC36xxEVM GUI
- Texas Instruments HSDC Pro Software
- Vivado Lab Solutions

3.2 Software Setup

1. Download and install the ADC36xxEVM LVDS GUI.
   a. While installing the ADC36xxEVM LVDS GUI, ensure that the FX3 USB drivers are also installed.
2. Download and install HSDC Pro. This will be used to view the captured data.
3. Download and install Vivado Lab Solutions from the AMD website. This is required to capture data from the FPGA.
4. Ensure that the Vivado Lab bin folder is added to your PATH system environment variable:
   a. Search for "Edit the system environment variables" in the start menu
   b. Click on "Environment Variables…"
   c. Under "System variables", locate and click on the "Path" variable
   d. Click on "Edit…"
   e. Click on "New" to add a new path
   f. Add the path to your Vivado Lab installation, which is dependent on where you installed Vivado Lab and what version you installed. The path to the bin folder typically looks something like this: *C:\Xilinx\Vivado_Lab\2023.1.1\bin*

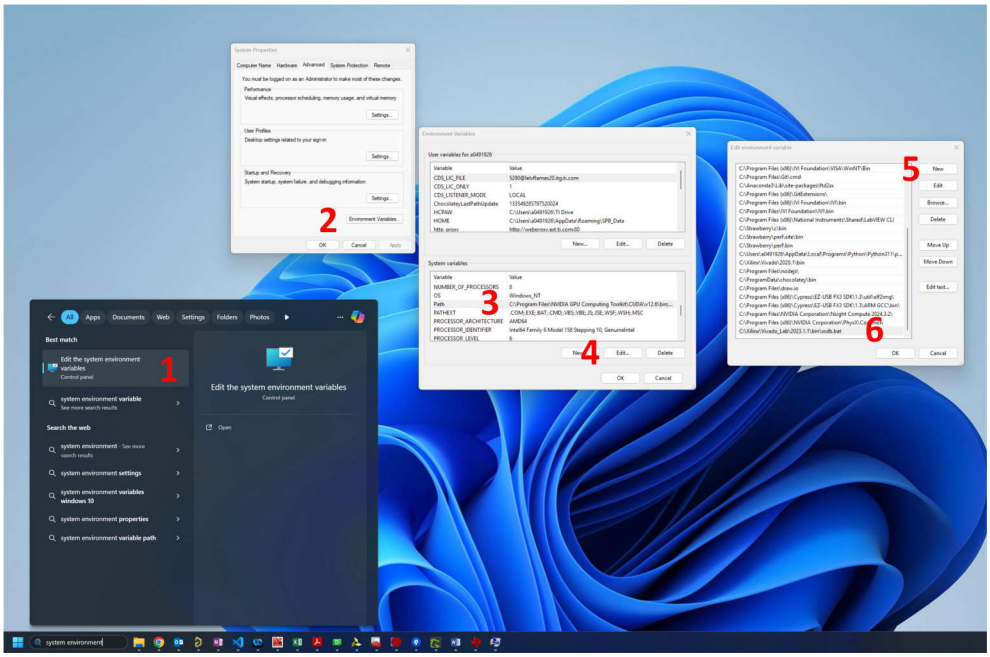


Figure 3-1. Environment Variable Setup

4 Setup Procedure

The following setup procedures will detail how to setup and use the hardware and software required for evaluation of all three variants of the ADC36xxEVM.

4.1 Setting up the ADC3683EVM

1. Ensure the software is set up according to the Software Setup section.
2. Ensure the hardware is set up according to the Hardware Setup section
3. To provide the CLK signal:
   a. Using an SMA cable and an inline 65 MHz band pass filter, connect the signal generator to the CLKn SMA connector (J5) on the ADC3683EVM.
   b. Set the signal generator's output signal frequency to 65 MHz and the signal amplitude to +10dBm.
4. By default, the EVM is configured to take a single ended input, so analog inputs should be applied to connectors CHAp (J7) for Channel A or CHBp (J9) for Channel B. To provide an analog input:
   a. Using an SMA cable and an inline 5 MHz band pass filter, connect the signal generator to analog input channel A.
   b. Set the signal generator's output signal frequency to 5.135 MHz (prime number) and 0dBm.
5. To provide a DCLK signal:
   a. Using an SMA cable, connect the signal generator to the DCLKIN SMA connector (J6).
   b. Set the signal generator's output frequency to 292.5MHz (18-bit, 2-wire, DDC bypass) and the signal amplitude to +2dBm.
6. Ensure all signal generators for clock, analog input and DCLK are referenced locked using the 10MHz REF on the back of the signal generators. For an example of this, please see figure below.

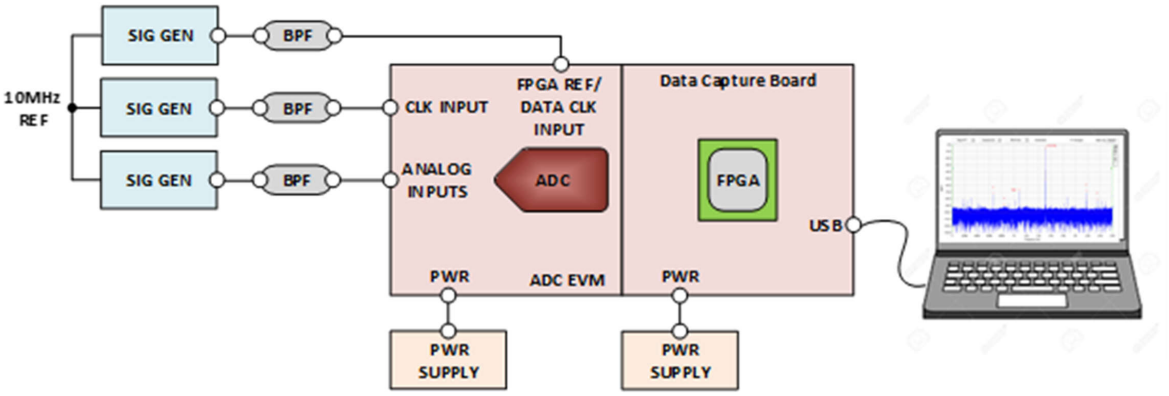


Figure 4-1. Basic Test Measurement Setup

7. Your setup should now look like the following:

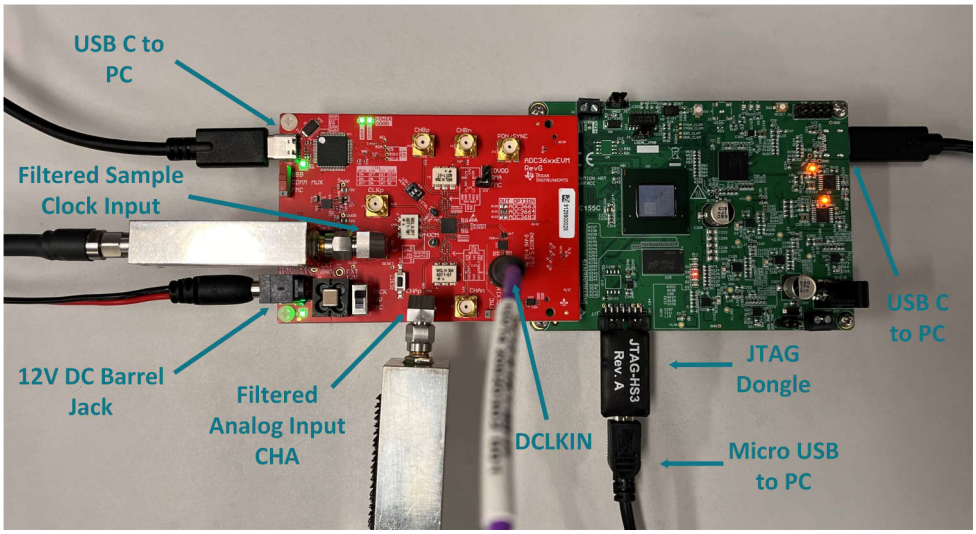


Figure 4-2. ADC3683EVM Hardware Setup

8. Open HSDC Pro. Always ensure that HSDC Pro is open **before** opening the ADC36xxEVM GUI.
9. Click on cancel when prompted to connect to a board. The GUI will handle all of the other HSDC Pro capture and configuration related operations.

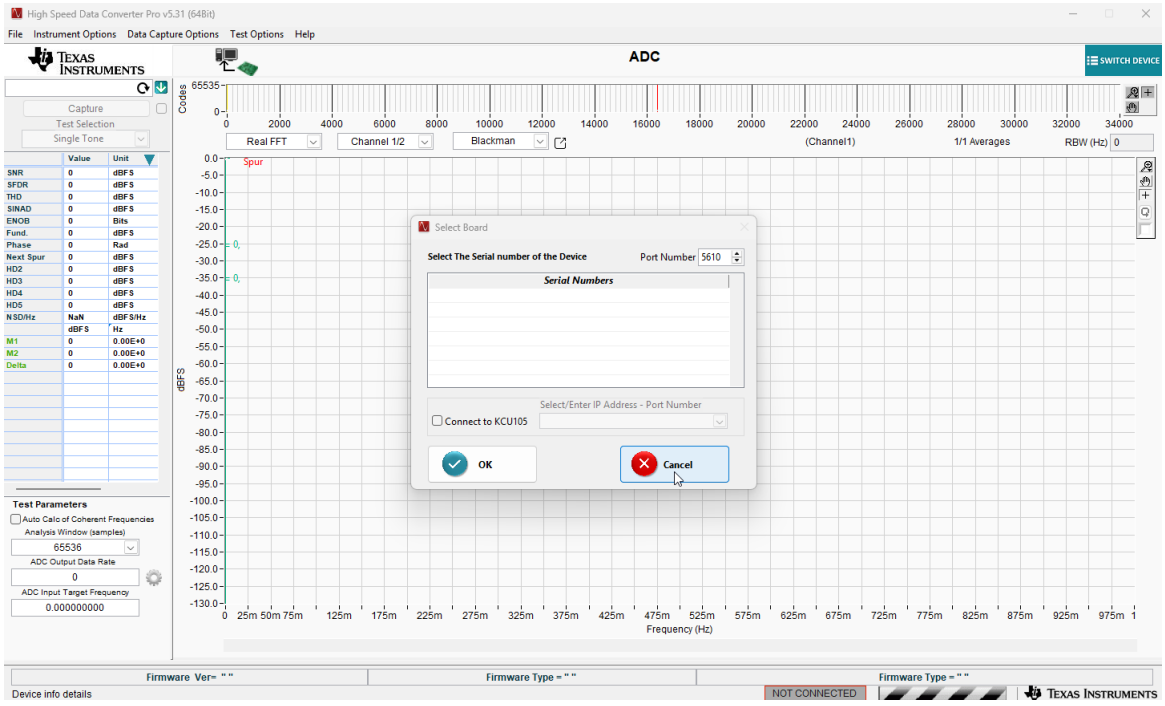


Figure 4-3. HSDC Pro

10. Open the ADC36xxEVM GUI. Allow a few seconds for the GUI to connect to the TSWDC155EVM FPGA Capture board. The TSWDC155EVM will power on, and several LEDs will become illuminated, as shown below.

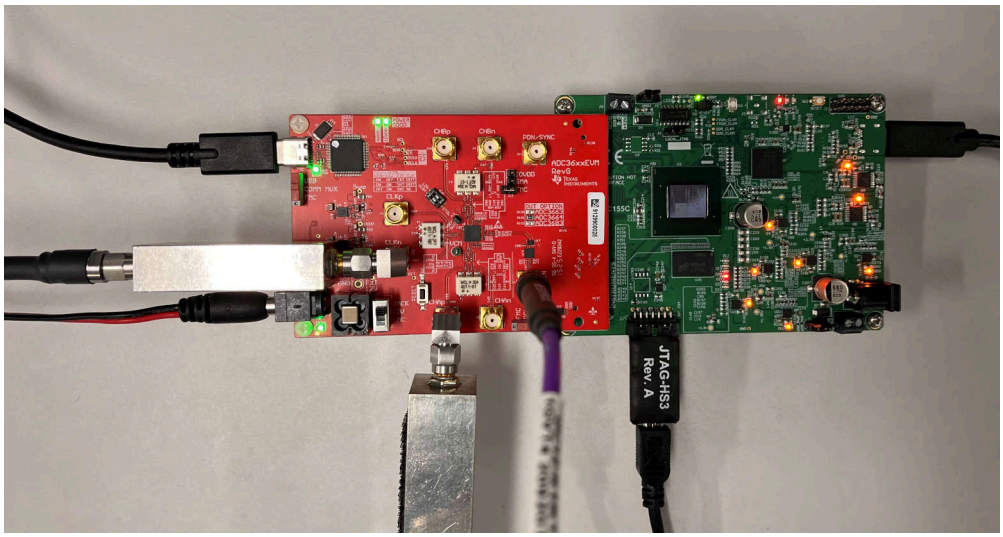


Figure 4-4. TSWDC155EVM powered on

11. When the GUI window has opened, you can configure the GUI into your desired mode. By default, the GUI is configured in 2-wire, bypass mode. These two defaults can remain the same. You will need to set the variant to ADC3683, resolution to 18-bit, and the Clocking Sample Frequency to 65MHz.

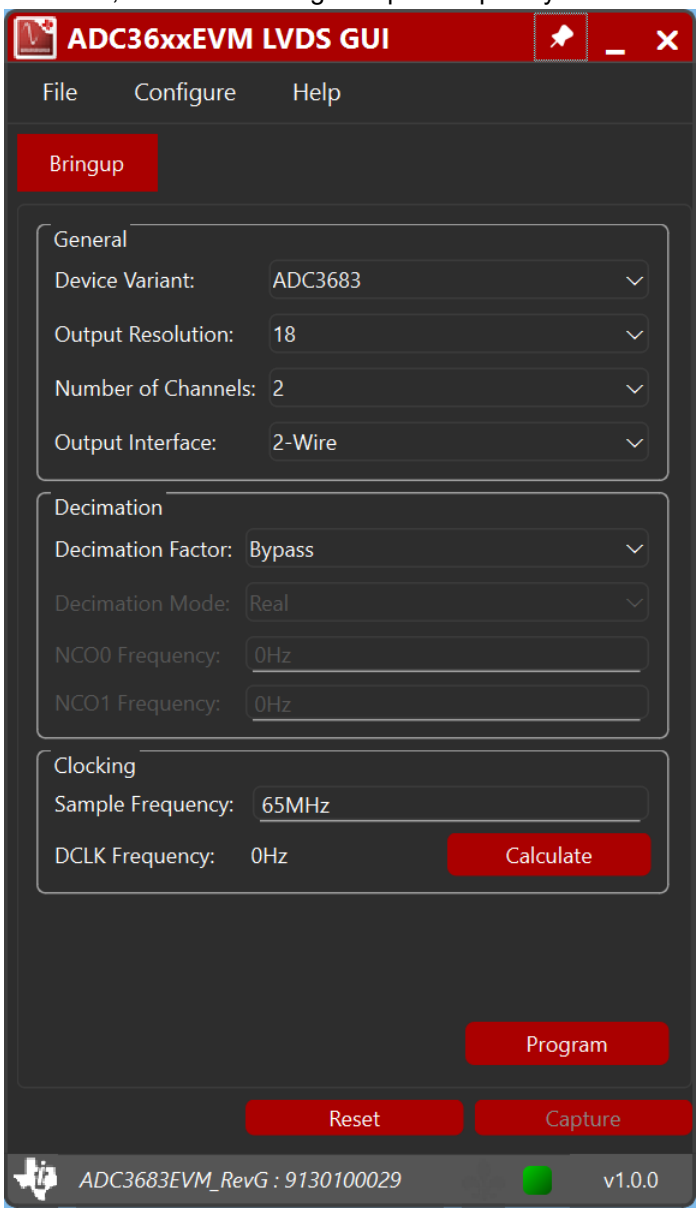


Figure 4-5. ADC36xx LVDS GUI Default With ADC3683 Configuration

12. Once the ADC mode has been selected, click on the “Calculate” button to calculate the necessary DCLK. For this mode, the DCLK should be 292.5MHz. Ensure this signal is provided to the DCLK input on the hardware setup.

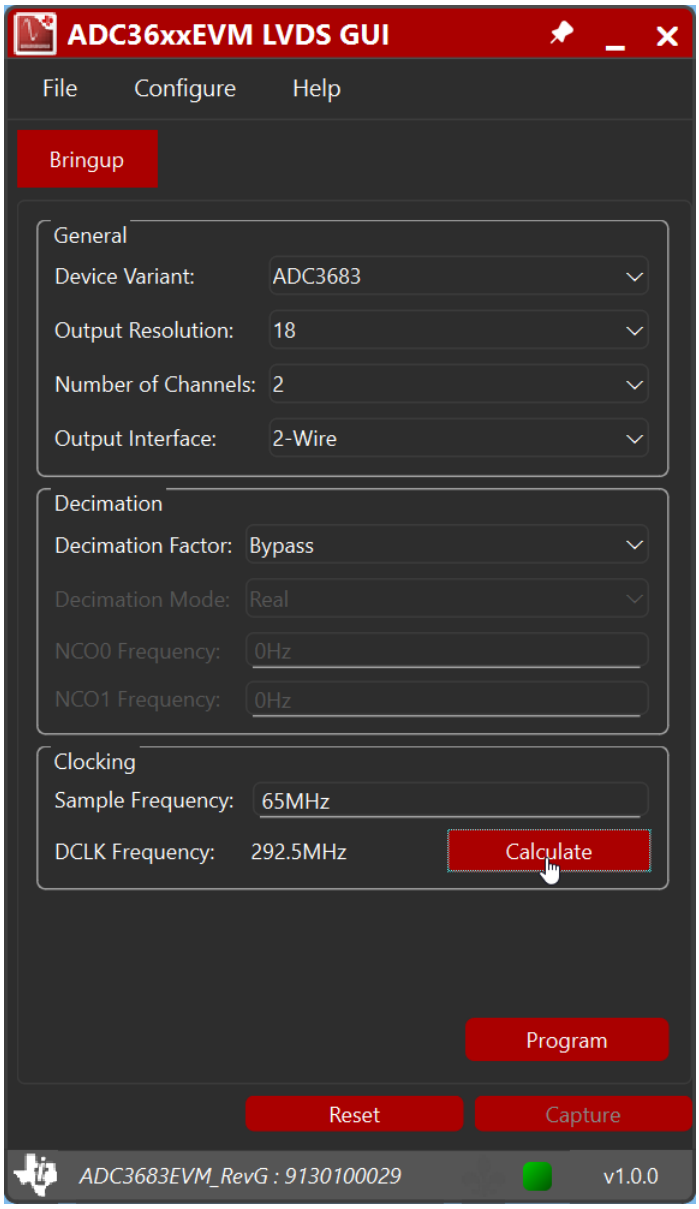


Figure 4-6. Calculating DCLK Frequency for ADC3683

13. Click the “Program” button. Allow a few seconds to program the ADC, program the FPGA, and configure the FPGA firmware.

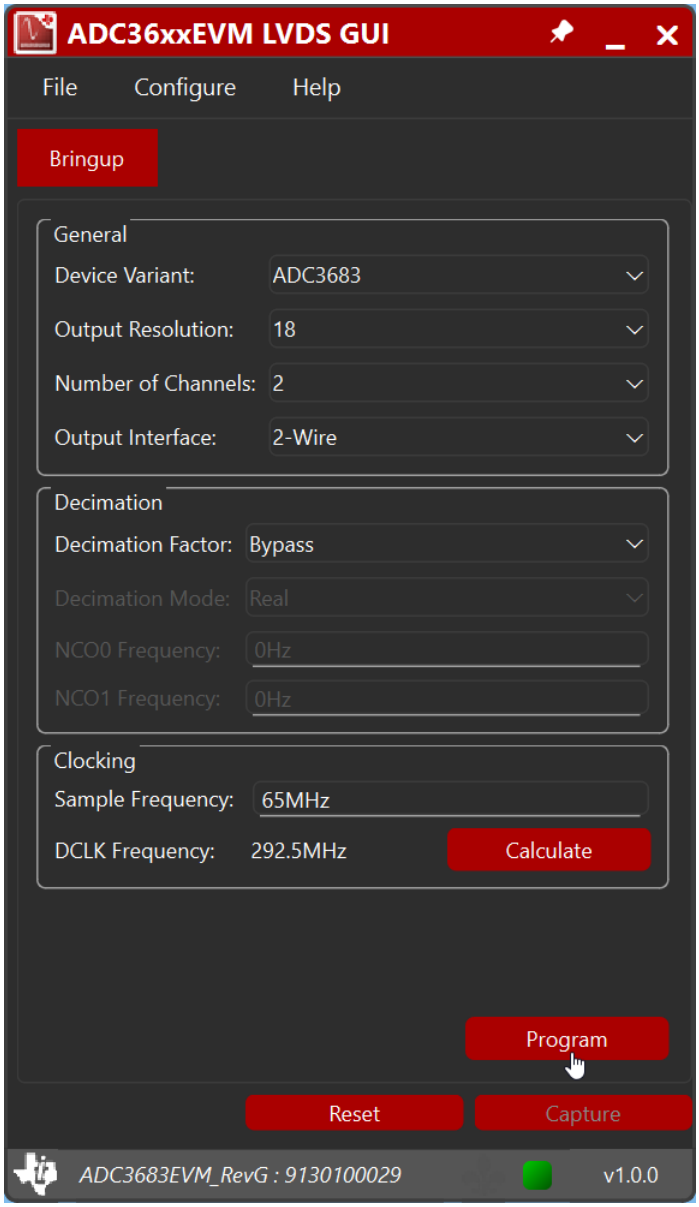


Figure 4-7. Programming the ADC3683EVM

14. Once programming is complete, click the "Capture" button to take an FFT data capture.

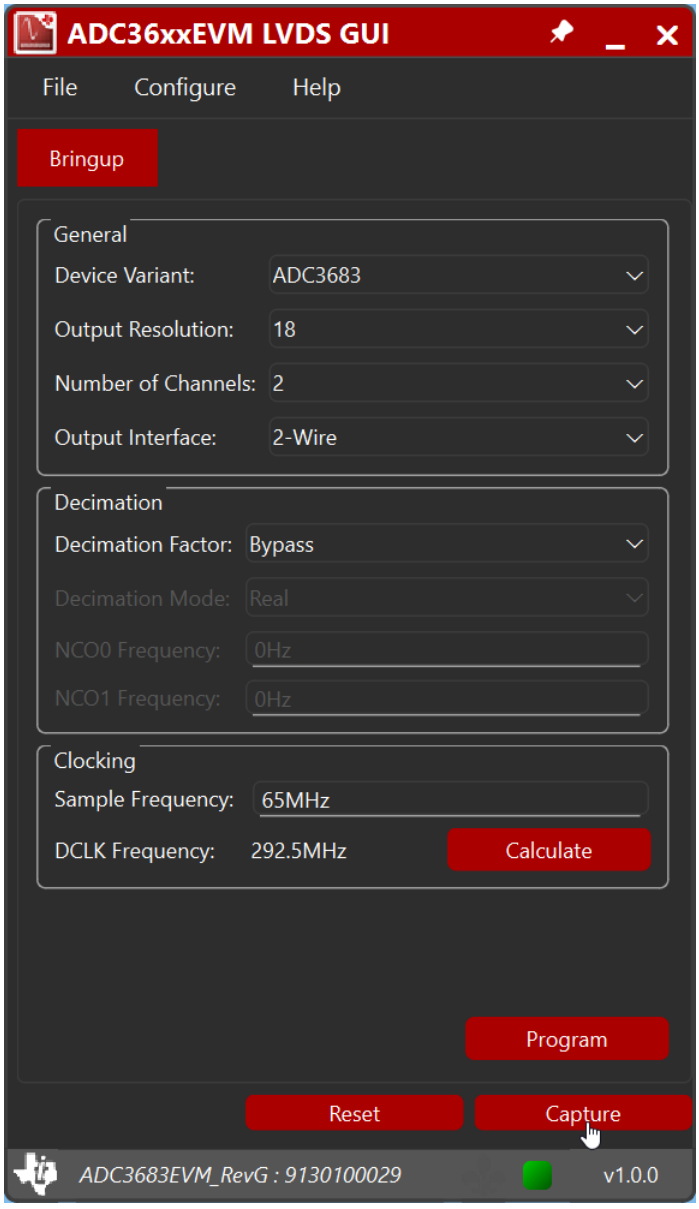


Figure 4-8. Capturing the FFT

15. After a few seconds, the captured data will appear in the HSDC Pro window, where you can view the performance of the device. For more functions and features of HSDC Pro, see the HSDC Pro User Guide.

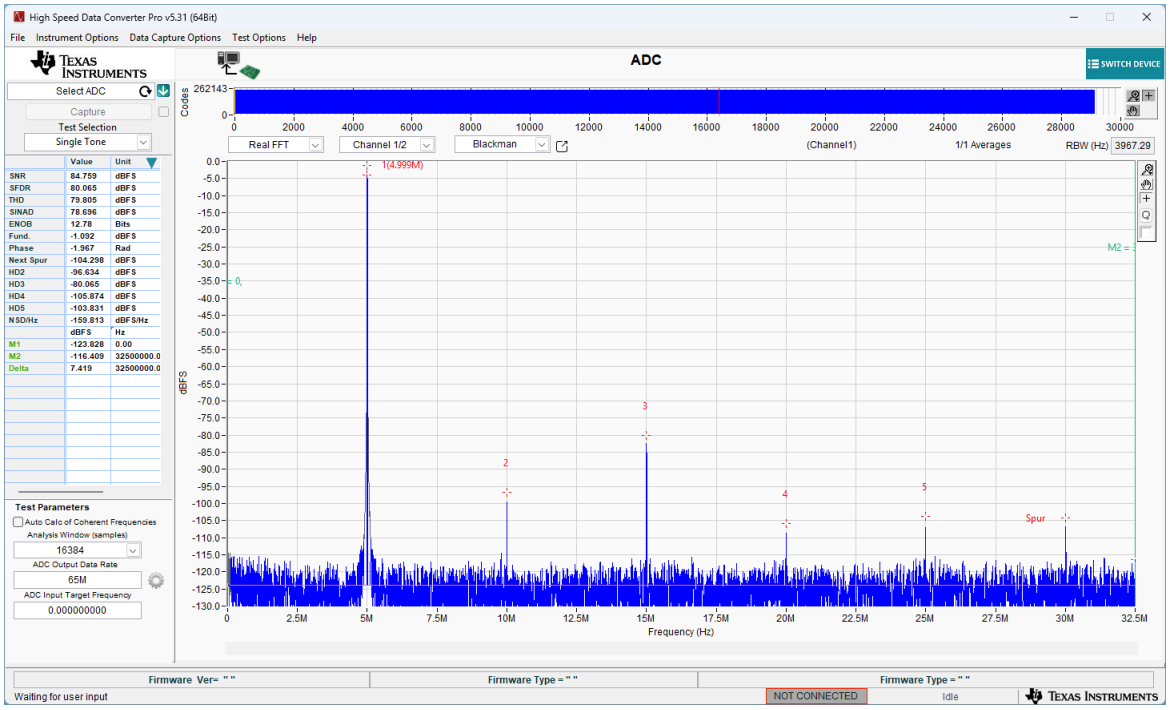


Figure 4-9. ADC3683EVM FFT Data Capture in HSDC Pro

16. If an error occurs when running the capture function, restart the GUI and follow steps 5-8 again.

4.2 Setting up the ADC3664EVM

1. Ensure the software is set up according to the Software Setup section.
2. Ensure the hardware is set up according to the Hardware Setup section
3. To provide the CLK signal:
   a. Using an SMA cable and an inline 125MHz band pass filter, connect the signal generator to the CLKn SMA connector (J5) on the ADC3664EVM.
   b. Set the signal generator's output signal frequency to 125MHz and the signal amplitude to +10dBm.
4. By default, the EVM is configured to take a single ended input, so analog inputs should be applied to connectors CHAp (J7) for Channel A or CHBp (J9) for Channel B. To provide an analog input:
   a. Using an SMA cable and an inline 5MHz band pass filter, connect the signal generator to analog input channel A.
   b. Set the signal generator's output signal frequency to 5.135MHz (prime number) and 0dBm.
5. To provide a DCLK signal:
   a. Using an SMA cable, connect the signal generator to the DCLKIN SMA connector (J6).
   b. Set the signal generator's output frequency to 437.5MHz (14-bit, 2-wire, DDC bypass) and the signal amplitude to +2dBm.

6. Ensure all signal generators for clock, analog input and DCLK are referenced locked using the 10MHz REF on the back of the signal generators. For an example of this, please see figure below.

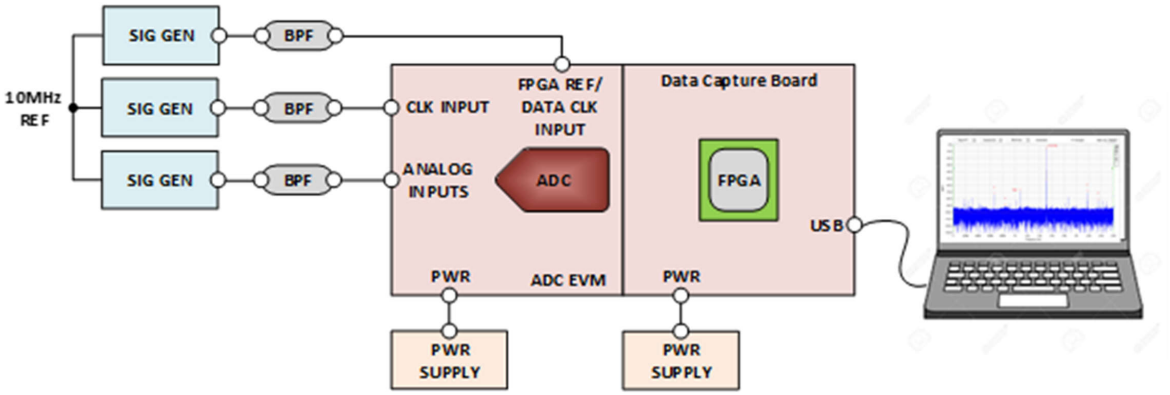


Figure 4-10. Basic Test Measurement Setup

7. Your setup should now look like the following:

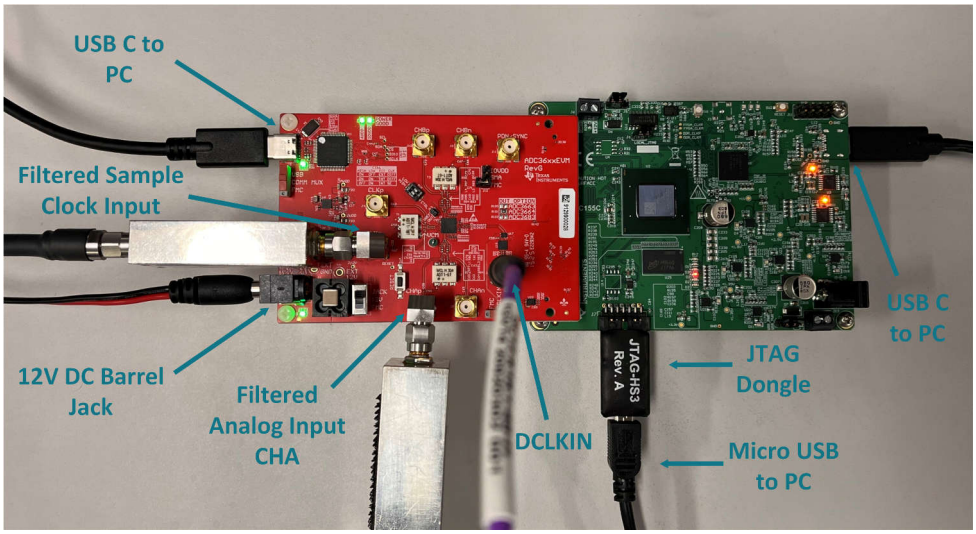


Figure 4-11. ADC3664EVM Hardware Setup

8. Open HSDC Pro. Always ensure that HSDC Pro is open **before** opening the ADC36xxEVM GUI.

9. Click on cancel when prompted to connect to a board. The GUI will handle all of the other HSDC Pro capture and configuration related operations.

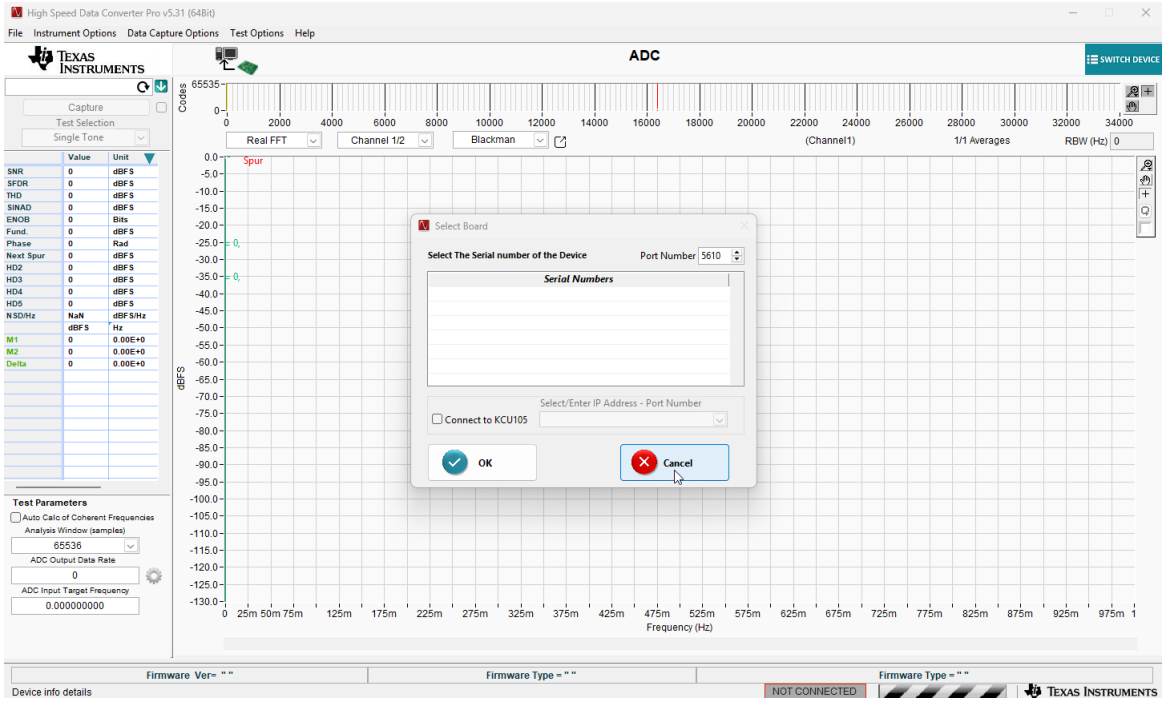


Figure 4-12. HSDC Pro

10. Open the ADC36xxEVM GUI. Allow a few seconds for the GUI to connect to the TSWDC155EVM FPGA Capture board. The TSWDC155EVM will power on, and several LEDs will become illuminated, as shown below.

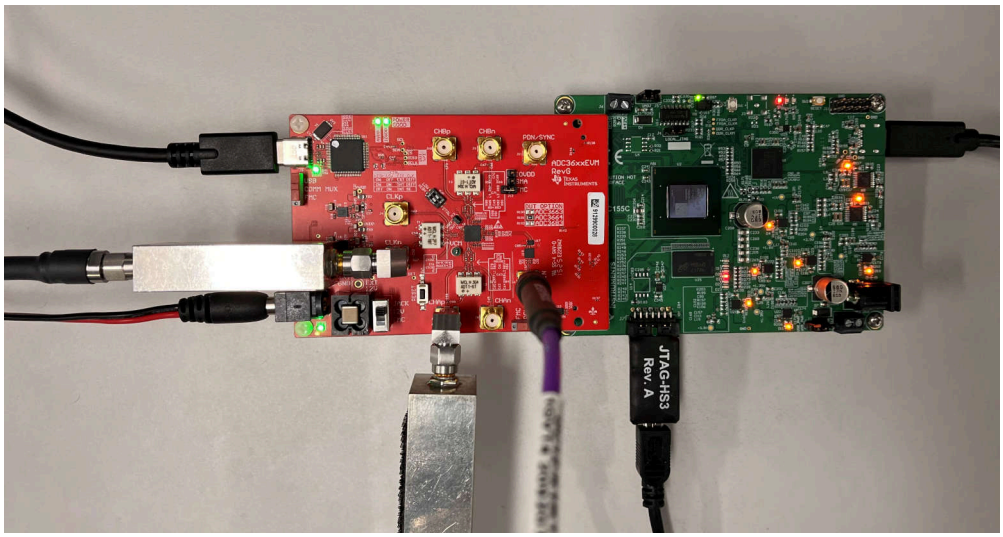


Figure 4-13. TSWDC155EVM powered on

11. When the GUI window has opened, you can configure the GUI into your desired mode. By default, the GUI is configured in 2-wire, bypass mode. These two defaults can remain the same. You will need to set the variant to ADC3664, resolution to 14-bit, and the Clocking Sample Frequency to 125MHz.

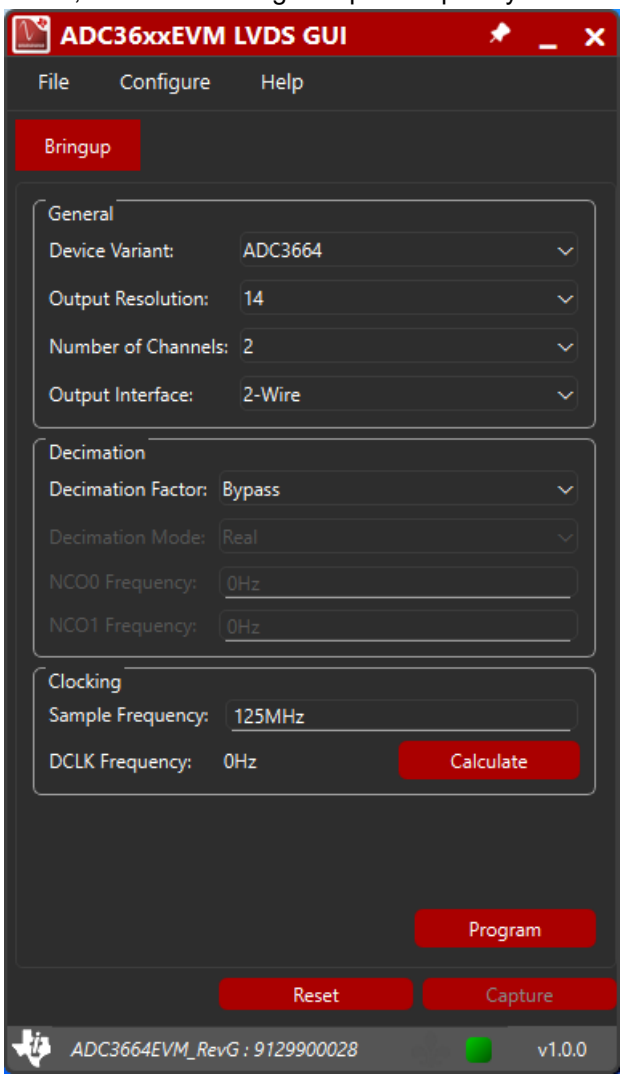


Figure 4-14. ADC36xx LVDS GUI Default With ADC3664 Configuration

12. Once the ADC mode has been selected, click on the “Calculate” button to calculate the necessary DCLK. For this mode, the DCLK should be 437.5MHz. Ensure this signal is provided to the DCLK input on the hardware setup.

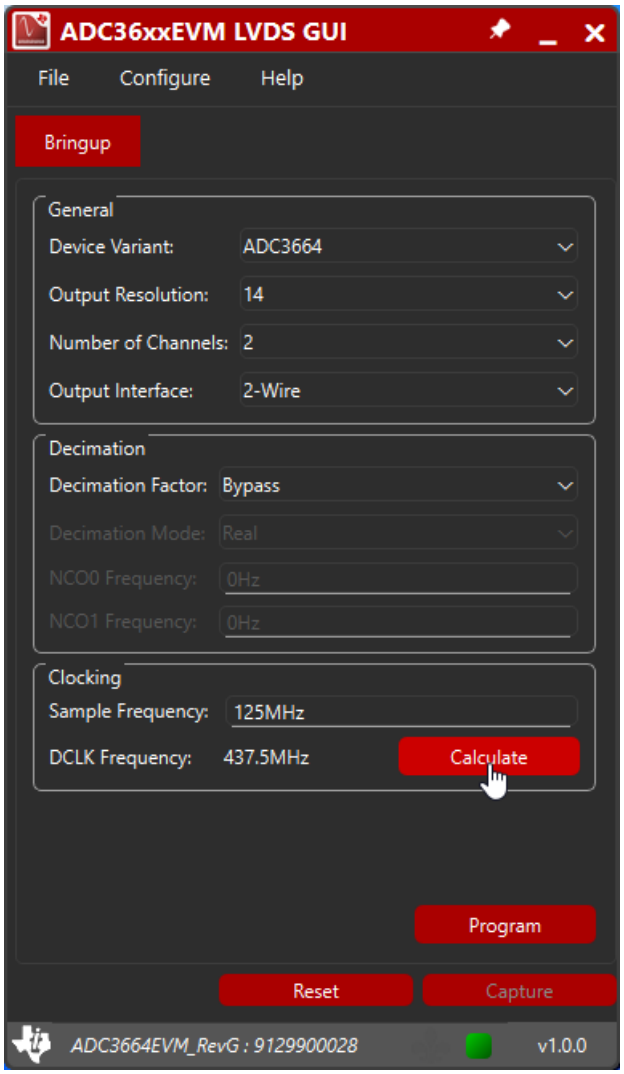


Figure 4-15. Calculating DCLK Frequency for ADC3664

13. Click the “Program” button. Allow a few seconds to program the ADC, program the FPGA, and configure the FPGA firmware.

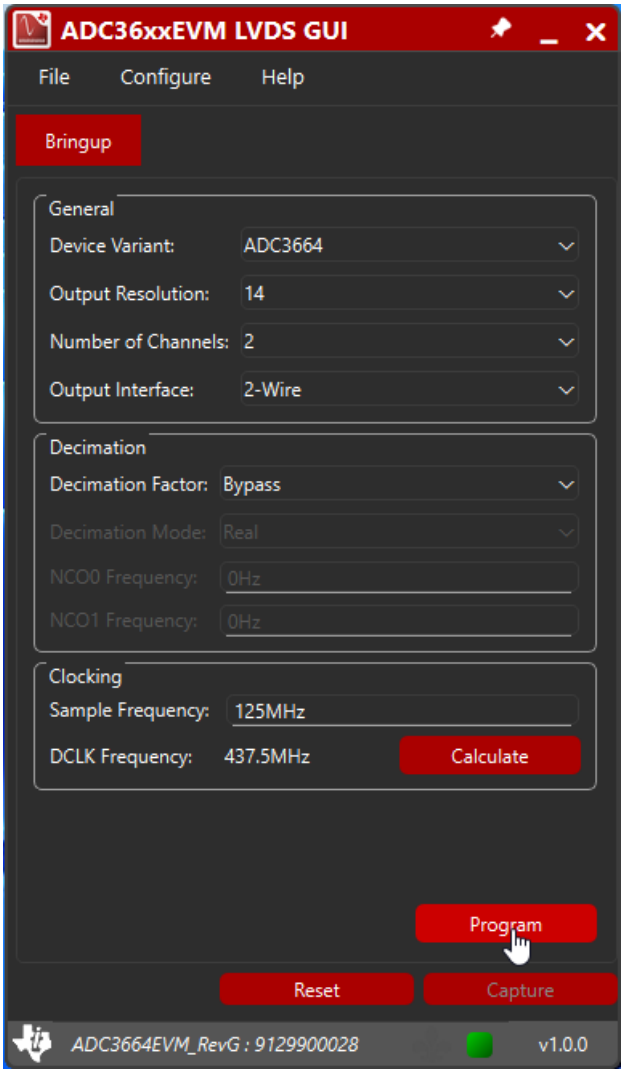


Figure 4-16. Programming the ADC3664EVM

14. Once programming is complete, click the "Capture" button to take an FFT data capture.

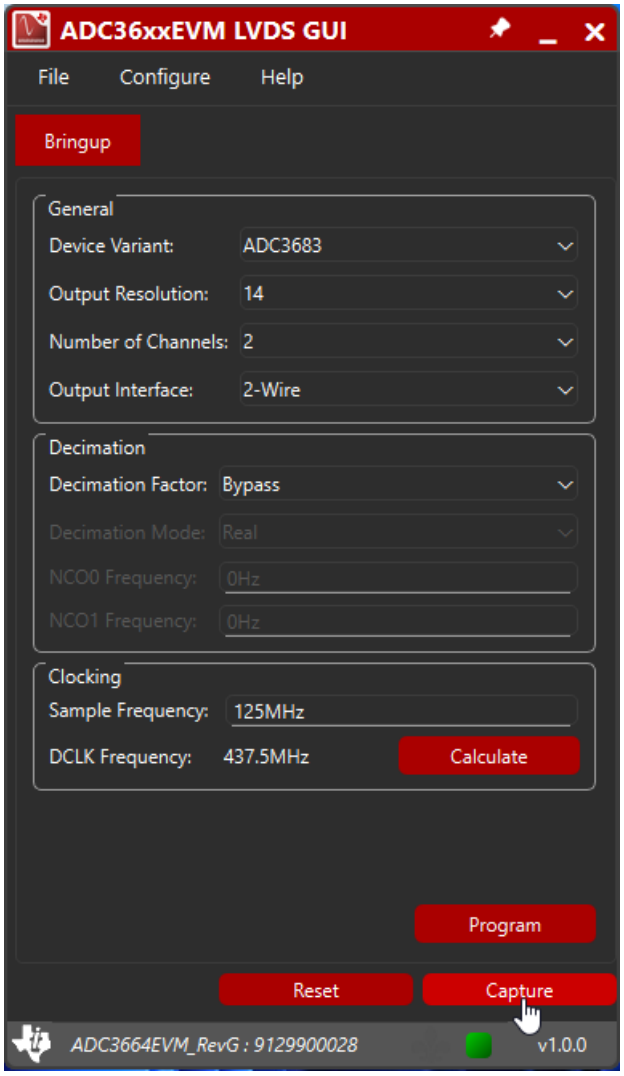


Figure 4-17. Capturing the FFT

15. After a few seconds, the captured data will appear in the HSDC Pro window, where you can view the performance of the device. For more functions and features of HSDC Pro, see the HSDC Pro User Guide.

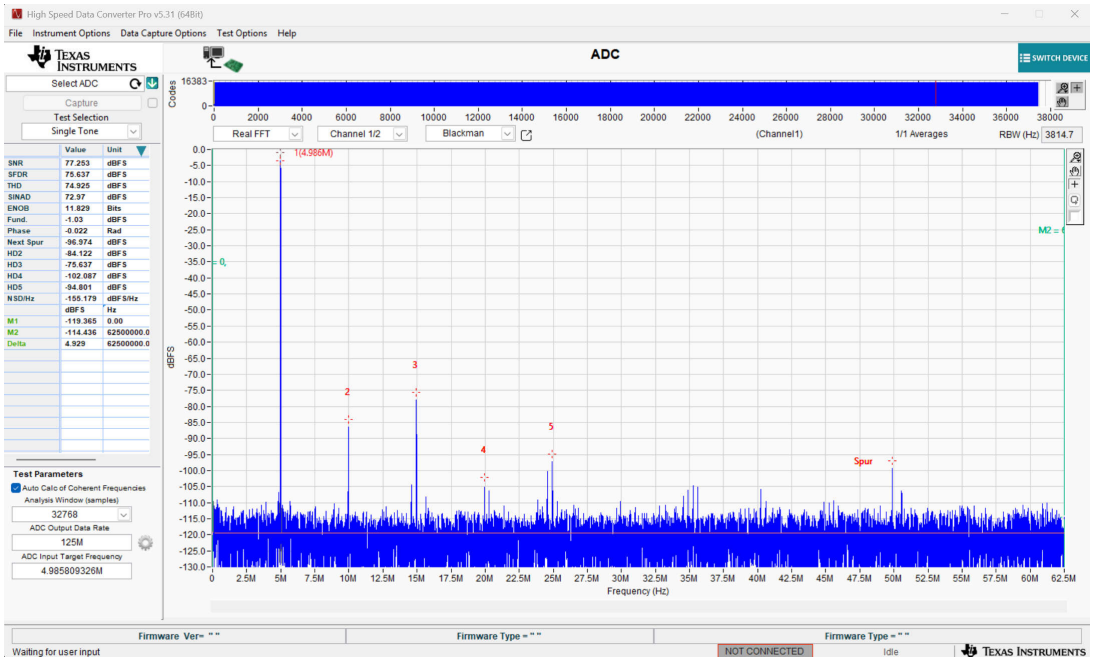


Figure 4-18. ADC3664EVM FFT Data Capture in HSDC Pro

16. If an error occurs when running the capture function, restart the GUI and follow steps 5-8 again.

4.3 Setting up the ADC3663EVM

1. Ensure the software is set up according to the Software Setup section.
2. Ensure the hardware is set up according to the Hardware Setup section
3. To provide the CLK signal:
   a. Using an SMA cable and an inline 65MHz band pass filter, connect the signal generator to the CLKn SMA connector (J5) on the ADC3663EVM.
   b. Set the signal generator's output signal frequency to 65MHz and the signal amplitude to +10dBm.
4. By default, the EVM is configured to take a single ended input, so analog inputs should be applied to connectors CHAp (J7) for Channel A or CHBp (J9) for Channel B. To provide an analog input:
   a. Using an SMA cable and an inline 5MHz band pass filter, connect the signal generator to analog input channel A.
   b. Set the signal generator's output signal frequency to 5.135MHz (prime number) and 0dBm.
5. To provide a DCLK signal:
   a. Using an SMA cable, connect the signal generator to the DCLKIN SMA connector (J6).
   b. Set the signal generator's output frequency to 260MHz (16-bit, 2-wire, DDC bypass) and the signal amplitude to +2dBm.
6. Ensure all signal generators for clock, analog input and DCLK are referenced locked using the 10MHz REF on the back of the signal generators. For an example of this, please see figure below.

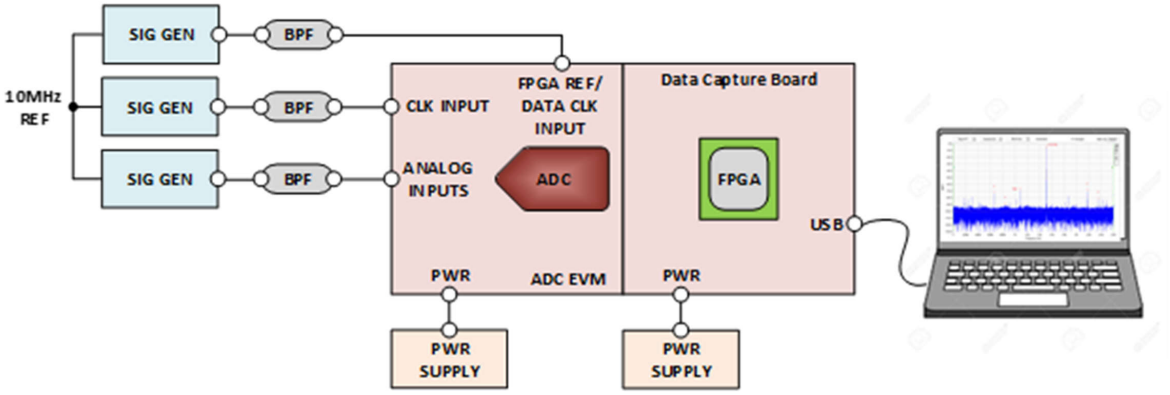


Figure 4-19. Basic Test Measurement Setup

7. Your setup should now look like the following:

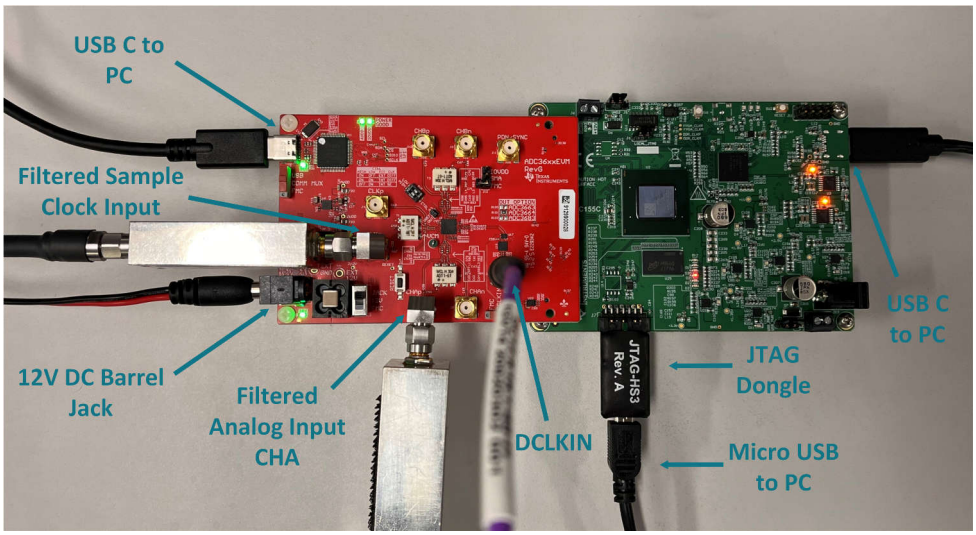


Figure 4-20. ADC3663EVM Hardware Setup

8. Open HSDC Pro. Always ensure that HSDC Pro is open **before** opening the ADC36xxEVM GUI.

9. Click on cancel when prompted to connect to a board. The GUI will handle all of the other HSDC Pro capture and configuration related operations.

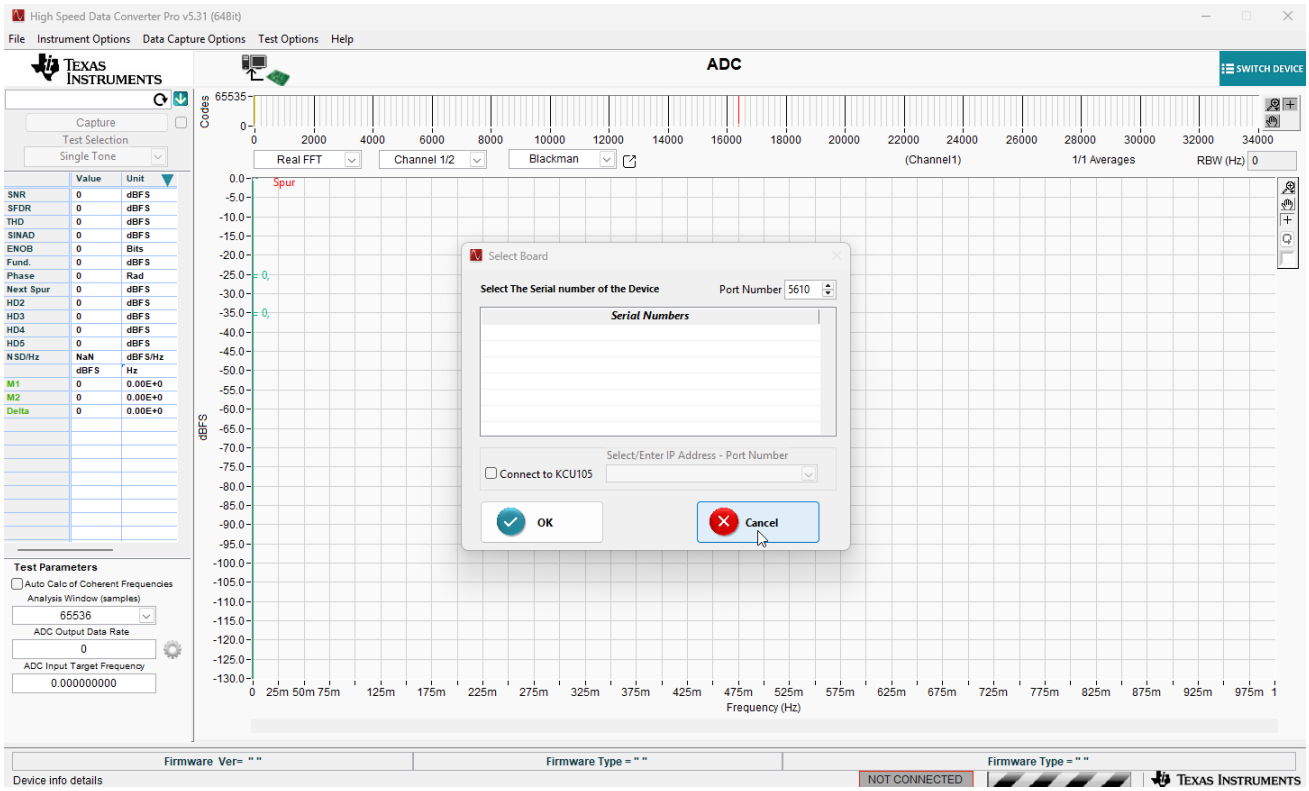


Figure 4-21. HSDC Pro

10. Open the ADC36xxEVM GUI. Allow a few seconds for the GUI to connect to the TSWDC155EVM FPGA Capture board. The TSWDC155EVM will power on, and several LEDs will become illuminated, as shown below.

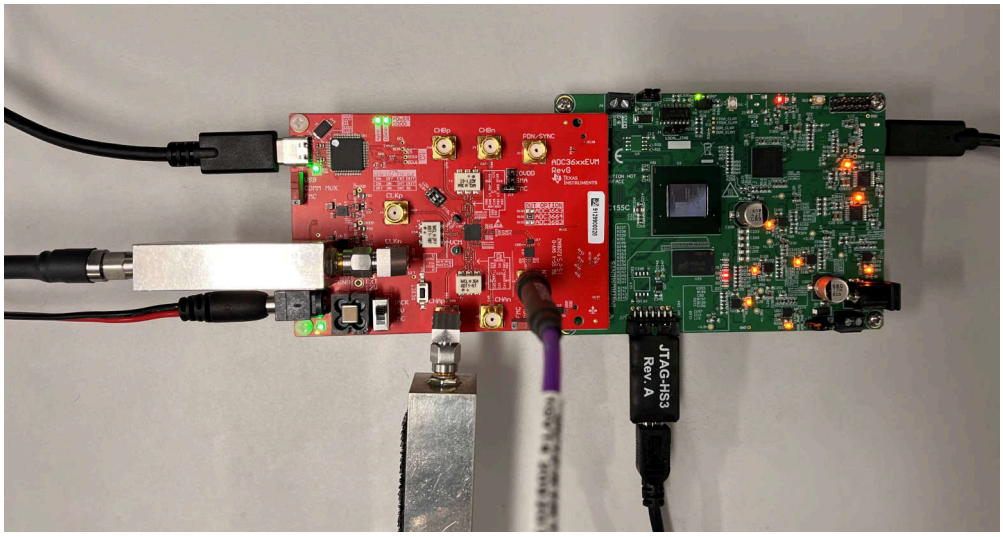


Figure 4-22. TSWDC155EVM powered on

11. When the GUI window has opened, you can configure the GUI into your desired mode. By default, the GUI is configured in 2-wire, bypass mode. These two defaults can remain the same. You will need to set the variant to ADC3663, resolution to 16-bit, and the Clocking Sample Frequency to 65MHz.

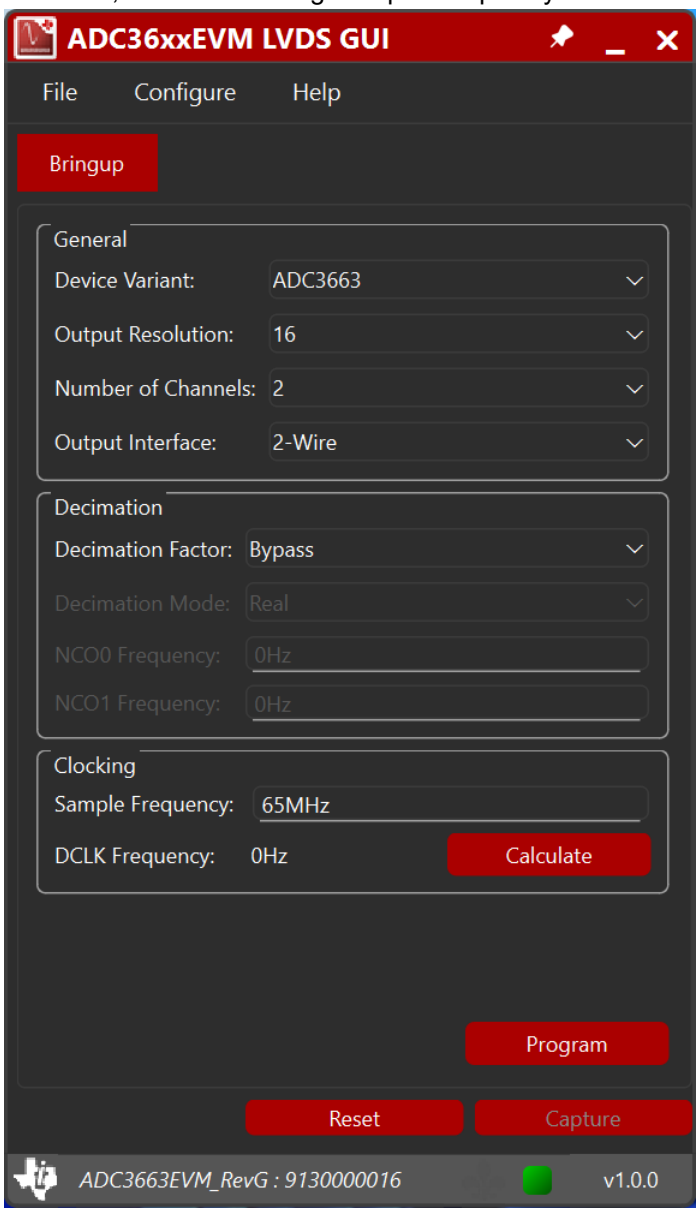


Figure 4-23. ADC36xx LVDS GUI Default With ADC3663 Configuration

12. Once the ADC mode has been selected, click on the “Calculate” button to calculate the necessary DCLK. For this mode, the DCLK should be 260MHz. Ensure this signal is provided to the DCLK input on the hardware setup.

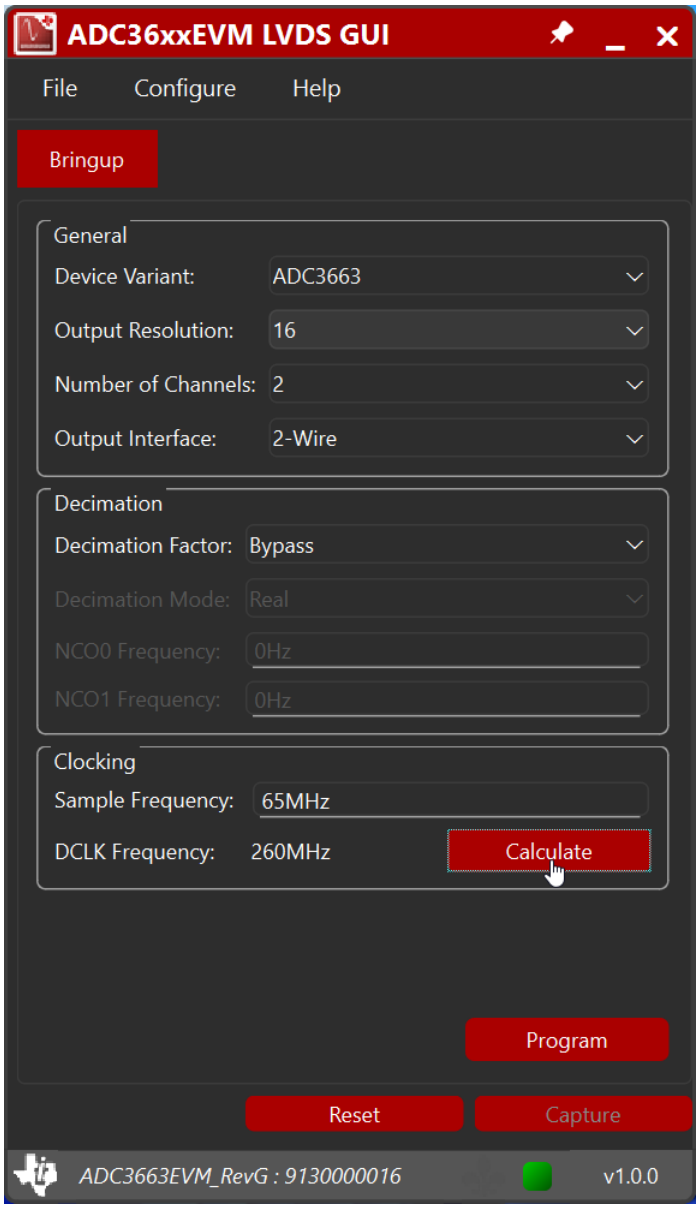


Figure 4-24. Calculating DCLK Frequency for ADC3663

13. Click the “Program” button. Allow a few seconds to program the ADC, program the FPGA, and configure the FPGA firmware.

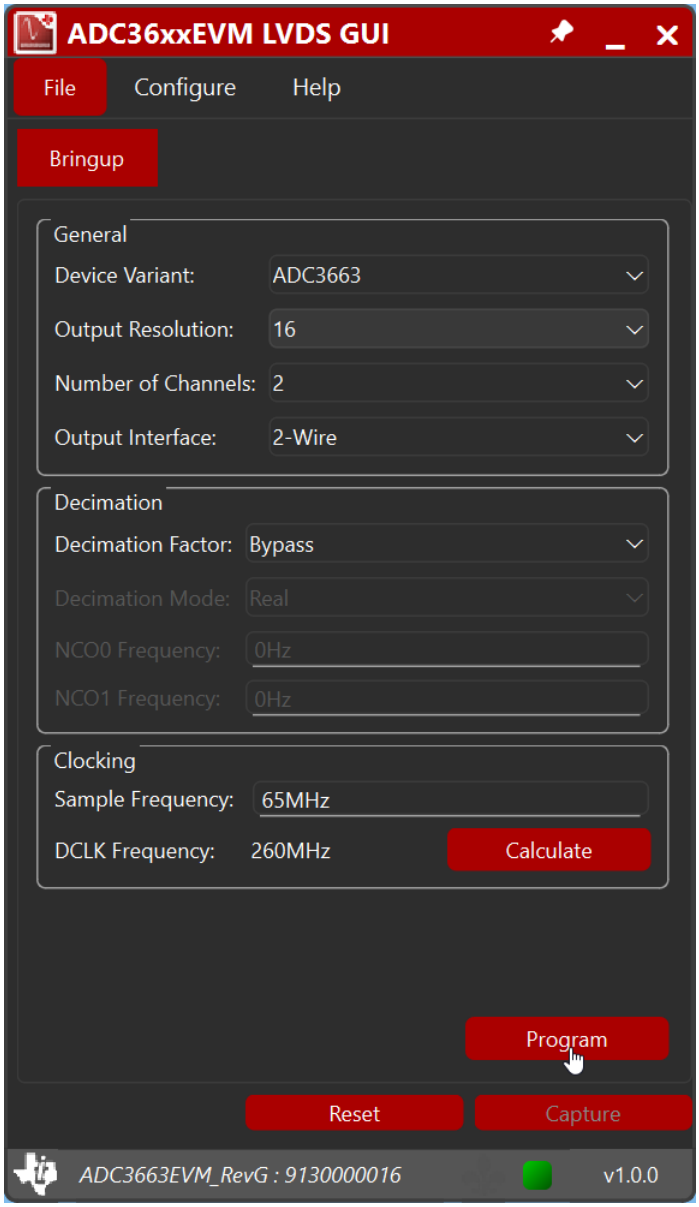


Figure 4-25. Programming the ADC3663EVM

14. Once programming is complete, click the "Capture" button to take an FFT data capture.

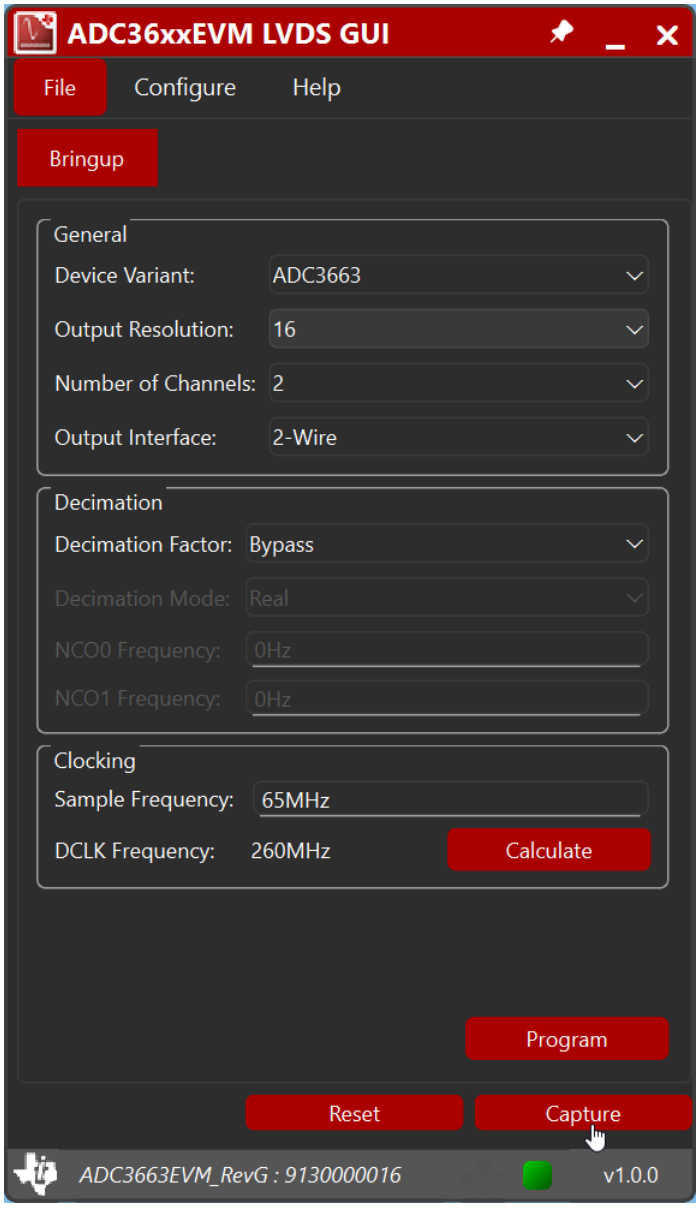


Figure 4-26. Capturing the FFT

15. After a few seconds, the captured data will appear in the HSDC Pro window, where you can view the performance of the device. For more functions and features of HSDC Pro, see the HSDC Pro User Guide.

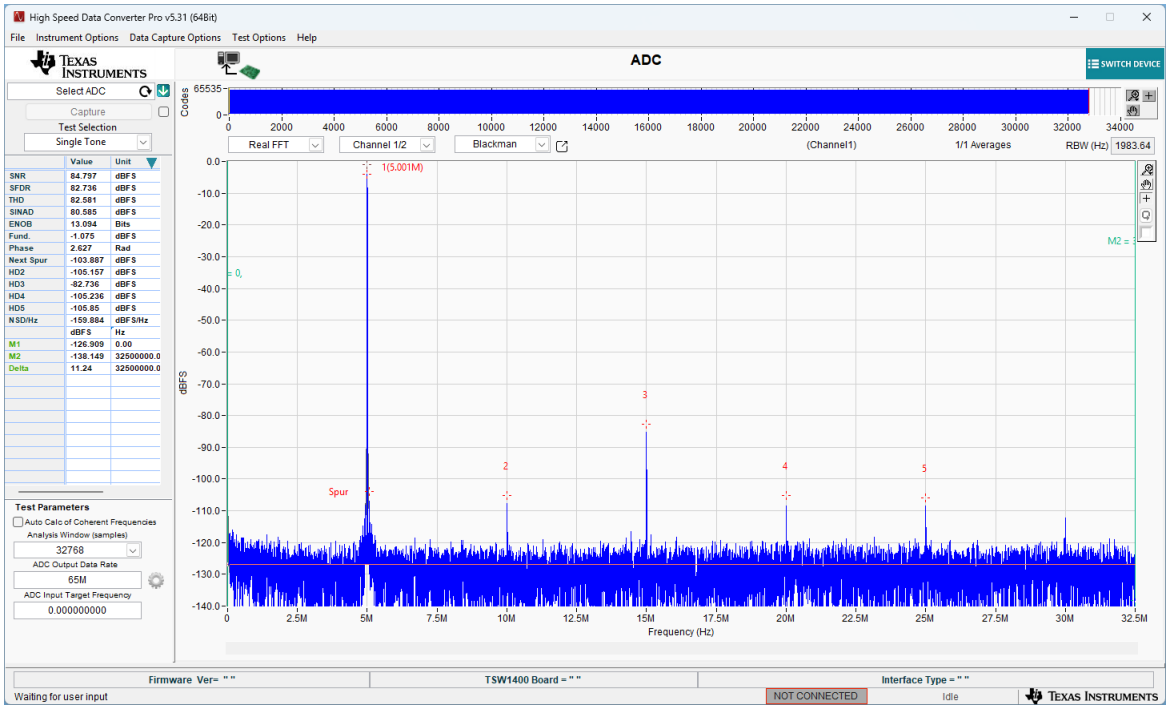


Figure 4-27. ADC3663EVM FFT Data Capture in HSDC Pro

16. If an error occurs when running the capture function, restart the GUI and follow steps 5-8 again.

5 Hardware Design Files

The design files (schematics, PCB layout, and bill of materials (BOM) are available on the product page: ADC3663EVM, ADC3664EVM, and ADC3683EVM.

6 Additional Information

6.1 Trademarks

All trademarks are the property of their respective owners.

7 References

- Texas Instruments, ADC3663EVM product page
- Texas Instruments, ADC3664EVM product page
- Texas Instruments, ADC3683EVM product page
- Texas Instruments, TSWDC155 Evaluation Module, user's guide
- Texas Instruments, High Speed Data Converter Pro GUI, user's guide
- Texas Instruments, ADC366x 16-Bit, 0.5-MSPS to 65-MSPS, Low-Noise, Low Power, Dual-Channel ADC, data sheet
- Texas Instruments, ADC3664 14-Bit, 125-MSPS, Low-Noise, Low Power Dual Channel ADC, data sheet
- Texas Instruments, ADC368x 18-bit 0.5 to 65-MSPS Low Noise Ultra-low Power Dual Channel ADC, data sheet

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