Application Brief

Designing for Daytime Running Lights with TPLD1202-Q1

Introduction

Daytime running lights (DRLs) are now widely seen in modern vehicles. Most designs are designed with a 555 timer and reference op amps to generate a pulse width modulation (PWM) and to detect faults. Both of these functions can be replaced with a single TPLD1202 device, in turn saving board space and costs, and simplifying designs.

PWM Dimming

The reference design *Automotive Daytime Running Light (DRL) LED Driver Reference Design with Linear Thermal Foldback* utilizes a 555 timer to help generate a PWM signal to dim the LEDs. Instead of using an external device, the TPLD1202 features a PWM generator with adjustable duty cycle and frequencies. The duty cycle is modified using counter data, calculated by Duty cycle (%) = (DATA/256) × 100. This ranges from a minimum of 0% to 99.61% duty cycle percentage.

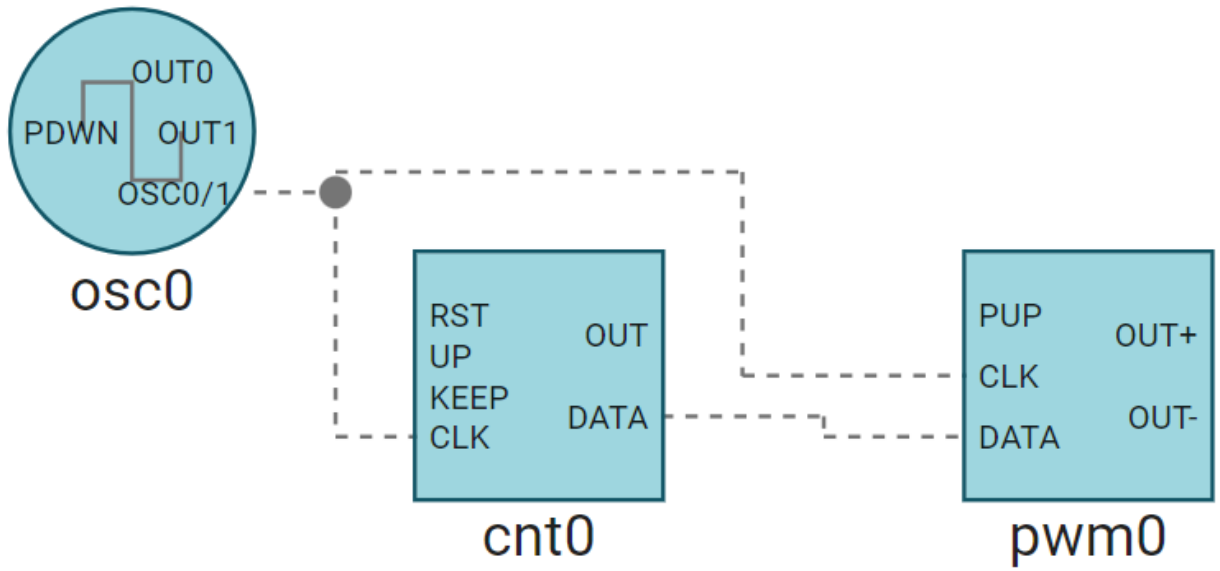

Figure 1. PWM Generator Block

For a detailed description of the PWM generator featured in TPLD1202-Q1, please refer to the applications brief *PWM Generators in TI Programmable Logic Devices*.

Fault Detection

Detecting a fault in an LED string is as simple as monitoring the MOSFET drain voltage. For more information, please refer to the two-part Technical Article:

- *Designing Daytime Running Lights, Part 1: Adding One-fail-all-fail LED Fault Detection*
- *Designing Daytime Running Lights, Part 2: Responding to an LED Fault*

As a summary, there are four different possible faults that can be detected in different ways:

- LED short in mirror string
  - $V_{drain} = (2 \times V_f) + (I_{mirror} \times R0)$
- LED short in reference string
  - $V_{drain} = I_{mirror} \times R0$
- Open circuit in mirror string
  - $V_{drain} = 0V$
- Open circuit in reference string
  - V_{drain} oscillations

Functional operation of the LED string results in $V_{drain,normal} = V_f + (I_{mirror} \times R0)$. We can see that the first three fault states result in a voltage higher or lower than $V_{drain,normal}$. A fault detector can be implemented with a window comparator, with an upper limit of 110% and lower limit of 90% of $V_{drain,normal}$. When V_{drain} is within 90-110% of $V_{drain,normal}$, the comparator outputs high, otherwise outputting low.

The fourth fault state can be difficult to detect as the oscillations make the output of the comparator pulse repeatedly. This is solved by latching the output of the window comparator the first time the voltage exits the “good” window.

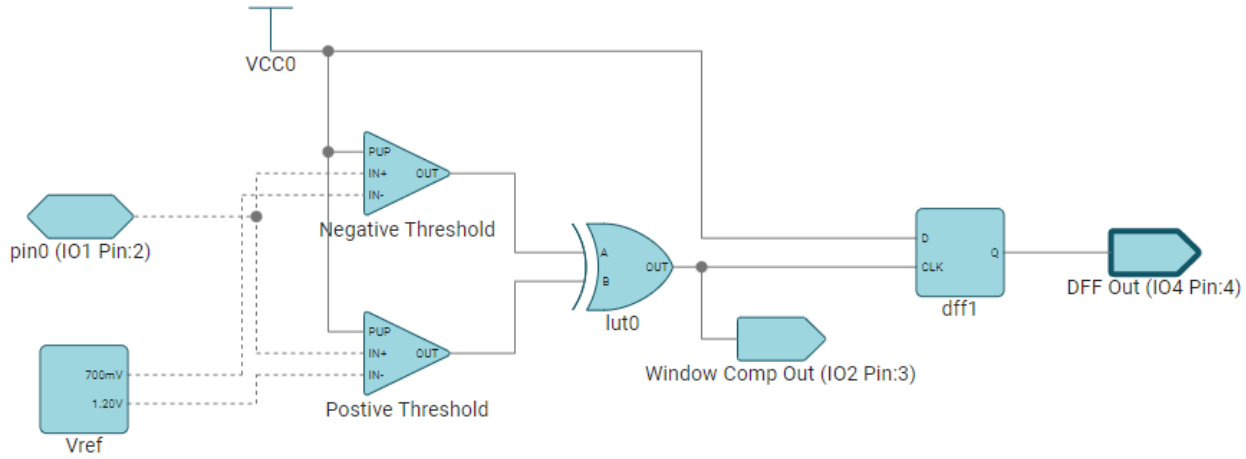

Figure 2. Fault Detection Implementation

The original design in *Designing Daytime Running Lights, Part 2: Responding to an LED Fault* is a minimum two device implementation that can be replaced by one TPLD. This, in addition to utilizing the TPLD PWM generator results in one TPLD1202 replacing 3+ devices.

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