

Fundamentals of JESD204D and Implementation in AFE819x



Benjamin Uhing

Abstract

The JEDEC JESD204D standard defines a high-speed serial interface for data converters (ADCs and DACs), and for the next generation communications applications requiring greater than 1 GHz of instantaneous bandwidth. Perhaps the most prevalent example can be wireless infrastructure systems and the associated signal bandwidth demands for the 5G and upcoming 6G definitions. Compared to the previous JESD204C standard, JESD204D increases the supported data rate to 112Gbps by employing PAM4 signaling and Reed-Solomon forward error correction (RS-FEC) to mitigate the resulting higher bit error rates (BER). A subset of Texas Instruments' AFE819x family of RF sampling transceivers implement JESD204D Subclass 1 to transmit and receive digital converter data for ADC and DAC cores. This implementation enables higher RF signal bandwidth and reduces system bill-of-materials (BOM) costs and power consumption by decreasing the required number of transceiver devices per radio product. The AFE819x family incorporates various test modes and error reporting mechanisms to facilitate JESD204D link bring-up and maintain the functionality of each layer. This application note details the AFE819x family's implementation of the JESD204D standard and outlines the included test modes and error reports for link bring-up and optimization.

For the full access to the application note, see *Leveraging JESD204D in AFE819x for Enhanced Bandwidth in Wireless Infrastructure* (SBAU477).

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