Analog Engineer's Circuit

Circuit Showing Overstress Protection on ADC With Integrated Analog Front End

Dale Li

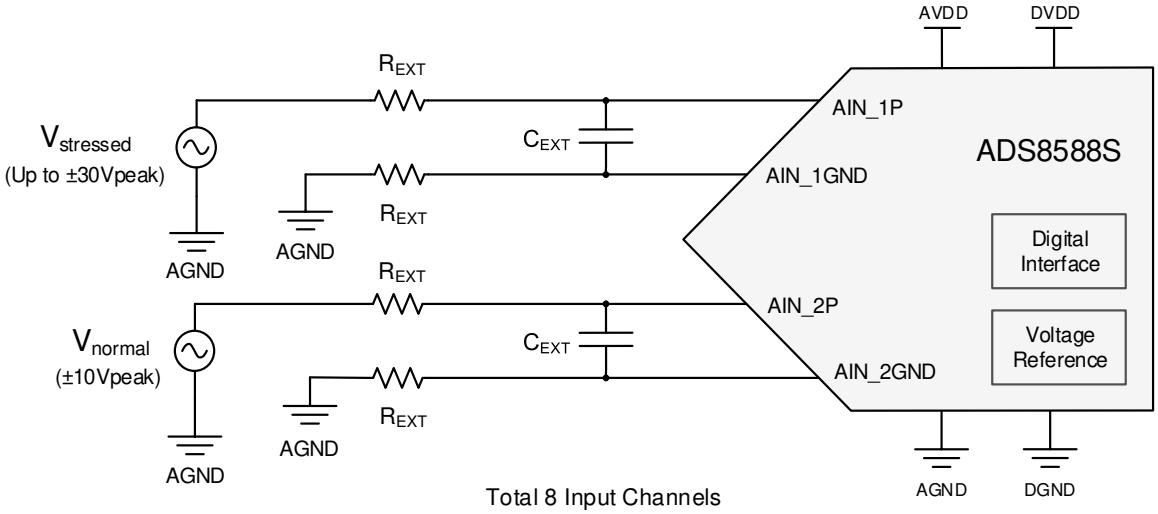
Input	ADC Input	Digital Output ADS7042
VinSEMin = –10V	CH_x = –10V	8000H
VinSE = 0V	CH_x = 0V	0000H
VinSEMax = +10V	CH_x = +10V	7FFFH

Power Supplies

AVDD	DVDD	Valid Input V_{normal}	Overvoltage Input $V_{stressed}$
5V	3.3V	±10V	

Design Description

For protection relay applications in smart grid markets, a simultaneous sampling ADC, such as ADS8588S, is widely used to maintain the phase information between different voltage and current. The working environment of these systems is very harsh and undesired signals with amplitudes up to ±30Vpk (60Vpp) can apply to the signal chain. Hence, it is important to protect the ADC input from overvoltage damage and also maintain good performance. This document shows how to design the overvoltage protection and also shows the performance impact of the overvoltage signal on adjacent channels. Finally, the performance impact results are compared between a Texas Instruments device and a pin for pin compatible competitor device.



Specifications

Specification	Calculated	Measured
60Vpp Overvoltage	Max Input Current = 1mA	SNR and THD performance and overvoltage feedthrough

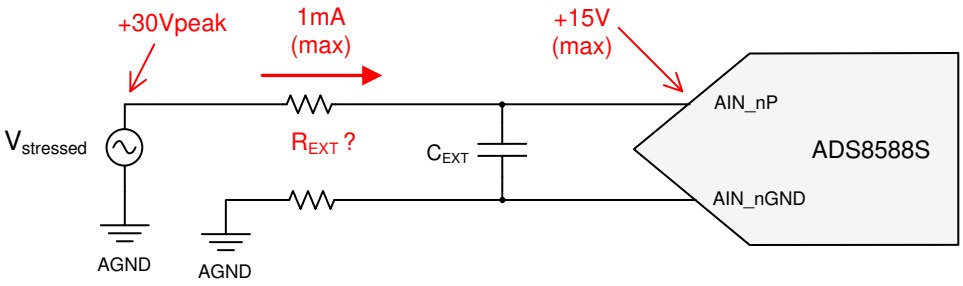
Design Notes

1. Use COG type capacitors for the C_{EXT} filter capacitor.
2. Review the *Electrical Overstress* video series for a theoretical explanation of overstress on amplifiers. Although this section covers amplifiers, the theory apples to data converters as well.

Component Selection

1. Find $R_{ext(min)}$ to limit the current less than 1mA. The suggested maximum current flowing into the ADS8588S input pins is ±10mA which is commonly required based on the internal structure of the ADC. This 10mA is an absolute maximum limit, and it is better to have some margins around this number, restricting the current less than 1mA is recommended. For this example design the minimum external resistance is 15kΩ.

$$R_{EXT} = \frac{30V - 15V}{1mA} = 15k\Omega$$

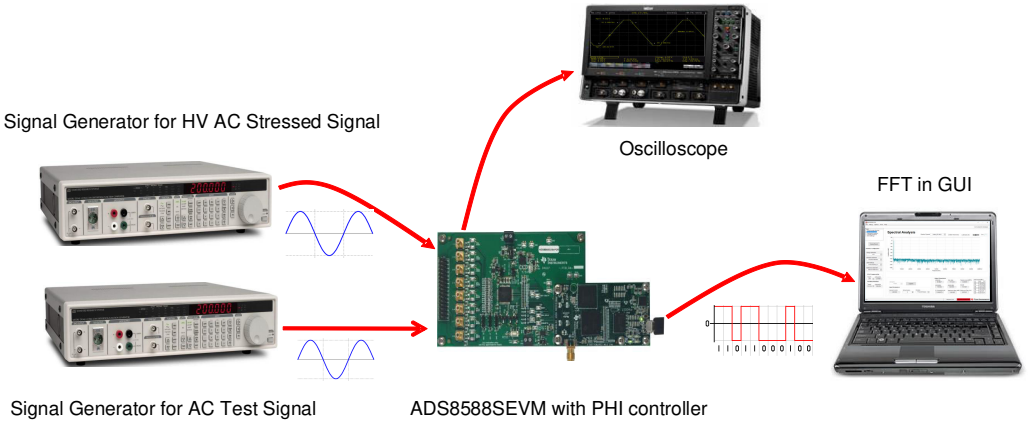


2. Choose R_{ext} or C_{ext} to set the bandwidth of the input filter to the desired frequency. Depending on the application, different cutoff frequencies are required. In this case the cutoff frequency must be 6.4kHz to accommodate 128 harmonics of a 50-Hz signal. In this case a 1-nF capacitor is also desired, as 1nF is a common industrial input filter capacitance value. After applying the equation, the external resistor (R_{ext}) is determined to be 24.9kΩ. Note that the external resistor calculated in this step is larger than the minimum resistance value from step 1 (is $R_{ext} > R_{ext(min)}$).

$$R_{EXT} = \frac{1}{2\pi \cdot f_c \cdot C_{EXT}} = \frac{1}{2\pi\,(6.4kHz)(1nF)} = 24.9k\Omega$$

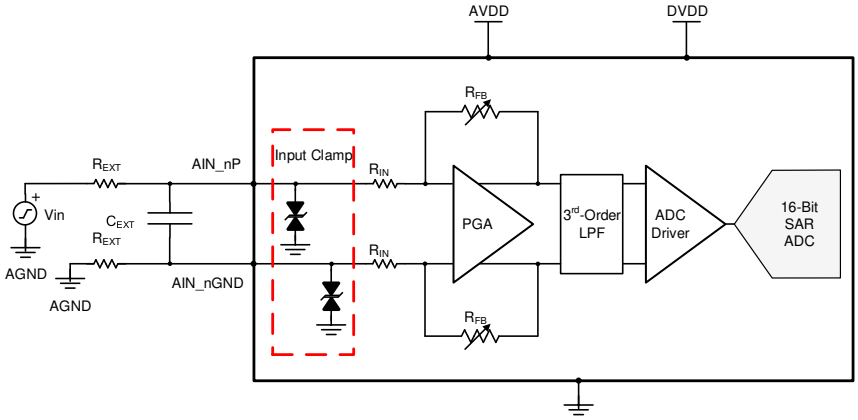
Test Setup

In a real world application with a multiple channel device, it is possible that one channel has an overvoltage signal applied to it and the other channels have valid signals on them. In this case it is desirable to have good performance on the channels with valid signals while protecting the channel with the overvoltage signal from damage. The measurements in this cookbook document are all done with an overvoltage signal applied to channel 1 and a valid signal applied to the other channels. All inputs are protected using the circuit designed in component selection. The following diagram shows the test setup.



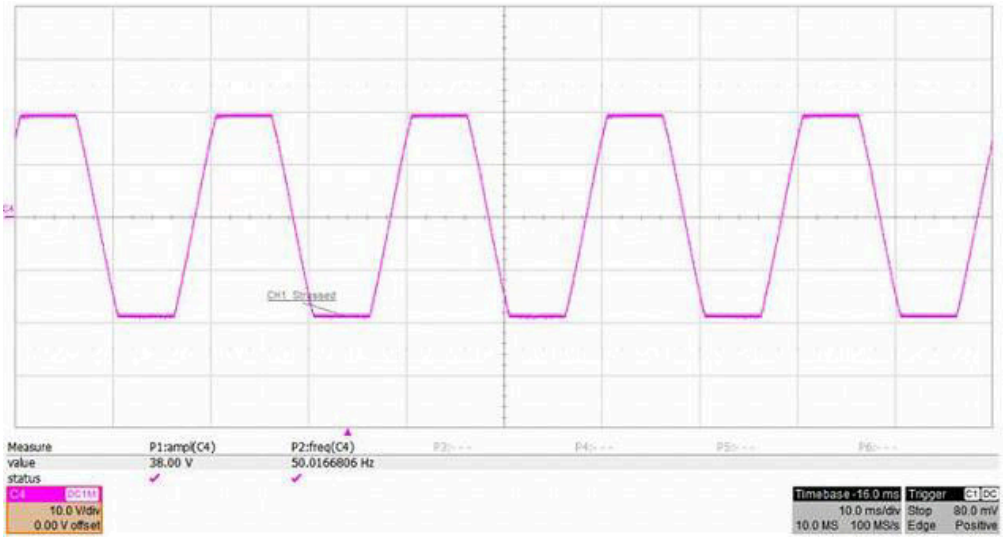
Device Protection

The following figure shows a simplified circuit for each analog input channel inside ADS8588S. An internal clamp protection circuit is designed on each of the 8 analog input channels and it allows each analog input to swing up to a maximum voltage of ±15V. For input voltages beyond ±15V the internal input clamp circuit turns on. Further increasing the overvoltage signal will result in higher current flow in the protection circuit (see the I-V Curve for input clamp protection circuit in the *ADS8588S 16-Bit, High-Speed, 8-Channel, Simultaneous-Sampling ADC with Bipolar Inputs on a Single Supply* data sheet). High input current can become destructive, degrading or even destroying the ADC device. This is why we limit the current to less than 1mA (see component selection section). Under a fault event the clamp protection circuit will turn on and limit the input voltage to approximately 15V and limit the current to less than 1mA.



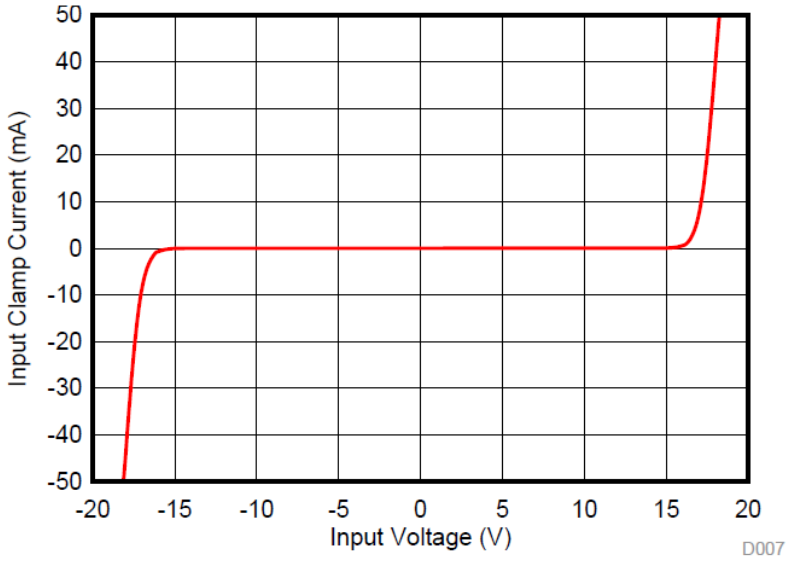
ADC Input (AIN_P) Under Overvoltage Condition

The following figure shows the ADC input voltage when the ±30Vpeak overvoltage signal is applied. Note that the clamp turns on and limits the ADC input to ±15Vpeak. The external resistor, R_{EXT}, limits the current to less than one milliamp to protect the ADC from damage.



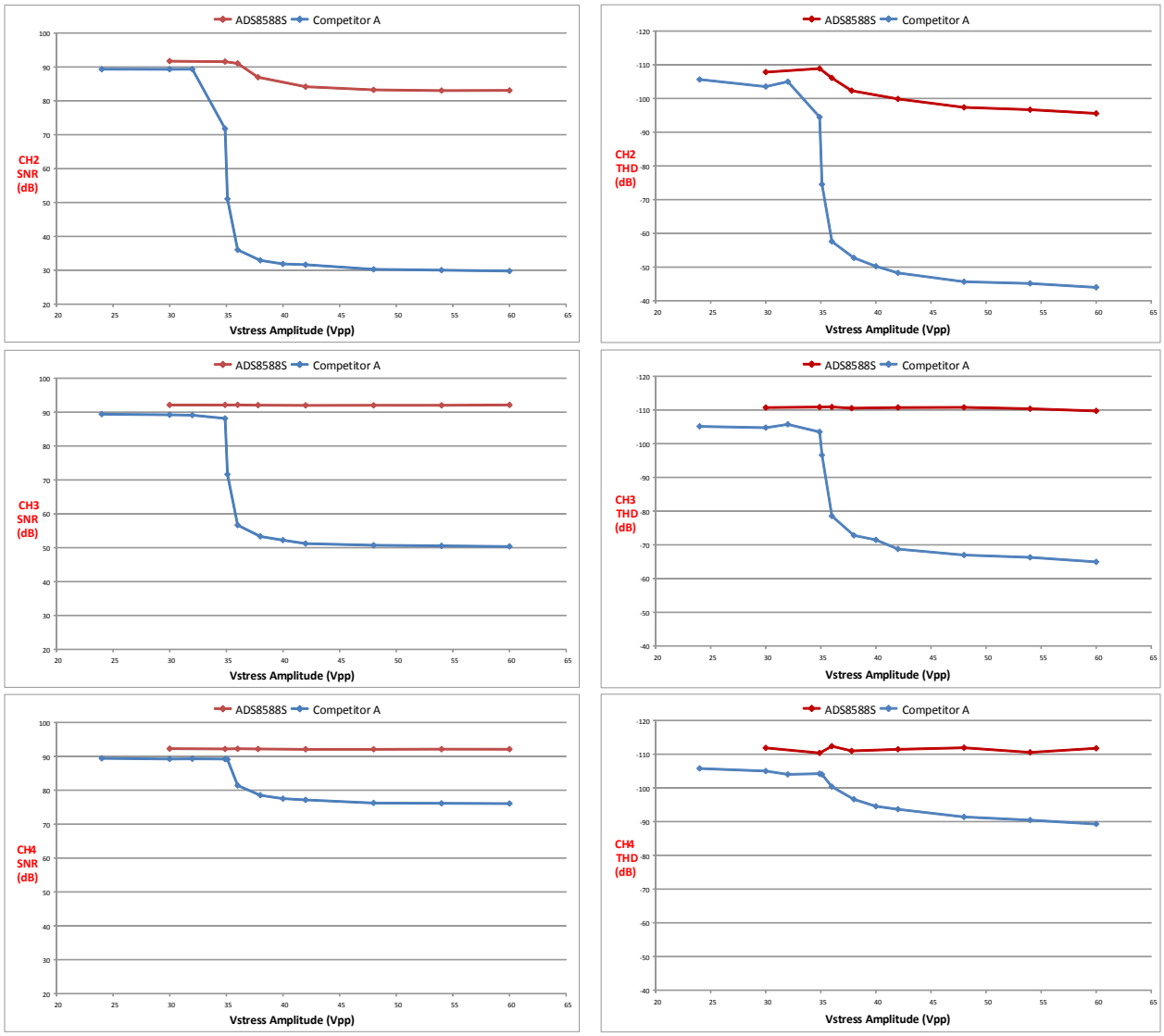
I-V Curve for the Internal Input Clamp Protection Circuit

The following figure shows the V-I curve for internal clamp. Note that it remains off and very low leakage for input voltage inside the ±15-V range. It turns on and limits the voltage outside of the ±15-V range.

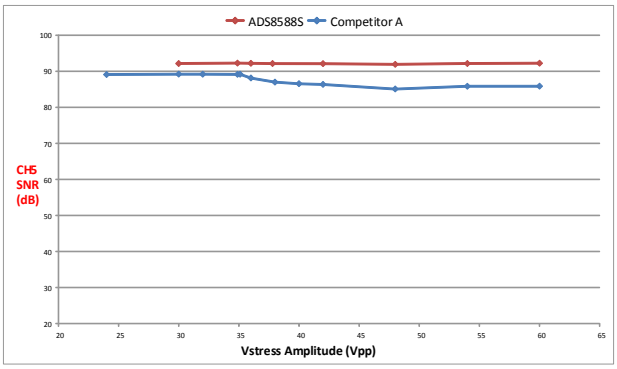


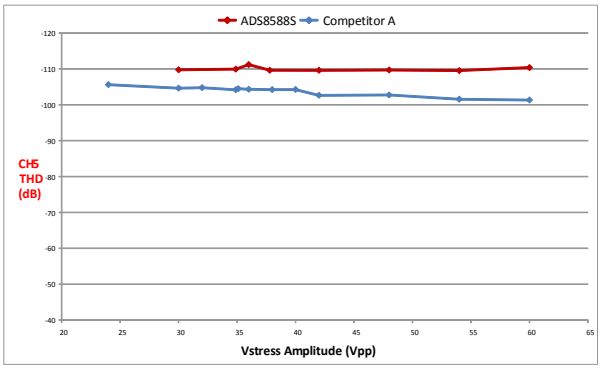
SNR and THD (Channel 1 = Overvoltage)

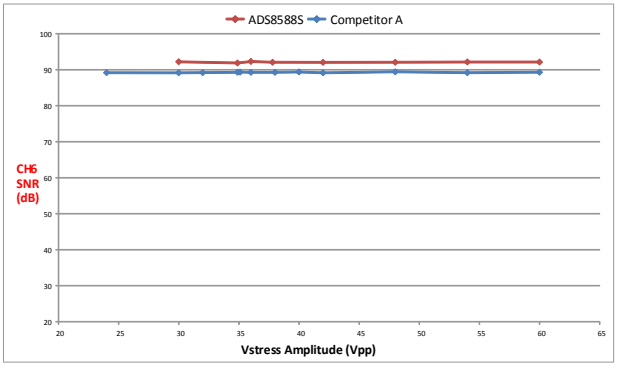
The following figures were taken with a ±30Vpeak (60Vpp) electrical overstress signal applied to channel 1 and the remainder of the channels are connected to a valid input signal (1kHz, –0.5dBFS sine wave). The SNR and THD of the channels with the valid input signal is measured with the overvoltage signal applied to channel 1. This test is done for the ADS8588S as well as a pin for pin comparable competitor device. Note that the ADS8588S SNR and THD are either not affected by the fault signal or the effect is minimal. Otherwise, the competitor device SNR and THD performance is substantially affected by the fault signal. Note that this circuit was also tested with ±15Vpeak, ±18Vpeak, ±21Vpeak, ±24Vpeak, and ±27Vpeak signals. As expected, larger overstress signals produce the worst-case results.

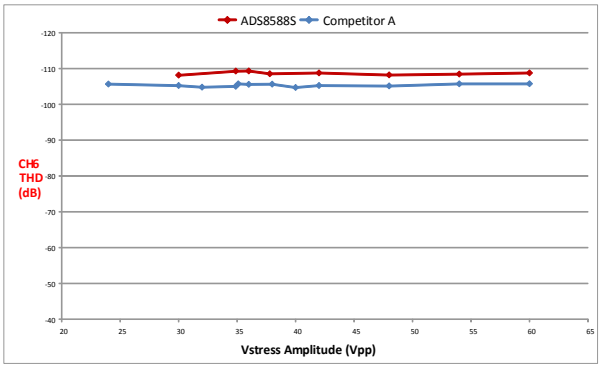


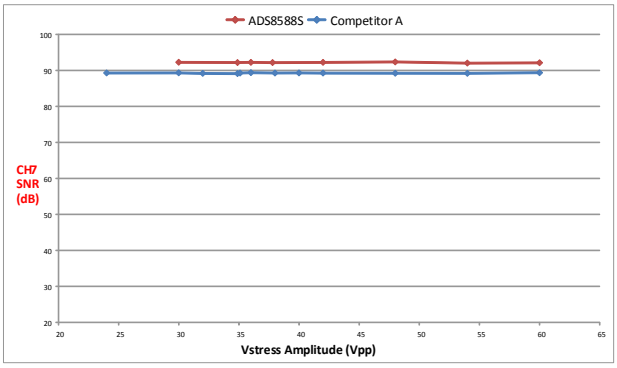
This is a continuation of the SNR and THD measurements where a ±30Vpeak (60Vpp) fault is applied to channel 1, and a valid input signal is applied to other channels performance verification.

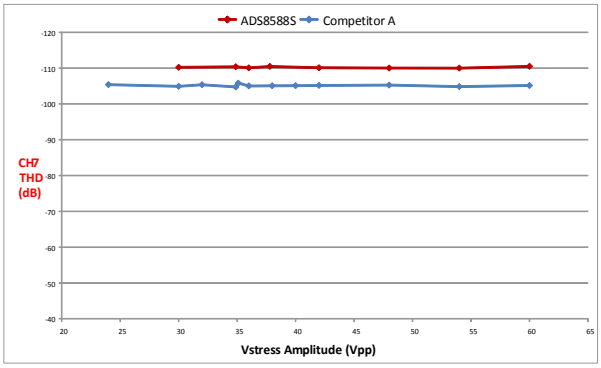


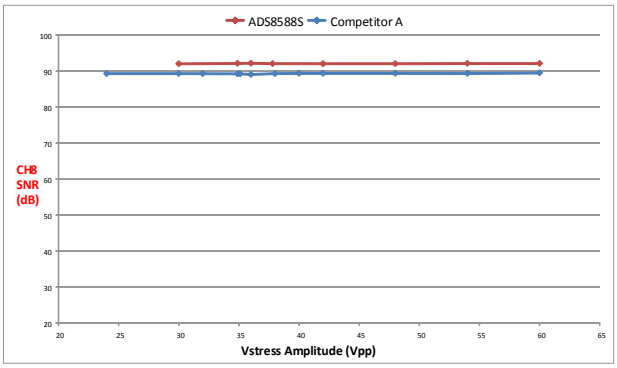


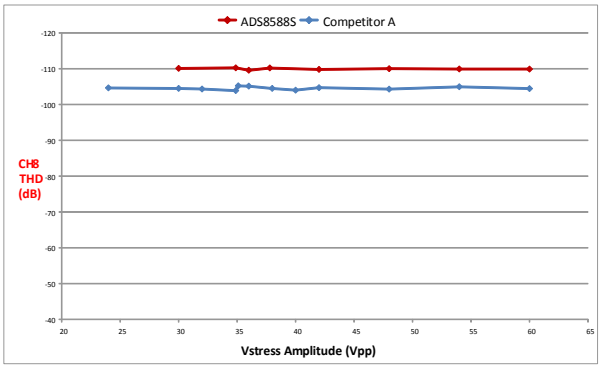






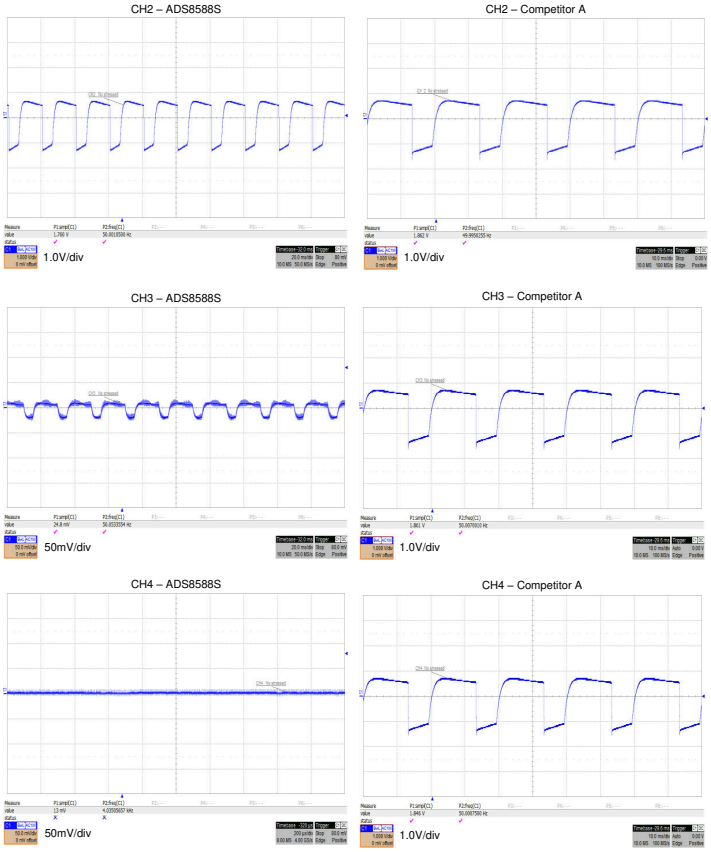




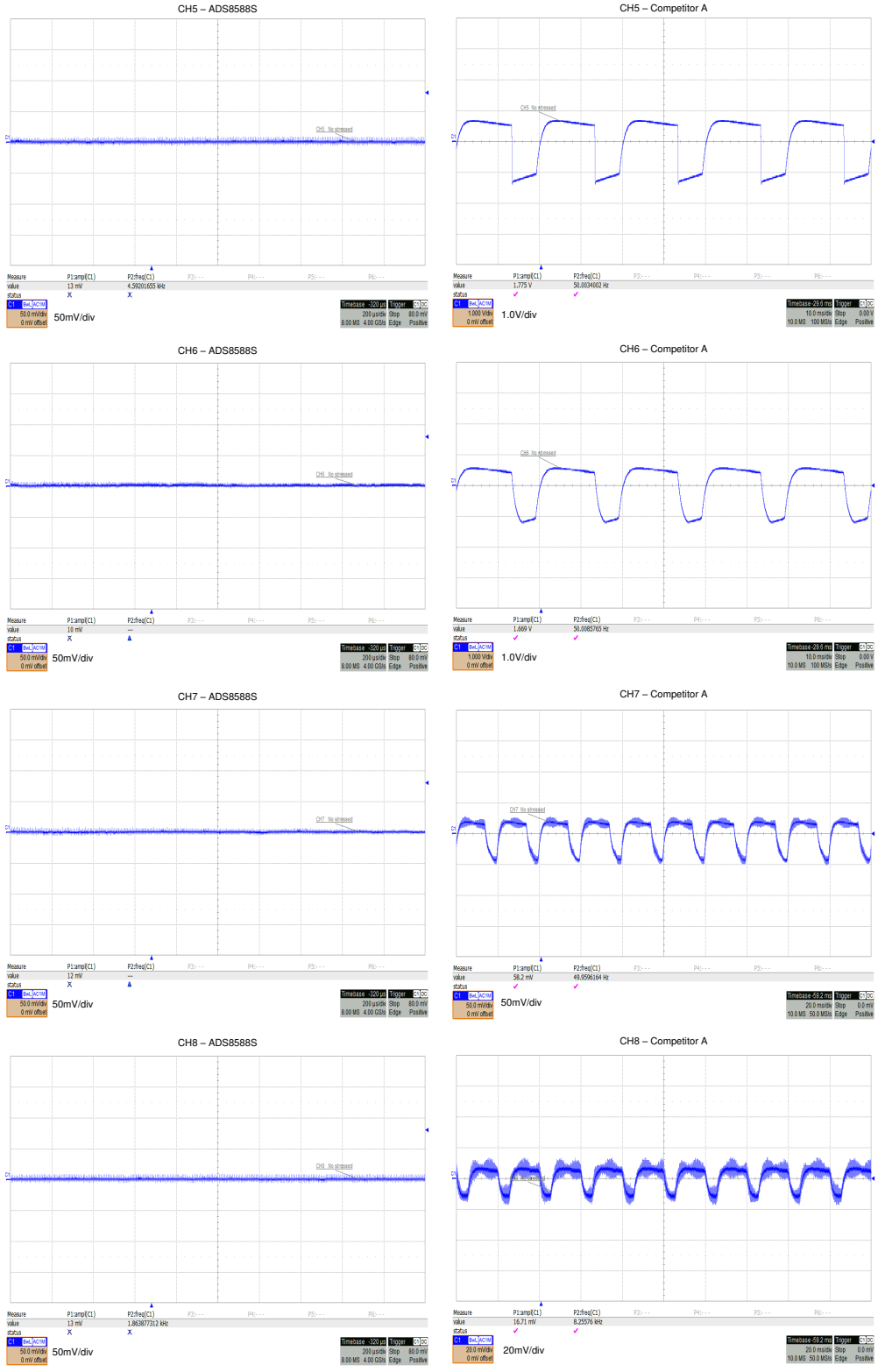


Feedthrough of Fault Signal to the Rest of the Channels

The following figures were taken with a ±30Vpeak (60Vpp) electrical overstress signal applied to channel 1 and the remainder of the channels are floating. The feedthrough of the overvoltage signal to the floating channels is measured using an oscilloscope. Note that both the ADS8588S and the competitor device are similar for channel 2. On the rest of the channels (CH3 to CH8) the feedthrough of the ADS8588S is much smaller than the TI device. This is a strong indication that for the ADS8588S the operation of channels with valid input signals will not be significantly impacted when one channel in the system has an overvoltage fault. Conversely, for the competitor device, all channels are adversely affected by the fault. Note that this circuit was also tested with ±15Vpeak, ±18Vpeak, ±21Vpeak, ±24Vpeak, and ±27Vpeak signals. As expected, larger overstress signals produce the worst case results.



This is a continuation of the feedthrough test showing that the ADS8588S channels with valid input signals are not affected by channels with faults.



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS8588S	16-bit, 8 Channel Simultaneous-Sampling, Bipolar-Input SAR ADC	16-Bit High-Speed 8-Channel Simultaneous-Sampling ADC With Bipolar Inputs on a Single Supply	Precision ADCs
REF5025	Low-noise, low drift, high precision voltage reference	2.5V, 3µVpp/V noise, 3-ppm/°C drift precision series voltage reference	Series voltage references

Design References

Texas Instruments, *Reducing Effects of External RC Filter Circuit on Gain and Drift Error for Integrated Analog Front Ends (AFEs): ±10V*, analog engineer's circuit

Texas Instruments, *Circuit to Increase Input Range on an Integrated Analog Front End (AFE) SAR ADC*, analog engineer's circuit

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