Analog Engineer's Circuit

Single-ended-to-differential circuit using an op amp and fully-differential amplifier (FDA) for bipolar signals

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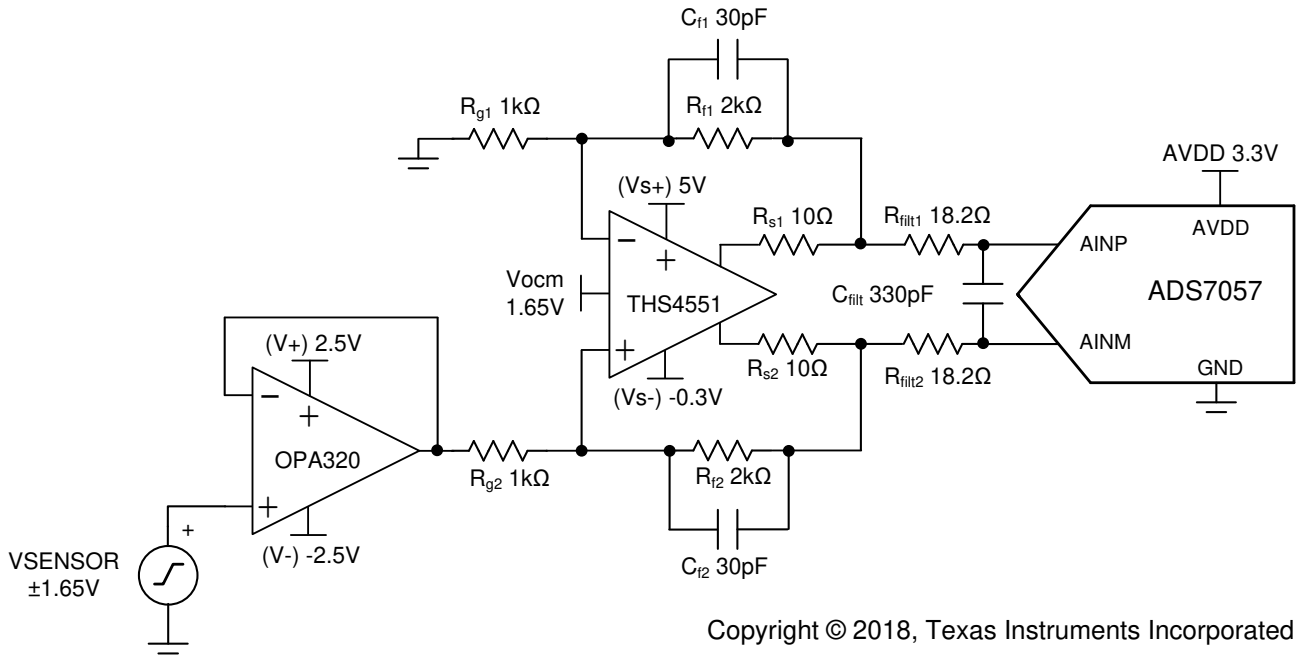
Input	ADC Input	Digital Output ADS7057
V_{in} Min = –3.3V	AINP = 0V AINM = 3.3V	2000_H 8192_{10}
V_{in} Max = 3.3V	AINP = 3.3V AINM = 0V	$1FFF_H$ 8191_{10}

Power Supplies		
AVDD	**GND**	**DVDD**
3.3V	0V	1.8V

Design Description

This design is intended to demonstrate how to convert a bipolar, single-ended signal into a unipolar, fully-differential signal and drive a differential ADC (for more information on these and other signal types, please refer to the *TI Precision Labs* training titled *SAR ADC Input Types*). Compared to a single-ended device, a fully-differential ADC has twice the dynamic range which improves the AC performance of the converter. Many common systems, for example *Sonar Receivers*, *Flow Meters*, and *Motor Controls*, benefit from the higher performance of a differential ADC. The equations and explanation of component selection in this design can be customized based on system specifications and needs. For more information on a similar design using a unipolar input signal, see the cookbook circuit titled *Single-Ended to Differential Signal Conversion for Unipolar Inputs*.



Specifications

Specification	Calculated	Simulated
Transient ADC Input Settling (at 250ksps)	< 0.5 · LSB = 201µV	134.7µV
Conditioned Signal Range (at 250ksps)	> 99% ADC FSR = > 6.53V	6.60V
Noise	43.8µV / √Hz	44.3µV / √Hz

Design Notes

1. The ADS7057 was selected because of the throughput (2.5Msps), size (2.25mm²) and low-latency (successive approximation register, or SAR, architecture).
2. Determine the linear range of the fully-differential amplifier (ADC driver) based on common mode, output swing, and linear open-loop gain specification. This is covered in the component selection section.
3. Determine the linear range of the op amp (signal conditioning) based on common mode, output swing, and linear open-loop gain specification. This is covered in the component selection section.
4. Select COG (NPO) capacitors for C_{filt}, to minimize distortion.
5. For best performance, consider using a 0.1% 20ppm/°C film resistor, or better, to minimize distortion.
6. The *TI Precision Labs - ADCs* training video series covers methods for selecting the charge bucket circuit R_{filtx} and C_{filt}. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown give good settling and AC performance for the amplifier and data converter in this example. If the design is modified, a different RC filter must be selected. Refer to *Introduction to SAR ADC Front-end Component Selection* (a *TI Precision Labs* training video) for an explanation of how to select the RC filter for best settling and AC performance.

Component Selection

1. Select a fully-differential amplifier capable of driving the ADC:
   THS4551 – Low noise, precision, 150MHz, fully-differential amplifier
   - Wide input common-mode voltage:

   $$V_{s-} - 0.1V < V_{cm} < V_{s+} - 1.3V$$

   - Linear output (requirement: 0V to 3.3V at each output):

   $$V_{s-} + 0.22V < V_{out} < V_{s+} - 0.22V$$

2. Select a wide bandwidth operational amplifier:
   OPA320 – Precision, zero-crossover, 20MHz, RRIO, operational amplifier
   - Gain bandwidth product > 12.5MHz (> 5 times the sampling rate)
   - Input common-mode voltage (requirement: ±1.65V):

   $$V_{-} - 0.1V < V_{cm} < V_{+} + 0.1V$$

   - Linear output:

   $$V_{-} + 0.03V < V_{out} < V_{+} - 0.03V$$

   $$V_{-} + 0.2V < V_{out} < V_{+} - 0.2V$$

   - Combined worst-case linear range (calculated from supplies used with OPA320):

   $$-2.3V < V_{out} < 2.3V$$

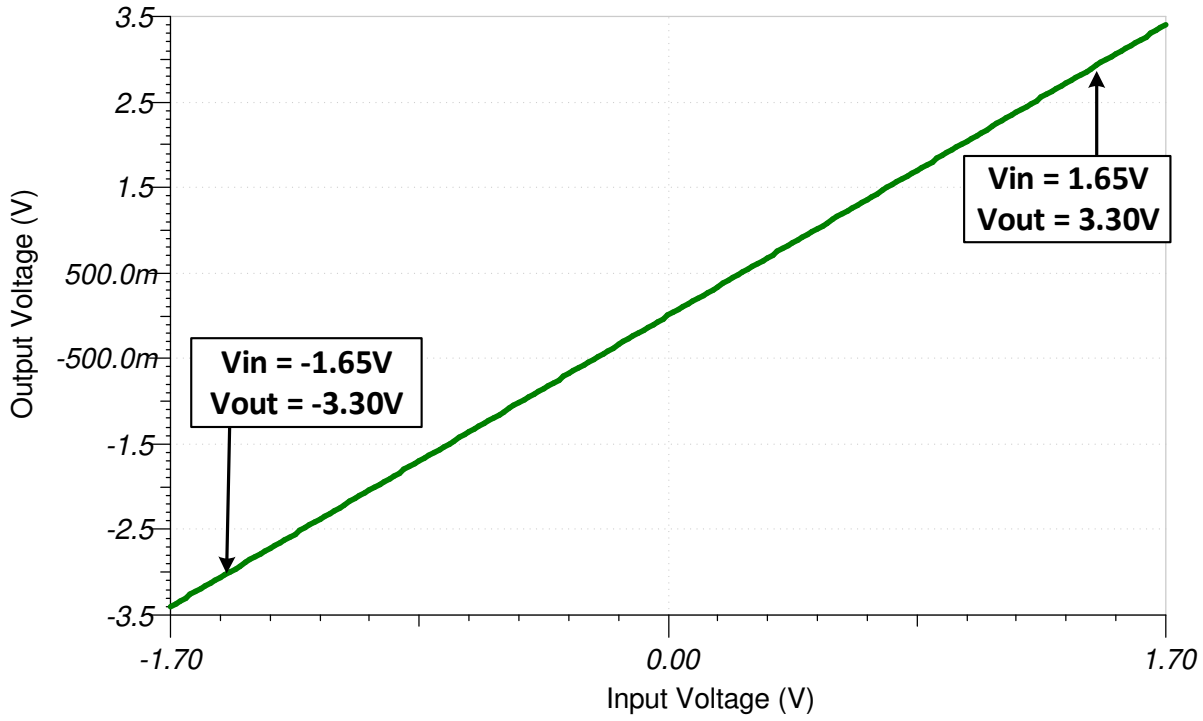
Note

The operational amplifier is used to protect the sensor from any charge kickbacks that occur when the ADC connects or disconnects the sampling capacitor. There is a possibility that this amplifier is not needed if the sensor has a high output impedance. A negative rail is used for both the OPA320 and THS4551 based on the assumption that the sensor is operating with a negative rail. This also provides the highest performance from the ADC by providing the full scale input range.

3. Select R_{fx} and R_{gx}
   - The combination of R_{fx} and R_{gx} sets the gain of the system. With an input range of ±1.65V and an ADC full scale of ±3.3V, a gain of 2 was selected for this system.
   - The values of R_{fx} = 2k and R_{gx} = 1k were selected to both provide the desired gain as well as limit the current through the feedback network, thus minimizing power consumption of the system.
4. Select R_{sx}
   - Connecting small resistors at the output of the amplifier is important and, in this case 10Ω, to flatten the output impedance and improve stability of the system.
5. Select R_{filtx} and C_{filt} values for settling of 250kHz input signal and sample rate of 2.5Msps:
   - *Refine the R_{filt} and C_{filt} Values* is a *TI Precision Labs* video showing the methodology for selecting R_{filtx} and C_{filt}. The final value of 18.2Ω and 330pF proved to settle to well below ½ of a least significant bit (LSB) within the acquisition window.

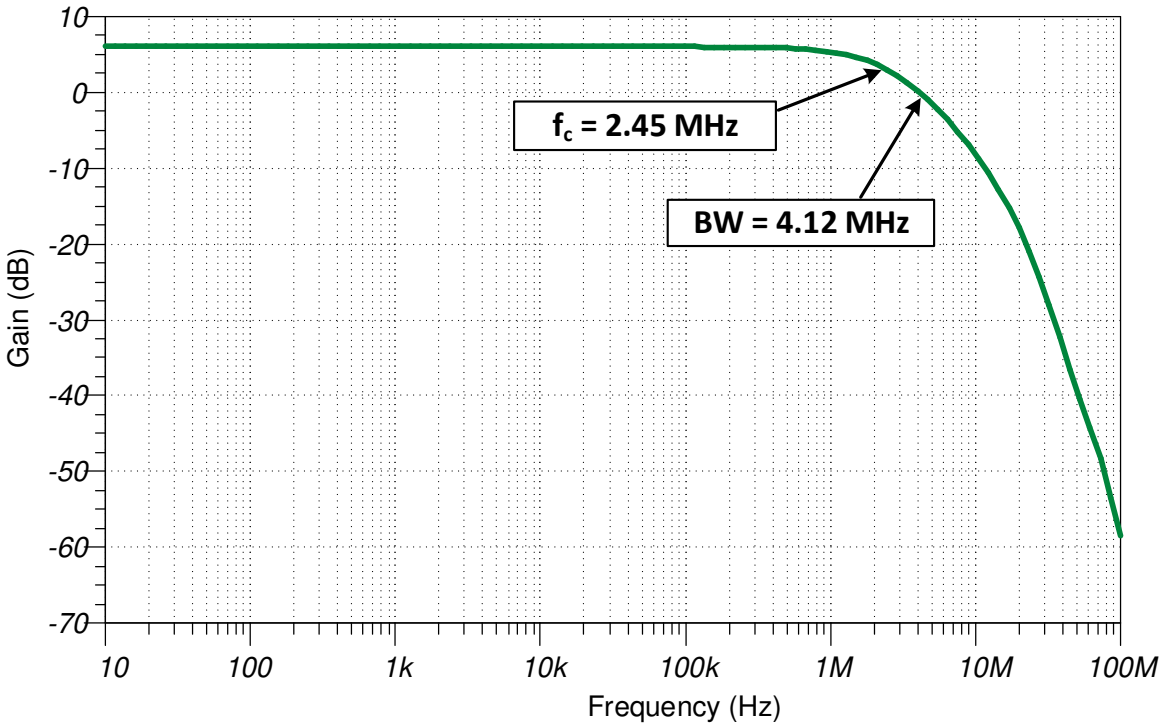
DC Transfer Characteristics

The following graph shows the simulated output for a ±1.65-V input. The analog front end has a linear output of ±3.3V which matches the full-scale range (FSR) of the ADC (with AVDD = 3.3V).



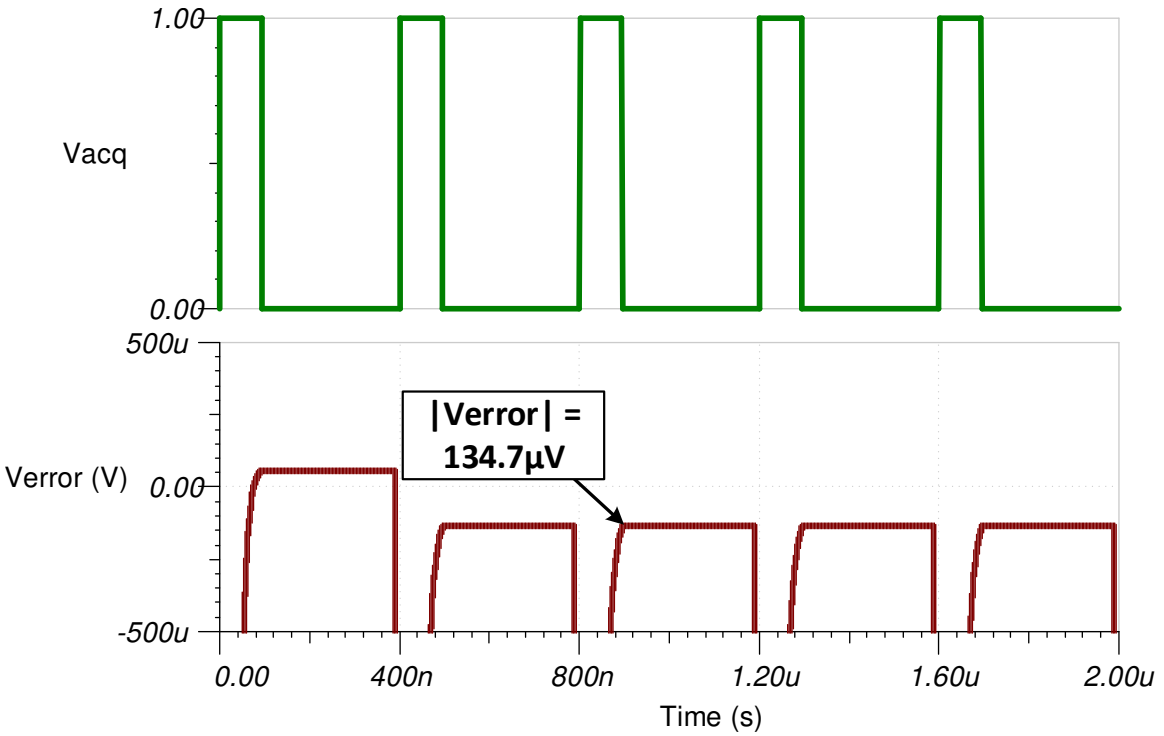
AC Transfer Characteristics

The bandwidth of the analog front end is simulated to be 4.12MHz at the gain of 0dB which is a linear gain of 1. This bandwidth allows the inputs of the ADC to adequately settle for a 250-ksps input signal.



Transient ADC Input Settling Simulation

The following simulation shows the ADC sample and hold capacitor settling for a 3.3V DC input signal. This simulation shows that the analog front end is able to drive the ADC with a large step input (from 0V to 3.3V) so the ADC settles to within ½ of an LSB (approximately 200µV) in the allotted acquisition time (95ns). Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject, and follow the link at the end of this design to download these simulation files.



Noise Simulation

This section details through a simplified noise calculation, providing a rough estimate to compare with the simulated result. The resistor noise is included in this calculation as the resistor noise is a significant portion of the overall noise of the system. Note that the resistor noise can be reduced by using smaller value resistors, but at the expense of increased power consumption through the feedback network.

$$f_c = \frac{1}{2\times\pi\times R_{filt}\times C_{filt}} = \frac{1}{2\times\pi\times 2\,k\Omega\times 30pF} = 2.65MHz$$

$$E_n = e_{OPA320}\times\sqrt{2\times K_n\times f_c} = \left(7nV/\sqrt{Hz}\right)\times\sqrt{2\times 1.57\times 2.65MHz} = 20.2\mu V/\sqrt{Hz}$$

$$E_{n\_OPA320} = E_n\times Gain = 20.2\mu V/\sqrt{Hz}\times 2 = 40.4\mu V/\sqrt{Hz}$$

$$E_{n\_THS4551} = e_{nTHS4551}\times\sqrt{2\times K_n\times f_c} = \left(3.3nV/\sqrt{Hz}\right)\times\sqrt{2\times 1.57\times 2.65MHz} = 9.52\mu V/\sqrt{Hz}$$

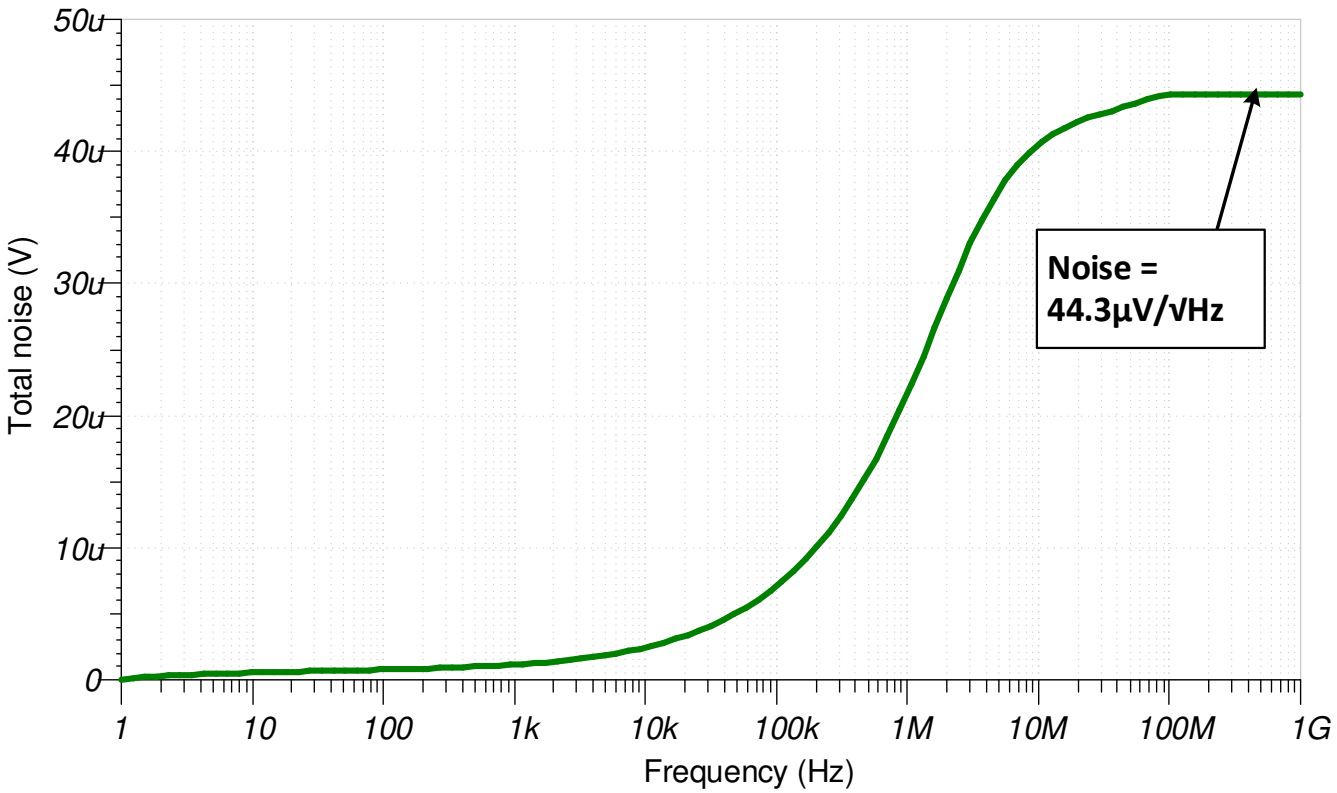
$$E_{Rg} = \frac{\sqrt{4\times k\times T\times R_g}}{1\times 10^{-9}}\times\frac{R_f}{R_g}\times\sqrt{2} = \frac{\sqrt{4\times 1.38\times 10^{-23}\times(273.15+25)\times 1000}}{1\times 10^{-9}}\times\frac{2000}{1000}\times\sqrt{2} = 11.47\mu V/\sqrt{Hz}$$

$$E_{Rf} = \frac{\sqrt{4\times k\times T\times R_f}}{1\times 10^{-9}}\times\sqrt{2} = \frac{\sqrt{4\times 1.38\times 10^{-23}\times(273.15+25)\times 2000}}{1\times 10^{-9}}\times\sqrt{2} = 8.11\mu V/\sqrt{Hz}$$

Total noise at output equation:

$$E_n = \sqrt{E_{nOPA320}{}^2 + E_{n\_THS4551}{}^2 + E_{Rg}{}^2 + E_{Rf}{}^2} = \sqrt{40.4^2 + 9.52^2 + 11.47^2 + 8.11^2} = 43.8\mu V/\sqrt{Hz}$$

Note that calculated and simulated match well. Refer to the *TI Precision Labs - ADCs* training video series for detailed theory on this subject.



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS7057	*14 bit, 2.5 Msps, fully-differential input, SPI, 2.25mm^2 package*	www.ti.com/product/ADS7057	www.ti.com/adcs
THS4551	*150MHz, 3.3nV/√Hz input voltage noise, fully-differential amplifier*	www.ti.com/product/THS4551	www.ti.com/opamp
OPA320	*Precision, zero-crossover, 20MHz, 0.9pA Ib, RRIO, operational amplifier*	www.ti.com/product/OPA320	www.ti.com/opamp

Note

The ADS7057 uses the AVDD as the reference input. Use a high-PSRR LDO, such as the TPS7A47, as the power supply.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to key files (TINA):

Design files for this circuit – http://www.ti.com/lit/zip/sbac181.

Link to Related Cookbooks

Single-Ended to Differential Signal Conversion for Unipolar Input

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2019) to Revision B (September 2024)	Page
• Updated the format for tables, figures, and cross-references throughout the document	1

Changes from Revision * (January 2018) to Revision A (March 2019)	Page
• Downstyle the title and changed title role to 'Data Converters'. Added link to circuit cookbook landing page	1

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