

# UCC28700-Q1 Constant-Voltage, Constant-Current Controller With Primary-Side Regulation

## 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
  - Device HBM Classification Level 2:  $\pm 2\text{ kV}$
  - Device CDM Classification Level C4B: 750 V
- **Functional Safety-Capable**
  - **Documentation** available to aid functional safety system design
- $< 30\text{-mW}$  Standby Power Consumption
- Primary-Side Regulation (PSR) Eliminates Opto-Coupler
- $\pm 5\%$  Voltage and Current Regulation
- 130-kHz Maximum Switching Frequency
- Quasi-Resonant Valley-Switching Operation for Highest Overall Efficiency
- Patent-Pending Frequency-Jitter Scheme to Ease EMI Compliance
- Wide VDD Range Allows Small Bias Capacitor
- Clamped Gate-Drive Output for MOSFET
- Protection Functions: Overvoltage, Low-Line, and Overcurrent
- Programmable Cable Compensation
- SOT23-6 Package

## 2 Applications

- Automotive AC-to-DC Power Conversion and DC-to-DC Power Conversion
- Auxiliary Power Supply for Automotive Power Train in HEV
- Flyback and Buck Power Converters

## 3 Description

The UCC28700-Q1 of flyback power supply controllers provides Constant-Voltage (CV) and Constant-Current (CC) output regulation without the use of an optical coupler. The devices process information from the primary power switch and an auxiliary flyback winding for precise control of output voltage and current. Low start-up current, dynamically controlled operating states and a tailored modulation profile support very low standby power without sacrificing start-up time or output transient response.

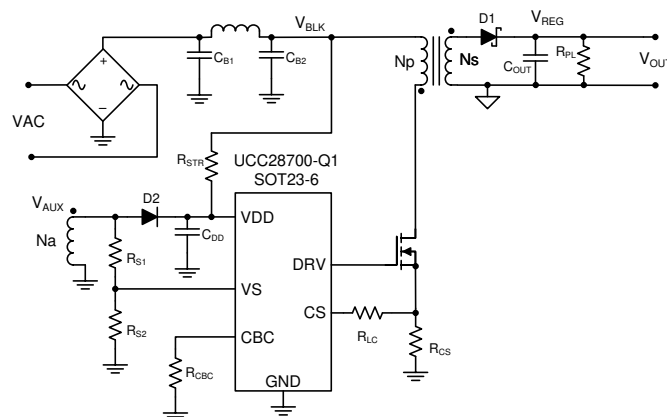
Control algorithms in the UCC28700-Q1 allows operating efficiencies to meet or exceed applicable standards. The output drive interfaces to a MOSFET power switch. Discontinuous Conduction Mode (DCM) with valley switching reduces switching losses. Modulation of switching frequency and primary current peak amplitude (FM and AM) keeps the conversion efficiency high across the entire load and line ranges.

The controllers have a maximum switching frequency of 130 kHz and always maintain control of the peak-primary current in the transformer. Protection features help keep primary and secondary component stresses in check. The UCC28700-Q1 allows the level of cable compensation to be programmed.

### Device Information (1)

| PART NUMBER | PACKAGE    | BODY SIZE (NOM)          |
|-------------|------------|--------------------------|
| UCC28700-Q1 | SOT-23 (6) | 2.90 mm $\times$ 1.60 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.



**Typical Application Schematic**



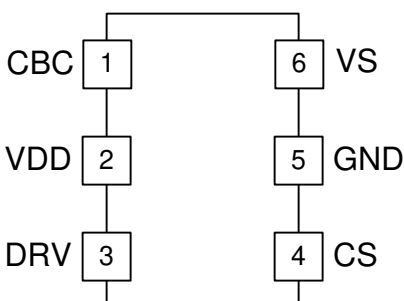
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## 4 Revision History

| Changes from Revision (January 2015) to Revision A (December 2020 ) | Page     |
|---------------------------------------------------------------------|----------|
| • Added Functional-Safety Information.....                          | <b>1</b> |

## 5 Pin Configuration and Functions



**Figure 5-1. UCC28700-Q1 SOT23-6 (DBV) Top View**

### 5.1 Pin Functions

| NAME | PIN         |     | I/O | DESCRIPTION                                                                                                                                                                                                                                                                                                                 |
|------|-------------|-----|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      | UCC28700-Q1 | NO. |     |                                                                                                                                                                                                                                                                                                                             |
| CBC  | 1           | I   |     | Cable Compensation (CBC) is a programming pin for compensation of cable voltage drop. Cable compensation is programmed with a resistor to GND.                                                                                                                                                                              |
| CS   | 4           | I   |     | Current Sense (CS) input connects to a ground-referenced current-sense resistor in series with the power switch. The resulting voltage is used to monitor and control the peak primary current. A series resistor can be added to this pin to compensate the peak switch current levels as the AC-mains input varies.       |
| DRV  | 3           | O   |     | Drive (DRV) is an output used to drive the gate of an external high voltage MOSFET switching transistor.                                                                                                                                                                                                                    |
| GND  | 5           | —   |     | The Ground (GND) pin is both the reference pin for the controller and the low-side return for the drive output. Special care should be taken to return all AC decoupling capacitors as close as possible to this pin and avoid any common trace length with analog signal return paths.                                     |
| VDD  | 2           | —   |     | VDD is the bias supply input pin to the controller. A carefully-placed bypass capacitor to GND is required on this pin.                                                                                                                                                                                                     |
| VS   | 6           | I   |     | Voltage Sense (VS) is an input used to provide voltage and timing feedback to the controller. This pin is connected to a voltage divider between an auxiliary winding and GND. The value of the upper resistor of this divider is used to program the AC-mains run and stop thresholds and line compensation at the CS pin. |

## 6 Specifications

### 6.1 Absolute Maximum Ratings <sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                                                  |           | MIN   | MAX           | UNIT |
|--------------------------------------------------|-----------|-------|---------------|------|
| Bias supply voltage                              | $V_{VDD}$ |       | 38            | V    |
| Continuous gate current sink                     | $I_{DRV}$ |       | 50            | mA   |
| Continuous gate current source                   | $I_{DRV}$ |       | Self-limiting |      |
| Peak VS pin current                              | $I_{VS}$  |       | -1.2          |      |
| Gate-drive voltage at DRV                        | $V_{DRV}$ | -0.5  | Self-limiting | V    |
| Voltage range                                    | VS        | -0.75 | 7             |      |
|                                                  | CS, CBC   | -0.5  | 5             |      |
| Operating junction temperature range             | $T_J$     | -55   | 150           | °C   |
| Lead temperature 0.6 mm from case for 10 seconds |           |       | 260           |      |
| Storage temperature, $T_{stg}$                   |           | -65   | 150           | °C   |

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under [Section 6.3](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. These ratings apply over the operating ambient temperature ranges unless otherwise noted.

### 6.2 ESD Ratings

|                                     |                                                         | VALUE | UNIT |
|-------------------------------------|---------------------------------------------------------|-------|------|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> | ±2000 | V    |
|                                     | Charged-device model (CDM), per AEC Q100-011            | ±750  |      |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|           |                                | MIN   | MAX | UNIT |
|-----------|--------------------------------|-------|-----|------|
| VDD       | Bias supply operating voltage  | 9     | 35  | V    |
| $C_{VDD}$ | VDD bypass capacitor           | 0.047 | 1   | μF   |
| $R_{CBC}$ | Cable-compensation resistance  | 10    |     | kΩ   |
| $I_{VS}$  | VS pin current                 | -1    |     | mA   |
| $T_J$     | Operating junction temperature | -40   | 125 | °C   |

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                                             | UCC28700-Q1 | UNIT |
|-------------------------------|-------------------------------------------------------------|-------------|------|
|                               |                                                             | DBV         |      |
|                               |                                                             | 6 PINS      |      |
| $\theta_{JA}$                 | Junction-to-ambient thermal resistance <sup>(2)</sup>       | 180         | °C/W |
| $\theta_{JCTop}$              | Junction-to-case (top) thermal resistance <sup>(3)</sup>    | 71.2        |      |
| $\theta_{JB}$                 | Junction-to-board thermal resistance <sup>(4)</sup>         | 44.4        |      |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter <sup>(5)</sup>   | 5.1         |      |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter <sup>(6)</sup> | 43.8        |      |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report ([SPRA953](#)).

- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter,  $\psi_{JT}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $R_{\theta JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter,  $\psi_{JB}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $R_{\theta JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).

## 6.5 Electrical Characteristics

over operating free-air temperature range,  $V_{DD} = 25\text{ V}$ ,  $R_{CBC} = \text{open}$ ,  $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ ,  $T_J = T_A$   
(unless otherwise noted)

| PARAMETER              |                                   | TEST CONDITIONS                                                        | MIN   | TYP  | MAX  | UNITS |
|------------------------|-----------------------------------|------------------------------------------------------------------------|-------|------|------|-------|
| BIAS SUPPLY INPUT      |                                   |                                                                        |       |      |      |       |
| I <sub>RUN</sub>       | Supply current, run               | I <sub>DRV</sub> = 0, run state                                        |       | 2.10 | 2.65 | mA    |
| I <sub>WAIT</sub>      | Supply current, wait              | I <sub>DRV</sub> = 0, wait state                                       |       | 85   | 110  |       |
| I <sub>START</sub>     | Supply current, start             | I <sub>DRV</sub> = 0, V <sub>VDD</sub> = 18 V, start state             |       | 1.0  | 1.5  |       |
| I <sub>FAULT</sub>     | Supply current, fault             | I <sub>DRV</sub> = 0, fault state                                      |       | 2.1  | 2.8  | mA    |
| UNDER-VOLTAGE LOCKOUT  |                                   |                                                                        |       |      |      |       |
| V <sub>VDD(on)</sub>   | VDD turn-on threshold             | V <sub>VDD</sub> low to high                                           | 17.5  | 21.0 | 23.0 | V     |
| V <sub>VDD(off)</sub>  | VDD turn-off threshold            | V <sub>VDD</sub> high to low                                           | 7.70  | 8.10 | 8.45 |       |
| VS INPUT               |                                   |                                                                        |       |      |      |       |
| V <sub>VSR</sub>       | Regulating level                  | Measured at no-load condition, T <sub>J</sub> = 25°C                   | 4.01  | 4.05 | 4.09 | V     |
| V <sub>VSNC</sub>      | Negative clamp level              | I <sub>VS</sub> = -300 μA, volts below ground                          | 190   | 250  | 325  | mV    |
| I <sub>VSB</sub>       | Input bias current                | V <sub>VS</sub> = 4 V                                                  | −0.25 | 0    | 0.25 | μA    |
| CS INPUT               |                                   |                                                                        |       |      |      |       |
| V <sub>CST(max)</sub>  | Max CS threshold voltage          | V <sub>VS</sub> = 3.7 V <sup>(1)</sup>                                 | 715   | 750  | 775  | mV    |
| V <sub>CST(min)</sub>  | Min CS threshold voltage          | V <sub>VS</sub> = 4.35 V <sup>(1)</sup>                                | 230   | 250  | 270  |       |
| K <sub>AM</sub>        | AM control ratio                  | V <sub>CST(max)</sub> / V <sub>CST(min)</sub>                          | 2.75  | 3.00 | 3.15 | V/V   |
| V <sub>CCR</sub>       | constant-current regulating level | CC regulation constant                                                 | 310   | 319  | 329  | mV    |
| K <sub>LC</sub>        | Line compensating current ratio   | I <sub>VSLs</sub> = -300 μA, I <sub>VSLs</sub> / current out of CS pin | 23    | 25   | 28   | A/A   |
| T <sub>CSLEB</sub>     | Leading-edge blanking time        | DRV output duration, V <sub>CS</sub> = 1 V                             | 195   | 235  | 275  | ns    |
| DRV                    |                                   |                                                                        |       |      |      |       |
| I <sub>DRS</sub>       | DRV source current                | V <sub>DRV</sub> = 8 V, V <sub>VDD</sub> = 9 V                         | 20    | 25   |      | mA    |
| R <sub>DRVLS</sub>     | DRV low-side drive resistance     | I <sub>DRV</sub> = 10 mA                                               |       | 6    | 12   |       |
| V <sub>DRCL</sub>      | DRV clamp voltage                 | V <sub>VDD</sub> = 35 V                                                |       | 14   | 16   | V     |
| R <sub>DRVSS</sub>     | DRV pull-down in start state      |                                                                        | 150   | 200  | 230  | kΩ    |
| PROTECTION             |                                   |                                                                        |       |      |      |       |
| V <sub>OVP</sub>       | Over-voltage threshold            | At VS input, T <sub>J</sub> = 25°C                                     | 4.52  | 4.60 | 4.68 | V     |
| V <sub>OCP</sub>       | Over-current threshold            | At CS input                                                            | 1.4   | 1.5  | 1.6  |       |
| I <sub>VSL(run)</sub>  | VS line-sense run current         | Current out of VS pin – increasing                                     | 190   | 220  | 260  | μA    |
| I <sub>VSL(stop)</sub> | VS line-sense stop current        | Current out of VS pin – decreasing                                     | 70    | 80   | 95   |       |
| K <sub>VSL</sub>       | VS line-sense ratio               | I <sub>VSL(run)</sub> / I <sub>VSL(stop)</sub>                         | 2.50  | 2.80 | 3.05 | A/A   |
| T <sub>J(stop)</sub>   | Thermal shut-down temperature     | Internal junction temperature                                          |       | 165  |      | °C    |
| CABLE COMPENSATION     |                                   |                                                                        |       |      |      |       |

**UCC28700-Q1**

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over operating free-air temperature range,  $V_{DD} = 25\text{ V}$ ,  $R_{CBC} = \text{open}$ ,  $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ ,  $T_J = T_A$   
 (unless otherwise noted)

| PARAMETER                                                | TEST CONDITIONS                                                      | MIN | TYP | MAX | UNITS |
|----------------------------------------------------------|----------------------------------------------------------------------|-----|-----|-----|-------|
| $V_{CBC(\text{max})}$ Cable compensation maximum voltage | Voltage at CBC at full load                                          | 2.8 | 3.0 | 3.4 | V     |
| $V_{CVS(\text{min})}$ Compensation at VS                 | $V_{CBC} = \text{open}$ , change in VS regulating level at full load | -45 | -15 | 25  | mV    |
| $V_{CVS(\text{max})}$ Maximum compensation at VS         | $V_{CBC} = 0\text{ V}$ , change in VS regulating level at full load  | 275 | 320 | 365 |       |

- (1) These devices automatically vary the control frequency and current sense thresholds to improve EMI performance, these threshold voltages and frequency limits represent average levels.

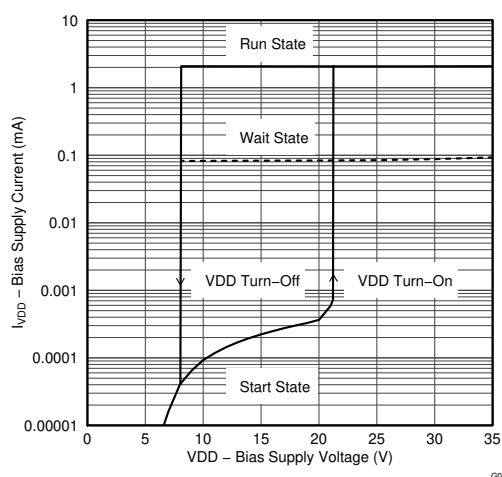
## 6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

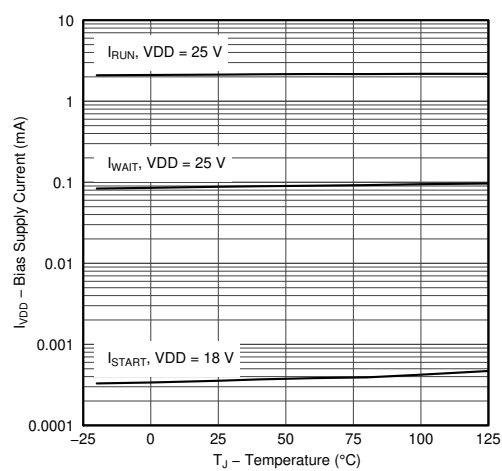
| PARAMETER                                        | TEST CONDITIONS                | MIN  | TYP  | MAX  | UNIT          |
|--------------------------------------------------|--------------------------------|------|------|------|---------------|
| $f_{SW(\text{max})}$ Maximum switching frequency | $V_{VS} = 3.7\text{ V}^{(1)}$  | 120  | 130  | 140  | kHz           |
| $f_{SW(\text{min})}$ Minimum switching frequency | $V_{VS} = 4.35\text{ V}^{(1)}$ | 875  | 1000 | 1100 | Hz            |
| $T_{ZTO}$ Zero-crossing timeout delay            |                                | 1.80 | 2.10 | 2.55 | $\mu\text{s}$ |

## 6.7 Typical Characteristics

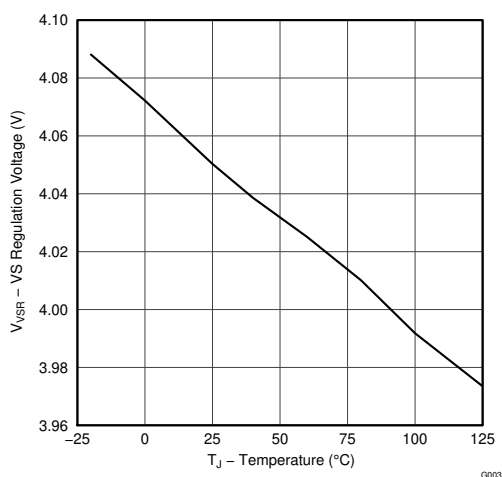
At VDD = 25 V, unless otherwise noted.



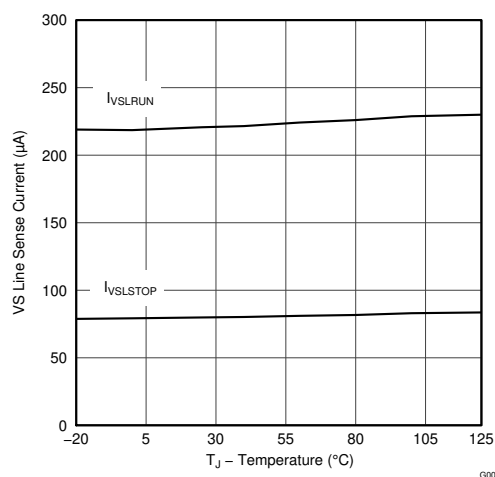
**Figure 6-1. Bias Supply Current vs. Bias Supply Voltage**



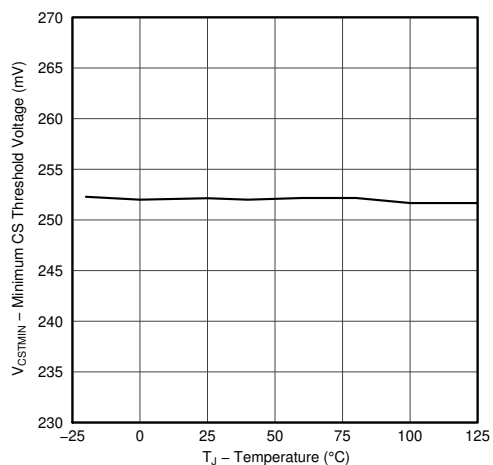
**Figure 6-2. Bias Supply Current vs. Temperature**



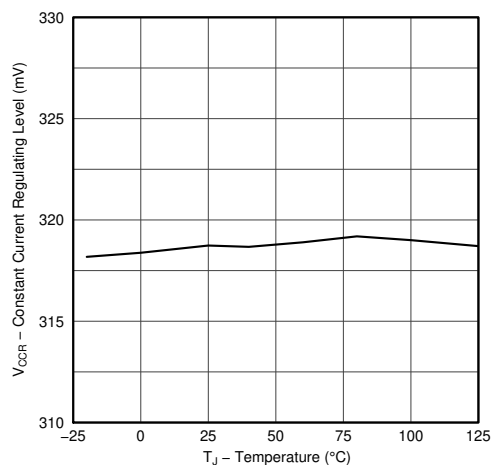
**Figure 6-3. VS Regulation Voltage vs. Temperature**



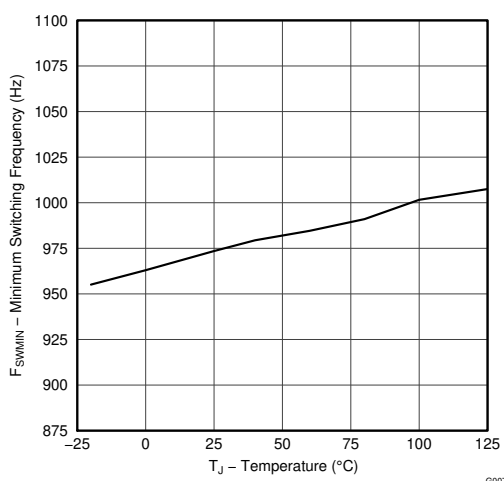
**Figure 6-4. Line-Sense Current vs. Temperature**



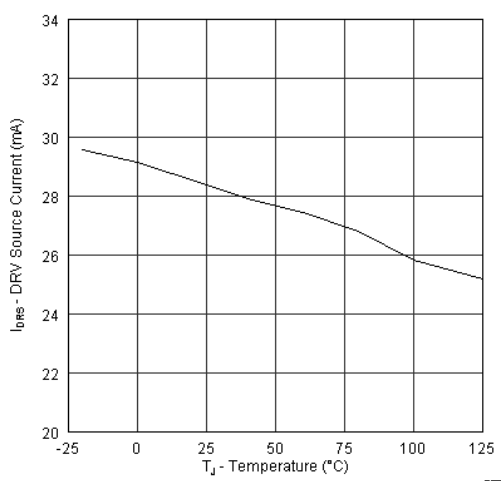
**Figure 6-5. Minimum CS Threshold Voltage vs. Temperature**



**Figure 6-6. Constant-Current Regulating Level vs. Temperature**

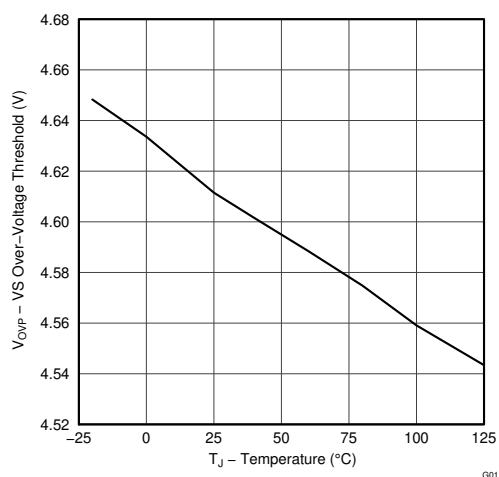


**Figure 6-7. Minimum Switching Frequency vs. Temperature**



V<sub>DRV</sub> = 8 V, V<sub>VDD</sub> = 9 V

**Figure 6-8. DRV Source Current vs. Temperature**



**Figure 6-9. Overvoltage Threshold vs. Temperature**

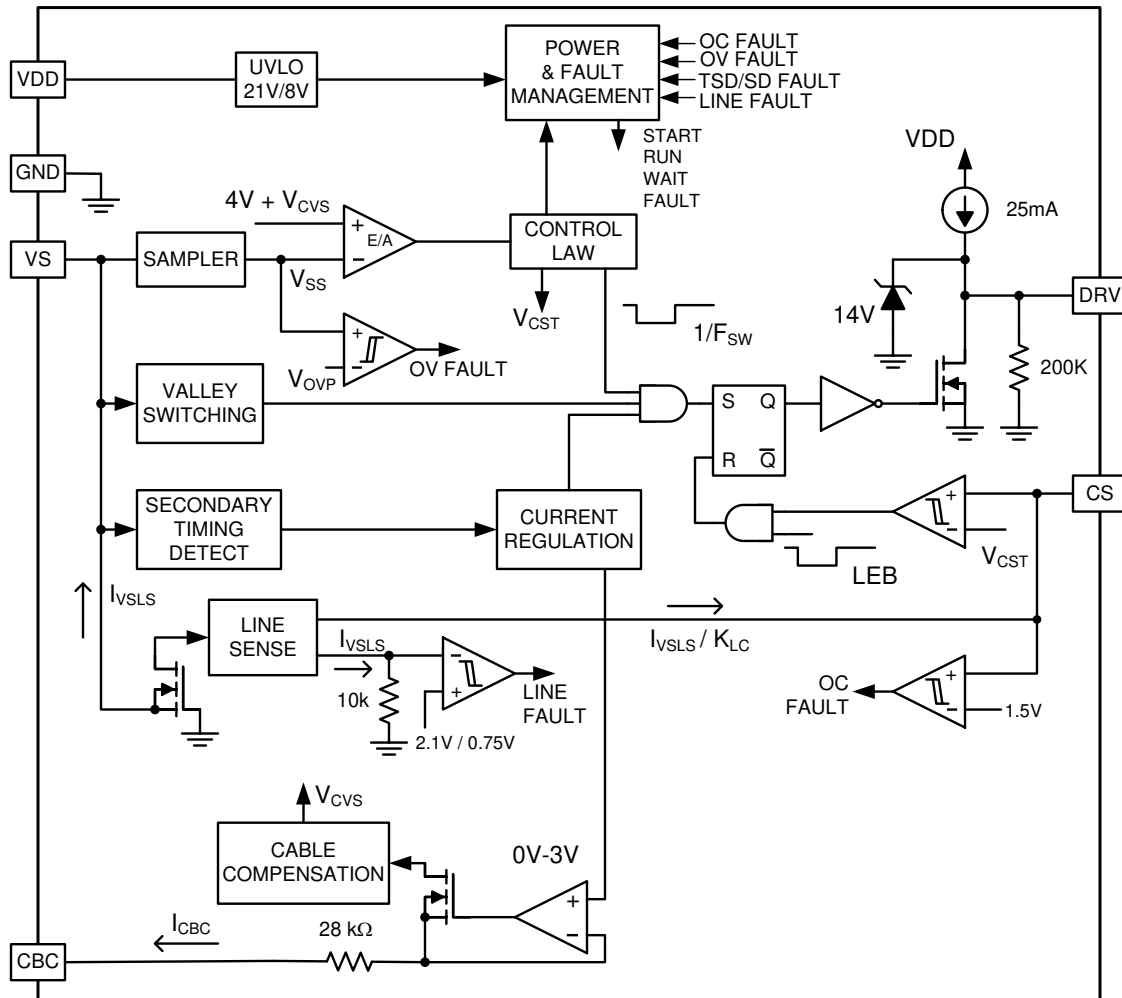
## 7 Detailed Description

### 7.1 Overview

The UCC28700-Q1 is a flyback power supply controller which provides accurate voltage and constant current regulation with primary-side feedback, eliminating the need for opto-coupler feedback circuits. The controller operates in discontinuous conduction mode with valley-switching to minimize switching losses. The modulation scheme is a combination of frequency and primary peak current modulation to provide high conversion efficiency across the load range. The control law provides a wide-dynamic operating range of output power to achieve the < 30-mW stand-by power requirement.

Another feature beneficial to achieve low stand-by power without excessive start-up time is a wide operating VDD range to allow a high-value VDD start-up resistance and low-value VDD capacitance. During low-power operating ranges the device has power management features to reduce the device operating current at operating frequencies below 44 kHz. The UCC28700-Q1 controller includes features in the modulator to reduce the EMI peak energy of the fundamental switching frequency and harmonics. Accurate voltage and constant current regulation, fast dynamic response, and fault protection are achieved with primary-side control. A complete charger solution can be realized with a straightforward design process, low cost and low component count.

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Detailed Pin Description

#### 7.3.1.1 VDD (Device Bias Voltage Supply)

The VDD pin is connected to a bypass capacitor to ground and a start-up resistance to the input bulk capacitor (+) terminal. The VDD turn-on UVLO threshold is 21 V and turn-off UVLO threshold is 8.1 V, with an available operating range up to 35 V. The USB charging specification requires the output current to operate in constant-current mode from 5 V to a minimum of 2 V; this is easily achieved with a nominal VDD of approximately 25 V. The additional VDD headroom up to 35 V allows for VDD to rise due to the leakage energy delivered to the VDD capacitor in high-load conditions. Also, the wide VDD range provides the advantage of selecting a relatively small VDD capacitor and high-value start-up resistance to minimize no-load stand-by power loss in the start-up resistor.

#### 7.3.1.2 GND (Ground)

This is a single ground reference external to the device for the gate drive current and analog signal reference. Place the VDD bypass capacitor close to GND and VDD with short traces to minimize noise on the VS and CS signal pins.

#### 7.3.1.3 VS (Voltage-Sense)

The VS pin is connected to a resistor divider from the auxiliary winding to ground. The output-voltage feedback information is sampled at the end of the transformer secondary current demagnetization time to provide an accurate representation of the output voltage. Timing information to achieve valley-switching and to control the duty cycle of the secondary transformer current is determined by the waveform on the VS pin. Avoid placing a filter capacitor on this input which would interfere with accurate sensing of this waveform.

The VS pin also senses the bulk capacitor voltage to provide for AC-input run and stop thresholds, and to compensate the current-sense threshold across the AC-input range. This information is sensed during the MOSFET on-time. For the AC-input run/stop function, the run threshold on VS is 220  $\mu$ A and the stop threshold is 80  $\mu$ A. The values for the auxiliary voltage divider upper-resistor  $R_{S1}$  and lower-resistor  $R_{S2}$  can be determined by the equations below.

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(run)}} \quad (1)$$

where

- $N_{PA}$  is the transformer primary-to-auxiliary turns ratio,
- $V_{IN(run)}$  is the AC RMS voltage to enable turn-on of the controller (run),
- $I_{VSL(run)}$  is the run-threshold for the current pulled out of the VS pin during the MOSFET on-time. (see the [Section 6.5](#) table)

$$R_{S2} = \frac{R_{S1} \times V_{VSR}}{N_{AS} \times (V_{OCV} + V_F) - V_{VSR}} \quad (2)$$

where

- $V_{OCV}$  is the converter regulated output voltage,
- $V_F$  is the output rectifier forward drop at near-zero current,
- $N_{AS}$  is the transformer auxiliary to secondary turns ratio,
- $R_{S1}$  is the VS divider high-side resistance,
- $V_{VSR}$  is the CV regulating level at the VS input (see the [Section 6.5](#) table).

### 7.3.1.4 DRV (Gate Drive)

The DRV pin is connected to the MOSFET gate pin, usually through a series resistor. The gate driver provides a gate-drive signal limited to 14 V. The turn-on characteristic of the driver is a 25-mA current source which limits the turn-on dv/dt of the MOSFET drain and reduces the leading-edge current spike, but still provides gate-drive current to overcome the Miller plateau. The gate-drive turn-off current is determined by the low-side driver  $R_{DS(on)}$  and any external gate-drive resistance. The user can reduce the turn-off MOSFET drain dv/dt by adding external gate resistance.

### 7.3.1.5 CS (Current Sense)

The current-sense pin is connected through a series resistor ( $R_{LC}$ ) to the current-sense resistor ( $R_{CS}$ ). The current-sense threshold is 0.75 V for  $I_{PP(max)}$  and 0.25 V for  $I_{PP(min)}$ . The series resistor  $R_{LC}$  provides the function of feed-forward line compensation to eliminate change in  $I_{PP}$  due to change in di/dt and the propagation delay of the internal comparator and MOSFET turn-off time. There is an internal leading-edge blanking time of 235 ns to eliminate sensitivity to the MOSFET turn-on current spike. It should not be necessary to place a bypass capacitor on the CS pin. The value of  $R_{CS}$  is determined by the target output current in constant-current (CC) regulation. The values of  $R_{CS}$  and  $R_{LC}$  can be determined by the equations below. The term  $\eta_{XFMR}$  is intended to account for the energy stored in the transformer but not delivered to the secondary. This includes transformer resistance and core loss, bias power, and primary-to-secondary leakage ratio.

**Example:** With a transformer core and winding loss of 5%, primary-to-secondary leakage inductance of 3.5%, and bias power to output power ratio of 1.5%. The  $\eta_{XFMR}$  value is approximately:  $1 - 0.05 - 0.035 - 0.015 = 0.9$ .

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2I_{OCC}} \times \eta_{XFMR} \quad (3)$$

where

- $V_{CCR}$  is a current regulation constant (see the [Section 6.5](#) table),
- $N_{PS}$  is the transformer primary-to-secondary turns ratio (a ratio of 13 to 15 is recommended for 5-V output),
- $I_{OCC}$  is the target output current in constant-current regulation,
- $\eta_{XFMR}$  is the transformer efficiency.

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times T_D \times N_{PA}}{L_P} \quad (4)$$

where

- $R_{S1}$  is the VS pin high-side resistor value,
- $R_{CS}$  is the current-sense resistor value,
- $T_D$  is the current-sense delay including MOSFET turn-off delay, add ~50 ns to MOSFET delay,
- $N_{PA}$  is the transformer primary-to-auxiliary turns ratio,
- $L_P$  is the transformer primary inductance,
- $K_{LC}$  is a current-scaling constant (see the [Section 6.5](#) table).

### 7.3.1.6 CBC (Cable Compensation)

The cable compensation pin is connected to a resistor to ground to program the amount of output voltage compensation to offset cable resistance. The cable compensation block provides a 0-V to 3-V voltage level on the CBC pin corresponding to 0 to  $I_{OCC}$  output current. The resistance selected on the CBC pin programs a current mirror that is summed into the VS feedback divider therefore increasing the output voltage as  $I_{OUT}$  increases. There is an internal series resistance of 28 k $\Omega$  to the CBC pin which sets a maximum cable compensation of a 5-V output to 400 mV when CBC is shorted to ground. The CBC resistance value can be determined by the equation below.

$$R_{CBC} = \frac{V_{CBC(max)} \times 3 \text{ k}\Omega \times (V_{OCV} + V_F)}{V_{VSR} \times V_{OCBC}} - 28 \text{ k}\Omega \quad (5)$$

where

- $V_O$  is the output voltage,
- $V_F$  is the diode forward voltage,
- $V_{OCBC}$  is the target cable compensation voltage at the output terminals,
- $V_{CBC(max)}$  is the maximum voltage at the cable compensation pin at the maximum converter output current (see the [Section 6.5](#) table),
- $V_{VSR}$  is the CV regulating level at the VS input (see the [Section 6.5](#) table).

### 7.3.2 Fault Protection

There is comprehensive fault protection incorporated into the UCC28700-Q1. Protection functions include:

- Output overvoltage
- Input undervoltage
- Internal overtemperature
- Primary overcurrent fault
- CS pin fault
- VS pin fault

A UVLO reset and restart sequence applies for all fault protection events.

The output over-voltage function is determined by the voltage feedback on the VS pin. If the voltage sample on VS exceeds 115% of the nominal  $V_{OUT}$ , the device stops switching and keeps the internal circuitry enabled to discharge the VDD capacitor to the UVLO turn-off threshold. After that, the device returns to the start state and a start-up sequence ensues.

The UCC28700-Q1 always operates with cycle-by-cycle primary peak current control. The normal operating range of the CS pin is 0.75 V to 0.25 V. There is additional protection if the CS pin reaches 1.5 V. This results in a UVLO reset and restart sequence. There is no leading-edge blanking on the 1.5-V threshold on CS.

The line input run and stop thresholds are determined by current information at the VS pin during the MOSFET on-time. While the VS pin is clamped close to GND during the MOSFET on-time, the current through  $R_{S1}$  is monitored to determine a sample of the bulk capacitor voltage. A wide separation of run and stop thresholds allows clean start-up and shut-down of the power supply with the line voltage. The run current threshold is 220  $\mu$ A and the stop current threshold is 80  $\mu$ A.

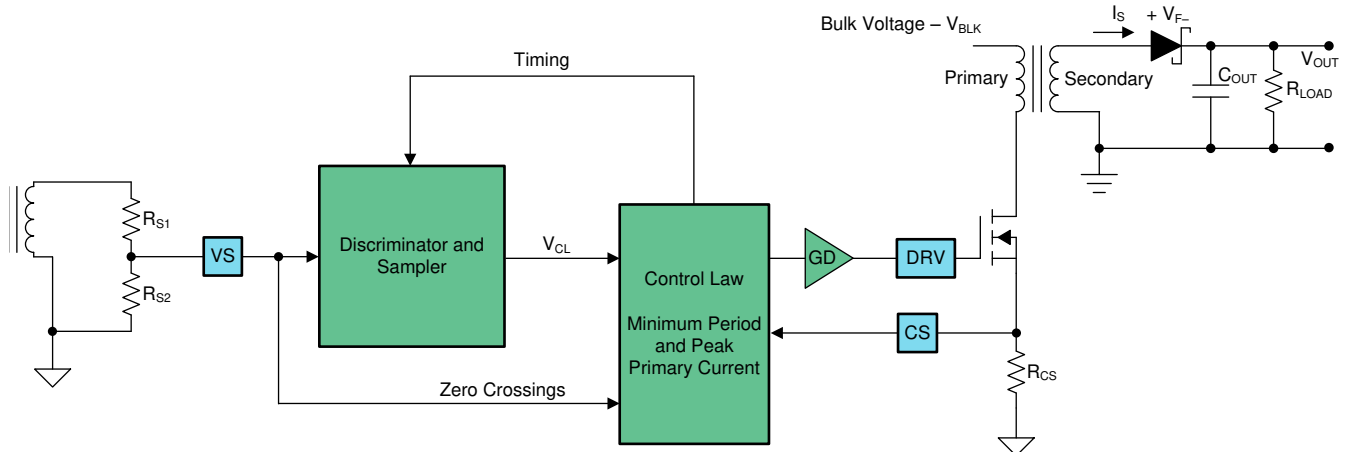
The internal overtemperature protection threshold is 165°C. If the junction temperature reaches this threshold the device initiates a UVLO reset cycle. If the temperature is still high at the end of the UVLO cycle, the protection cycle repeats.

Protection is included in the event of component failures on the VS pin. If complete loss of feedback information on the VS pin occurs, the controller stops switching and restarts.

## 7.4 Device Functional Modes

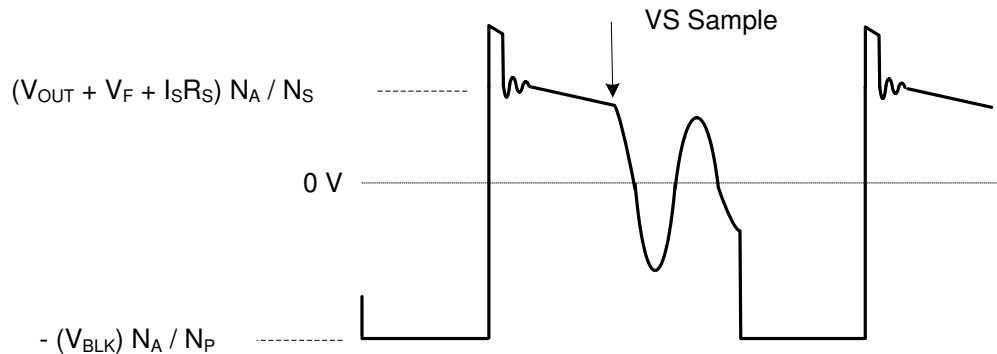
### 7.4.1 Primary-Side Voltage Regulation

Figure 7-1 shows a simplified flyback converter with the main voltage regulation blocks of the device shown. The power train operation is the same as any DCM flyback circuit but accurate output voltage and current sensing is the key to primary-side control.



**Figure 7-1. Simplified Flyback Converter (with the main voltage regulation blocks)**

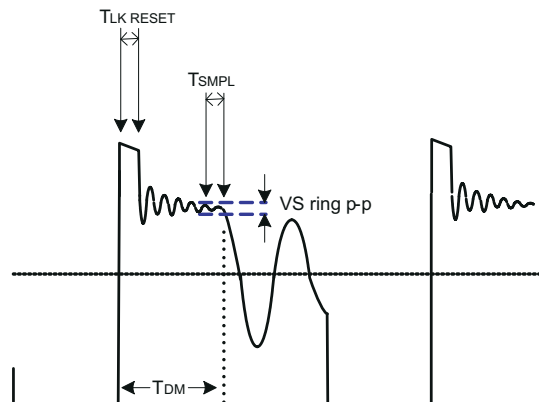
In primary-side control, the output voltage is sensed on the auxiliary winding during the transfer of transformer energy to the secondary. As shown in Figure 7-2 it is clear there is a down slope representing a decreasing total rectifier  $V_F$  and resistance voltage drop ( $I_S R_S$ ) as the secondary current decreases to zero. To achieve an accurate representation of the secondary output voltage on the auxiliary winding, the discriminator reliably blocks the leakage inductance reset and ringing, continuously samples the auxiliary voltage during the down slope after the ringing is diminished, and captures the error signal at the time the secondary winding reaches zero current. The internal reference on VS is 4.05 V; the resistor divider is selected as outlined in the VS pin description.



**Figure 7-2. Auxiliary Winding Voltage**

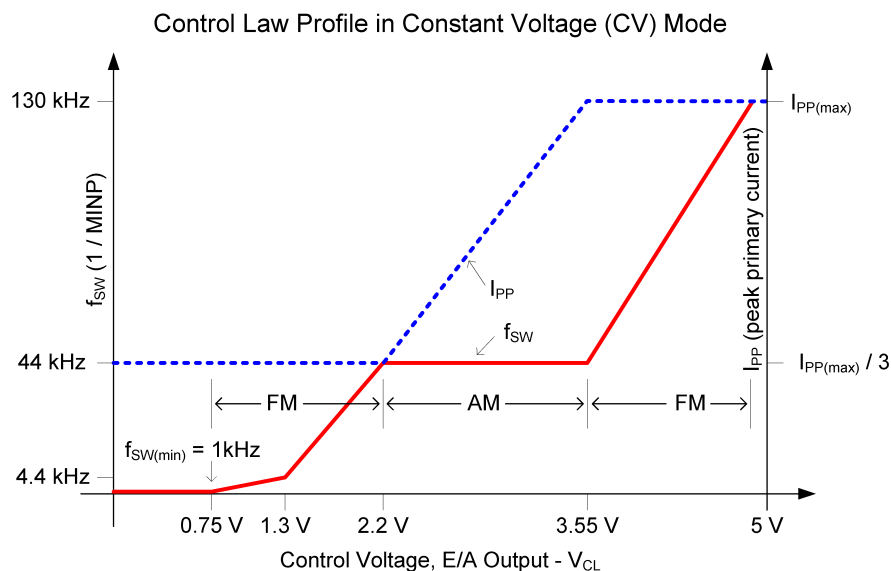
The UCC28700-Q1 VS signal sampler includes signal discrimination methods to ensure an accurate sample of the output voltage from the auxiliary winding. There are however some details of the auxiliary winding signal to ensure reliable operation, specifically the reset time of the leakage inductance and the duration of any subsequent leakage inductance ring. Refer to Figure 7-3 for a detailed illustration of waveform criteria to ensure a reliable sample on the VS pin. The first detail to examine is the duration of the leakage inductance reset pedestal,  $T_{LK\_RESET}$  in Figure 7-3. Because this can mimic the waveform of the secondary current decay, followed by a sharp downslope, it is important to keep the leakage reset time less than 500 ns for  $I_{PRI}$  minimum, and less than 1.5  $\mu$ s for  $I_{PRI}$  maximum. The second detail is the amplitude of ringing on the  $V_{AUX}$  waveform following  $T_{LK\_RESET}$ . The peak-to-peak voltage at the VS pin should be less than approximately 100 mV<sub>p-p</sub> at least 200 ns before the end of the demagnetization time,  $t_{DM}$ . If there is a concern with excessive ringing, it

usually occurs during light or no-load conditions, when  $t_{DM}$  is at the minimum. The tolerable ripple on  $V_S$  is scaled up to the auxiliary winding voltage by  $R_{S1}$  and  $R_{S2}$ , and is equal to  $100 \text{ mV} \times (R_{S1} + R_{S2}) / R_{S2}$ .



**Figure 7-3. Auxiliary Waveform Details**

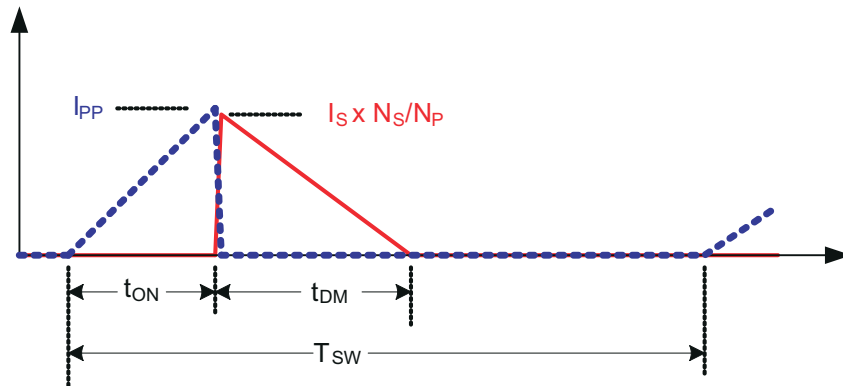
During voltage regulation, the controller operates in frequency modulation mode and amplitude modulation mode as illustrated in Figure 7-4 below. The internal operating frequency limits of the device are 130 kHz maximum and 1 kHz minimum. The transformer primary inductance and primary peak current chosen sets the maximum operating frequency of the converter. The output preload resistor and efficiency at low power determines the converter minimum operating frequency. There is no stability compensation required for the UCC28700-Q1 controller.



**Figure 7-4. Frequency and Amplitude Modulation Modes (during voltage regulation)**

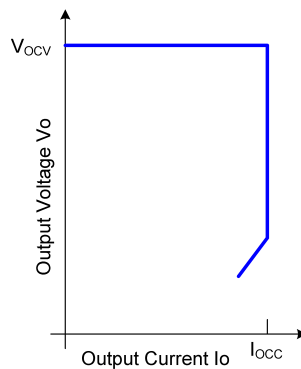
### 7.4.2 Primary-Side Current Regulation

Timing information at the VS pin and current information at the CS pin allow accurate regulation of the secondary average current. The control law dictates that as power is increased in CV regulation and approaching CC regulation the primary-peak current is at  $I_{PP(max)}$ . Referring to Figure 7-5 below, the primary-peak current, turns ratio, secondary demagnetization time ( $t_{DM}$ ), and switching period ( $T_{SW}$ ) determine the secondary average output current. Ignoring leakage inductance effects, the average output current is given by Equation 6. When the average output current reaches the regulation reference in the current control block, the controller operates in frequency modulation mode to control the output current at any output voltage at or below the voltage regulation target as long as the auxiliary winding can keep VDD above the UVLO turn-off threshold.



**Figure 7-5. Transformer Currents**

$$I_{OUT} = \frac{I_{PP}}{2} \times \frac{N_P}{N_S} \times \frac{t_{DM}}{T_{SW}} \quad (6)$$

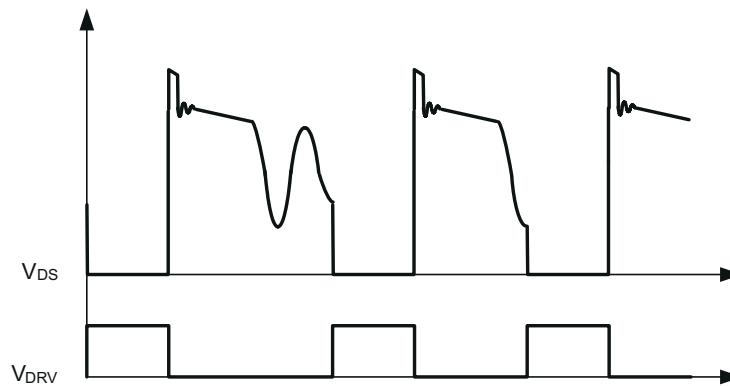


**Figure 7-6. Typical Target Output V-I Characteristic**

### 7.4.3 Valley-Switching

The UCC28700-Q1 utilizes valley-switching to reduce switching losses in the MOSFET, to reduce induced-EMI, and to minimize the turn-on current spike at the sense resistor. The controller operates in valley-switching in all load conditions unless the  $V_{DS}$  ringing has diminished.

Referring to [Figure 7-7](#) below, the UCC28700-Q1 operates in a valley-skipping mode in most load conditions to maintain an accurate voltage or current regulation point and still switch on the lowest available  $V_{DS}$  voltage.



**Figure 7-7. Valley-Skipping Mode**

### 7.4.4 Start-Up Operation

Upon application of input voltage to the converter, the start-up resistor connected to VDD from the bulk capacitor voltage ( $V_{BLK}$ ) charges the VDD capacitor. During charging of the VDD capacitor the device bias supply current is less than 1.5  $\mu\text{A}$ . When VDD reaches the 21-V UVLO turn-on threshold, the controller is enabled and the converter starts switching. The initial three cycles are limited to  $I_{PP(\min)}$ . This allows sensing any initial input or output faults with minimal power delivery. After the initial three cycles at minimum  $I_{PP(\min)}$ , the controller responds to the condition dictated by the control law. The converter remains in discontinuous mode during charging of the output capacitor(s), maintaining a constant output current until the output voltage is in regulation.

## 8 Applications and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The UCC28700-Q1 flyback power supply controller provides constant voltage (CV) and constant current (CC) output regulation to help meet USB-compliant adaptors and charger requirements. These devices use the information obtained from auxiliary winding sensing (VS) to control the output voltage and do not require optocoupler/TL431 feedback circuitry. Not requiring optocoupler feedback reduces the component count and makes the design more cost effective.

### 8.2 Typical Application

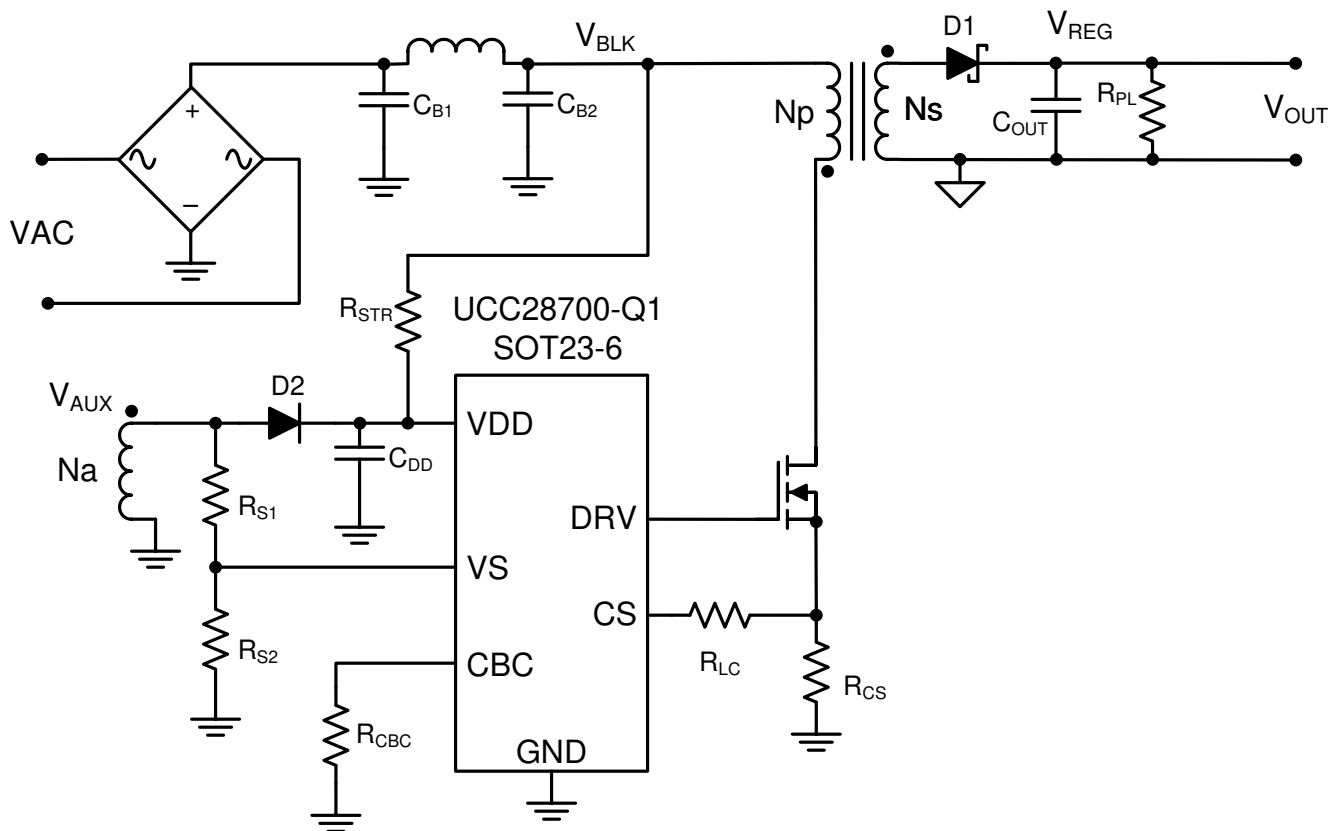


Figure 8-1. Typical Application Circuit

## 8.2.1 Design Requirements

**Table 8-1. Design Parameters**

| PARAMETER                                           | SYMBOL         | NOTES AND CONDITIONS                                                                                                       | MIN  | NOM     | MAX  | UNIT |
|-----------------------------------------------------|----------------|----------------------------------------------------------------------------------------------------------------------------|------|---------|------|------|
| <b>INPUT CHARACTERISTICS</b>                        |                |                                                                                                                            |      |         |      |      |
| Input Voltage                                       | $V_{IN}$       |                                                                                                                            | 100  | 115/230 | 240  | V    |
| Line Frequency                                      | $f_{LINE}$     |                                                                                                                            | 47   | 50/60   | 64   | Hz   |
| No Load Input Power                                 | $P_{SB\_CONV}$ | $V_{IN} = \text{Nom}$ , $I_O = 0 \text{ A}$                                                                                |      |         | 30   | mW   |
| Brownout Voltage                                    | $V_{IN(RUN)}$  | $I_O = \text{Nom}$                                                                                                         |      | 70      |      | V    |
| <b>OUTPUT CHARACTERISTICS</b>                       |                |                                                                                                                            |      |         |      |      |
| Output Voltage                                      | $V_O$          | $V_{IN} = \text{Nom}$ , $I_O = \text{Nom}$                                                                                 | 4.75 | 5       | 5.25 | V    |
| Output Voltage Ripple                               | $V_{RIPPLE}$   | $V_{IN} = \text{Nom}$ , $I_O = \text{Max}$                                                                                 |      |         | 0.1  | V    |
| Output Current                                      | $I_O$          | $V_{IN} = \text{Min to Max}$                                                                                               |      | 1       | 1.05 | A    |
| Output OVP                                          | $V_{OVP}$      | $I_{OUT} = \text{Min to Max}$                                                                                              |      | 5.75    |      | V    |
| Transient Response                                  |                |                                                                                                                            |      |         |      |      |
| Load Step ( $V_O = 4.1 \text{ V to } 6 \text{ V}$ ) | $V_{O\Delta}$  | (0.1 A to 0.6 A) or (0.6 A to 0.1 A)<br>$V_{O\Delta} = 0.9 \text{ V}$ for $C_{OUT}$ calculation<br>in applications section | 4.1  | 5       | 6    | V    |
| <b>SYSTEMS CHARACTERISTICS</b>                      |                |                                                                                                                            |      |         |      |      |
| Switching Frequency                                 |                |                                                                                                                            |      |         | 105  | kHz  |
| Full Load Efficiency (115/230 V RMS Input)          | $\eta$         | $I_O = 1 \text{ A}$                                                                                                        | 74%  |         | 76%  |      |

## 8.2.2 Detailed Design Procedure

This procedure outlines the steps to design a constant-voltage, constant-current flyback converter using the UCC28700-Q1 controller. Please refer to the [Figure 8-1](#) for circuit details and section [Section 11.1.1](#) for variable definitions used in the applications equations below.

### 8.2.2.1 Transformer Parameter Verification

The transformer turns ratio selected affects the MOSFET  $V_{DS}$  and secondary rectifier reverse voltage so these should be reviewed. The UCC28700-Q1 controller requires a minimum on time of the MOSFET ( $T_{ON}$ ) and minimum  $D_{MAG}$  time ( $T_{DMAG}$ ) of the secondary rectifier in the high line, minimum load condition. The selection of  $F_{MAX}$ ,  $L_P$  and  $R_{CS}$  affects the minimum  $T_{ON}$  and  $T_{DMAG}$ .

The secondary rectifier and MOSFET voltage stress can be determined by the equations below.

$$V_{REV} = \frac{V_{IN(max)} \times \sqrt{2}}{N_{PS}} + V_{OCV} + V_{OCBC} \quad (7)$$

For the MOSFET  $V_{DS}$  voltage stress, an estimated leakage inductance voltage spike ( $V_{LK}$ ) needs to be included.

$$V_{DSPK} = (V_{IN(max)} \times \sqrt{2}) + (V_{OCV} + V_F + V_{OCBC}) \times N_{PS} + V_{LK} \quad (8)$$

The following equations are used to determine if the minimum  $T_{ON}$  target of 300 ns and minimum  $T_{DMAG}$  target of 1.1  $\mu$ s is achieved.

$$T_{ON(min)} = \frac{L_P}{V_{IN(max)} \times \sqrt{2}} \times \frac{I_{PP(max)} \times V_{CST(min)}}{V_{CST(max)}} \quad (9)$$

$$T_{DMAG(min)} = \frac{T_{ON(min)} \times V_{IN(max)} \times \sqrt{2}}{N_{PS} \times (V_{OCV} + V_F)} \quad (10)$$

### 8.2.2.2 Output Capacitance

The output capacitance value is typically determined by the transient response requirement from no-load. For example, in some USB charger applications there is a requirement to maintain a minimum  $V_O$  of 4.1 V with a load-step transient of 0 mA to 500 mA. The equation below assumes that the switching frequency can be at the UCC28700-Q1 minimum of  $f_{SW(min)}$ .

$$C_{OUT} = \frac{I_{TRAN} \left( \frac{1}{f_{SW(min)}} + 150 \mu s \right)}{V_{O\Delta}} \quad (11)$$

Another consideration of the output capacitor(s) is the ripple voltage requirement which is reviewed based on secondary peak current and ESR. A margin of 20% is added to the capacitor ESR requirement in the equation below.

$$R_{ESR} = \frac{V_{RIPPLE} \times 0.8}{I_{PP(max)} \times N_{PS}} \quad (12)$$

### 8.2.2.3 VDD Capacitance, $C_{DD}$

The capacitance on VDD needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage in constant-current regulation. At this time the auxiliary winding can sustain the voltage to the UCC28700-Q1. The total output current available to the load and to charge the output capacitors is the constant-current regulation target. The equation below assumes the output current of the flyback is available to charge the output capacitance until the minimum output voltage is achieved. There is an estimated 1 mA of gate-drive current in the equation and 1 V of margin added to VDD.

$$C_{DD} = \frac{(I_{RUN} + 1\text{mA}) \times \frac{C_{OUT} \times V_{OCC}}{I_O}}{(V_{DD(on)} - V_{DD(off)}) - 1\text{V}} \quad (13)$$

### 8.2.2.4 VDD Start-Up Resistance, $R_{STR}$

Once the VDD capacitance is known, the start-up resistance from  $V_{BULK}$  to achieve the turn-on time target can be determined.

$$R_{STR} = \frac{\sqrt{2} \times V_{IN(min)}}{I_{START} + \frac{V_{DD(on)} \times C_{DD}}{T_{STR}}} \quad (14)$$

### 8.2.2.5 VS Resistor Divider, Line Compensation, and Cable Compensation

The VS divider resistors determine the output voltage regulation point of the flyback converter, also the high-side divider resistor ( $R_{S1}$ ) determines the line voltage at which the controller enables continuous DRV operation.  $R_{S1}$  is initially determined based on transformer auxiliary to primary turns ratio and desired input voltage operating threshold.

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(run)}} \quad (15)$$

The low-side VS pin resistor is selected based on desired  $V_O$  regulation voltage.

$$R_{S2} = \frac{R_{S1} \times V_{VSR}}{N_{AS} \times (V_{OCV} + V_F) - V_{VSR}} \quad (16)$$

The UCC28700-Q1 can maintain tight constant-current regulation over input line by utilizing the line compensation feature. The line compensation resistor ( $R_{LC}$ ) value is determined by current flowing in  $R_{S1}$  and expected gate drive and MOSFET turn-off delay. Assume a 50-ns internal delay in the UCC28700-Q1.

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times T_D \times N_{PA}}{L_P} \quad (17)$$

On the UCC28700-Q1 which has adjustable cable compensation, the resistance for the desired compensation level at the output terminals can be determined using the equation below.

$$R_{CBC} = \frac{V_{CBC(max)} \times 3\text{ k}\Omega \times (V_{OCV} + V_F)}{V_{VSR} \times V_{OCBC}} - 28\text{ k}\Omega \quad (18)$$

### 8.2.2.6 Input Bulk Capacitance and Minimum Bulk Voltage

Determine the minimum voltage on the input capacitance,  $C_{B1}$  and  $C_{B2}$  total, in order to determine the maximum  $N_p$  to  $N_s$  turns ratio of the transformer. The input power of the converter based on target full-load efficiency, minimum input RMS voltage, and minimum AC input frequency are used to determine the input capacitance requirement.

Maximum input power is determined based on  $V_{OCV}$ ,  $I_{OCC}$ , and the full-load efficiency target.

$$P_{IN} = \frac{V_{OCV} \times I_{OCC}}{\eta} \quad (19)$$

The below equation provides an accurate solution for input capacitance based on a target minimum bulk capacitor voltage. To target a given input capacitance value, iterate the minimum capacitor voltage to achieve the target capacitance.

$$C_{BULK} = \frac{2P_{IN} \times \left( 0.25 + \frac{1}{2\pi} \times \arcsin \left( \frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}} \right) \right)}{\left( 2V_{IN(min)}^2 - V_{BULK(min)}^2 \right) \times f_{LINE}} \quad (20)$$

### 8.2.2.7 Transformer Turns Ratio, Inductance, Primary-Peak Current

The maximum primary-to-secondary turns ratio can be determined by the target maximum switching frequency at full load, the minimum input capacitor bulk voltage, and the estimated DCM quasi-resonant time.

Initially determine the maximum available total duty cycle of the on time and secondary conduction time based on target switching frequency and DCM resonant time. For DCM resonant time, assume 500 kHz if you do not have an estimate from previous designs. For the transition mode operation limit, the period required from the end of secondary current conduction to the first valley of the  $V_{DS}$  voltage is  $\frac{1}{2}$  of the DCM resonant period, or 1  $\mu$ s assuming 500-kHz resonant frequency.  $D_{MAX}$  can be determined using the equation below.

$$D_{MAX} = 1 - \left( \frac{T_R}{2} \times f_{MAX} \right) - D_{MAGCC} \quad (21)$$

Once  $D_{MAX}$  is known, the maximum turns ratio of the primary to secondary can be determined with the equation below.  $D_{MAGCC}$  is defined as the secondary diode conduction duty cycle during constant-current, CC, operation. It is set internally by the UCC28700-Q1 at 0.425. The total voltage on the secondary winding needs to be determined; which is the sum of  $V_{OCV}$ , the secondary rectifier  $V_F$ , and the cable compensation voltage ( $V_{OCBC}$ ). For the 5-V USB charger applications, a turns ratio range of 13 to 15 is typically used.

$$N_{PS(max)} = \frac{D_{MAX} \times V_{BULK(min)}}{D_{MAGCC} \times (V_{OCV} + V_F + V_{OCBC})} \quad (22)$$

Once an optimum turns ratio is determined from a detailed transformer design, use this ratio for the following parameters.

The UCC28700-Q1 controller constant-current regulation is achieved by maintaining a maximum  $D_{MAG}$  duty cycle of 0.425 at the maximum primary current setting. The transformer turns ratio and constant-current regulating voltage determine the current sense resistor for a target constant current.

Since not all of the energy stored in the transformer is transferred to the secondary, a transformer efficiency term is included. This efficiency number includes the core and winding losses, leakage inductance ratio, and bias power ratio to rated output power. For a 5-V, 1-A charger example, bias power of 1.5% is a good estimate. An overall transformer efficiency of 0.9 is a good estimate to include 3.5% leakage inductance, 5% core and winding loss, and 1.5% bias power.

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2I_{OCC}} \times \eta_{XFMR} \quad (23)$$

The primary transformer inductance can be calculated using the standard energy storage equation for flyback transformers. Primary current, maximum switching frequency and output and transformer power losses are included in the equation below. Initially determine transformer primary current.

Primary current is simply the maximum current sense threshold divided by the current sense resistance.

$$I_{PP(max)} = \frac{V_{CST(max)}}{R_{CS}} \quad (24)$$

$$L_P = \frac{2(V_{OCV} + V_F + V_{OCBC}) \times I_{OCC}}{\eta_{XFMR} \times I_{PP(max)}^2 \times f_{MAX}} \quad (25)$$

The secondary winding to auxiliary winding transformer turns ratio ( $N_{AS}$ ) is determined by the lowest target operating output voltage in constant-current regulation and the  $V_{DD}$  UVLO of the UCC28700-Q1. There is

additional energy supplied to VDD from the transformer leakage inductance energy which allows a lower turns ratio to be used in many designs.

$$N_{AS} = \frac{V_{DD(off)} + V_{FA}}{V_{OCC} + V_F} \quad (26)$$

### 8.2.2.8 Standby Power Estimate

Assuming no-load standby power is a critical design parameter, determine estimated no-load power based on target converter maximum switching frequency and output power rating.

The following equation estimates the stand-by power of the converter.

$$P_{SB\_CONV} = \frac{P_{OUT} \times f_{MIN}}{\eta_{SB} \times K_{AM}^2 \times f_{MAX}} \quad (27)$$

For a typical USB charger application, the bias power during no-load is approximately 2.5 mW. This is based on 25-V VDD and 100-μA bias current. The output preload resistor can be estimated by  $V_{OCV}$  and the difference in the converter stand-by power and the bias power. The equation for output preload resistance accounts for bias power estimated at 2.5 mW.

$$R_{PL} = \frac{V_{OCV}^2}{P_{SB\_CONV} - 2.5 \text{ mW}} \quad (28)$$

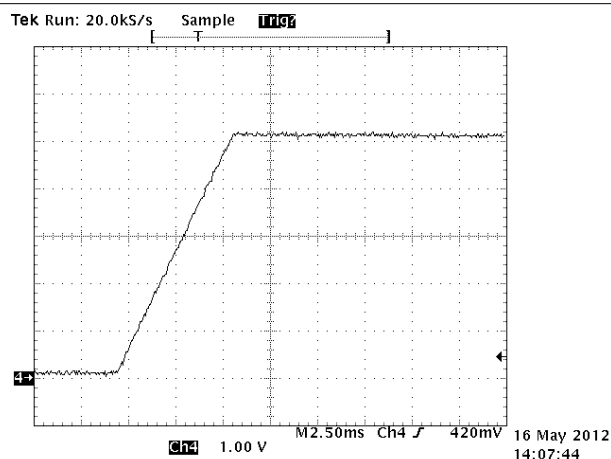
Typical start-up resistance values for  $R_{STR}$  range from 13 MΩ to 20 MΩ to achieve 1-s start-up time. The capacitor bulk voltage for the loss estimation is the highest voltage for the stand-by power measurement, typically 325  $V_{DC}$ .

$$P_{RSTR} = \frac{V_{BLK}^2}{R_{STR}} \quad (29)$$

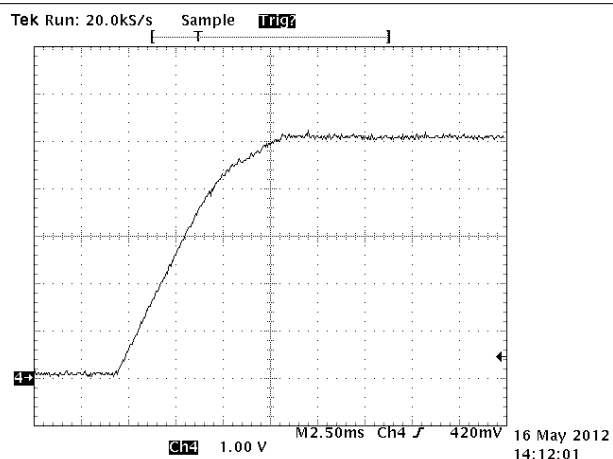
For the total stand-by power estimation add an estimated 2.5 mW for snubber loss to the start-up resistance and converter stand-by power loss.

$$P_{SB} = P_{SB\_CONV} + P_{RSTR} + 2.5 \text{ mW} \quad (30)$$

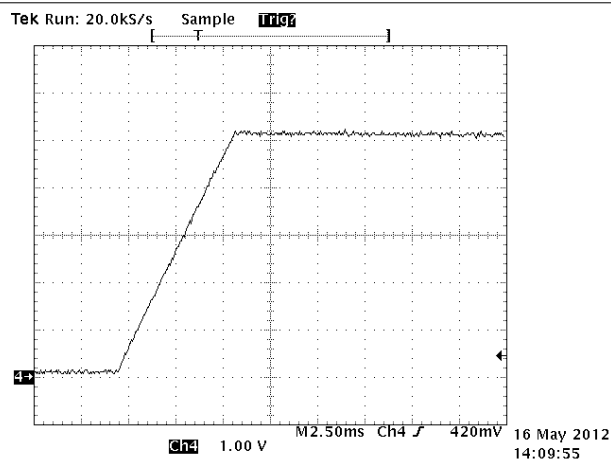
### 8.2.3 Application Curves



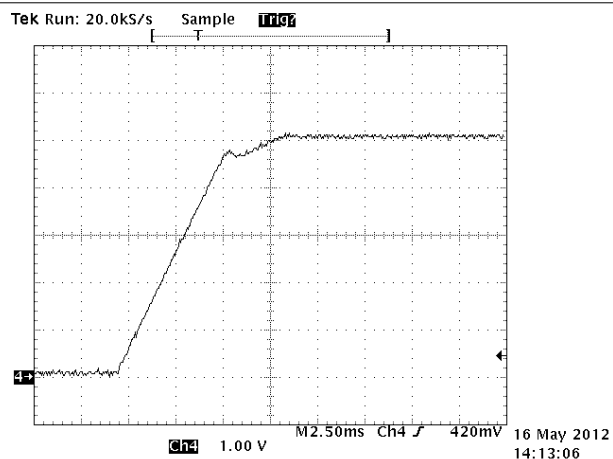
**Figure 8-2. Output at Startup at 115-V RMS (No Load)**



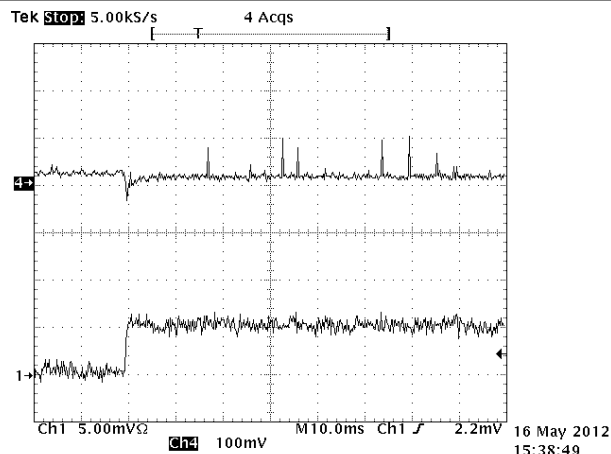
**Figure 8-3. Output at Startup at 115-V RMS (5-Ω Load)**



**Figure 8-4. Output at Startup at 230-V RMS (No Load)**

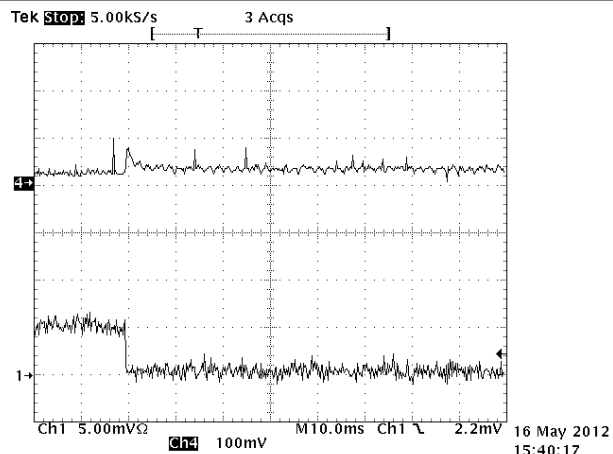


**Figure 8-5. Output at Startup at 230-V RMS (5-Ω Load)**



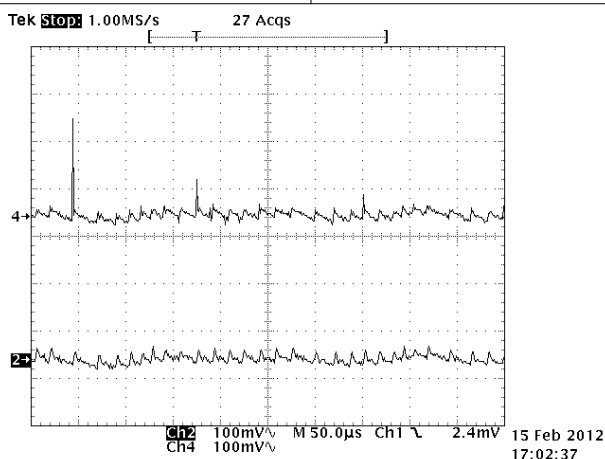
CH1 =  $I_O$ , CH4 =  $V_O$  With a 5-V Offset

**Figure 8-6. Load Transients: (0.1-A to 0.6-A Load Step)**



CH1 =  $I_O$ , CH4 =  $V_O$  With a 5-V Offset

**Figure 8-7. Load Transients: (0.6-A to 0.1-A Load Step)**



CH4 =  $V_O$ , Output voltage at EVM output

CH2 =  $V_O$ , Output voltage measured at the end of the 3M of cable in parallel with a 1- $\mu$ F capacitor. The output voltage has less than 50 mV of output ripple at the end of the cable.

**Figure 8-8. Output Ripple Voltage at Full Load**

## 9 Power Supply Recommendations

The UCC28700-Q1 is intended for AC/DC converters with input voltage range of 85 V<sub>AC(rms)</sub> to 265 V<sub>AC(rms)</sub> using Flyback topology. It can be used in other applications and converter topologies with different input voltages. Be sure that all voltages and currents are within the recommended operating conditions and absolute maximum ratings of the device.

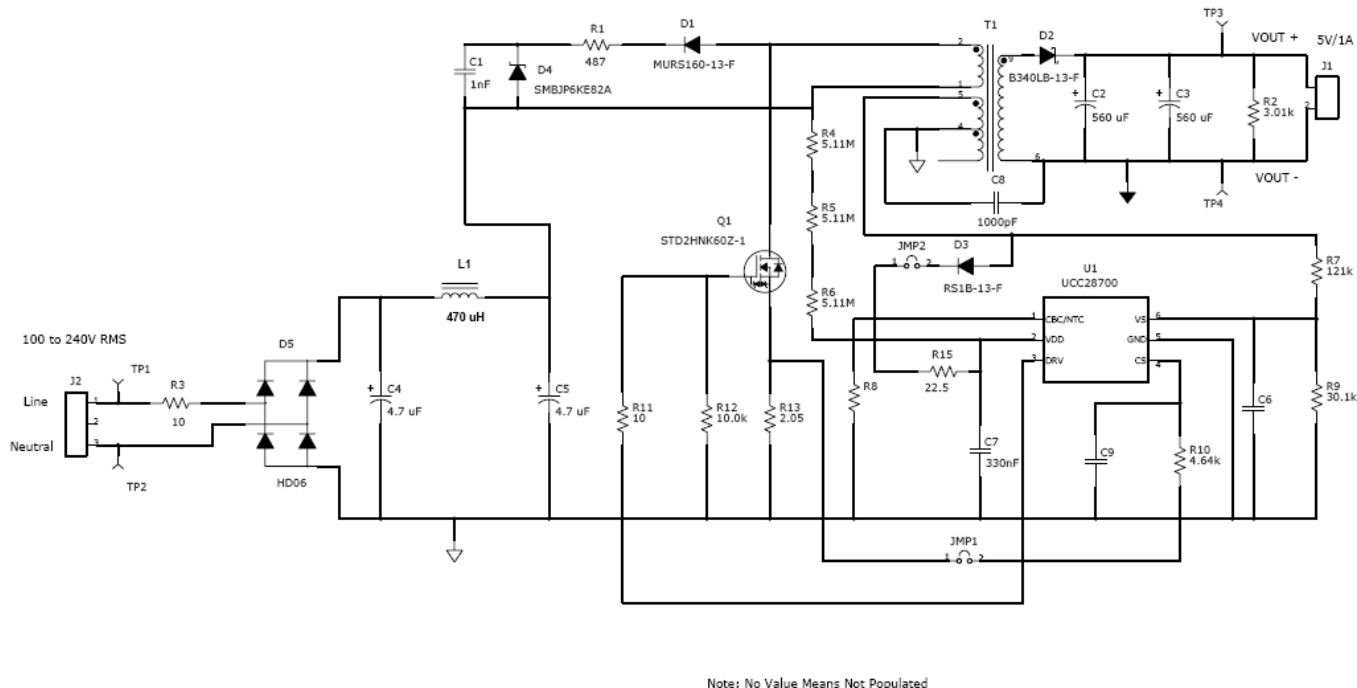
To maintain output current regulation over the entire input voltage range, design the converter to operate close to  $f_{MAX}$  when in full-load conditions.

To improve thermal performance increase the copper area connected to GND pins.

## 10 Layout

### 10.1 Layout Guidelines

- High frequency bypass Capacitor C7 should be placed across Pin 2 and 5 as close as you can get it to the pins.
- Resistor R15 and C7 form a low pass filter and the connection of R15 and C7 should be as close to the VDD pin as possible.
- C9 should be put as close to CS pin and R10 as possible. This forms a low pass filter with R10.
- The connection for C9 and R10 should be as close to the CS pin as possible.
- Please note that C9 may not be required in all designs. However, it is wise to put a place holder for it in your design.
- The VS pin controls the output voltage through the transformer turns ratio and the voltage divider of R7 and R9. Note the trace with between the R7, R9 and VS pin should be; as short as; possible to reduce/eliminate possible EMI coupling.
- Note the IC ground and power ground should meet at the bulk capacitor's (C4 and C5) return. Try to ensure that high frequency/high current from the power stage does not go through the signal ground.
  - The high frequency/high current path that you need to be cautious of on the primary is C4, C5 +, T1 (P1,P2), Q1d, Q1s, R13 to the return of C4 and C5.
- Try to keep all high current loops as short as possible.
- Keep all high current/high frequency traces away from or perpendicular to other traces in the design.
- Traces on the voltage clamp formed by D1, R1, D4 and C4 as short as possible.
- C4 return needs to be as close to the bulk capacitor supply as possible. This reduces the magnitude of dv/dt caused by large di/dt.
- Avoid mounting semiconductors under magnetics.



**Figure 10-1. 5-W USB Adapter Schematic**

## 10.2 Layout Example

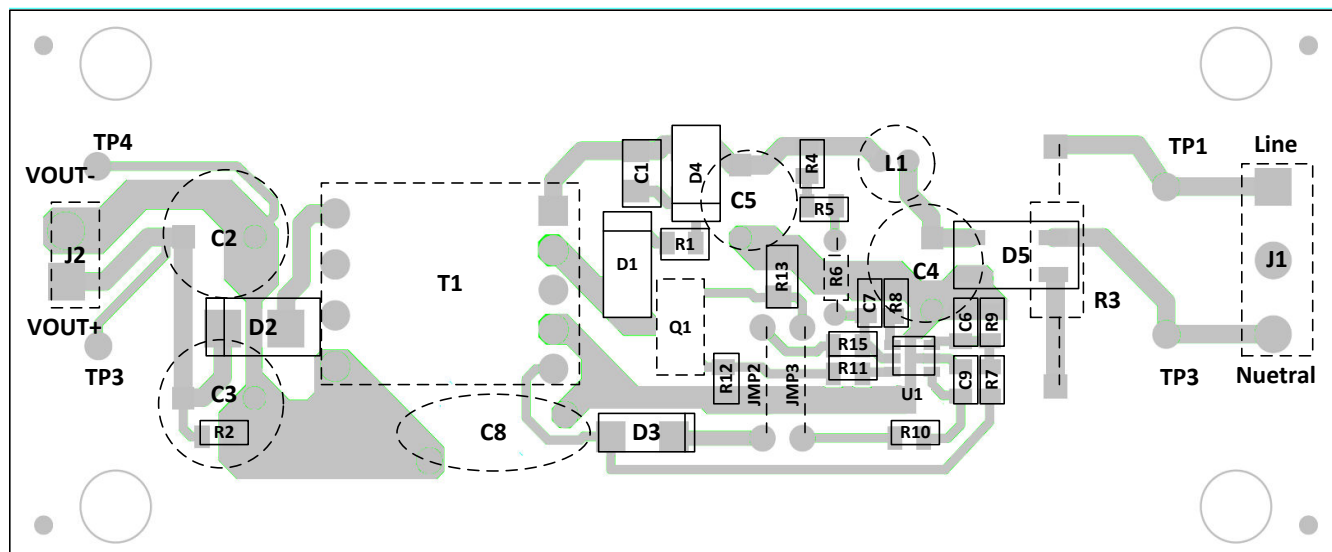


Figure 10-2. Layout Example

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Device Nomenclature

##### 11.1.1.1 Capacitance Terms in Farads

|            |                                                    |
|------------|----------------------------------------------------|
| $C_{BULK}$ | total input capacitance of $C_{B1}$ and $C_{B2}$ . |
| $C_{DD}$   | minimum required capacitance on the VDD pin.       |
| $C_{OUT}$  | minimum output capacitance required.               |

##### 11.1.1.2 Duty Cycle Terms

|             |                                                     |
|-------------|-----------------------------------------------------|
| $D_{MAGCC}$ | secondary diode conduction duty cycle in CC, 0.425. |
| $D_{MAX}$   | MOSFET on-time duty cycle.                          |

##### 11.1.1.3 Frequency Terms in Hertz

|               |                                                                                                          |
|---------------|----------------------------------------------------------------------------------------------------------|
| $f_{LINE}$    | minimum line frequency.                                                                                  |
| $f_{MAX}$     | target full-load maximum switching frequency of the converter.                                           |
| $f_{MIN}$     | minimum switching frequency of the converter, add 15% margin over the $f_{SW(min)}$ limit of the device. |
| $f_{SW(min)}$ | minimum switching frequency (see the <a href="#">Section 6.5</a> table)                                  |

##### 11.1.1.4 Current Terms in Amperes

|                |                                                                           |
|----------------|---------------------------------------------------------------------------|
| $I_{OCC}$      | converter output constant-current target.                                 |
| $I_{PP(max)}$  | maximum transformer primary current.                                      |
| $I_{START}$    | start-up bias supply current (see the <a href="#">Section 6.5</a> table). |
| $I_{TRAN}$     | required positive load-step current.                                      |
| $I_{VSL(run)}$ | VS pin run current (see the <a href="#">Section 6.5</a> table).           |

##### 11.1.1.5 Current and Voltage Scaling Terms

|          |                                                                                            |
|----------|--------------------------------------------------------------------------------------------|
| $K_{AM}$ | maximum-to-minimum peak primary current ratio (see the <a href="#">Section 6.5</a> table). |
| $K_{LC}$ | current-scaling constant (see the <a href="#">Section 6.5</a> table).                      |

##### 11.1.1.6 Transformer Terms

|          |                                                 |
|----------|-------------------------------------------------|
| $L_P$    | transformer primary inductance.                 |
| $N_{AS}$ | transformer auxiliary-to-secondary turns ratio. |
| $N_{PA}$ | transformer primary-to-auxiliary turns ratio.   |
| $N_{PS}$ | transformer primary-to-secondary turns ratio.   |

##### 11.1.1.7 Power Terms in Watts

|                |                                                      |
|----------------|------------------------------------------------------|
| $P_{IN}$       | converter maximum input power.                       |
| $P_{OUT}$      | full-load output power of the converter.             |
| $P_{RSTR}$     | VDD start-up resistor power dissipation.             |
| $P_{SB}$       | total stand-by power.                                |
| $P_{SB\_CONV}$ | $P_{SB}$ minus start-up resistor and snubber losses. |

##### 11.1.1.8 Resistance Terms in $\Omega$

|           |                                        |
|-----------|----------------------------------------|
| $R_{CS}$  | primary current programming resistance |
| $R_{ESR}$ | total ESR of the output capacitor(s).  |

|                        |                                                                 |
|------------------------|-----------------------------------------------------------------|
| <b>R<sub>PL</sub></b>  | preload resistance on the output of the converter.              |
| <b>R<sub>S1</sub></b>  | high-side VS pin resistance.                                    |
| <b>R<sub>S2</sub></b>  | low-side VS pin resistance.                                     |
| <b>R<sub>STR</sub></b> | maximum start-up resistance to achieve the turn-on time target. |
| <b>R<sub>STR</sub></b> | V <sub>DD</sub> start-up resistance.                            |

#### **11.1.1.9 Timing Terms in Seconds**

|                              |                                                                                 |
|------------------------------|---------------------------------------------------------------------------------|
| <b>T<sub>D</sub></b>         | current-sense delay including MOSFET turn-off delay; add 50 ns to MOSFET delay. |
| <b>T<sub>DMAG(min)</sub></b> | minimum secondary rectifier conduction time.                                    |
| <b>T<sub>ON(min)</sub></b>   | minimum MOSFET on time.                                                         |
| <b>T<sub>R</sub></b>         | resonant frequency during the DCM (discontinuous conduction mode) time.         |
| <b>T<sub>STR</sub></b>       | converter start-up time requirement.                                            |

#### 11.1.1.10 Voltage Terms in Volts

|                 |                                                                                                                     |
|-----------------|---------------------------------------------------------------------------------------------------------------------|
| $V_{BLK}$       | highest bulk capacitor voltage for stand-by power measurement.                                                      |
| $V_{BULK(min)}$ | minimum voltage on $C_{B1}$ and $C_{B2}$ at full power.                                                             |
| $V_{OCBC}$      | target cable compensation voltage at the output terminals.                                                          |
| $V_{CBC(max)}$  | maximum voltage at the CBC pin at the maximum converter output current (see the <a href="#">Section 6.5</a> table). |
| $V_{CCR}$       | constant-current regulating voltage (see the <a href="#">Section 6.5</a> table).                                    |
| $V_{CST(max)}$  | CS pin maximum current-sense threshold (see the <a href="#">Section 6.5</a> table).                                 |
| $V_{CST(min)}$  | CS pin minimum current-sense threshold (see the <a href="#">Section 6.5</a> table).                                 |
| $V_{DD(off)}$   | UVLO turn-off voltage (see the <a href="#">Section 6.5</a> table).                                                  |
| $V_{DD(on)}$    | UVLO turn-on voltage (see the <a href="#">Section 6.5</a> table).                                                   |
| $V_{O\Delta}$   | output voltage drop allowed during the load-step transient.                                                         |
| $V_{DSPK}$      | peak MOSFET drain-to-source voltage at high line.                                                                   |
| $V_F$           | secondary rectifier forward voltage drop at near-zero current.                                                      |
| $V_{FA}$        | auxiliary rectifier forward voltage drop.                                                                           |
| $V_{LK}$        | estimated leakage inductance energy reset voltage.                                                                  |
| $V_{OCV}$       | regulated output voltage of the converter.                                                                          |
| $V_{OCC}$       | target lowest converter output voltage in constant-current regulation.                                              |
| $V_{REV}$       | peak reverse voltage on the secondary rectifier.                                                                    |
| $V_{RIPPLE}$    | output peak-to-peak ripple voltage at full-load.                                                                    |
| $V_{VSR}$       | CV regulating level at the VS input (see the <a href="#">Section 6.5</a> table).                                    |

#### 11.1.1.11 AC Voltage Terms in $V_{RMS}$

|               |                                         |
|---------------|-----------------------------------------|
| $V_{IN(max)}$ | maximum input voltage to the converter. |
| $V_{IN(min)}$ | minimum input voltage to the converter. |
| $V_{IN(run)}$ | converter input start-up (run) voltage. |

#### 11.1.1.12 Efficiency Terms

|               |                                                                                                                                                                                         |
|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $\eta_{SB}$   | estimated efficiency of the converter at no-load condition, not including start-up resistance or bias losses. For a 5-V USB charger application, 60% to 65% is a good initial estimate. |
| $\eta$        | converter overall efficiency.                                                                                                                                                           |
| $\eta_{XFMR}$ | transformer primary-to-secondary power transfer efficiency.                                                                                                                             |

## 11.2 Documentation Support

### 11.2.1 Related Documentation

For related documentation see the following:

*Using the UCC28700EVM-068, Evaluation Module, [SLUU968](#)*

- 

### 11.3 Trademarks

All trademarks are the property of their respective owners.

## Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|---------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">UCC28700QDBVRQ1</a> | Active        | Production           | SOT-23 (DBV)   6 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | 700Q                |
| UCC28700QDBVRQ1.A               | Active        | Production           | SOT-23 (DBV)   6 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | 700Q                |
| UCC28700QDBVRQ1.B               | Active        | Production           | SOT-23 (DBV)   6 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | 700Q                |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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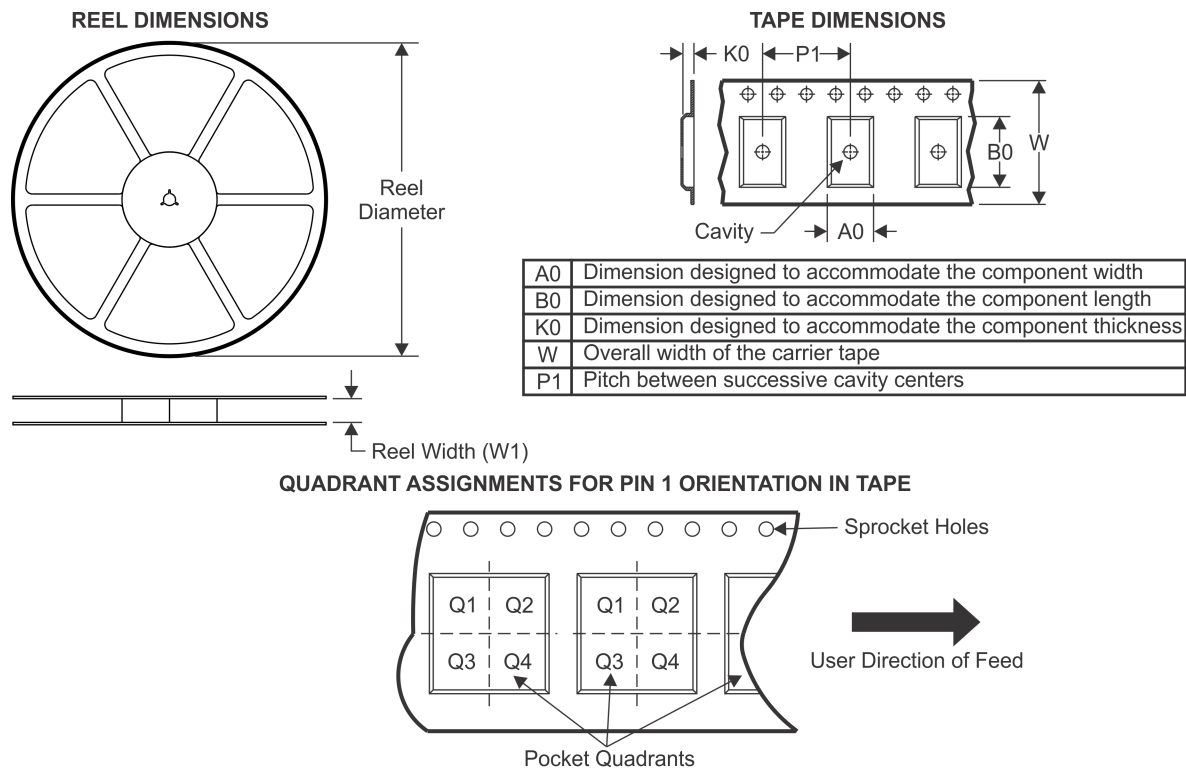
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### OTHER QUALIFIED VERSIONS OF UCC28700-Q1 :

- Catalog : [UCC28700](#)

NOTE: Qualified Version Definitions:

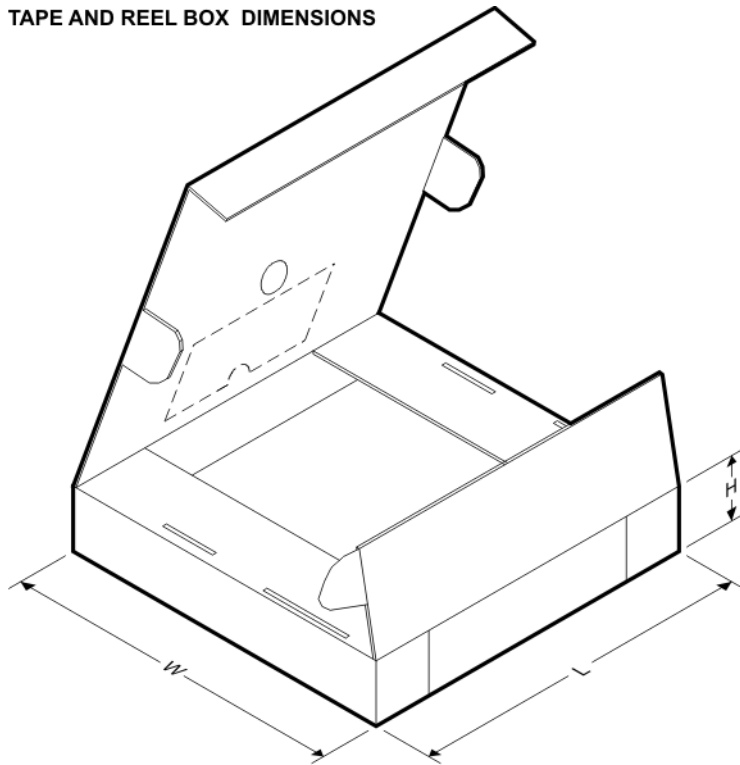
- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| UCC28700QDBVRQ1 | SOT-23       | DBV             | 6    | 3000 | 178.0              | 9.0                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |

## TAPE AND REEL BOX DIMENSIONS

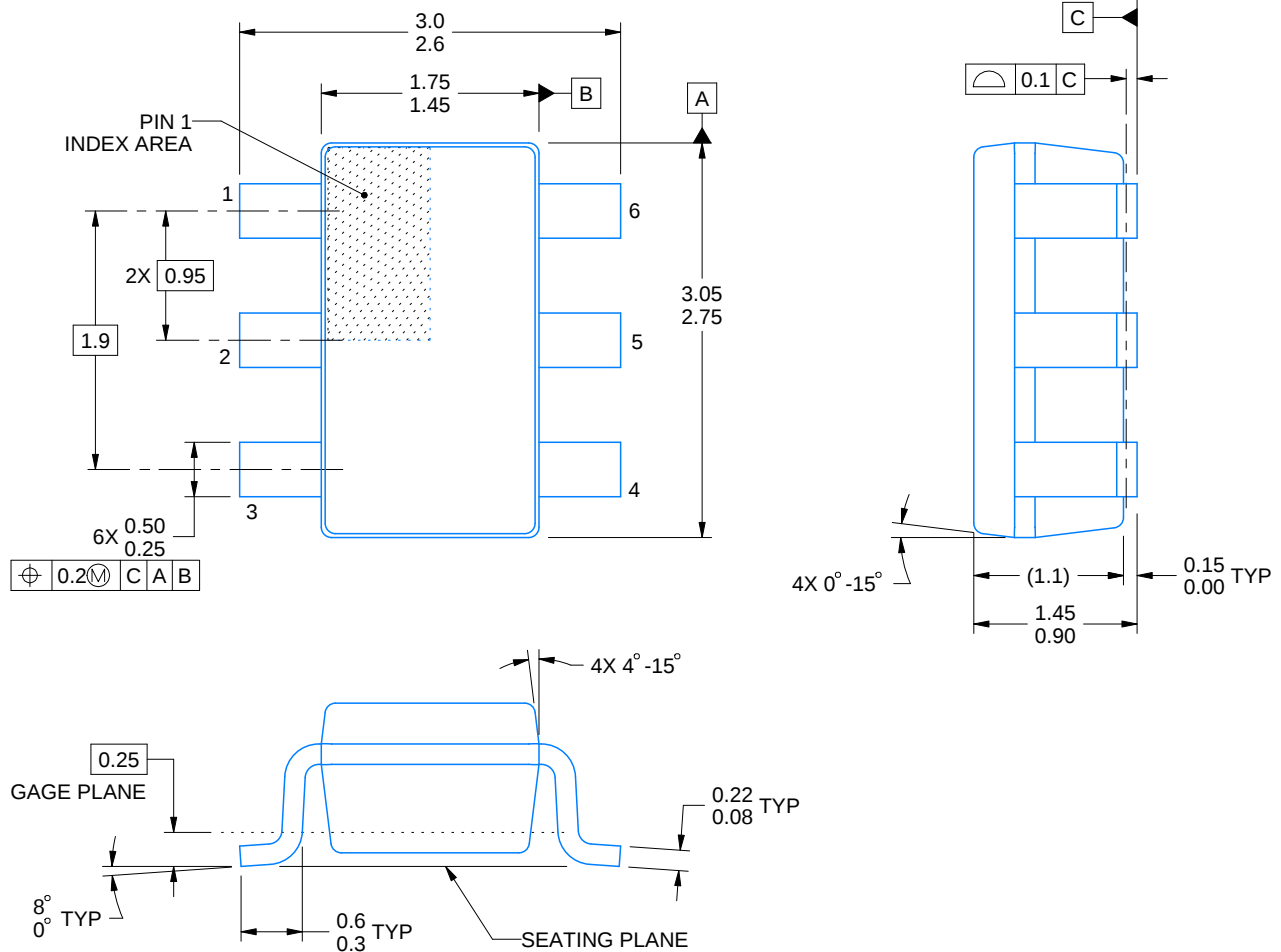


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| UCC28700QDBVRQ1 | SOT-23       | DBV             | 6    | 3000 | 180.0       | 180.0      | 18.0        |

**DBV0006A****PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



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**NOTES:**

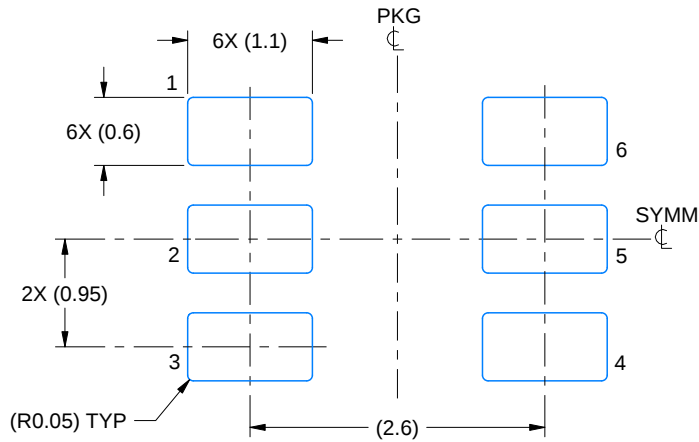
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

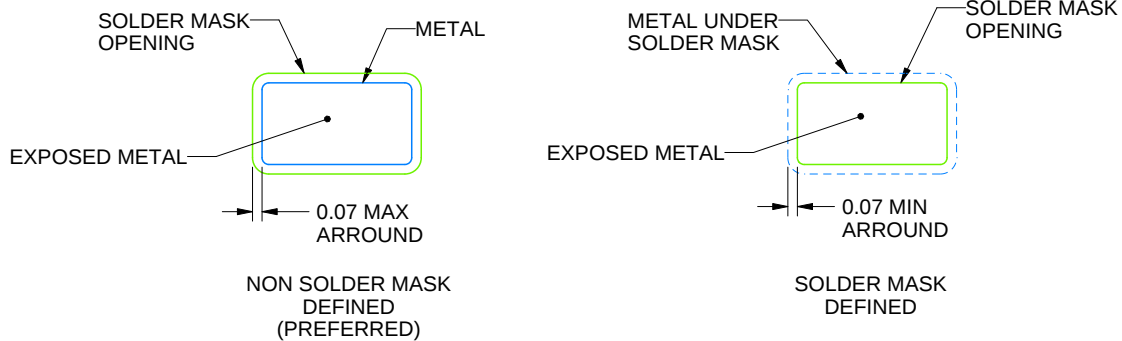
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

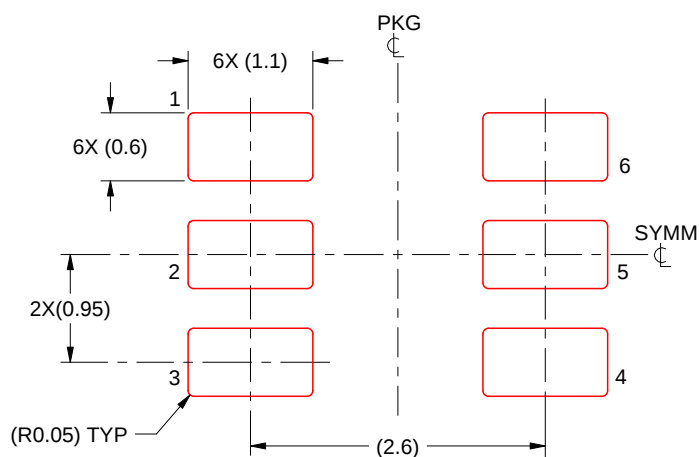
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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