UCC27211A-Q1 Automotive 120V, 3.7A/4.5A Half-Bridge Driver with 8V UVLO

1 Features

- AEC-Q100 Qualified for Automotive Applications: Device Temperature Grade 1
- –40°C to +150°C junction temperature range
- Drives two N-channel MOSFETs in high-side and low-side configuration with independent inputs
- Maximum boot voltage 120V DC
- 3.7A source, 4.5A sink output currents
- Input pins can tolerate –10V to +20V and are independent of supply voltage range
- TTL compatible inputs
- 8V to 17V VDD operating range, (20V ABS MAX)
- 7.2ns rise and 5.5ns fall time with 1000pF load
- Fast propagation delay times (20ns typical)
- 4ns delay matching
- Symmetrical undervoltage lockout for high-side and low-side driver
- Available in the industry standard SO-PowerPAD SOIC-8 package

2 Applications

- Automotive DC/DC converters and OBC
- 2-wheeler and 3-wheeler traction drive and battery pack
- Electric power steering (EPS)
- Wireless charging
- Smart glass module

3 Description

The UCC27211A-Q1 device driver is based on the popular UCC27201 MOSFET drivers; but, this device offers several significant performance improvements.

The peak output pullup and pulldown current has been increased to 3.7A source and 4.5A sink and thereby allows for driving large power MOSFETs with minimized switching losses during the transition through the Miller Plateau of the MOSFET. The input structure can directly handle –10VDC, which increases robustness and also allows direct interface to gate-drive transformers without using rectification diodes. The inputs are also independent of supply voltage and have a 20V maximum rating.

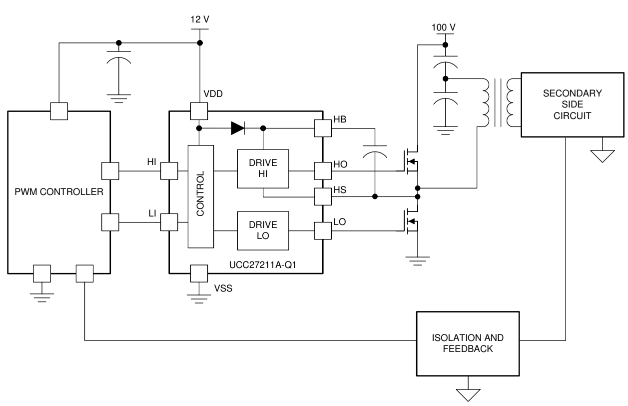
The switching node of the UCC27211A-Q1 (HS pin) can handle –(24 - VDD) V maximum, which allows the high-side channel to be protected from inherent negative voltages caused by parasitic inductance and stray capacitance. The UCC27211A-Q1 (TTL inputs) has increased hysteresis that allows for interface to analog or digital PWM controllers with enhanced noise immunity.

The low-side and high-side gate drivers are independently controlled and matched to 4ns between the turn on and turn off of each other. An on-chip 120V rated bootstrap diode eliminates the external discrete diodes. Undervoltage lockout is provided for both the high-side and the low-side drivers which provides symmetric turn on and turn off behavior and forces the outputs low if the drive voltage is below the specified threshold.

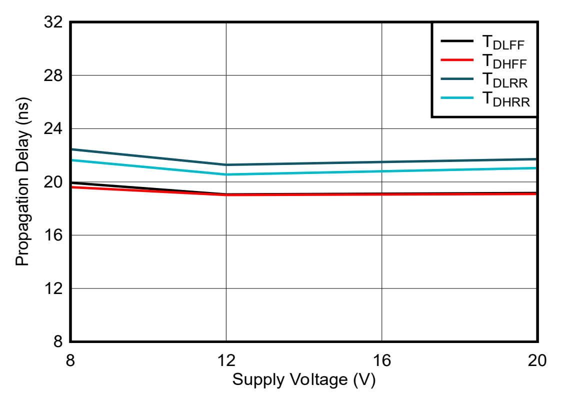
Device Information

PART NUMBER	PACKAGE[(1)]	BODY SIZE (NOM)
UCC27211A-Q1	DDA (PowerPAD™ SOIC, 8)	4.9mm × 3.9mm
	D (SOIC, 8)	4.9mm × 3.9mm

(1) For all available packages, see Section 12.



Typical Application Diagram



Propagation Delays vs Supply Voltage T = 25°C

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4 Pin Configuration and Functions

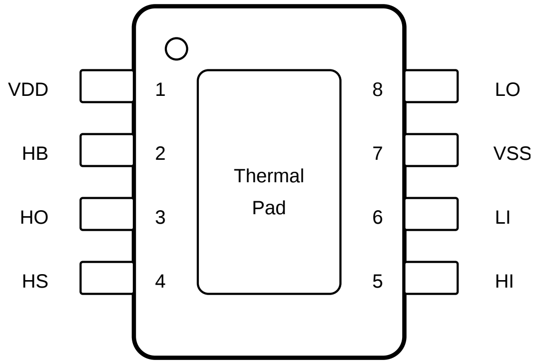


Figure 4-1. DDA Package 8-Pin SO-PowerPAD Top View

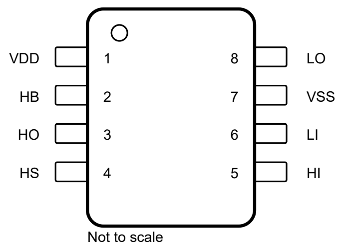


Figure 4-2. D Package 8-Pin SOIC Bottom View

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
HB	2	P	High-side bootstrap supply. The bootstrap diode is on-chip but the external bootstrap capacitor is required. Connect positive side of the bootstrap capacitor to this pin. Typical range of HB bypass capacitor is 0.022µF to 0.1µF. The capacitor value is dependant on the gate charge of the high-side MOSFET and must also be selected based on speed and ripple criteria.
HI	5	I	High-side input.[(1)]
HO	3	O	High-side output. Connect to the gate of the high-side power MOSFET.
HS	4	P	High-side source connection. Connect to source of high-side power MOSFET. Connect the negative side of bootstrap capacitor to this pin.
LI	6	I	Low-side input.[(1)]
LO	8	O	Low-side output. Connect to the gate of the low-side power MOSFET.
VDD	1	P	Positive supply to the lower-gate driver. De-couple this pin to V_{SS} (GND). Typical decoupling capacitor range is 0.22µF to 4.7µF (See [(2)]).
VSS	7	—	Negative supply terminal for the device that is generally grounded.
Thermal pad[(3)]		—	Used on the DDA package only. Electrically referenced to V_{SS} (GND). Connect to a large thermal mass trace or GND plane to dramatically improve thermal performance.

(1) HI or LI input is assumed to connect to a low impedance source signal. The source output impedance is assumed less than 100Ω. If the source impedance is greater than 100Ω, add a bypassing capacitor, each, between HI and VSS and between LI and VSS. The added capacitor value depends on the noise levels presented on the pins, typically from 1nF to 10nF should be effective to eliminate the possible noise effect. When noise is present on two pins, HI or LI, the effect is to cause HO and LO malfunctions to have wrong logic outputs.
(2) For cold temperature applications TI recommends the upper capacitance range. Follow the *Layout Guidelines* for PCB layout.
(3) The thermal pad is not directly connected to any leads of the package; however, it is electrically and thermally connected to the substrate which is the ground of the device.

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range and all voltages are with respect to V_{ss} (unless otherwise noted).[1]

			MIN	MAX	UNIT
V_{DD}	Supply voltage		–0.3	20	V
V_{HI}, V_{LI}	Input voltages on HI and LI		–10	20	V
V_{LO}	Output voltage on LO	DC	–0.3	V_{DD} + 0.3	V
		Repetitive pulse < 100ns[2]	–2	V_{DD} + 0.3	
V_{HO}	Output voltage on HO	DC	V_{HS} – 0.3	V_{HB} + 0.3	V
		Repetitive pulse < 100ns[2]	V_{HS} – 2	V_{HB} + 0.3	
V_{HS}	Voltage on HS	DC	–1	115	V
		Repetitive pulse < 100ns[2]	–(24V – V_{DD})	115	
V_{HB}	Voltage on HB		–0.3	120	V
	Voltage on HB-HS		–0.3	20	V
T_J	Operating junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Values are verified by characterization and are not production tested.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

Over operating free-air temperature range and all voltages are with respect to V_{SS} (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	8	12	17	V
V_{HS}	Voltage on HS	–1		105	V
	Voltage on HS (repetitive pulse < 100ns)[(1)]	–(24V – V_{DD})		110	V
V_{HB}	Voltage on HB	V_{HS} + 8.0, V_{DD} – 1		V_{HS} + 17, 115	V
SR_{HS}	Voltage slew rate on HS			50	V/ns
T_J	Operating junction temperature	–40		150	°C

(1) Values are verified by characterization and are not production tested.

5.4 Thermal Information

THERMAL METRIC[(1)]		UCC27211A-Q1		UNIT
		D (SOIC)	DDA (PowerPad™ SOIC)	
		8 Pins	8 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.5	44.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.1	68.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.6	20	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7	6.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	58.7	20	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	8.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

5.5 Electrical Characteristics

V_{DD} = V_{HB} =12V, V_{HS} = V_{SS} = 0V, No load on LO or HO, T_A = T_J = –40°C to +150°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{DD}	VDD quiescent current	V_{LI} = V_{HI} = 0V		0.11	0.19	mA
I_{DDO}	VDD operating current	f = 500kHz, C_{LOAD} = 0		1.4	3	mA
I_{HB}	Boot voltage quiescent current	V_{LI} = V_{HI} = 0V		0.065	0.12	mA
I_{HBO}	Boot voltage operating current	f = 500kHz, C_{LOAD} = 0		1.3	3	mA
I_{HBS}	HB to VSS quiescent current	V_{HS} = V_{HB} = 105V		0.0005	1	µA
I_{HBSO}	HB to VSS operating current	f = 500kHz, C_{LOAD} = 0		0.03	1	mA
INPUT						
V_{HIT_HI}	Input voltage high threshold		1.7	2.3	2.55	V
V_{HIT_LI}	Input voltage high threshold		1.7	2.3	2.55	V
V_{LIT_HI}	Input voltage low threshold		1.2	1.6	1.9	V
V_{LIT_LI}	Input voltage low threshold		1.2	1.6	1.9	V
$V_{IHYS\ HI}$	Input voltage hysteresis			0.7		V
$V_{IHYS\ LI}$	Input voltage hysteresis			0.7		V
R_{IN_HI}	Input pulldown resistance	V_{IN} = 3V		68		kΩ
R_{IN_LI}	Input pulldown resistance	V_{IN} = 3V		68		kΩ
UNDERVOLTAGE PROTECTION (UVLO)						
V_{DDR}	VDD rising threshold		6.2	7	7.8	V
V_{DDHYS}	VDD threshold hysteresis			0.5		V
V_{HBR}	VHB rising threshold		5.6	6.7	7.9	V
V_{HBHYS}	VHB threshold hysteresis			1.1		V
BOOTSTRAP DIODE						
V_F	Low-current forward voltage	$I_{VDD - HB}$ = 100µA		0.65	0.85	V
V_{FI}	High-current forward voltage	$I_{VDD - HB}$ = 100mA		0.9	1.05	V
R_D	Dynamic resistance, ΔVF/ΔI	$I_{VDD - HB}$ = 160mA and 180mA	0.3	0.55	0.85	Ω
LO GATE DRIVER						
V_{LOL}	Low level output voltage	I_{LO} = 100mA		0.07	0.19	V
V_{LOH}	High level output voltage	I_{LO} = -100mA, V_{LOH} = V_{DD} – V_{LO}		0.11	0.29	V
	Peak pullup current(1)	V_{LO} = 0 V		3.7		A
	Peak pulldown current(1)	V_{LO} = 12V		4.5		A
HO GATE DRIVER						
V_{HOL}	Low level output voltage	I_{HO} = 100mA		0.07	0.19	V
V_{HOH}	High level output voltage	I_{HO} = –100mA, V_{HOH} = V_{HB}- V_{HO}		0.11	0.29	V
	Peak pullup current(1)	V_{HO} = 0 V		3.7		A
	Peak pulldown current(1)	V_{HO} = 12V		4.5		A

(1) Parameter not tested in production.

5.6 Switching Characteristics

$V_{DD} = V_{HB} = 12V$, $V_{HS} = V_{SS} = 0V$, No load on LO or HO, $T_A = T_J$ = –40°C to +150°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROPAGATION DELAYS						
t_{DLFF}	VLI falling to VLO falling	C_{LOAD} = 0pF, from V_{LIT} of LI to 90% of LO falling	10	19	30	ns
t_{DHFF}	VHI falling to VHO falling	C_{LOAD} = 0pF, from V_{LIT} of HI to 90% of HO falling	10	19	30	ns
t_{DLRR}	VLI rising to VLO rising	C_{LOAD} = 0pF, from V_{HIT} of LI to 10% of LO rising	10	20	42	ns
t_{DHRR}	VHI rising to VHO rising	C_{LOAD} = 0pF, C_{LOAD} = 0pF, from V_{HIT} of HI to 10% of HO rising	10	20	42	ns
DELAY MATCHING						
t_{MON}	LI ON, HI OFF	T_J = 25°C		4	9.5	ns
t_{MON}	LI ON, HI OFF	T_J = -40°C to 150°C		4	17	ns
t_{MOFF}	LI OFF, HI ON	T_J = 25°C		4	9.5	ns
t_{MOFF}	LI OFF, HI ON	T_J = -40°C to 150°C		4	17	ns
OUTPUT RISE AND FALL TIME						
t_{R_LO}	LO rise time	C_{LOAD} = 1000pF, from 10% to 90%		7.2		ns
t_{R_HO}	HO rise time	C_{LOAD} = 1000pF, from 10% to 90%		7.2		ns
t_{F_LO}	LO fall time	C_{LOAD} = 1000pF, from 10% to 90%		5.5		ns
t_{F_HO}	HO fall time	C_{LOAD} = 1000pF, from 10% to 90%		5.5		ns
$t_{R\_LO\_p1}$	LO rise time (3V to 9V)	C_{LOAD} = 0.1µF, (3V to 9V)		0.27	0.6	µs
$t_{R\_HO\_p1}$	HO rise time (3V to 9V)	C_{LOAD} = 0.1µF, (3V to 9V)		0.27	0.6	µs
$t_{F\_LO\_p1}$	LO fall time (9V to 3V)	C_{LOAD} = 0.1µF, (9V to 3V)		0.16	0.4	µs
$t_{F\_HO\_p1}$	HO fall time (9V to 3V)	C_{LOAD} = 0.1µF, (9V to 3V)		0.16	0.4	µs
MISCELLANEOUS						
t_{IN_PW}	Minimum input pulse width that changes the output LO				40	ns
t_{IN_PW}	Minimum input pulse width that changes the output HO				40	ns
t_{OFF_BSD}	Bootstrap diode turnoff time[(1)] [(2)]	I_F = 20 mA, I_{REV} = 0.5A[(3)]		20		ns

(1) Parameter not tested in production.
(2) Typical values for T_A = 25°C.
(3) I_F: Forward current applied to bootstrap diode, I_{REV}: Reverse current applied to bootstrap diode.

5.7 Timing Diagrams

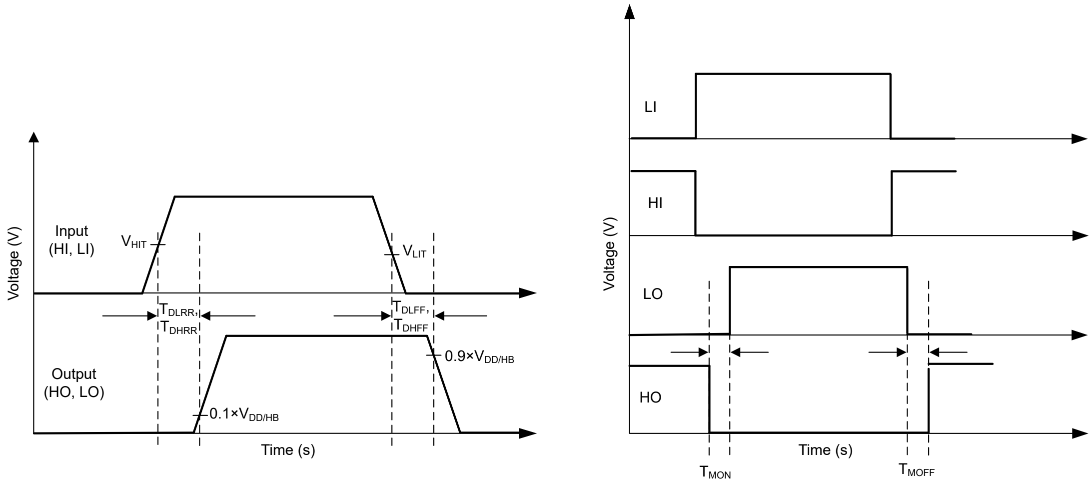


Figure 5-1. Timing Diagrams

5.8 Typical Characteristics

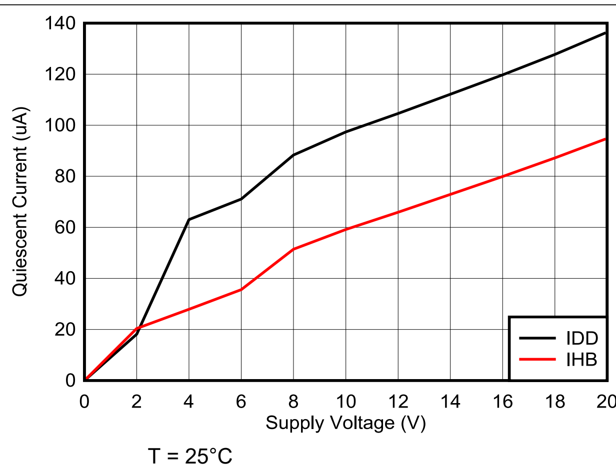


Figure 5-2. Quiescent Current vs Supply Voltage

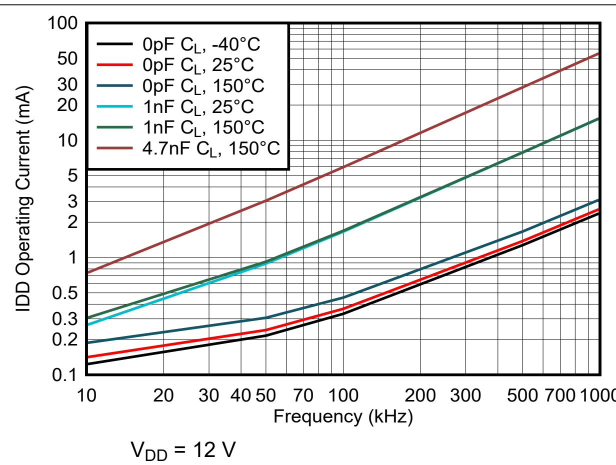


Figure 5-3. IDD Operating Current vs Frequency

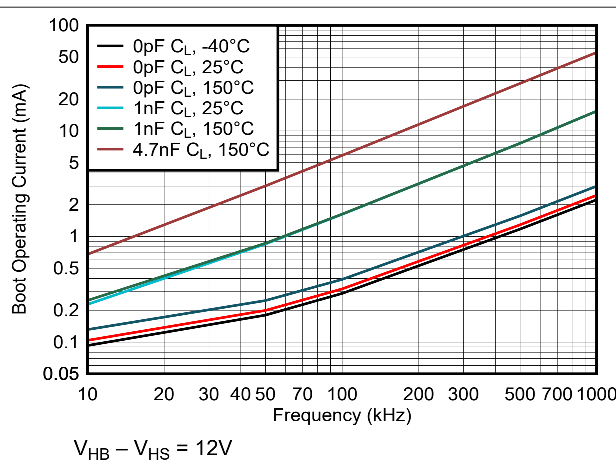


Figure 5-4. Boot Voltage Operating Current vs Frequency (HB To HS)

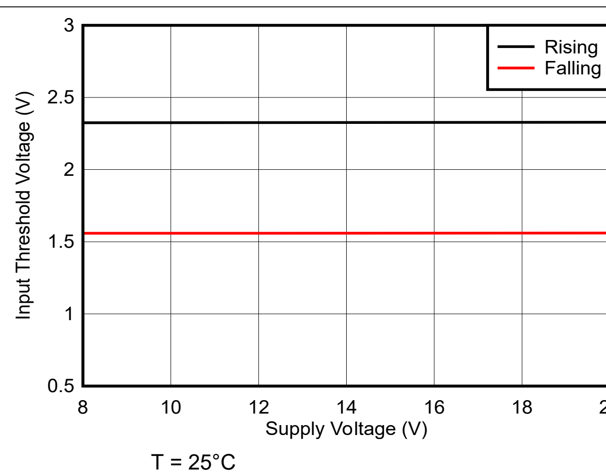


Figure 5-5. Input Threshold vs Supply Voltage

5.8 Typical Characteristics (continued)

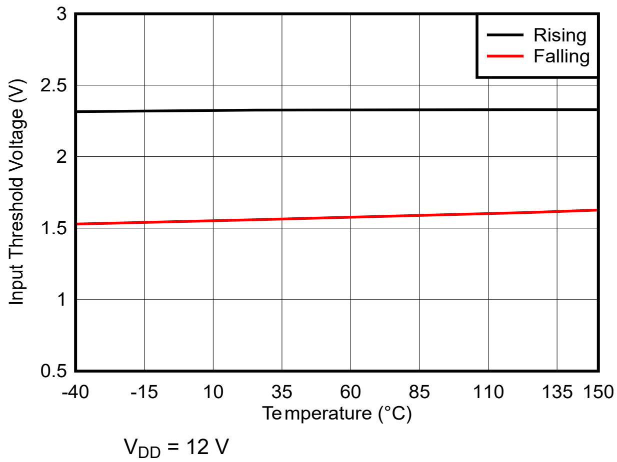


Figure 5-6. Input Thresholds vs Temperature

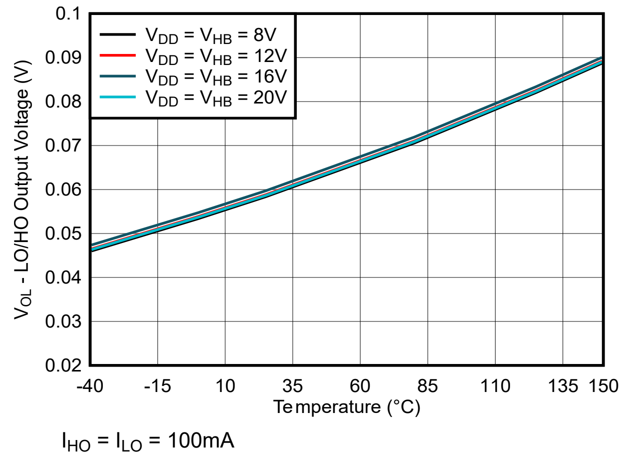


Figure 5-7. LO and HO Low-Level Output Voltage vs Temperature

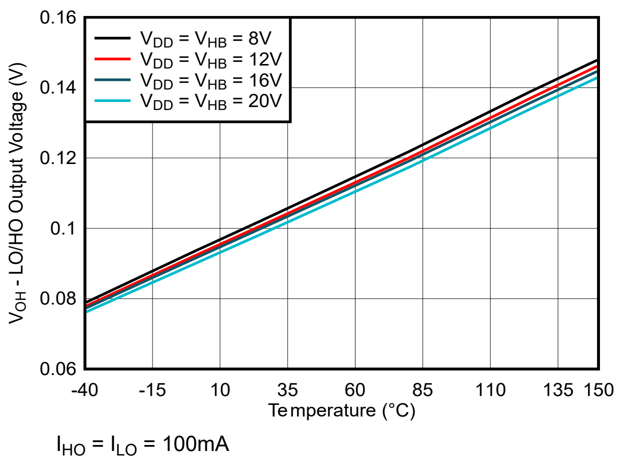


Figure 5-8. LO and HO High-Level Output Voltage vs Temperature

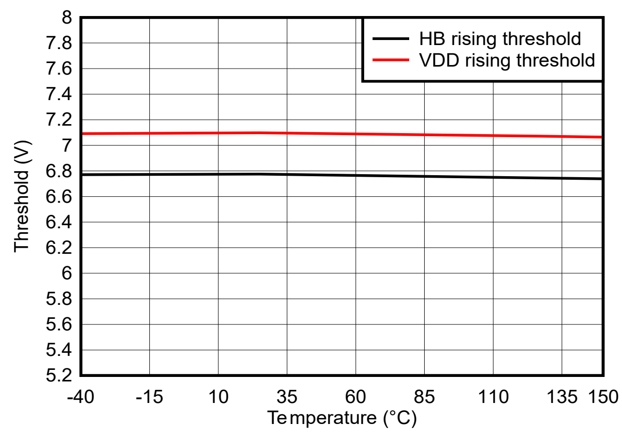


Figure 5-9. Undervoltage Lockout Threshold vs Temperature

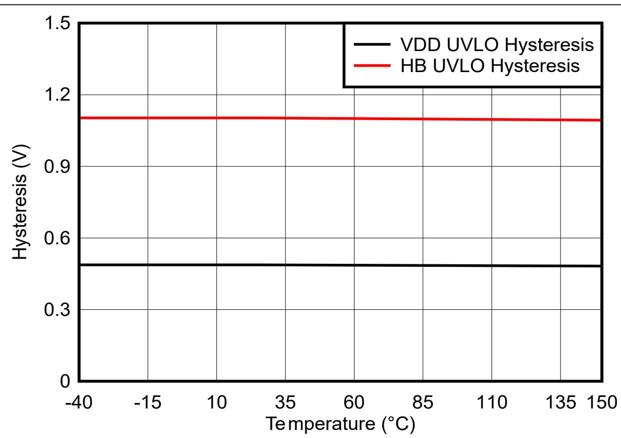


Figure 5-10. Undervoltage Lockout Threshold Hysteresis vs Temperature

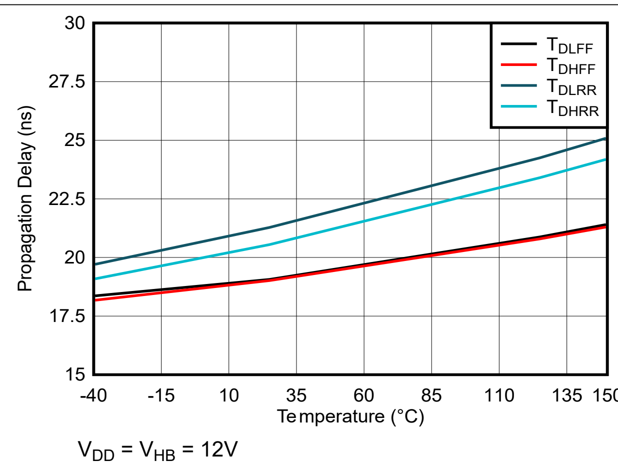


Figure 5-11. Propagation Delays vs Temperature

5.8 Typical Characteristics (continued)

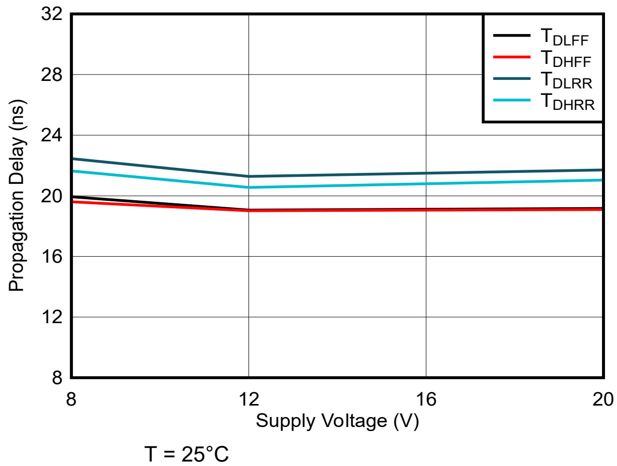


Figure 5-12. Propagation Delays vs Supply Voltage (V_{DD} = V_{HB})

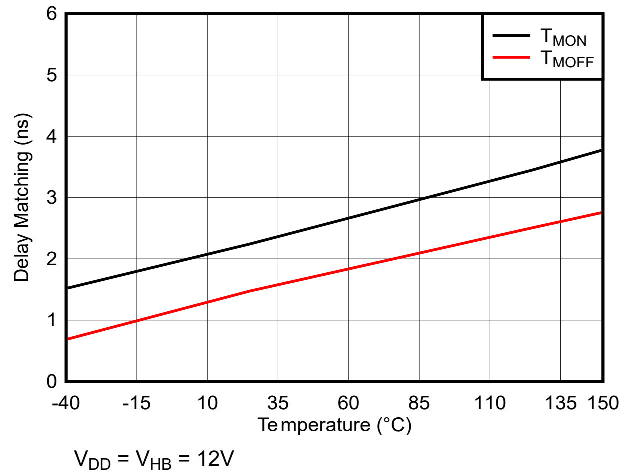


Figure 5-13. Delay Matching vs Temperature

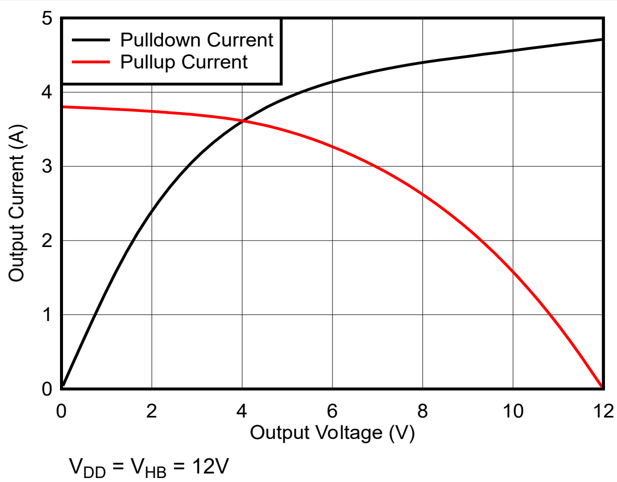


Figure 5-14. Output Current vs Output Voltage

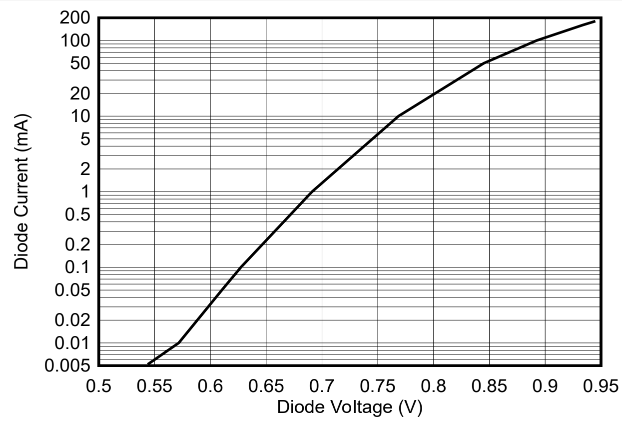


Figure 5-15. Diode Current vs Diode Voltage

6 Detailed Description

6.1 Overview

The UCC27211A-Q1 device is designed to drive both the high-side and low-side of N-Channel MOSFETs in a half- and full-bridge or synchronous-buck configuration. The floating high-side driver can operate with supply voltages of up to 120V, which allows for N-Channel MOSFET control in half-bridge, full-bridge, push-pull, two-switch forward, and active clamp forward converters.

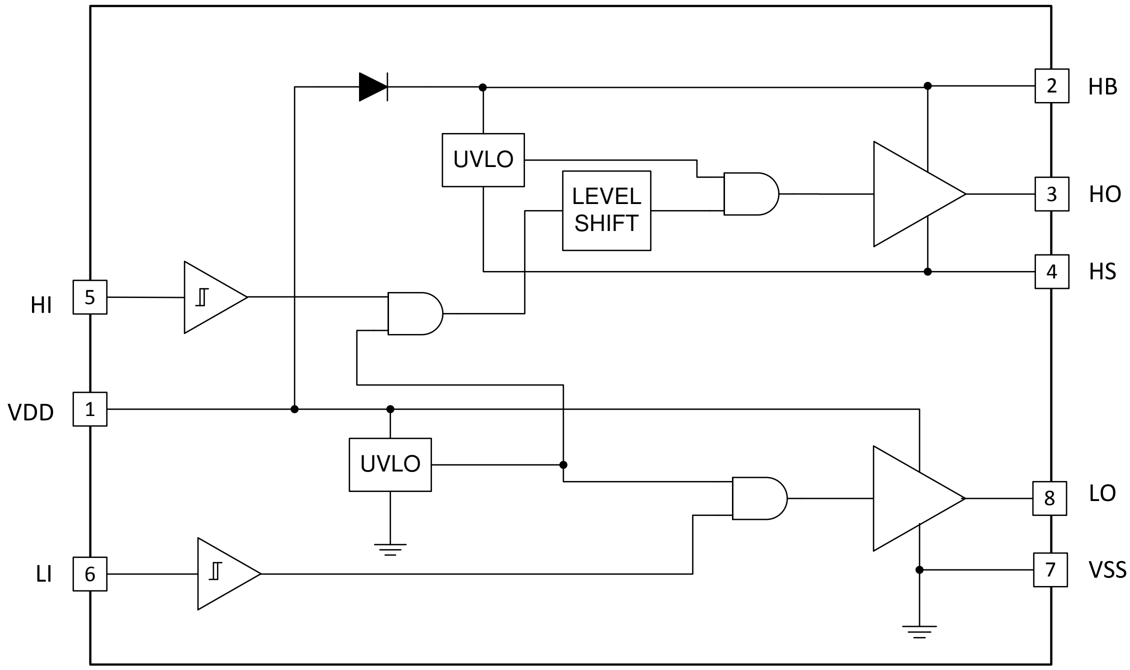
The UCC27211A -Q1 device features 3.7A source and 4.5A sink capability, industry best-in-class switching characteristics and a host of other features listed in Table 6-1. These features combine to ensure efficient, robust and reliable operation in high-frequency switching power circuits.

Table 6-1. UCC27211A-Q1 Highlights

FEATURE	BENEFIT
3.7A source and 4.5A sink current	High peak current ideal for driving large power MOSFETs with minimal power loss (fast-drive capability at Miller plateau)
Input pins (HI and LI) can directly handle –10VDC up to 20VDC	Increased robustness and ability to handle undershoot and overshoot can interface directly to gate-drive transformers without having to use rectification diodes.
120V internal boot diode	Provides voltage margin to meet telecom 100V surge requirements
Switch node (HS pin) able to handle –(24 – VDD) V maximum for 100ns	Allows the high-side channel to have extra protection from inherent negative voltages caused by parasitic inductance and stray capacitance
Robust ESD circuitry to handle voltage spikes	Excellent immunity to large dV/dT conditions
20ns propagation delay with 7.2ns rise time and 5.5ns fall time	Best-in-class switching characteristics and extremely low-pulse transmission distortion
4ns (typical) delay matching between channels	Avoids transformer volt-second offset in bridge
Symmetrical UVLO circuit	Ensures high-side and low-side shut down at the same time
TTL optimized thresholds with increased hysteresis	Complementary to analog or digital PWM controllers; increased hysteresis offers added noise immunity

In the UCC27211A-Q1 device, the high side and low side each have independent inputs that allow maximum flexibility of input control signals in the application. The boot diode for the high-side driver bias supply is internal to the device. The UCC27211A-Q1 is a TTL or logic compatible device. The high-side driver is referenced to the switch node (HS), which is typically the source pin of the high-side MOSFET and drain pin of the low-side MOSFET. The low-side driver is referenced to V_{SS}, which is typically ground. The UCC27211A-Q1 functions are divided into the input stages, UVLO protection, level shift, boot diode, and output driver stages.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Input Stages

The input stages of the UCC27211A-Q1 device have impedance of 68kΩ nominal and input capacitance is approximately 4pF. Pulldown resistance to V_{SS} (ground) is 68kΩ. The logic level compatible input provides a rising threshold of 2.3V and a falling threshold of 1.6V.

6.3.2 Undervoltage Lockout (UVLO)

The bias supplies for the high-side and low-side drivers have UVLO protection. V_{DD} as well as V_{HB} to V_{HS} differential voltages are monitored. The V_{DD} UVLO disables both drivers when V_{DD} is below the specified threshold. The rising V_{DD} threshold is 7V with 0.5V hysteresis. The VHB UVLO disables only the high-side driver when the V_{HB} to V_{HS} differential voltage is below the specified threshold. The V_{HB} UVLO rising threshold is 6.7V with 1.1V hysteresis.

6.3.3 Level Shift

The level shift circuit is the interface from the high-side input to the high-side driver stage which is referenced to the switch node (HS). The level shift allows control of the HO output referenced to the HS pin and provides excellent delay matching with the low-side driver.

6.3.4 Boot Diode

The boot diode necessary to generate the high-side bias is included in the UCC27211A-Q1 family of drivers. The diode anode is connected to V_{DD} and cathode connected to V_{HB}. With the V_{HB} capacitor connected to HB and the HS pins, the V_{HB} capacitor charge is refreshed every switching cycle when HS transitions to ground. The boot diode provides fast recovery times, low diode resistance, and voltage rating margin to allow for efficient and reliable operation.

6.3.5 Output Stages

The output stages are the interface to the power MOSFETs in the power train. High slew rate, low resistance and high peak current capability of both output drivers allow for efficient switching of the power MOSFETs. The low-side output stage is referenced from V_{DD} to V_{SS} and the high side is referenced from V_{HB} to V_{HS}.

6.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See the *Undervoltage Lockout (UVLO)* section for information on UVLO operation mode. In the normal mode the output state is dependent on states of the HI and LI pins. Table 6-2 lists the output states for different input pin combinations.

Table 6-2. Device Logic Table

HI PIN	LI PIN	HO(1)	LO(2)
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H

(1) HO is measured with respect to HS.
(2) LO is measured with respect to VSS.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

To affect fast switching of power devices and reduce associated switching power losses, a powerful gate driver is employed between the PWM output of controllers and the gates of the power semiconductor devices. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation will be often encountered because the PWM signal from the digital controller is often a 3.3V logic signal which cannot effectively turn on a power switch. Level shifting circuitry is needed to boost the 3.3V signal to the gate-drive voltage (such as 12V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power because they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers, and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

Finally, emerging wide band-gap power device technologies such as GaN based switches, which are capable of supporting very high switching frequency operation, are driving very special requirements in terms of gate drive capability. These requirements include operation at low VDD voltages (5V or lower), low propagation delays and availability in compact, low-inductance packages with good thermal capability. Gate-driver devices are extremely important components in switching power, and they combine the benefits of high-performance, low-cost component count and board-space reduction as well as simplified system design.

7.2 Typical Application

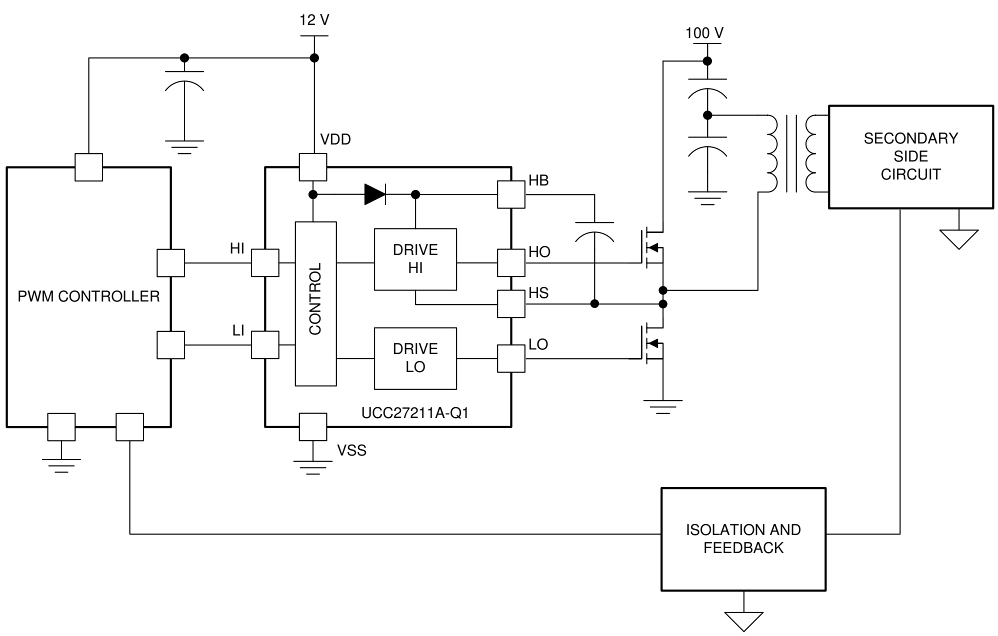


Figure 7-1. UCC27211A-Q1 Typical Application Diagram 1

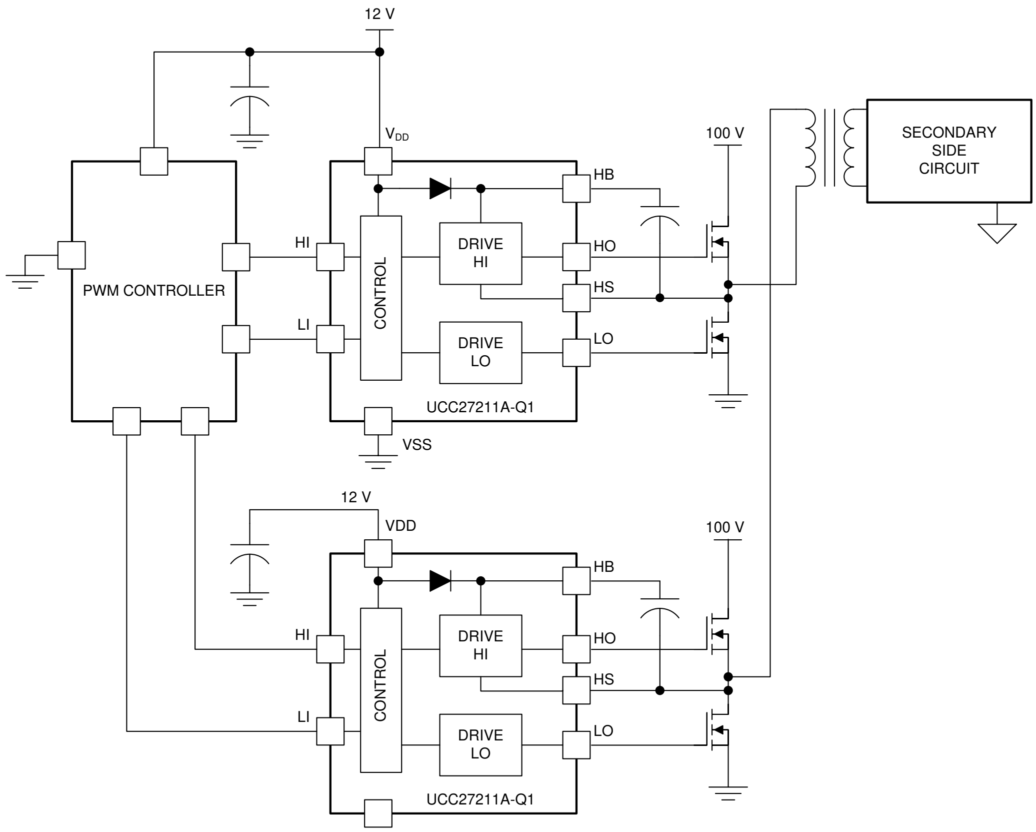


Figure 7-2. UCC27211A-Q1 Typical Application Diagram 2

7.2.1 Design Requirements

For this design example, use the parameters listed in Table 7-1.

Table 7-1. Design Specifications

DESIGN PARAMETER	EXAMPLE VALUE
Supply voltage, VDD	12V
Voltage on HS, VHS	0V to 100V
Voltage on HB, VHB	12V to 112V
Output current rating, IO	–4.5A/3.7A
Operating frequency	500kHz

7.2.2 Detailed Design Procedure

7.2.2.1 Input Threshold Type

The UCC27211A-Q1 device has an input maximum voltage range from –10V to 20V. This increased robustness means that both parts can be directly interfaced to gate drive transformers. The UCC27211A-Q1 device features TTL compatible input threshold logic with wide hysteresis. The threshold voltage levels are low voltage and independent of the VDD supply voltage, which allows compatibility with both logic-level input signals from microcontrollers as well as higher-voltage input signals from analog controllers. See the Electrical Characteristics table for the actual input threshold voltage levels and hysteresis specifications for the UCC27211A-Q1 device.

7.2.2.2 V_{DD} Bias Supply Voltage

The bias supply voltage to be applied to the VDD pin of the device should never exceed the values listed in the Absolute Maximum Ratings table. However, different power switches demand different voltage levels to be applied at the gate terminals for effective turnon and turnoff. With certain power switches, a positive gate voltage may be required for turnon and a negative gate voltage may be required for turnoff, in which case the VDD bias supply equals the voltage differential. With a wide operating range from 8V to 17V, the UCC27211A-Q1 device can be used to drive a variety of power switches, such as Si MOSFETs, IGBTs, and wide-bandgap power semiconductors.

7.2.2.3 Peak Source and Sink Currents

Generally, the switching speed of the power switch during turnon and turnoff should be as fast as possible in order to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds with the targeted power MOSFET. The system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power MOSFET (such as dV_{DS}/dt). For example, the system requirement might state that a SPP20N60C3 power MOSFET must be turned-on with a dV_{DS}/dt of 20V/ns or higher with a DC bus voltage of 400V in a continuous-conduction-mode (CCM) boost PFC-converter application. This type of application is an inductive hard-switching application and reducing switching power losses is critical. This requirement means that the entire drain-to-source voltage swing during power MOSFET turnon event (from 400V in the OFF state to $V_{DS(on)}$ in on state) must be completed in approximately 20ns or less. When the drain-to-source voltage swing occurs, the Miller charge of the power MOSFET (QGD parameter in the SPP20N60C3 data sheet is 33nC typical) is supplied by the peak current of gate driver. According to power MOSFET inductive switching mechanism, the gate-to-source voltage of the power MOSFET at this time is the Miller plateau voltage, which is typically a few volts higher than the threshold voltage of the power MOSFET, $V_{GS(TH)}$.

To achieve the targeted dV_{DS}/dt, the gate driver must be capable of providing the Q_{GD} charge in 20ns or less. In other words a peak current of 1.65A (= 33nC / 20ns) or higher must be provided by the gate driver. The UCC27211A gate driver is capable of providing 4A peak sourcing current which clearly exceeds the design requirement and has the capability to meet the switching speed needed. The 2.4× overdrive capability provides an extra margin against part-to-part variations in the Q_{GD} parameter of the power MOSFET along with additional flexibility to insert external gate resistors and fine tune the switching speed for efficiency versus EMI optimizations. However, in practical designs the parasitic trace inductance in the gate drive circuit of the PCB will have a definitive role to play on the power MOSFET switching speed. The effect of this trace inductance is to limit the dI/dt of the output current pulse of the gate driver. In order to illustrate this, consider output current pulse waveform from the gate driver to be approximated to a triangular profile, where the area under the triangle (½ × I_{PEAK} × time) would equal the total gate charge of the power MOSFET (QG parameter in SPP20N60C3 power MOSFET datasheet = 87nC typical). If the parasitic trace inductance limits the dI/dt then a situation may occur in which the full peak current capability of the gate driver is not fully achieved in the time required to deliver the QG required for the power MOSFET switching. In other words the time parameter in the equation would dominate and the I_{PEAK} value of the current pulse would be much less than the true peak current capability of the device, while the required QG is still delivered. Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver is capable of achieving the targeted switching speed. Thus, placing the gate driver device very close to the power MOSFET and designing a tight gate drive-loop with minimal PCB trace inductance is important to realize the full peak-current capability of the gate driver.

7.2.2.4 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used and the acceptable level of pulse distortion to the system. The UCC27211A-Q1 device features 20ns (typical) propagation delays, which ensures very little pulse distortion and allows operation at very high-frequencies. See the Electrical Characteristics table for the propagation and switching characteristics of the UCC27211A-Q1 device.

7.2.2.5 Power Dissipation

Power dissipation of the gate driver has two portions as shown in Equation 1.

$$P_{DISS} = P_{DC} + P_{SW} \tag{1}$$

Use Equation 2 to calculate the DC portion of the power dissipation (PDC).

$$PDC = I_Q \times V_{DD} \tag{2}$$

where

- I_Q is the quiescent current for the driver.

The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through, and so forth). The UCC27211A-Q1 features very low quiescent currents (less than 0.17mA, refer to the Electrical Characteristics table and contain internal logic to eliminate any shoot-through in the output driver stage. Thus the effect of the PDC on the total power dissipation within the gate driver can be safely assumed to be negligible. The power dissipated in the gate-driver package during switching (PSW) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage VG, which is very close to input bias supply voltage VDD)
- Switching frequency
- Use of external gate resistors. When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly simple. The energy that must be transferred from the bias supply to charge the capacitor is given by Equation 3.

$$EG = ½C_{LOAD} \times V_{DD}{}^2 \tag{3}$$

  – where
  – C_{LOAD} is load capacitor
  – V_{DD} is bias voltage feeding the driver

There is an equal amount of energy dissipated when the capacitor is charged and when it is discharged. This leads to a total power loss given by Equation 4.

$$PG = C_{LOAD} \times V_{DD}{}^2 \times f_{SW} \tag{4}$$

where

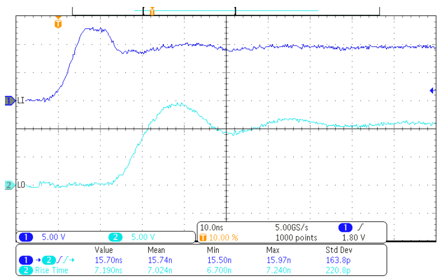
- f_{SW} is the switching frequency

The switching load presented by a power MOSFET/IGBT is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Qg, determine the power that must be dissipated when switching a capacitor which is calculated using the equation $Q_G = C_{LOAD} \times V_{DD}$ to provide Equation 5 for power.

$$P_G = C_{LOAD} \times V_{DD}{}^2 \times f_{SW} = Q_G \times V_{DD} \times f_{SW} \tag{5}$$

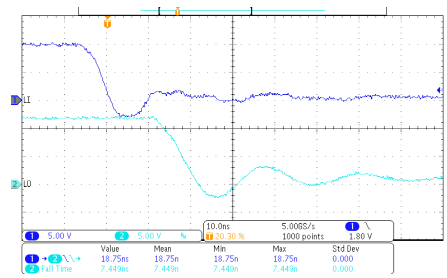
This power P_G is dissipated in the resistive elements of the circuit when the MOSFET/IGBT is being turned on and off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate-drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor.

7.2.3 Application Curves



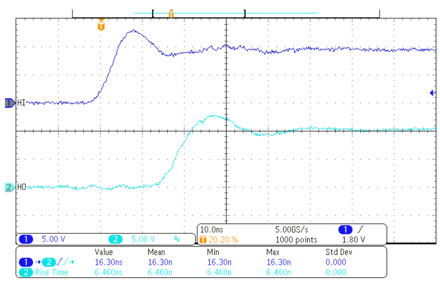
C_L = 1nF V_{DD} = 12 V

Figure 7-3. LO Rise Time and LI to LO Turn-on Propagation Delay



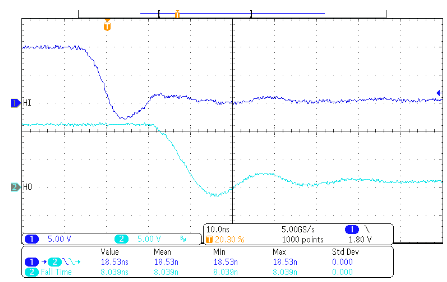
C_L = 1nF V_{DD} = 12 V

Figure 7-4. LO Fall Time and LI to LO Turn-off Propagation Delay



C_L = 1nF V_{DD} = 12 V

Figure 7-5. HO Rise Time and HI to HO Turn-on Propagation Delay



C_L = 1nF V_{DD} = 12 V

Figure 7-6. HO Fall Time and HI to HO Turn-off Propagation Delay

8 Power Supply Recommendations

The bias supply voltage range for which the UCC27211A-Q1 device is recommended to operate is from 8V to 17V. The lower end of this range is governed by the internal undervoltage-lockout (UVLO) protection feature on the V_{DD} pin supply circuit blocks. Whenever the driver is in UVLO condition when the V_{DD} pin voltage is below the $V_{(ON)}$ supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20V absolute maximum voltage rating of the V_{DD} pin of the device (which is a stress rating). Keeping a 3V margin to allow for transient voltage spikes, the maximum recommended voltage for the V_{DD} pin is 17V. The UVLO protection feature also involves a hysteresis function, which means that when the V_{DD} pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification $V_{DD(hys)}$. Therefore, ensuring that, while operating at or near the 8V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown. During system shutdown, the device operation continues until the V_{DD} pin voltage has dropped below the $V_{(OFF)}$ threshold, which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system start-up the device does not begin operation until the V_{DD} pin voltage has exceeded the $V_{(ON)}$ threshold.

The quiescent current consumed by the internal circuit blocks of the device is supplied through the V_{DD} pin. Although this fact is well known, it is important to recognize that the charge for source current pulses delivered by the LO pin is also supplied through the same V_{DD} pin. As a result, every time a current is sourced out of the LO pin, a corresponding current pulse is delivered into the device through the V_{DD} pin. Thus, ensure that a local bypass capacitor is provided between the V_{DD} and GND pins and located as close to the device as possible for the purpose of decoupling is important. A lo-ESR, ceramic surface-mount capacitor is required. TI recommends using a capacitor in the range 0.22µF to 4.7µF between V_{DD} and GND. In a similar manner, the current pulses delivered by the HO pin are sourced from the HB pin. Therefore a 0.022µF to 0.1µF local decoupling capacitor is recommended between the HB and HS pins.

9 Layout

9.1 Layout Guidelines

To improve the switching characteristics and efficiency of a design, the following layout rules must be followed.

- Locate the driver as close as possible to the MOSFETs.
- Locate the V_{DD} – V_{SS} and V_{HB}-V_{HS} (bootstrap) capacitors as close as possible to the device (see Figure 9-1).
- Pay close attention to the GND trace. Use the thermal pad of the DRM package as GND by connecting it to the VSS pin (GND). The GND trace from the driver goes directly to the source of the MOSFET, but must not be in the high current path of the MOSFET drain or source current.
- Use similar rules for the HS node as for GND for the high-side driver.
- For systems using multiple and UCC27211A -Q1 device, TI recommends that dedicated decoupling capacitors be located at V_{DD}-V_{SS} for each device.
- Care must be taken to avoid placing VDD traces close to LO, HS, and HO signals.
- Use wide traces for LO and HO closely following the associated GND or HS traces. A width of 60 to 100mils is preferable where possible.
- Use as least two or more vias if the driver outputs or SW node must be routed from one layer to another. For GND, the number of vias must be a consideration of the thermal pad requirements as well as parasitic inductance.
- Avoid LI and HI (driver input) going close to the HS node or any other high dV/dT traces that can induce significant noise into the relatively high impedance leads.

A poor layout can cause a significant drop in efficiency or system malfunction, and it can even lead to decreased reliability of the whole system.

9.2 Layout Example

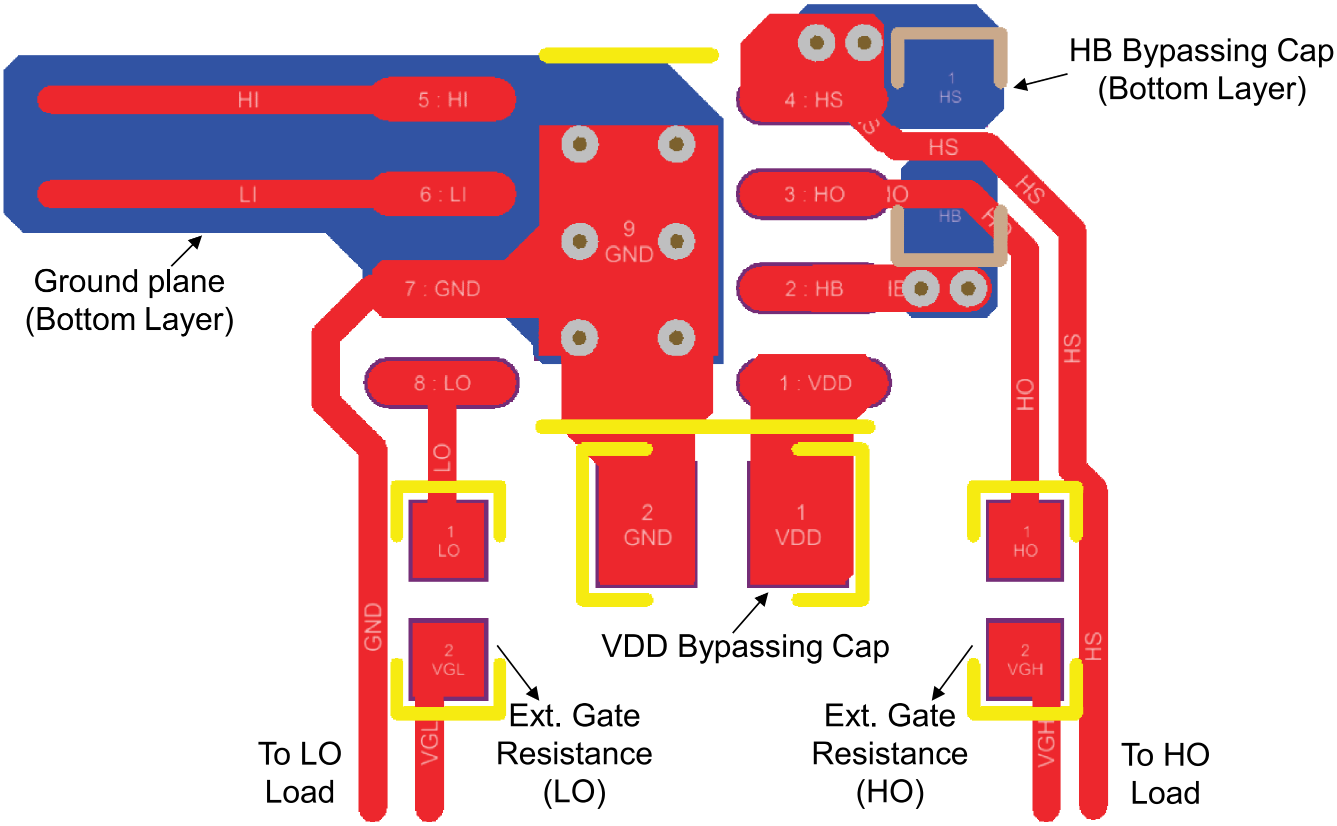


Figure 9-1. UCC27211A-Q1 PCB Layout Example

9.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive-power requirements of the load and the thermal characteristics of the package. For a gate driver to be useful over a particular temperature range, the package must allow for efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package are listed in Thermal Information. For detailed information regarding the table, refer to the Application Note from Texas Instruments entitled *Semiconductor and IC Package Thermal Metrics* (SPRA953). The UCC27211A-Q1 device is offered in an 8-pin SO-PowerPAD package.

10 Device and Documentation Support

10.1 Third-Party Products Disclaimer

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10.2 Documentation Support

10.2.1 Related Documentation

PowerPAD™ Thermally Enhanced Package, Application Report (SLMA002)

PowerPAD™ Made Easy, Application Report (SLMA004)

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

PowerPAD™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (July 2024) to Revision C (September 2025)	Page
• Updated DDA (PowerPad™ SOIC) thermal information	5

12 Mechanical, Packaging, and Orderable Information

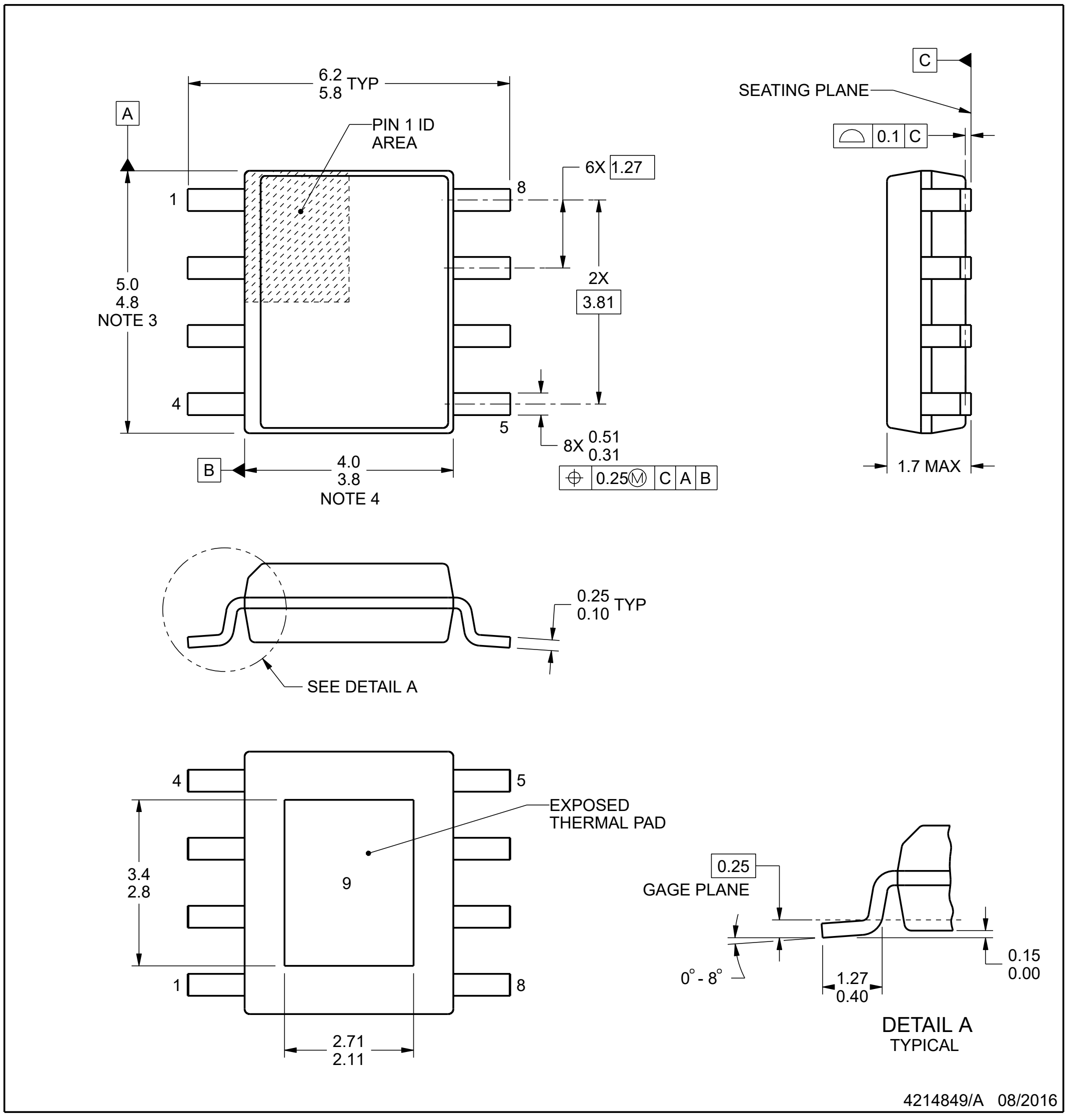
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.

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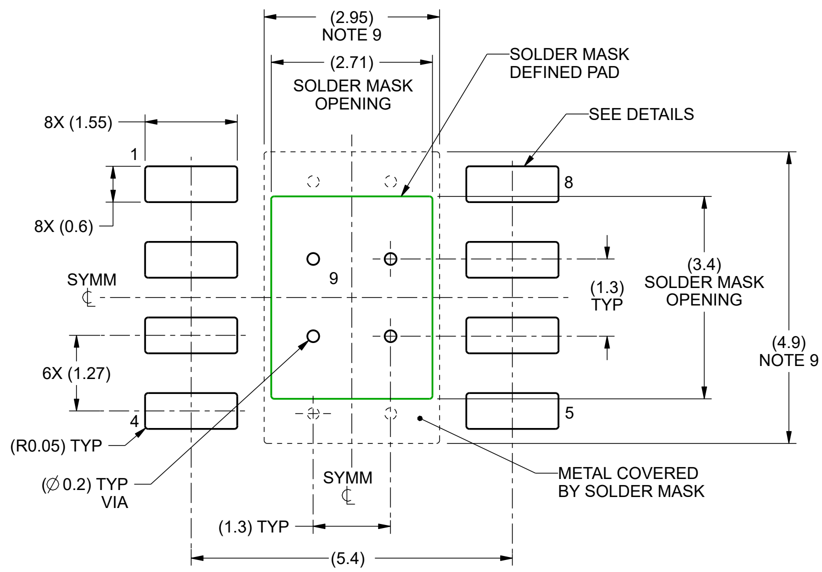
EXAMPLE BOARD LAYOUT

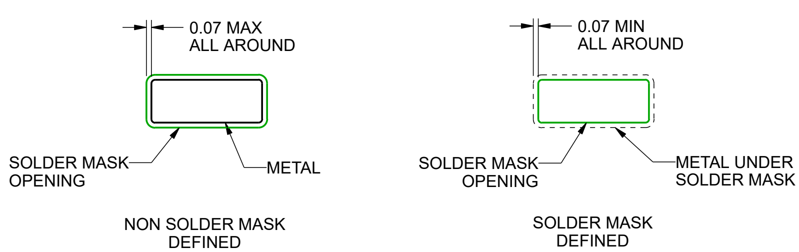
DDA0008B

PowerPAD ™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

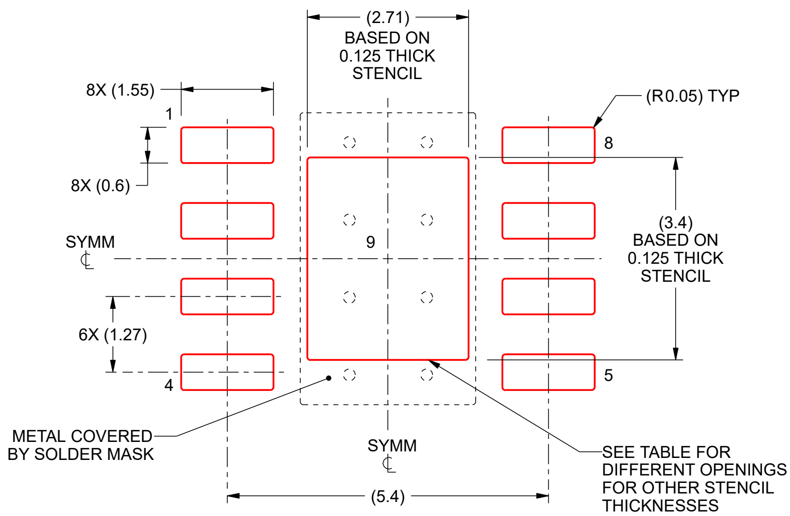
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD ™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC27211AQDDARQ1	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	27211Q
UCC27211AQDDARQ1.A	Active	Production	null (null) |	2500 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	See UCC27211AQDDARQ1	27211Q
UCC27211AQDDARQ1.B	Active	Production	null (null) |	2500 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	See UCC27211AQDDARQ1	27211Q
UCC27211AQDRQ1	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	27211Q
UCC27211AQDRQ1.B	Active	Production	null (null) |	3000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	See UCC27211AQDRQ1	27211Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC27211A-Q1 :

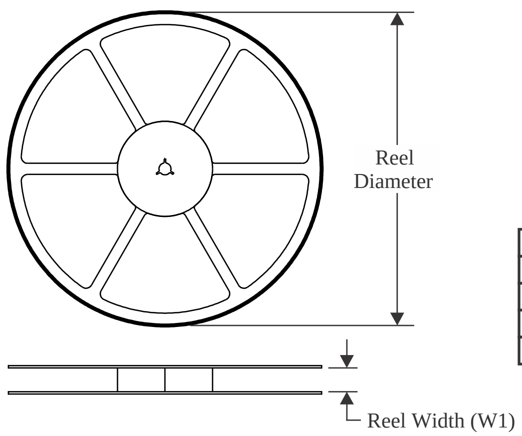
- Catalog : UCC27211A

NOTE: Qualified Version Definitions:

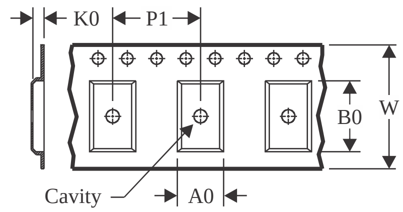
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

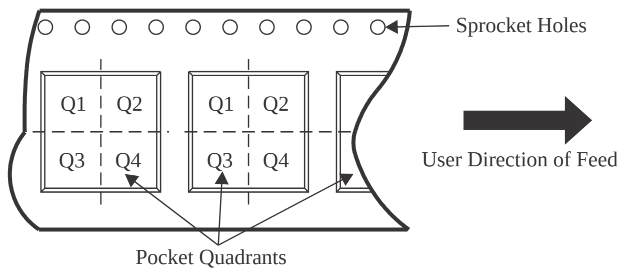


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

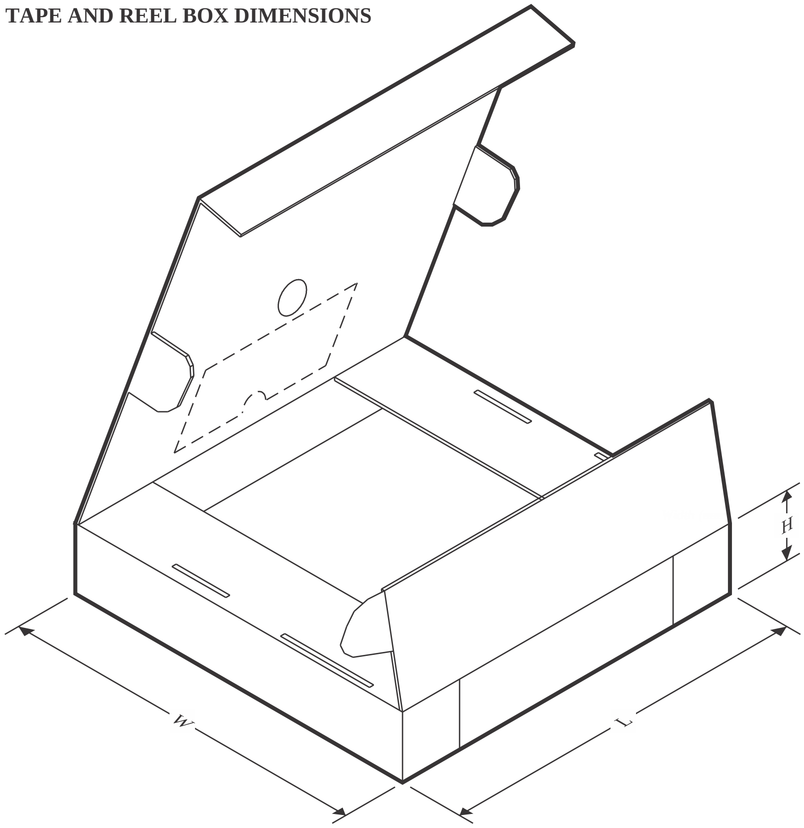
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27211AQDDARQ1	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

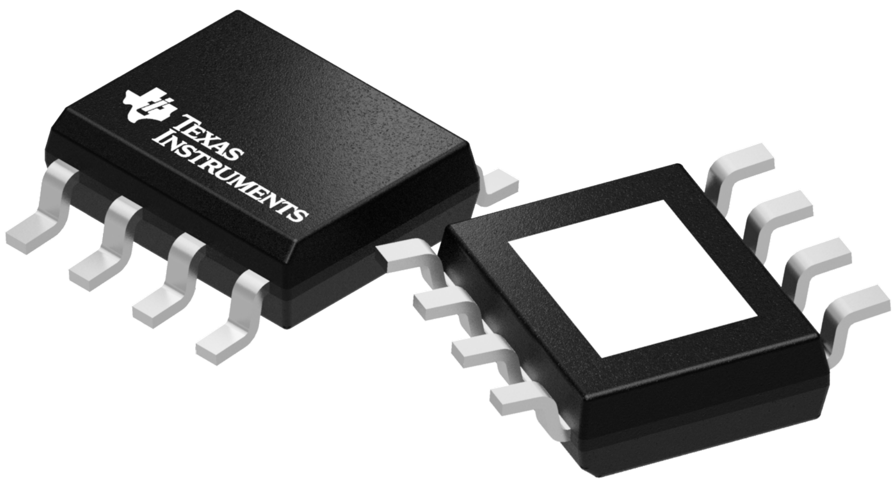


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27211AQDDARQ1	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

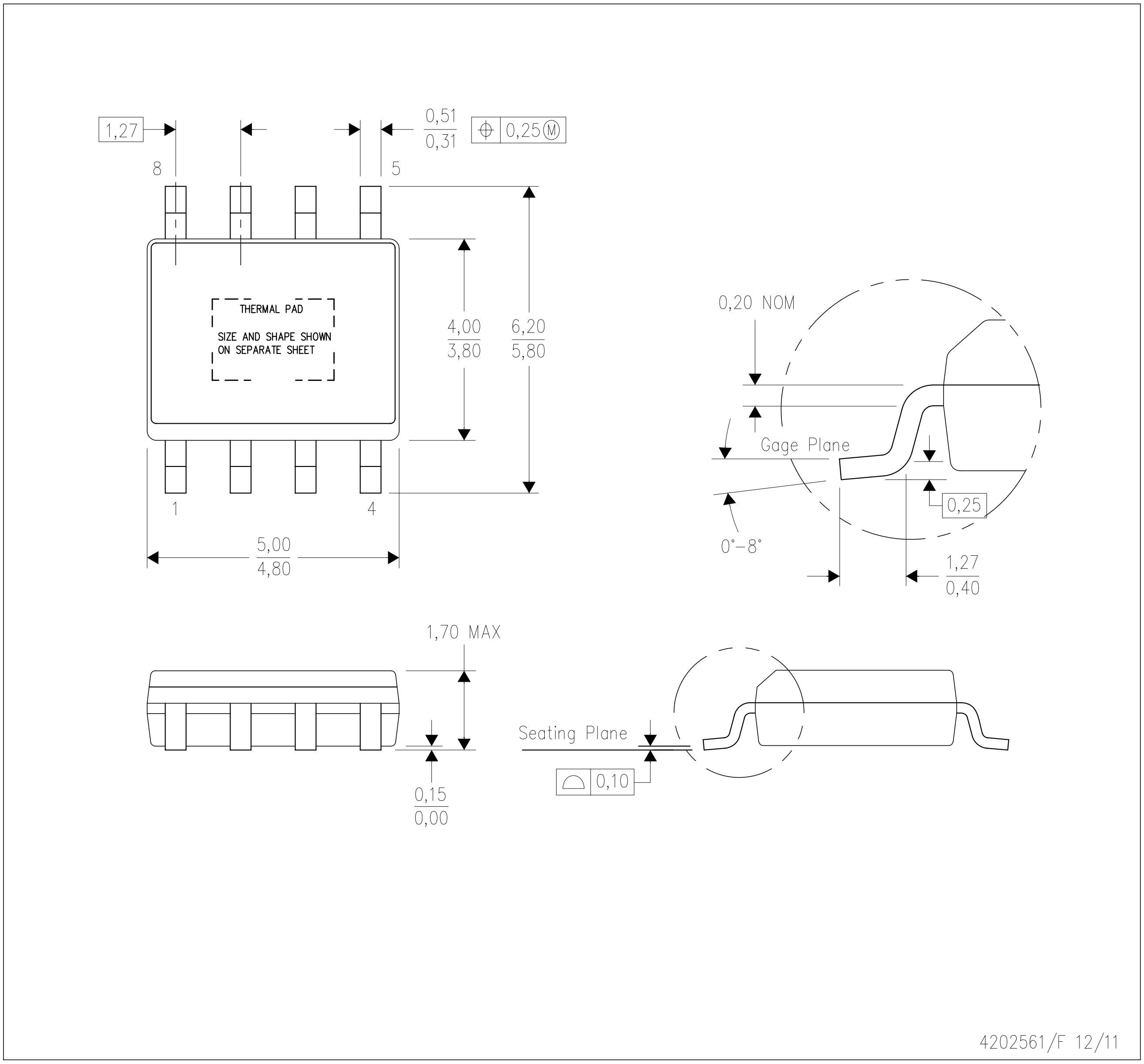
DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. This package complies to JEDEC MS–012 variation BA

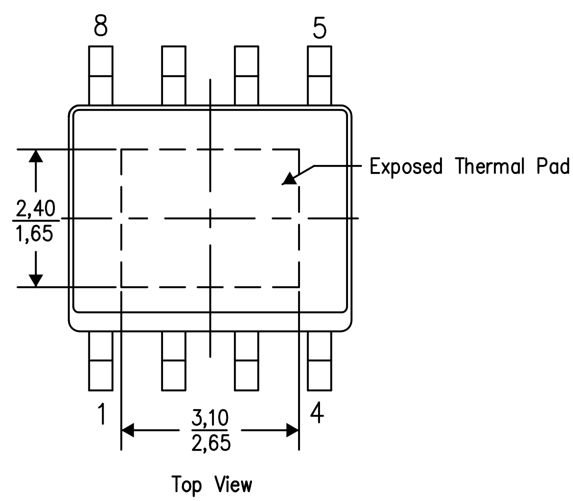
DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206322-6/L 05/12

NOTE: A. All linear dimensions are in millimeters

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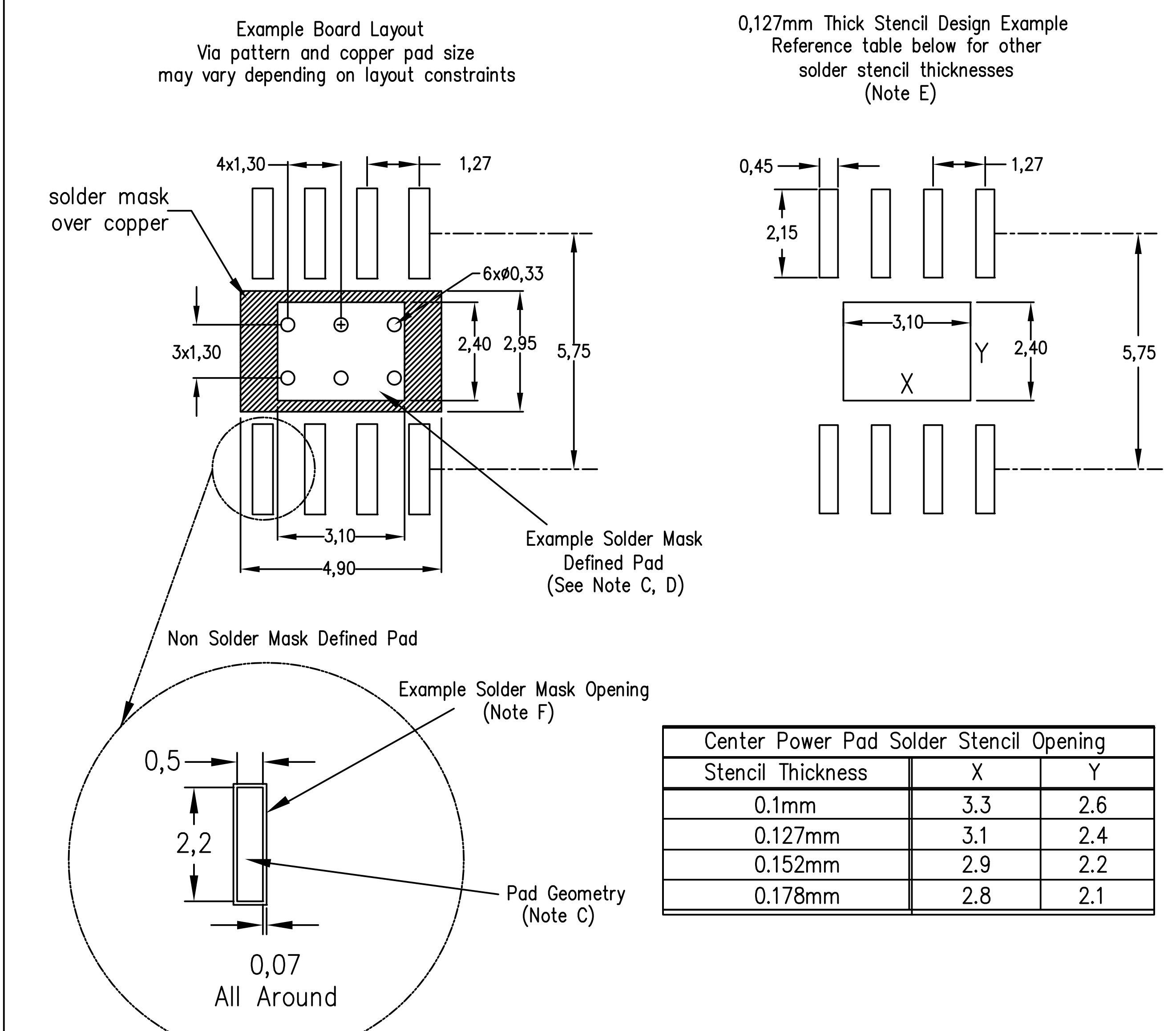
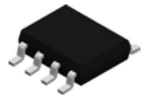
DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE



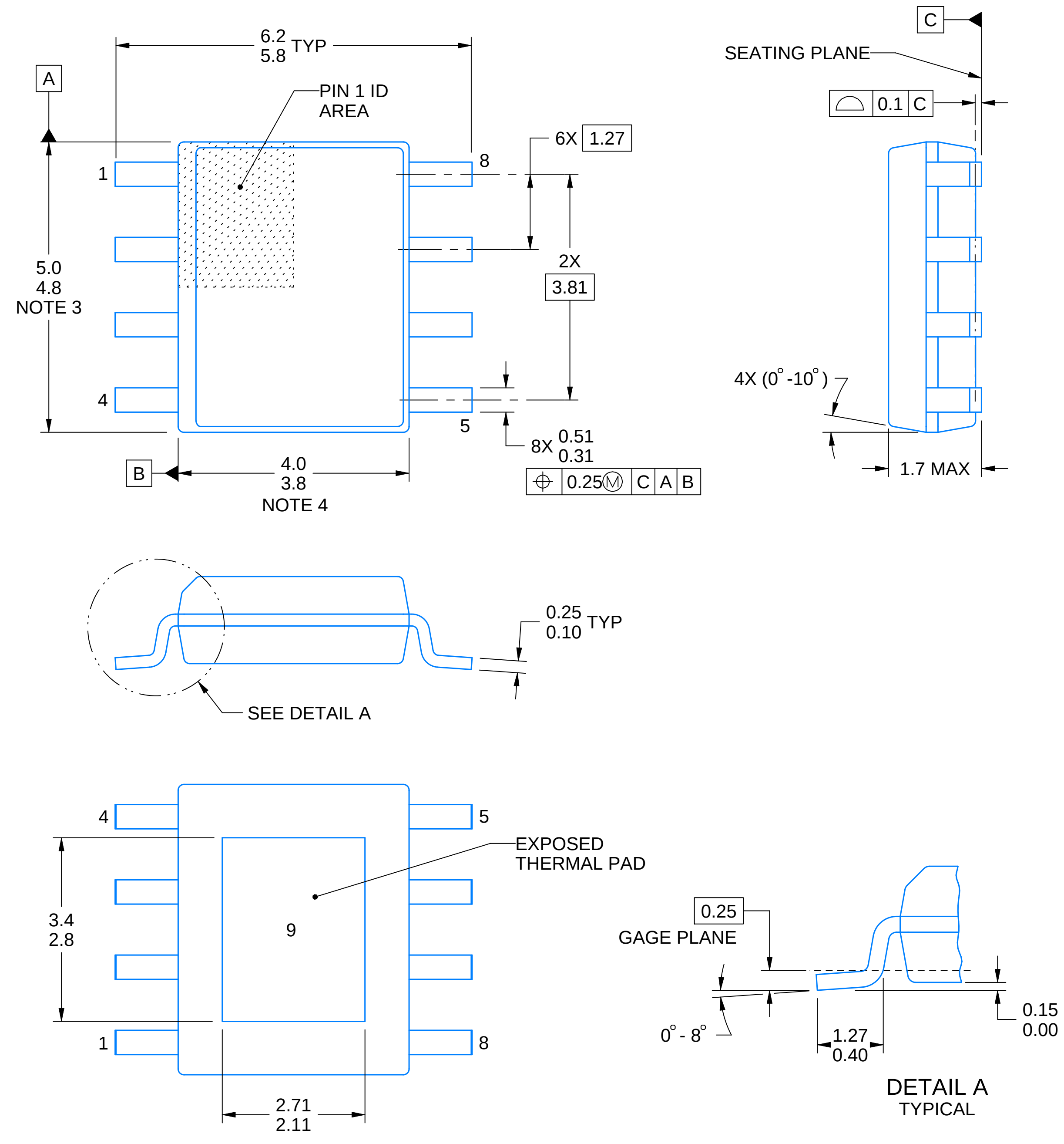
Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

4208951-6/D 04/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PLASTIC SMALL OUTLINE

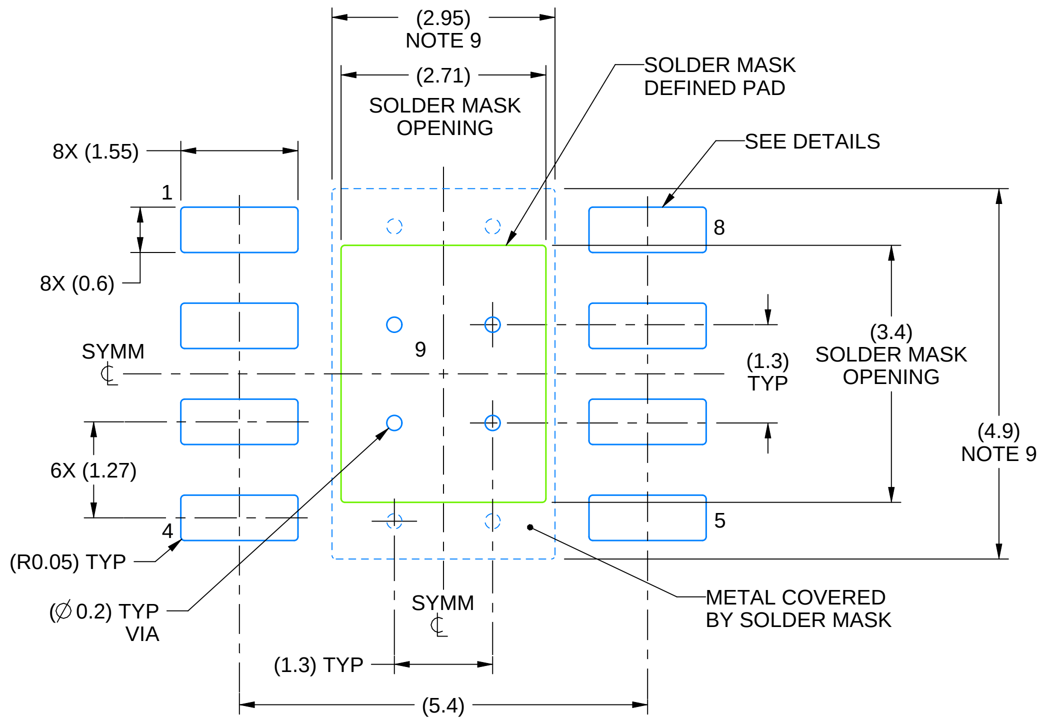


4214849/B 09/2025

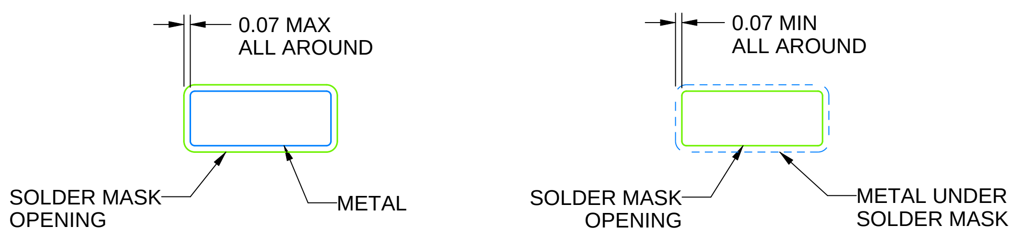
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS
PADS 1-8

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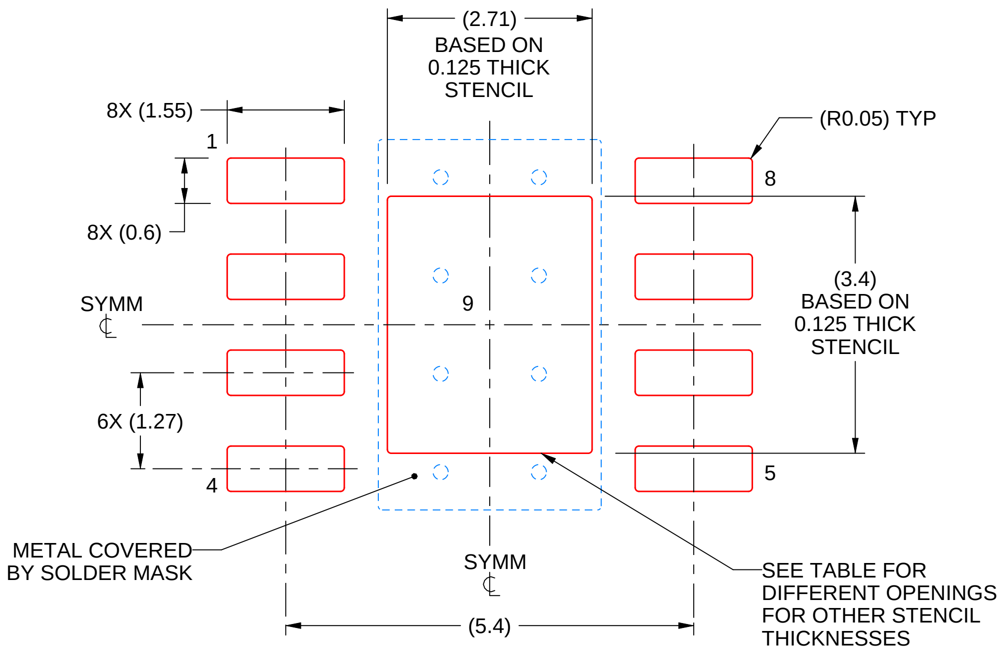
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

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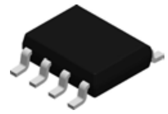
NOTES: (continued)

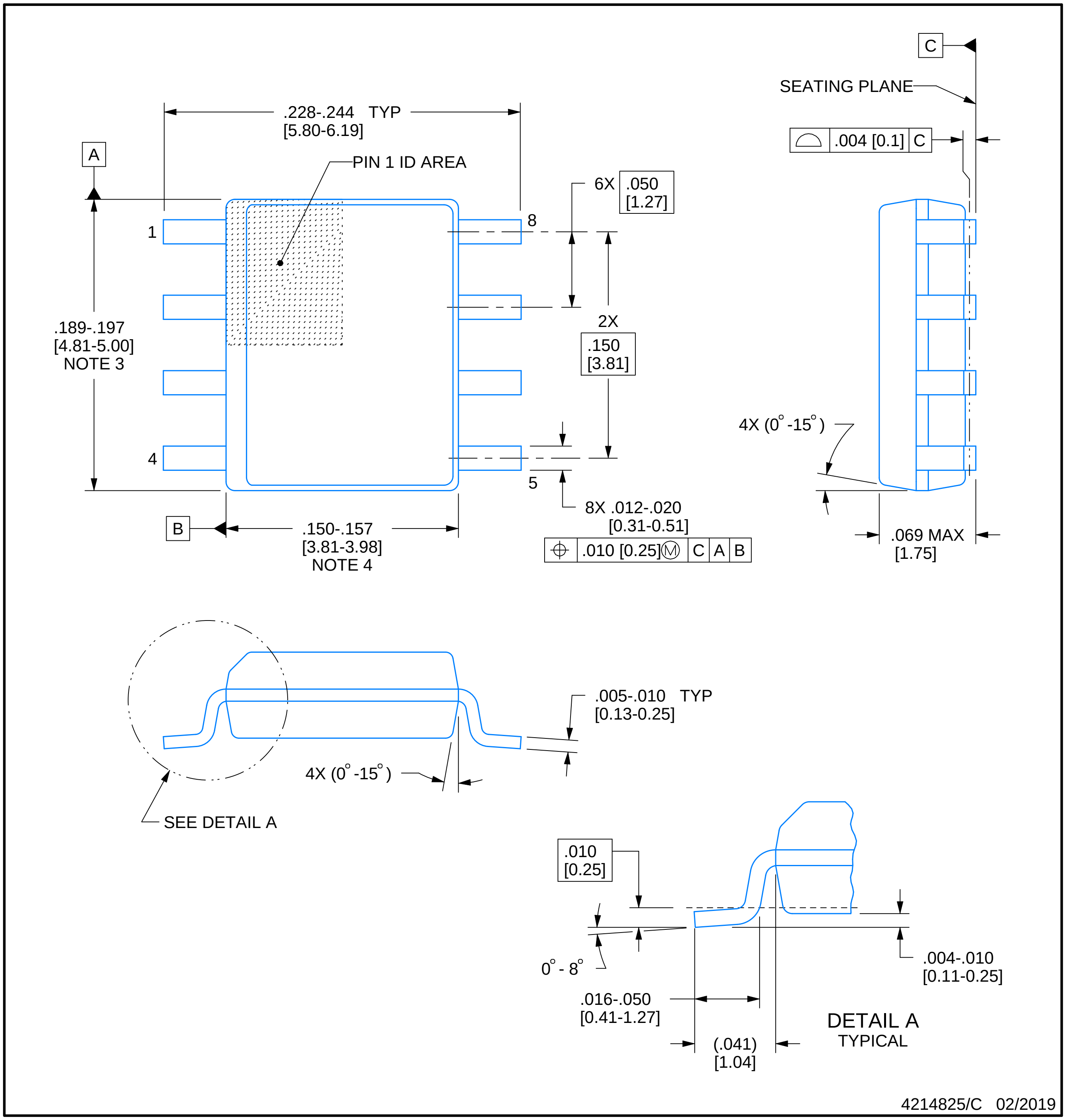
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

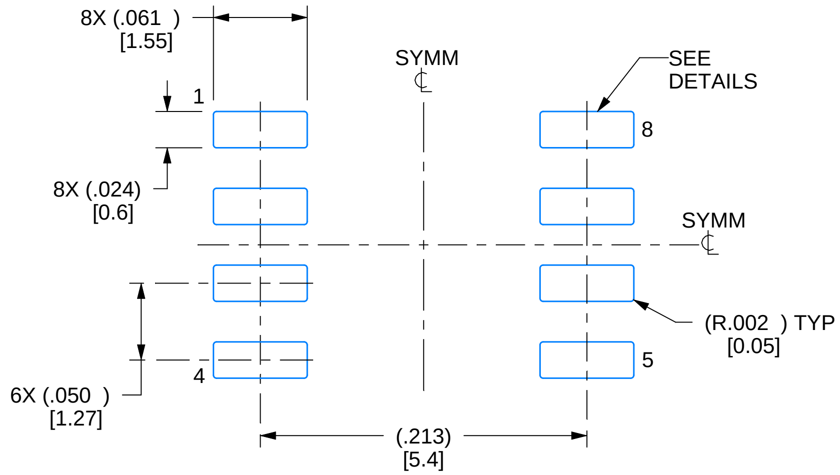
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

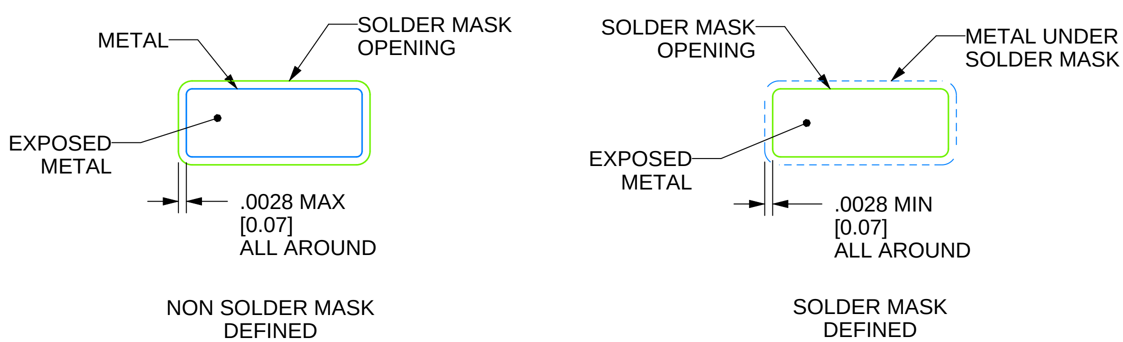


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

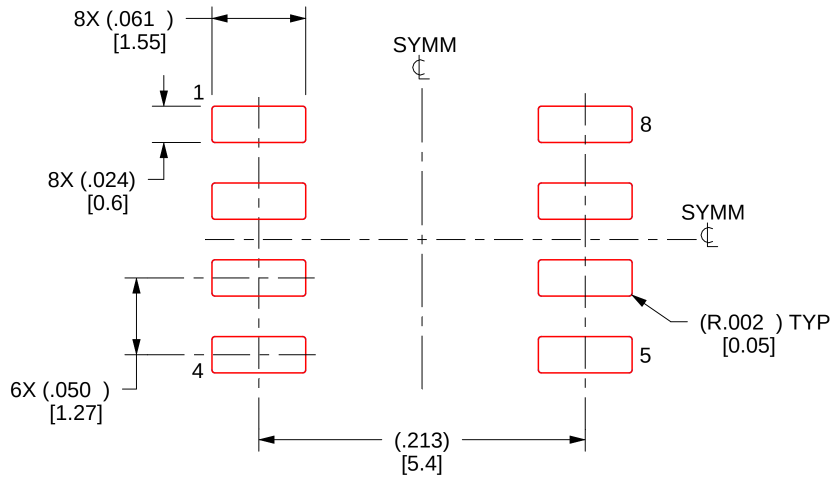


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265