UCC23710 Opto-Input Single Channel Isolated Protection Gate Driver for SiC/IGBT

1 Features

- 5kV$_{RMS}$ single-channel isolated gate driver
- SiC MOSFETs and IGBTs up to 1500V$_{pk}$
- 36V maximum output drive voltage (V$_{DD}$-V$_{EE}$)
- ±5A drive strength
- 300V/ns minimum CMTI
- 250ns response time fast DESAT protection with 9V threshold
- 2.5A internal active Miller clamp
- 200mA soft turn-off during fault conditions
- Alarm $\overline{FLT}$ on overcurrent
- Fault rest mechanism : Reset on PWM input
- 12V V$_{DD}$ UVLO
- 100ns (maximum) propagation delay and 30ns (maximum) pulse/part skew
- SOIC-16DW wide body package with creepage and clearance distance > 8mm
- Operating junction temperature –40°C to 150°C

2 Applications

- AC and brushless DC motor drives
- Industrial inverters and Uninterruptible Power Supply (UPS)
- Building automation and Grid automation

3 Description

The UCC23710 is a galvanic isolated single channel gate driver designed for SiC MOSFETs and IGBTs up to 1500V$_{DC}$ operatng voltage with advanced protection features, best-in-class dynamic performance, and robustness. UCC23710 has up to ±5A peak source and sink current.

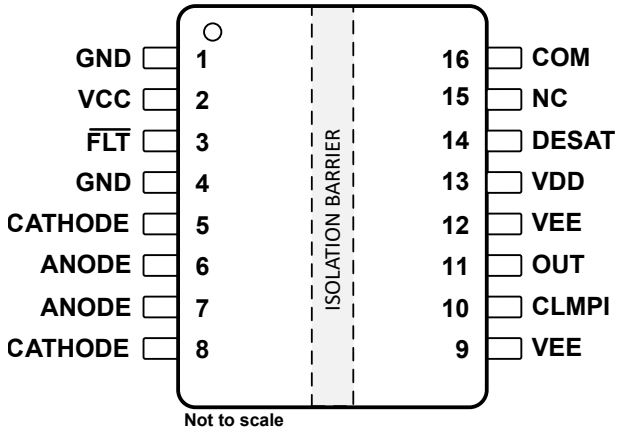
The input side is isolated from the output side with SiO_2 isolation technology, supporting up to 1.5kV$_{PK}$ working voltage, 10kV$_{PK}$ surge immunity, as well as providing low part-to-part skew and >300V/ns common-mode transient immunity.

The UCC23710 includes the state-of-art protection features, such as overcurrent protection with DESAT protection with soft turn-off (STO), active Miller clamp, fault diagnosticsand input and output side power supply UVLO to optimize SiC and IGBT switching behavior and robustness.

Package Information

PART NUMBER	FEATURES	PACKAGE(1)	BODY SIZE (NOM)
UCC23710B	9V DESAT, 12V VDD UVLO, Fault Latch-off	DW (SOIC-16)	10.3mm × 7.5mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Device Pin Configuration

Table of Contents

4 Pin Configuration and Functions

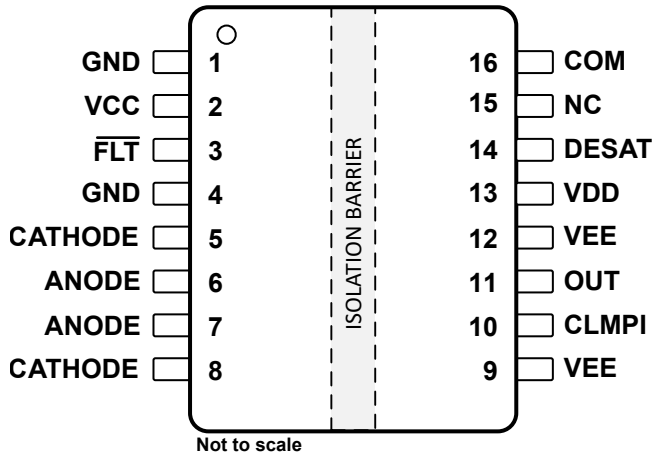


Figure 4-1. UCC23710 DW (SOIC-16) Package Top View

Table 4-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
GND	1,4	P	Input side Ground Rail
VCC	2	P	Input power supply from 3 V to 5.5V. Bypass with a >1µF capacitor to GND. Place decoupling capacitor close to the pin.
$\overline{\text{FLT}}$	3	O	Active low fault alarm output upon DESAT detection. $\overline{\text{FLT}}$ is in open-drain configuration and can be paralleled with other faults.
CATHODE	5,8	I	Cathode
ANODE	6,7	I	Anode
VEE	9,12	P	Negative supply rail for gate drive voltage. Bypass with a >10µF capacitor to COM to support specified gate driver sink peak current capability. Place decoupling capacitor close to the pin.
CLMPI	10	O	Internal Active Miller clamp, connecting this pin directly to the gate of the power transistor. Leave floating or tie to VEE if unused.
OUT	11	O	Gate driver output
VDD	13	P	Positive supply rail for gate drive voltage. Bypass with a >10µF capacitor to COM to support specified gate driver source peak current capability. Place decoupling capacitor close to the pin.
DESAT	14	O	Desaturation current protection input. Tie to COM if unused.
COM	16	P	Common ground reference, connecting to emitter pin for IGBT and source pin for SiC-MOSFET.

(1) P = Power, G = Ground, I = Input, O = Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VCC	VCC - GND	–0.3	6	V
VDD	VDD - COM	–0.3	36	V
VEE	VEE - COM	–17.5	0.3	V
V_{MAX}	VDD - VEE	–0.3	36	V
$I_{F(AVG)}$			25	mA
$I_{F(TRAN)}$ <1US PULSE, 300pps			1	A
$V_{R(MAX)}$	Reverse Input Voltage		5	V
OUT	DC	VEE-0.3	VDD	V
	Transient, less than 100ns(2)	VEE-5.0	VDD+5.0	V
CLMPI	Voltage on CLMPI, reference to VEE	–0.3	VDD	V
DESAT	Voltage on DESAT, reference to COM	–0.3	VDD+0.3	V
$V_{\overline{FLT}}$	$\overline{FLT}$ pin Voltage	–0.3	6	V
$I_{\overline{FLT}}$	$\overline{FLT}$ pin input current		20	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Values are verified by characterization on bench.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VCC	VCC-GND	3	5.5	V
V_{FLT}	VCC-GND	0	5.5	V
VDD	VDD-COM	13	30	V
VEE	VEE-COM	-16	0	V
V_{MAX}	VDD-VEE	-	30	V
I_F(ON)	Input Diode Forward Current (Diode "ON")	5	20	mA
V_F(OFF)	Anode voltage - Cathode voltage (Diode "OFF")	-5	0.8	V
T_A	Ambient temperature	–40	125	°C
T_J	Junction temperature	–40	150	°C

5.4 Thermal Information

THERMAL METRIC[1]		UCC2371X DW (SOIC) 16 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	18.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	36.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	VCC = 5V, VDD-COM = 20V, COM-VEE = 5V, IF(on) = 5mA, 140 kHz, 50% Duty Cycle for 10nF load, Ta = 25℃		720		mW
P_{D1}	Maximum power dissipation by transmitter side	VCC = 5V, VDD-COM = 20V, COM-VEE = 5V, IF(on) = 5mA, 140 kHz, 50% Duty Cycle for 10nF load, Ta = 25℃		20		mW
P_{D2}	Maximum power dissipation by receiver side	VCC = 5V, VDD-COM = 20V, COM-VEE = 5V, IF(on) = 5mA, 140 kHz, 50% Duty Cycle for 10nF load, Ta = 25℃		700		mW

5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
GENERAL				
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	> 8	mm
CPG	External Creepage[1]	Shortest terminal-to-terminal distance across the package surface	> 8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 17	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material Group	According to IEC 60664–1	I	
	Overvoltage Category per IEC 60664–1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN V VDE 0884-10 (VDE V 0884-10): 2016-12				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1500	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test; see Figure 1	1060	V_{RMS}
		DC voltage	1500	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test) V_{TEST}= 1.2 × V_{IOTM}, t = 1 s (100% production test)	7071	V_{PK}
V_{IMP}	Maximum inpulse voltage [2]	Tested in air, 1.2/50-µs waveform per IEC 62368-1	7692	V_{PK}
V_{IOSM}	Maximum surge isolation voltage [3]	Test method per IEC 60065, 1.2/50 µs waveform, V_{TEST} = 1.6 × V_{IOSM} = 11300 V_{PK} (qualification)	10000	V_{PK}

5.6 Insulation Specifications (continued)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
q_{pd}	Apparent charge (4)	Method a: After I/O safety test subgroup 2/3, V_{ini} =V_{IOTM}, tini = 60 s; Vpd(m) = 1.2 × V_{IORM} = 2545 V_{PK}, tm = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1,V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM} = 3394 V_{PK}, tm = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), V_{ini} = V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM} = x V_{PK}, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output (5)	V_{IO} = 0.5 × sin (2πft), f = 1 MHz	~ 1	pF
R_{IO}	Insulation resistance, input to output (5)	V_{IO} = 500 V, T_A = 25°C	≥ 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	≥ 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	≥ 10^9	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} = 5000 V_{RMS}, t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO} = 6000 V_{RMS}, t = 1 s (100% production)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and ribs on the PCB are used to help increase these specifications.
(2) Testing is carried out in air to determine the surge immunity of the package.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

5.7 Safety-Related Certifications

VDE	UL	CQC
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify according to UL 1577 Component Recognition Program	Plan to certify according to GB4943.1
Agency Qualification Planned	Agency Qualification Planned	Agency Qualification Planned

5.8 Safety Limiting Values

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{θJA}$ = 73.6°C/W, VCC = 5V, T_J = 150°C, T_A = 25°C			59	mA
		$R_{θJA}$ = 73.6°C/W, VDD - VEE = 30V, T_J = 150°C, T_A = 25°C			39	
P_S	Safety input, output, or total power	$R_{θJA}$ = 73.6°C/W, T_J = 150°C, T_A = 25°C			900	mW
T_S	Maximum safety temperature(1)				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J , specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A. The junction-to-air thermal resistance, R_{qJA}, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter: T_J = T_A + R_{qJA} ´ P, where P is the power dissipated in the device. $T_{J(max)}$ = T_S = T_A + R_{qJA} ´ P_S, where $T_{J(max)}$ is the maximum allowed junction temperature. P_S = I_S ´ V_I , where VI is the maximum supply voltage.

5.9 Electrical Characteristics

VCC = 3.3 V or 5.0 V, 1-µF capacitor from VCC to GND, VDD - COM = 20 V, 18 V or 15V, COM - VEE = 0 V, 5 V, 8 V or 15V, C_L = 100 pF, -40°C < T_J < 150°C (unless otherwise noted)(1) (2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT STAGE						
I_{FLH}	Low to High Input Forward Current Threshold	V_{DD}-V_{EE} = 15 V		1	2.7	mA
I_{F_HYS}	Input Forward Current Hysteresis	V_{DD}-V_{EE} = 15 V		0.3		mA
V_F	Input Forward Voltage	I_F = 10 mA	1.4	1.7	2	V
$\Delta V_F/\Delta T$	Input Forward Voltage Temp. Coefficient	I_F = 10 mA		0.7		mV/°C
V_R	Input Reverese Breakdown Voltage	I_R = 10 uA	6			V
C_{IN}	Input Capacitance	f_s = 0.5 MHz, +/- 250 mV		4		pF
POWER SUPPLY QUIESCENT CURRENT						
I_{VCCQ}	VCC quiescent current	OUT = High, f_s = 0 Hz	1		2	mA
		OUT = Low, f_s = 0 Hz	1		2	mA
I_{VDDQ}	VDD quiescent current	OUT = High, f_s = 0 Hz	1	2.3	4	mA
		OUT = Low, f_s = 0 Hz	1	2.0	3	mA
I_{VEEQ}	VEE quiescent current	OUT = High, f_s = 0 Hz, COM-VEE=5V		-1.8		mA
		OUT = Low, f_s = 0 Hz, COM-VEE=5V		-1.5		mA
POWER SUPPLY PROTECTION						
$V_{VDD\_UVLO\_ON}$	VDD UVLO rising threshold	VDD-COM	11.4	12	12.6	V
$V_{VDD\_UVLO\_OFF}$	VDD UVLO falling threshold	VDD-COM	10.45	11	11.55	V
V_{VDD_HYST}	VDD UVLO hysteresis for 12V UVLO			1.1		V
t_{VDDFIL}	VDD UVLO deglitch time			5		µs
$t_{VDD+ \text{ to OUT}}$	VDD UVLO on delay to output high	IF(on) = 5mA	2	4.6	7	µs
$t_{VDD- \text{ to OUT}}$	VDD UVLO on delay to output low			5.4	8.5	µs
GATE DRIVER STAGE						
I_{OUT}	Peak source current	C_L = 0.22µF, f_S = 1kHz		5		A
I_{OUT}	Peak sink current	C_L = 0.22µF, f_S = 1kHz		5		A
R_{OUTH}	Output pull-up resistance	IOH = 1A, C_L=220nF, Fsw = 1khz		0.7		Ω
R_{OUTL}	Output pull-down resistance	IOL = -1A, C_L=220nF, Fsw = 1khz		0.7		Ω
ACTIVE PULLDOWN						
V_{OUTPD}	Output active pull down on OUT	I_{OUT} = 0.1×$I_{OUT(typ)}$, VDD=OPEN, VEE=COM	1.4	2.0	2.5	V
INTERNAL MILLER CLAMP						
V_{CLMPTH}	Miller clamp threshold voltage	Reference to VEE	1.5	2.1	2.5	V
V_{CLMPI}	Output low clamp voltage	I_{CLMPI} = 20 mA		16		mV
I_{CLMPI}	Output low clamp current	V_{CLMPI} = 0V, VEE = –2.5V		2.3		A
R_{CLMPI}	Miller clamp pull down resistance	I_{CLMPI} = 0.2A		0.8		Ω
t_{DCLMPI}	Miller clamp ON delay time	C_L = 1.8nF		38	50	ns
SHORT CIRCUIT CLAMPING						
V_{OUT_CLMP}	V_{OUT} - V_{DD}	OUT = High, I_{OUT} = 500mA, t_{CLP}=10us		0.8		V
DESAT PROTECTION						
I_{CHG}	Blanking capacitor charge current	V_{DESAT} = 2.0V	210	250	297	µA
I_{DCHG}	Blanking capacitor discharge current	V_{DESAT} = 6.0V (for $V_{DESATTH}$ > 6.5) V_{DESAT} = 5.0V (for $V_{DESATTH}$ = 6.5)	25	40		mA
$V_{DESATTH}$	Detection threshold		8.4	9	9.6	V

5.9 Electrical Characteristics (continued)

VCC = 3.3 V or 5.0 V, 1-µF capacitor from VCC to GND, VDD - COM = 20 V, 18 V or 15V, COM - VEE = 0 V, 5 V, 8 V or 15V, C_L = 100 pF, -40℃ < T_J < 150℃ (unless otherwise noted)(1) (2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{DESATLEB}$	Leading edge blank time		320	470	540	ns
$t_{DESATFIL}$	DESAT deglitch filter		100	180	260	ns
$t_{DESATOFF}$	DESAT propagation delay to OUT 90%	V_{DESAT}>$V_{DESATTH}$		200		ns
$t_{DESATFLT}$	DESAT to $\overline{FLT}$ low delay			260		ns
SOFT TURN OFF						
I_{STO}	Internal Soft Turn Off Current	V_{OUT}=8V, C_L = 0.18µF, f_S = 1kHz,		0.25		A
FAULT REPORTING ($\overline{FLT}$)						
t_{FLT_RST}	Fault flag clear time after device reset	From IF rising to Fault clearing		60		ns
$t_{FLTMUTE}$	Output mute time on overcurrent fault			22		us
R_{ODON}	Open drain output on resistance	I_{ODON} = 5mA		8.8		Ω
V_{FLT_OD}	Open drain low output voltage				0.15xV_{CC}	V
COMMON MODE TRANSIENT IMMUNITY						
CMTI	Common-mode Transient Immunity(3)	V_{CM} = 1200 V	300			V/ns

(1) Currents are positive into and negative out of the specified terminal.
(2) All voltages are referenced to COM unless otherwise noted
(3) For best CMTI performance, it is recommended to use a single resistor to the Anode pin, and connecting Cathode pin directly to GND.

5.10 Switching Characteristics

VCC = 5.0 V, 1-µF capacitor from VCC to GND, VDD - COM = 20V, 18V or 15V, COM - VEE = 3 V, 5 V or 8 V, C_L = 100pF, -40℃<T_J<150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PDLH}	Propagation delay time low-to-high				150	ns
t_{PDHL}	Propagation delay time low-to-high				150	ns
PWD	Pulse width distortion (t_{PDHL}-t_{PDLH})				30	ns
t_{sk-pp}	Part to part skew	Rising or falling propagation delay			30	ns
t_r	Driver output rise time	C_L = 1.8nF		15		ns
t_f	Driver output fall time	C_L = 1.8nF		15		ns
f_{MAX}	Maximum switching frequency				1000	kHz

5.11 Typical Characteristics

OUT = Open

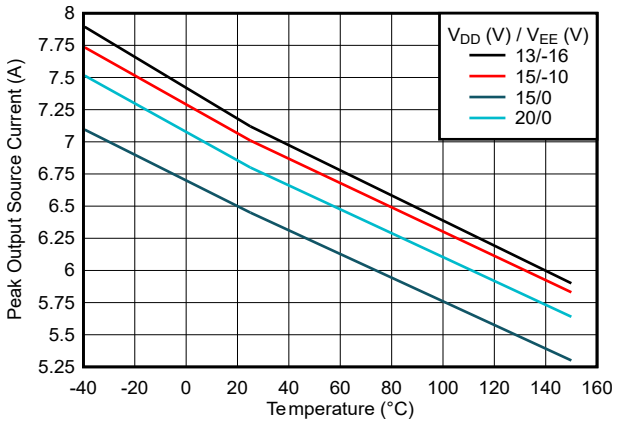


Figure 5-1. Output High Drive Current vs Temperature

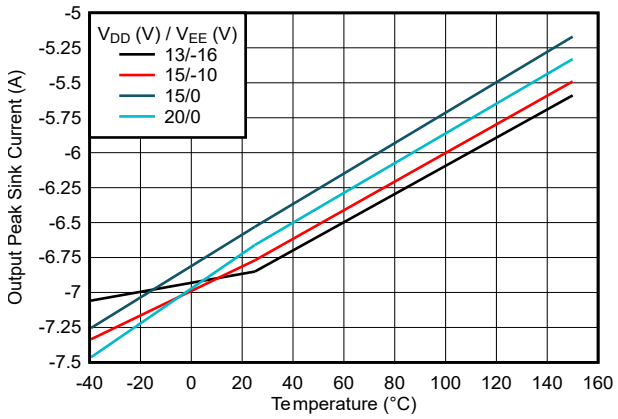


Figure 5-2. Output Low Driver Current vs Temperature

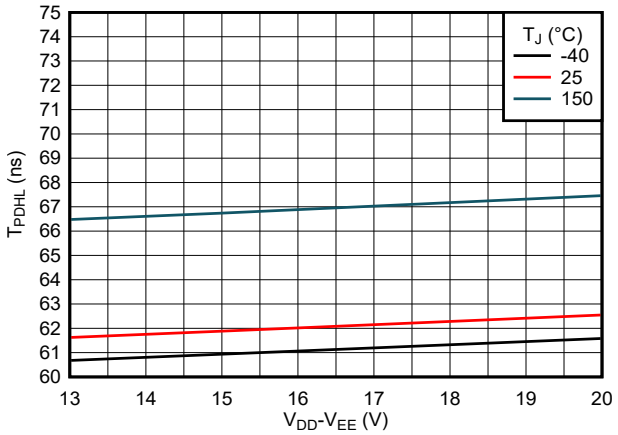


Figure 5-3. Propagation Delay t_{PDHL} vs Temperature

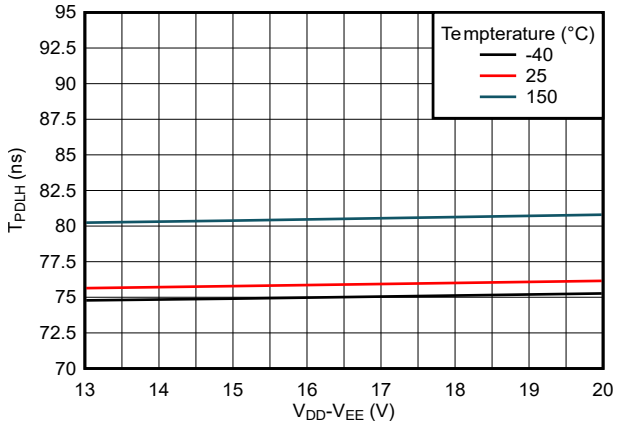


Figure 5-4. Propagation Delay t_{PDLH} vs Temperature

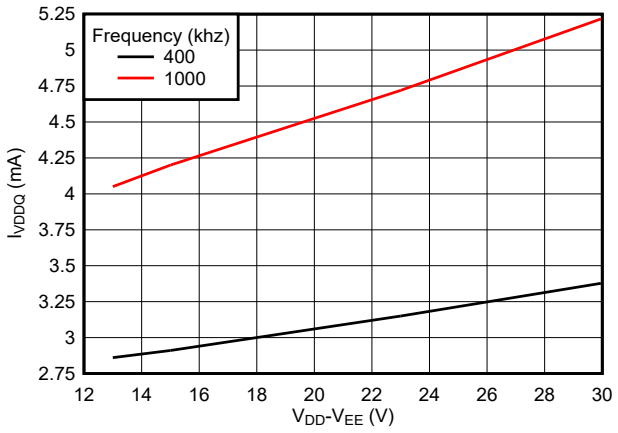


Figure 5-5. I_{VCCQ} Supply Current vs Input Frequency

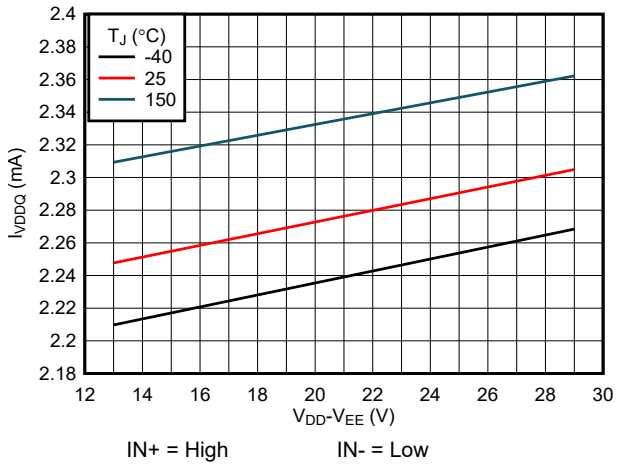


Figure 5-6. I_{VDDQ} Supply Current vs Temperature

5.11 Typical Characteristics (continued)

OUT = Open

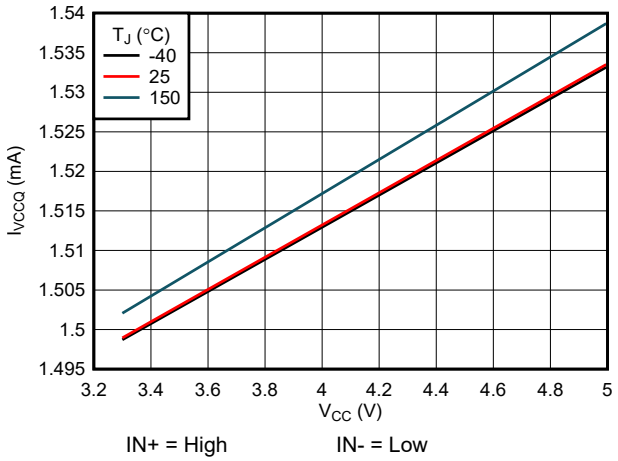


Figure 5-7. I_{VCCQ} Supply Current vs Temperature

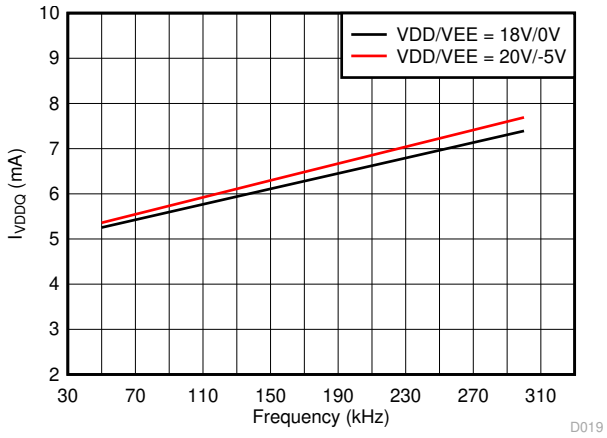


Figure 5-8. I_{VEEQ} Supply Current vs Input Frequency

6 Detailed Description

6.1 Overview

The device is an advanced isolated gate driver, incorporating protection and sensing features, specifically designed for use with silicon carbide (SiC) MOSFETs and insulated gate bipolar transistors (IGBTs). The device is capable of supporting operating voltages of up to 1500 V_{DC}, based on SiC MOSFETs and IGBTs, and is suitable for applications exceeding 10 kW, including motor drives, on-board and off-board battery chargers, solar inverters, and other high-power systems.

The device features galvanic isolation, implemented through magnetic isolation technology, which provides a reliable and reinforced isolation barrier between the low-voltage digital signal processor/microcontroller (DSP/MCU) and the high-voltage side. This isolation technology enables the device to support working voltages of up to 1.5-kV_{DC} peak and surge immunity of up to 10-kV_{peak}.

The device is capable of delivering a peak sink and source current of ±5 A, allowing it to drive SiC MOSFET modules and IGBT modules directly, without the need for an additional buffer stage. Furthermore, the device can be used to drive higher power modules or parallel modules, with the addition of an external buffer stage.

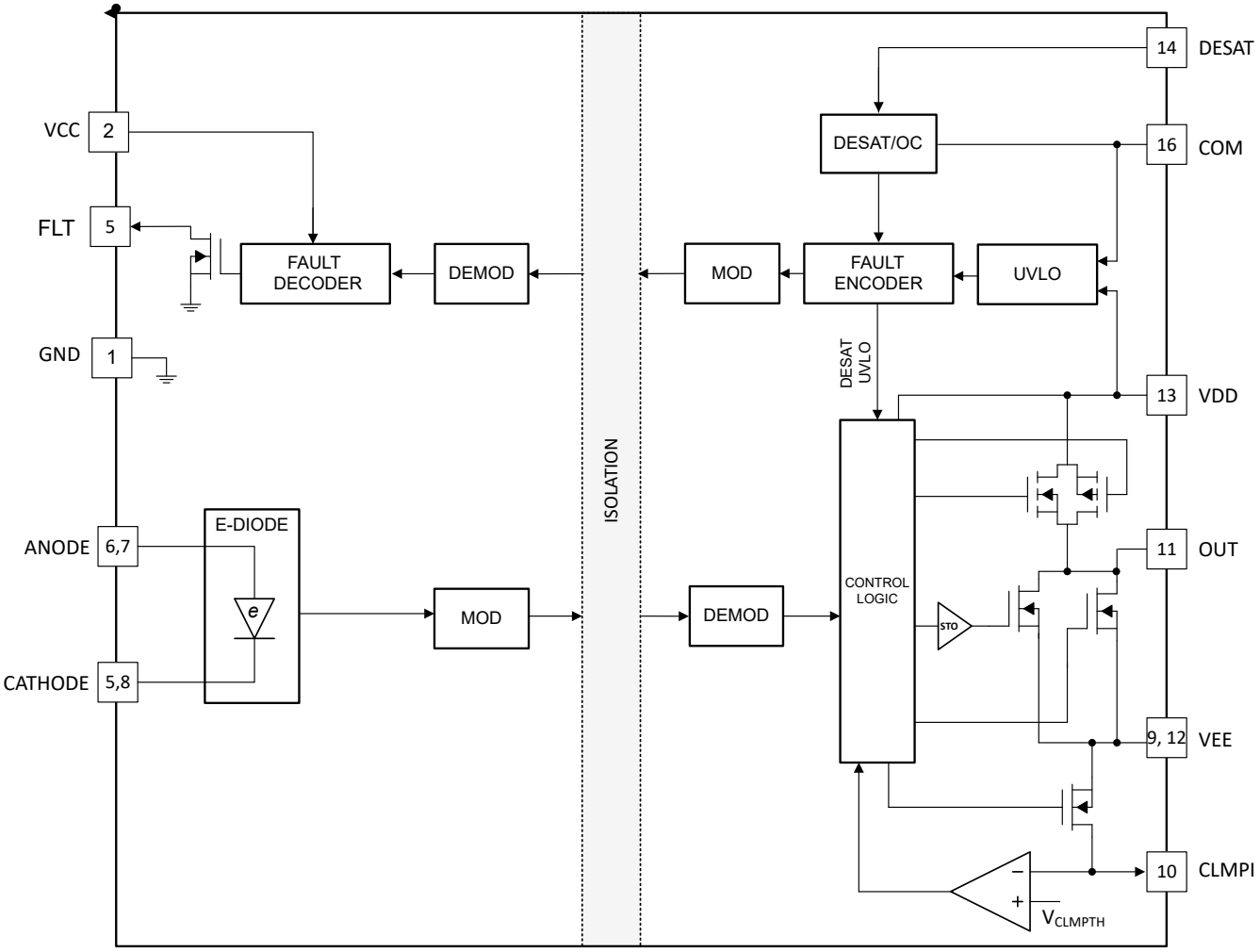
The input side of the device is isolated from the output side, with a reinforced isolation barrier based on magnetic isolation technology. The device's strong drive strength enables fast switching speeds, reducing switching losses, while its minimum common-mode transient immunity (CMTI) of 300 V/ns ensures the reliability of the system, even at high switching speeds. The device's small propagation delay and part-to-part skew minimize the deadtime setting, reducing conduction losses.

The device includes an extensive range of protection and monitoring features, designed to increase the reliability and robustness of SiC MOSFET and IGBT based systems. These features include an output side power supply undervoltage lockout (UVLO), suitable for switches with gate voltages ≥ 15 V, as well as an active Miller clamp feature, which prevents false turn-on caused by Miller capacitance during fast switching.

The device also features state-of-the-art desaturation (DESAT) detection, with a fast detection time, and a fault reporting function to the low-voltage side DSP/MCU. In the event of a DESAT fault, the device triggers a soft turn-off, minimizing short-circuit energy and reducing overshoot voltage on the switches. These advanced protection and monitoring features ensure the reliable operation of SiC MOSFET and IGBT based systems, while minimizing the risk of damage or malfunction.

6.2 Functional Block Diagram

Functional Block Diagram



6.3 Feature Description

6.3.1 Power Supplies

The input-side power supply VCC can support a wide voltage range from 3 V to 5.5 V to support both 3.3-V and 5-V controller signaling.

The output-side power supply, VDD to VEE, can support a wide range up to 30 V. The minimum VDD to VEE voltage will depend on the VDD UVLO variant being used. The device can support either unipolar or bipolar supplies. The negative power supply, VEE, with respect to source or emitter, COM, is usually adopted to avoid false turn on when the other switch in the phase leg is turned on. Negative voltage is important for SiC MOSFETs due to their fast switching speeds, as well as for IGBTs when not using an active Miller clamp. VDD is monitored by undervoltage comparators to enure valid operation. See Section 6.3.2 for more information about the VDD undervoltage lockout protections.

6.3.2 VDD Undervoltage Lockout (UVLO)

The UCC23710 implements UVLO protection features VDD. When the supply voltage is lower than the threshold voltage, the driver output is held low. The driver output will enable onece V_{DD}-COM>$V_{VDD\_UVLO\_ON}$. The UVLO protection feature not only reduces the power consumption of the driver itself during low voltage power supply conditions, but also increases the efficiency of the power stage. For SiC MOSFETs and IGBTs, the on-resistance

reduces while the gate-source voltage or gate-emitter voltage increases. If the power semiconductor is turned on with a low VDD value, the conduction loss increases significantly and can lead to a thermal issue and efficiency reduction of the power stage.

The UVLO protection blocks feature comparator thresholds with hysteresis and deglitch filters on the inputs to help improve noise immunity of the power supply. During the turn-on and turn-off switching transients, the driver sources and sinks a peak transient current from the power supply, which can result in sudden voltage drop of the power supply. With hysteresis and UVLO deglitch filters, the internal UVLO protection blocks will ignore small noises during the normal switching transients.

Timing digrams of the UVLO protection feature of VCC and VDD are shown in Figure 6-1.

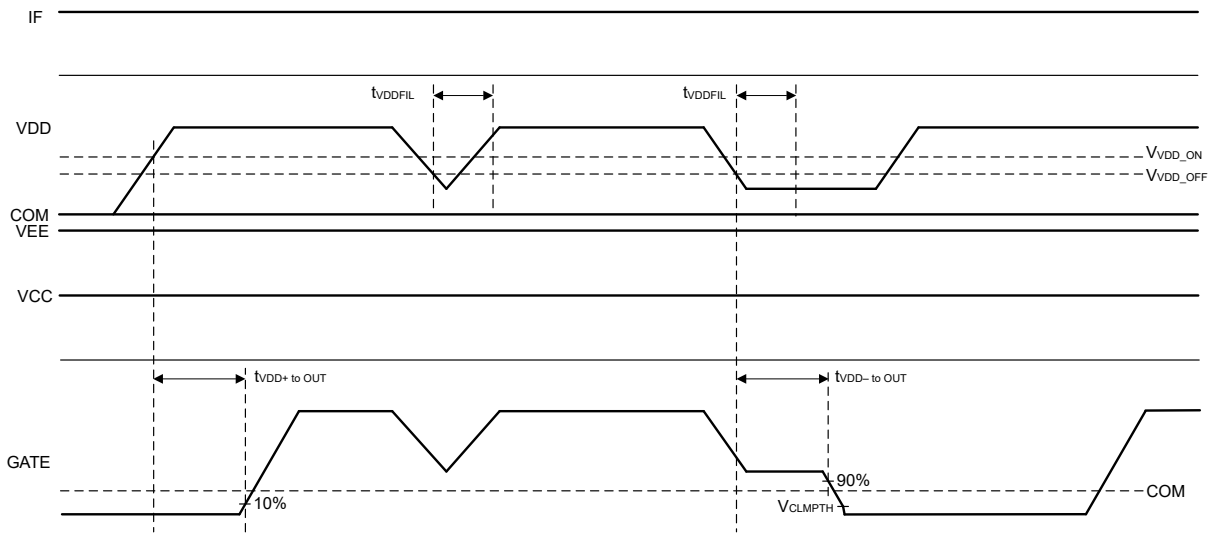


Figure 6-1. VDD Protection Timing Diagram

6.3.3 Opto-Emulated Input

The input stage of UCC23710 integrates a diode emulator(e-diode) interfacing through its Anode and Cathode. When the e-diode is forward biased by applying a positive voltage to the Anode with respect to the Cathode, a forward current I_F flows into the e-diode. The forward voltage drop across the e-diode is 1.7V (typ). An external resistor on the Anode should be used to limit the forward current. When IF exceeds the threshold current I_{FLH} (1mA typ.), a high frequency signal is transmitted across the isolation barrier that is then detected by the receiver and V_{OUT} is driven high. The dynamic impedance of the e-diode is very small(<1.0Ω) and the temperature coefficient of the e-diode forward voltage drop is 0.7mV/°C typically. This leads to excellent stability of the forward current I_F across all operating conditions. If the Anode voltage drops below V_{F_HL} (0.8V), or reverse biased, the gate driver output is driven low.The recommended range for the forward current is 5mA to 20mA.

The reverse breakdown voltage of the e-diode is ~6V . For normal operation, a reverse bias of up to 5V is allowed. The large reverse breakdown voltage of the e-diode enables UCC23710 to be operated in interlock architecture. The system designer has the flexibility to choose a 3.3V or 5.0V signal source to drive the input stage of UCC23710 using an appropriate input resistor. Interlock architecture prevents both the e-diodes from being "ON" at the same time, preventing shoot through in the IGBTs. It also ensures that if both PWM signals are erroneously stuck high (or low) simultaneously, both gate driver outputs will be driven low.

For best noise immunity performance, it is recommended to place the current limiting resistor connected to the anode. Cathode should be connected directly to ground.

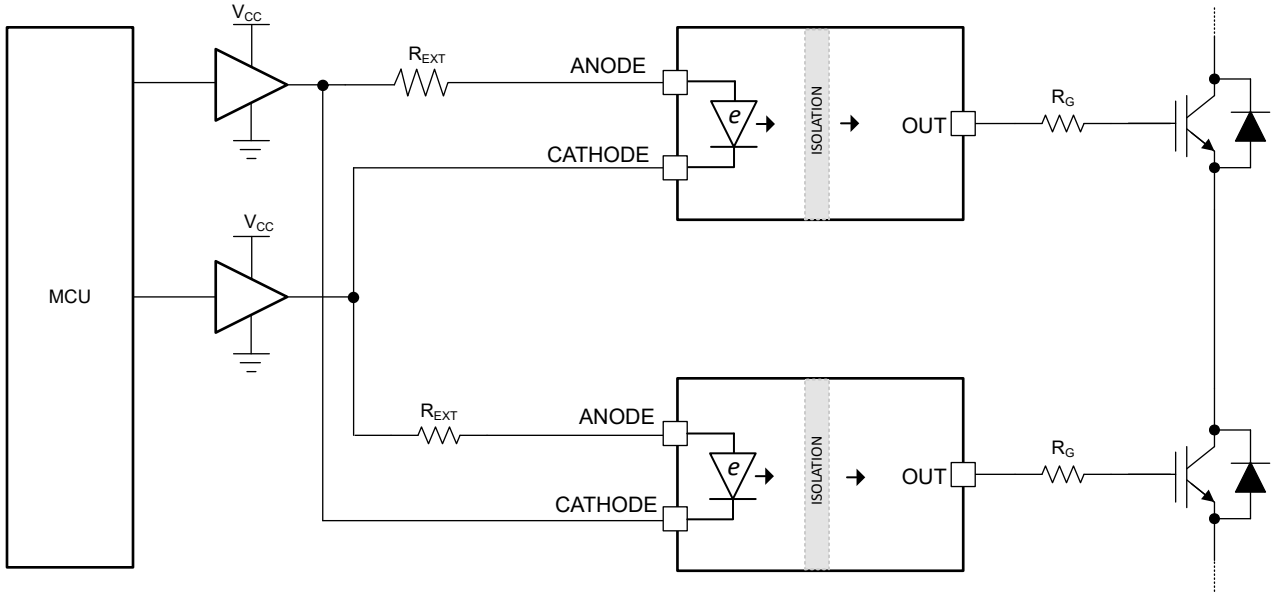


Figure 6-2. Interlock Architecture

6.3.4 Driver Stage

The device has ±5-A peak drive strength and is suitable for high power applications. The high drive strength can drive a SiC MOSFET module, IGBT module or paralleled discrete devices directly without extra buffer stage. The device can also be used to drive higher power modules or parallel modules with extra buffer stage. Regardless of the values of VDD, the peak sink and source current can be kept at 5 A. The driver features an important safety function wherein, when the input pins are in floating condition, OUT is held in LOW state. The driver stage as depicted in Figure 6-3, has rail-to-rail output by implementing an NMOS pull-up with intrinsic bootstrap gate drive. Under DC conditions, a PMOS is used to keep OUT tied to VDD as shown in the figure. The low pullup impedance of the NMOS results in strong drive strength during the turn-on transient, which shortens the charging time of the input capacitance of the power semiconductor. See Figure 6-4for an input-to-output timing diagram.

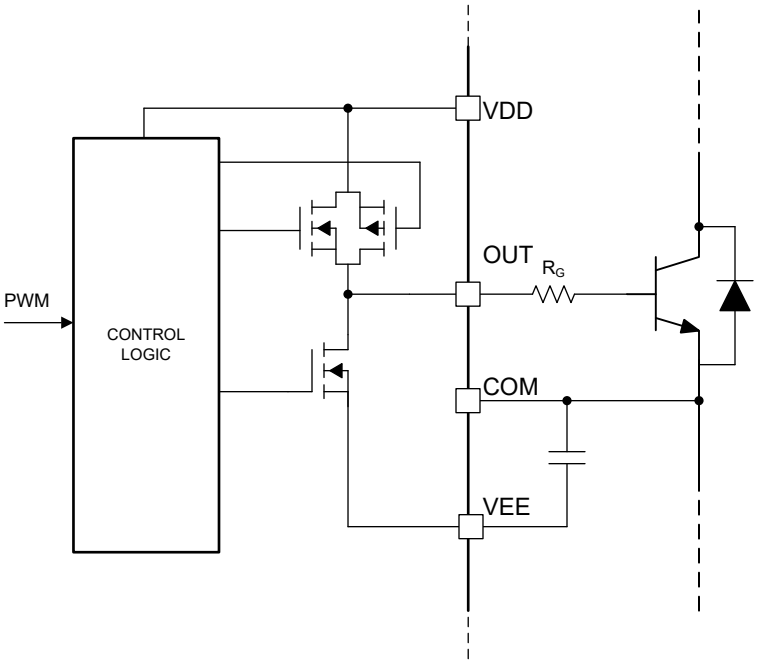


Figure 6-3. Gate Driver Output Stage

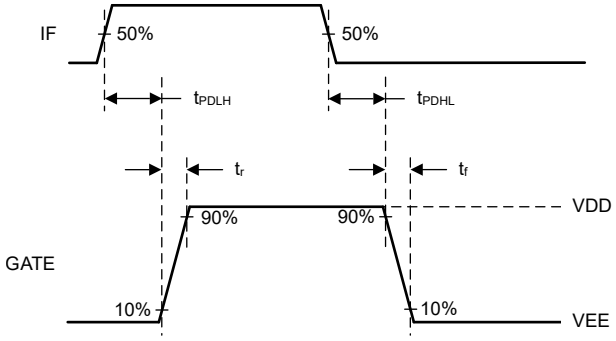


Figure 6-4. Input-to-Output Timing Diagram

6.3.5 Active Pulldown

UCC23710 implements an active pulldown feature to ensure the OUT pin is clamped to VEE when VDD is open. The OUT pin in high-impedance state when VDD is open. However, if voltage is present on the OUTL pin external to the gate driver, the voltage drives the pull-down FET through Ra and will pull down the output preventing the device from being turned on as shown in Figure 6-5.

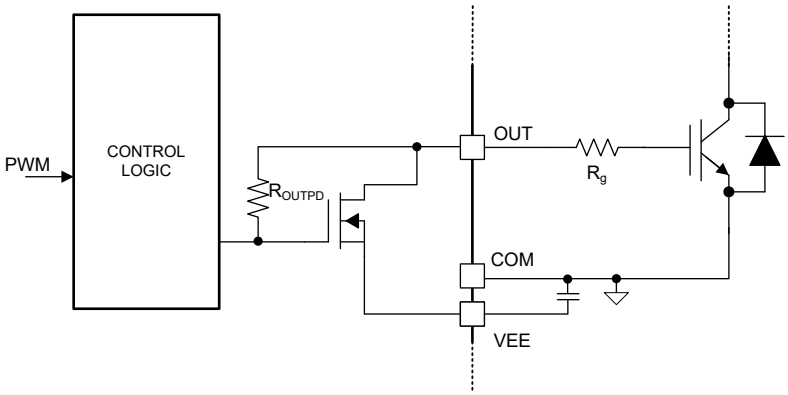


Figure 6-5. Active Pulldown

6.3.6 Short Circuit Clamping

The UCC23710 has integrated diodes to prevent OUT from exceeding VDD. The short circuit clamping function clamps the voltages at the driver outputs to be slightly higher than VDD during power switch short circuit conditions. The clamped gate voltage limits the short circuit current and prevents the IGBT or MOSFET gate from overvoltage breakdown or degradation.

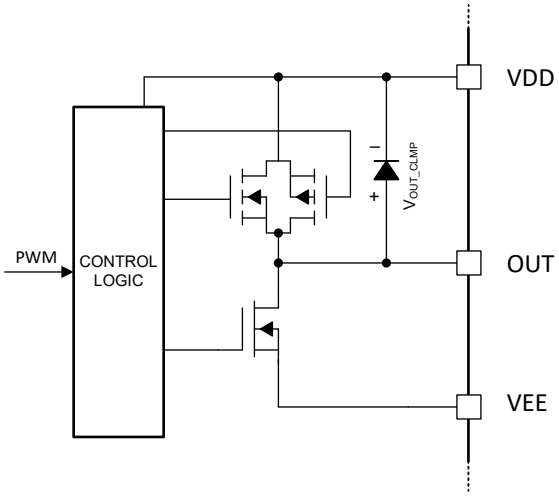


Figure 6-6. Short Circuit Clamping

6.3.7 Internal Active Miller Clamp

The UCC23710 has an active Miller clamp function to add an additional low impedance path to prevent unintentional turn-on while the driver is in the OFF state. In half-bridge applications it is possible for the body diode of the power semiconductor device to conduct while the driver is in the OFF state during deadtime. When this occurs, and the other power semiconductor device in the phase leg turns on, the drain-to-source or collector-to-emitter voltage will increase rapidly, causing high dV/dt across the Miller capacitance. This high dV/dt induces a current spike that can charge the gate capacitance and cause shoot-through if the main turn-off path isn't strong enough due to an external turn-off resistor, long PCB routing traces, or both.

The internal active Miller clamp function provides an internal strong pull-down FET. The FET is turned on when the power semiconductor device gate voltage is less than the Miller clamp threshold, V_{CLMPTH}. The gate voltage is sensed through the CLMPI pin. A simplified block diagram is shown in Figure 6-7 and a timing diagram is shown in Figure 6-8.

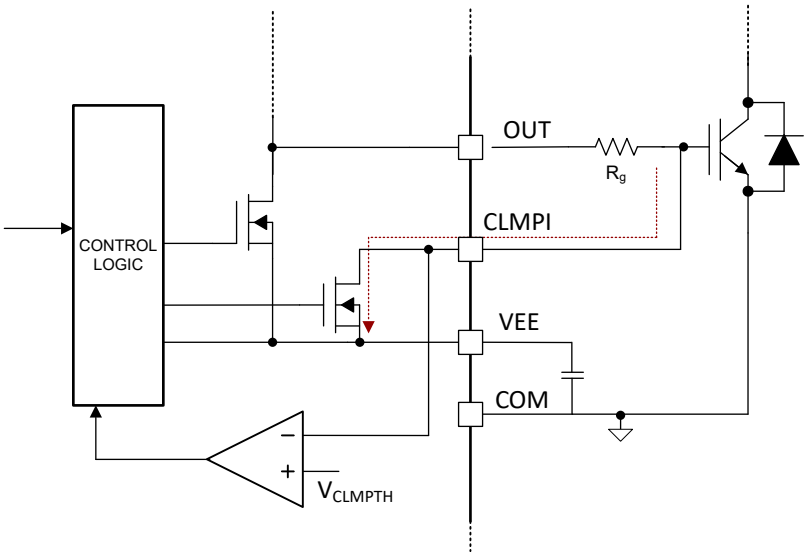


Figure 6-7. Internal Active Miller Clamp

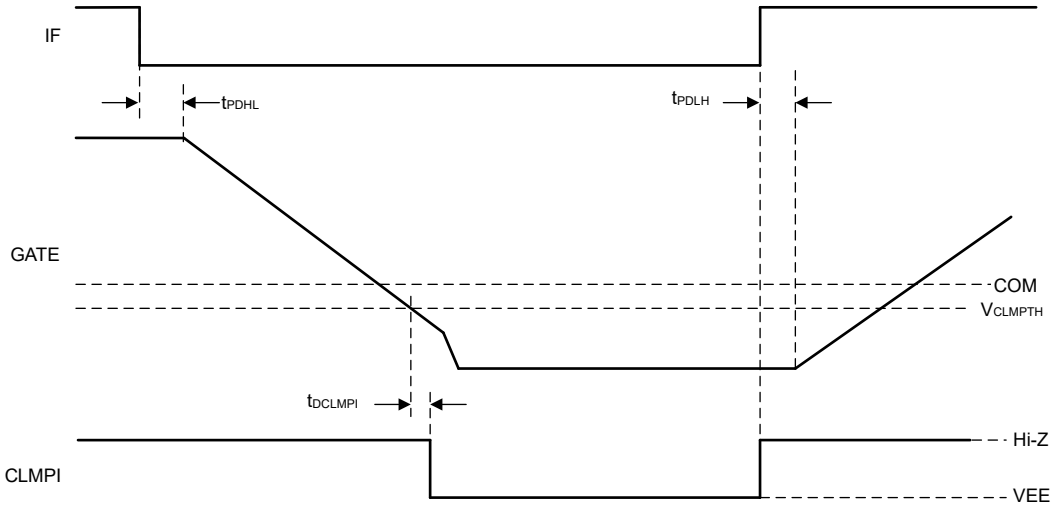


Figure 6-8. Internal Active Miller Clamp Timing Diagram

6.3.8 Desaturation (DESAT) Protection

The UCC23710 implements a fast overcurrent and short circuit protection feature to protect the power semiconductor device from catastrophic breakdown during a fault. The DESAT pin threshold, $V_{DESATTH}$, is with respect to COM, the source or emitter of the power semiconductor device. When the driver is in the off state, the DESAT pin is pulled down by an internal MOSFET to prevent DESAT from false triggering. When the driver is in the on state, an internal current source is activated to charge an external capacitor. The UCC23710 features an internal leading edge blanking time after OUT switches to the on state to avoid false triggers from noise during the switching transient. When the driver turns off, the internal pulldown MOSFET discharges the voltage of the DESAT pin. A simplified block diagram of the DESAT circuit is shown in Figure 6-9. Timing diagrams showing a DESAT fault, soft turn-off, fault reporting, and fault reset are shown in Figure 6-10.

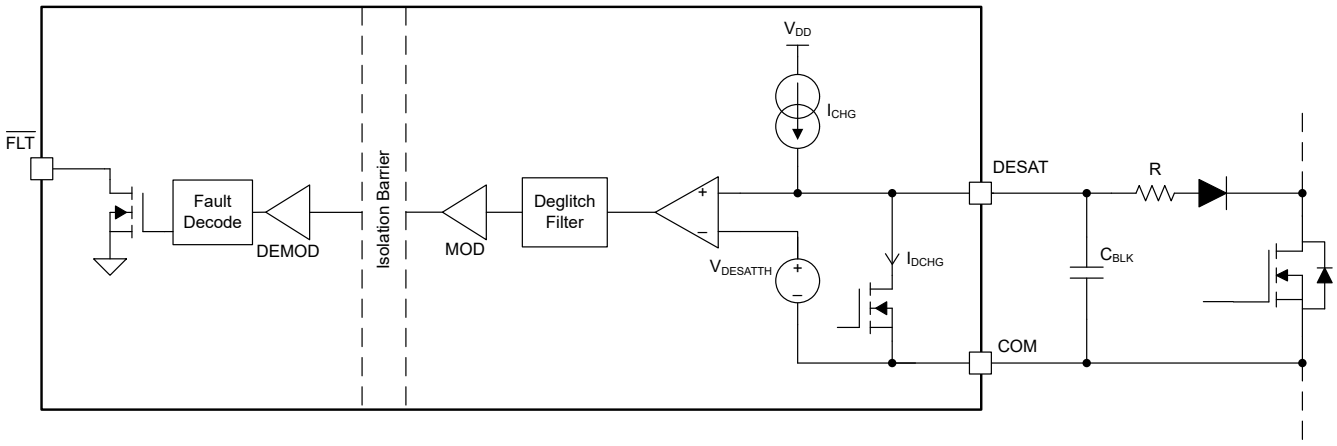


Figure 6-9. DESAT Protection

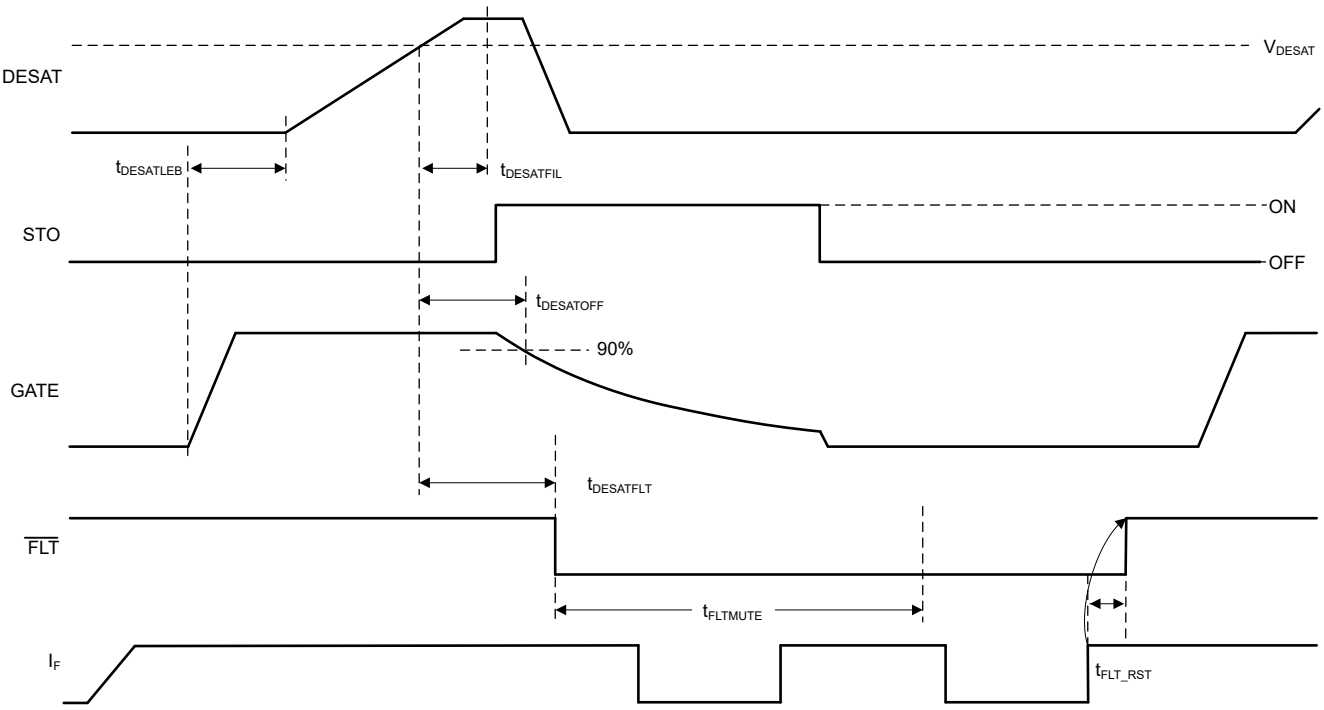


Figure 6-10. DESAT Protection Timing Diagram with Soft Shutdown with latch-off

6.3.9 Soft Turn Off (STO)

When a DESAT fault is detected, the UCC23710 initiates a soft turn off (STO) to protect the power semiconductor device. When an overcurrent or short circuit event happens, the STO feature slowly discharges the gate voltage to limit the overshoot voltage on the switching device created by high dI/dt due to the channel current. There is a tradeoff that needs to be made between the overshoot voltage and the short circuit energy. The turn-off speed must be slow enough to limit the overshoot voltage, but the shutdown time must not be too long that the large energy dissipation in the device can cause breakdown. When a DESAT fault is detected, STO current is sunk through OUT. Timing diagrams are shown in Figure 6-10.

6.3.10 Fault ($\overline{FLT}$) and Reset

The $\overline{FLT}$ pin is open drain and can report a fault signal to the DSP/MCU when a fault is detected through the DESAT pin. The $\overline{FLT}$ pin is pulled down to GND after a fault is detected, and is held low until the device is reset. The device has a fault mute time $t_{FLTMUTE}$, within which the device will not reset.

To reset the device, the device must see a low to high PWM input transition after $t_{FLTMUTE}$. If toggled before mute time expires, the device will not reset.

A timing diagram is shown in Figure 6-10.

6.4 Device Functional Modes

Table 6-1 lists the device function.

Table 6-1. Function Table

INPUT				OUTPUT		NOTE
VCC	VDD	IF	DESAT	$\overline{FLT}$	OUT	
PU	PD	X	NO	HiZ	LO	VDD UVLO
PU	PU	X	NO	HiZ	LO	DISABLED
PU	Open	X	NO	HiZ	HiZ	OPEN VDD
PU	PU	LO	NO	HiZ	LO	INPUT CONTROLLED
PU	PU	HI	NO	HiZ	HI	
PU	PU	LO	YES	LO	STO	DESAT/OC EVENT
PU	PU	HI	YES	LO	STO	
PD	PU	HI	YES	HiZ	STO	

PU = Power Up (Supply greater than UVLO rising threshold); PD = Power Down (Supply less than UVLO falling threshold); X: Irrelevant; HI = Output High; LO = Output Low; HiZ = High Impedance, STO = Soft Turn-Off

7 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

UCC23710 is a single-channel device designed for driving power semiconductor devices, including MOSFETs, IGBTs, and SiC MOSFETs, in applications such as motor control, industrial inverters, and switched-mode power supplies. The device features an emulated diode (e-diode) input stage, which replaces the traditional LED input stage found in standard opto-isolated gate drivers.

To activate the e-diode, a forward current (I_F) within the range of 5mA to 20mA must be applied to the anode. This forward current drives the gate driver output to a high state, thereby enabling the power FET. However, due to the limited current drive capability of most microcontrollers (MCUs), a buffer is typically required between the MCU and the input stage of the device.

The buffer power supply voltage is typically 5V or 3.3V, and a series resistor (R_{EXT}) is necessary to limit the current flowing into the e-diode. The selection of the optimal Rs value is critical, as it must be chosen to ensure that the e-diode forward current remains within the recommended range of 5mA to 20mA, while also considering the resistor tolerance, buffer supply voltage tolerance, and output impedance of the buffer.

The e-diode is capable of sustaining a continuous forward current of 25mA, with a forward voltage drop (V_f) exhibiting a tight part-to-part variation of 1.4V min to 2V max. The temperature coefficient of the forward voltage drop is less than 0.7mV/°C, and the dynamic impedance of the e-diode in the forward-biased region is approximately 1Ω. These characteristics contribute to the excellent stability of the e-diode forward current. The current driven input stage offers excellent noise immunity that is need in high power motor drive systems, especially in cases where the MCU cannot be located close to the isolated gate driver. UCC23710 offers best in class CMTI performance of >300kV/us.

The output power supply can be externally configured as a single isolated supply up to 30V or as an isolated bipolar supply, provided that the difference between the positive and negative supply voltages (V_{DD}-V_{EE}) does not exceed 30V. Alternatively, the output power supply can be bootstrapped using an external diode and capacitor, provided that the system utilizes a single power supply referenced to the power ground.

7.2 Typical Application

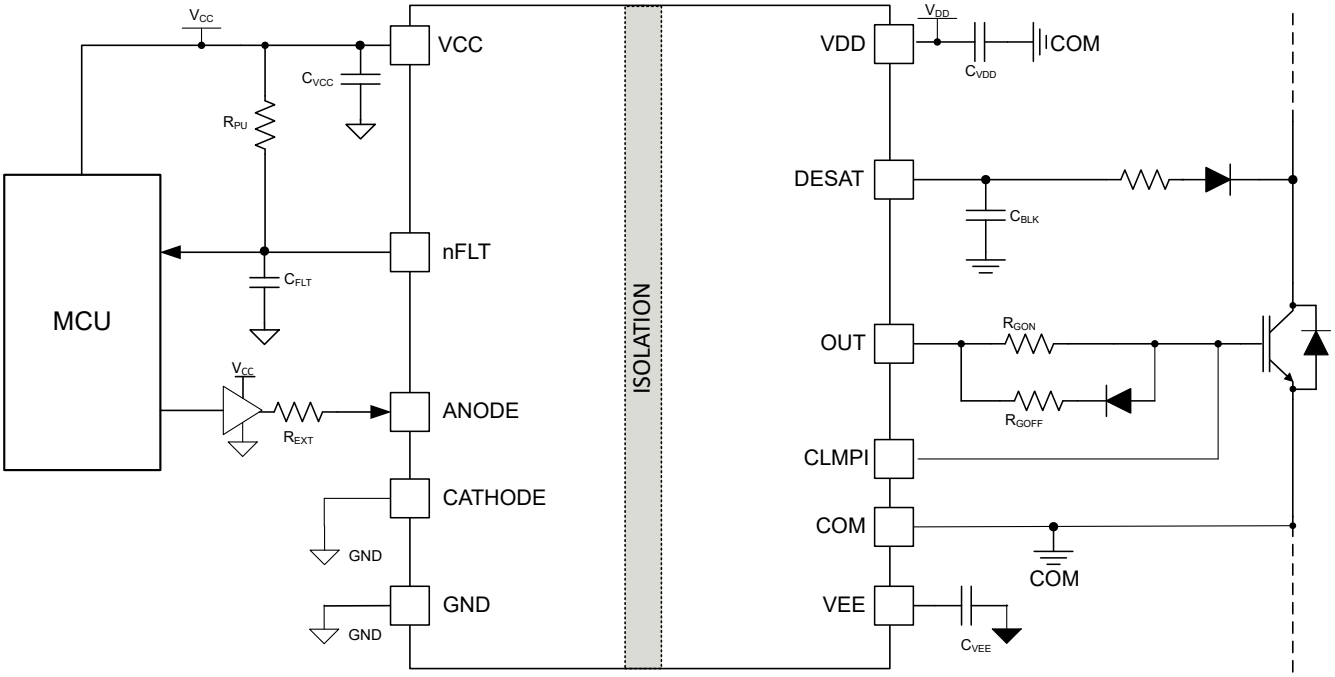


Figure 7-1. Typical Application Schematic

7.2.1 Design Requirements

Table 7-1 lists the recommended conditions to observe the input and output of the UCC23710 gate driver.

Table 7-1. UCC23710 Design Requirements

PARAMETER	VALUE	UNIT
V_{DD}	15	V
I_F	10	mA
Switching frequency	10	kHz

7.2.2 Detailed Design Procedure

7.2.2.1 Selecting the Input Resistor

The input resistor limits the current that flows into the e-diode when it is forward biased. The threshold current I_{FLH} is 1mA typ. The recommended operating range for the forward current is 5mA to 20mA (e-diode ON). All the electrical specifications are ensured in this range. The resistor should be selected such that for typical operating conditions, I_F is 10mA. Following are the list of factors that will affect the exact value of this current:

1. Supply voltage V_{SUP} variation
2. Manufacturer's tolerance for the resistor and variation due to temperature
3. e-diode forward voltage drop variation (at I_F=10mA, V_F= typ 1.7V, min 1.4V, max 2V, with a temperature coefficient < 0.7mV/°C and dynamic impedance < 1Ω)

See Figure 7-2 for the schematic using a single buffer and anode resistor combination to drive the input stage of the UCC23710. The input resistor can be selected using Table 7-2. For best CMTI performance, connect Cathode to ground.

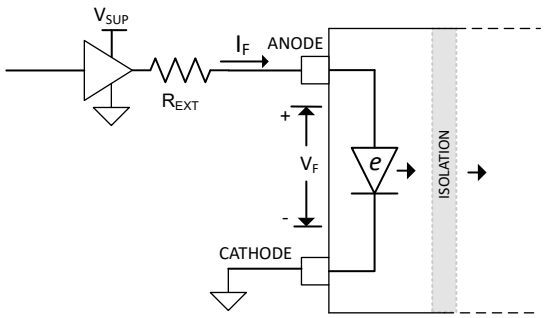


Figure 7-2. Driving the Input Stage with One Buffer and Anode Resistor

Table 7-2. R_{EXT} Values to Drive the Input Stage

	R_{EXT} Ω		
Configuration	Min	Typ	Max
Single buffer and R_{EXT}	115	312	757

7.2.2.2 Gate Driver Output Resistor

The external gate-driver resistors, $R_{G(ON)}$ and $R_{G(OFF)}$ are used to:

1. Limit ringing caused by parasitic inductances and capacitances
2. Limit ringing caused by high voltage or high current switching dv/dt, di/dt, and body-diode reverse recovery
3. Fine-tune gate drive strength, specifically peak sink and source current to optimize the switching loss
4. Reduce electromagnetic interference (EMI)

The output stage has a pull up with a peak source current of 5A. Use Equation 1 to estimate the peak source current as an example.

$$I_{OH} = \min\left[5A, \frac{V_{DD} - V_{GDF}}{\left(R_{OH} + R_{GON} + R_{GFET_{INT}}\right)}\right] \quad (1)$$

where

- R_{GON} is the external turnon resistance.
- R_{GFET_Int} is the power transistor internal gate resistance, found in the power transistor data sheet. Assume 0Ω for this example
- I_{OH} is the peak source current which is the minimum value between 5A, the gate-driver peak source current, and the calculated value based on the gate-drive loop resistance.
- V_{GDF} is the forward voltage drop for each of the diodes in series with R_{GON} and R_{GOFF}. The diode drop for this example is 0.7V.

In this example, the peak source current is approximately 1.15A as calculated in Equation 2.

$$I_{OH} = \min\left[5A, \frac{15}{2.5\Omega + 10\Omega + 0\Omega}\right] = 1.2A \quad (2)$$

Similarly, use Equation 3 to calculate the peak sink current.

$$I_{OL} = \min\left[5A, \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{GON} \,||\, R_{GOFF} + R_{GFET_{INT}}}\right] \quad (3)$$

where

- R_{GOFF} is the external turnoff resistance.
- I_{OL} is the peak sink current which is the minimum value between 5A, the gate-driver peak sink current, and the calculated value based on the gate-drive loop resistance.

In this example, the peak sink current is the minimum of 5A and Equation 4.

$$I_{OL} = \min\left[5A, \frac{15 - 0.7}{0.7\Omega + 10\Omega \,||\, 10\Omega + 0\Omega}\right] = 2.51A \quad (4)$$

The diodes shown in series with R_{GOFF}, in Figure 7-1 ensure the gate drive current flows through the intended path, respectively, during turn-on and turn-off. Note that the diode forward drop reduces the voltage level at the gate of the power switch. To achieve rail-to-rail gate voltage levels, add a resistor from the V_{OUT} pin to the power switch gate, with a resistance value approximately 20 times higher than R_{GOFF}. For the examples described in this section, a good choice is 100Ω to 200Ω.

Note

The estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate-driver loop can slow down the peak gate-drive current and introduce overshoot and undershoot. Therefore, TI strongly recommends that the gate-driver loop should be minimized. Conversely, the peak source and sink current is dominated by loop parasitics when the input capacitance of the power transistor is very small (typically less than 1nF) because the rising and falling time is too small and close to the parasitic ringing period.

7.2.2.3 $\overline{FLT}$ Output

$\overline{FLT}$ pin is an open-drain output. A 5-kΩ resistor can be used as pullup resistor for the $\overline{FLT}$ pins.

To improve the noise immunity due to the parasitic coupling and common mode noise, a low pass filter can be added between the $\overline{FLT}$ pin and the microcontroller. A filter capacitor between 100pF to 300pF can be added.

7.2.2.4 Estimate Gate-Driver Power Loss

The total loss, P_G, in the gate-driver subsystem includes the power losses (P_{GD}) of the UCC23710 device and the power losses in the peripheral circuitry, such as the external gate-drive resistor.

The P_{GD} value is the key power loss which determines the thermal safety-related limits of the UCC23710 device, and it can be estimated by calculating losses from several components.

The first component is the static power loss, P_{GDQ}, which includes power dissipated in the input stage (P_{GDQ_IN}) as well as the quiescent power dissipated in the output stage (P_{GDQ_OUT}) when operating with a certain switching frequency under no load. P_{GDQ_IN} is determined by I_F and V_F and is given by Equation 5. The P_{GDQ_OUT} parameter is measured on the bench with no load connected to V_{OUT} pin at a given V_{DD}, switching frequency, and ambient temperature. In this example, V_{DD} is 15V. The current on the power supply, with PWM switching at 10kHz, is measured to be I_{DD} = 1.33mA . Therefore, use Equation 6 to calculate P_{GDQ_OUT}.

$$P_{GDQ_{IN}} = \frac{1}{2} \times V_F \times I_F \quad (5)$$

$$P_{GDQ_{OUT}} = V_{DD} \times I_{DD} \quad (6)$$

The total quiescent power (without any load capacitance) dissipated in the gate driver is given by the sum of Equation 5 and Equation 6 as shown in Equation 7.

$$P_{GDQ} = P_{GDQ_{IN}} + P_{GDQ_{OUT}} = 9mW + 20mW = 29mW \quad (7)$$

The second component is the switching operation loss, P_{GDSW}, with a given load capacitance which the driver charges and discharges the load during each switching cycle. Use Equation 8 to calculate the total dynamic loss from load switching, P_{GSW}.

$$P_{GSW} = V_{DD} \times Q_G \times f_{SW} \quad (8)$$

where

- Q_G is the gate charge of the power transistor at V_{DD}.

So, for this example application the total dynamic loss from load switching is approximately 18mW as calculated in Equation 9.

$$P_{GSW} = 15V \times 120nC \times 10kHz = 18mW \quad (9)$$

Q_G represents the total gate charge of the power transistor switching 520V at 50A, and is subject to change with different testing conditions. The UCC23710 gate-driver loss on the output stage, P_{GDO}, is part of P_{GSW}. P_{GDO} is equal to P_{GSW} if the external gate-driver resistance and power-transistor internal resistances are 0Ω, and all the gate driver-loss is dissipated inside the UCC23710. If an external turn-on and turn-off resistance exists, the total loss is distributed between the gate driver pull-up/down resistance, external gate resistance, and power-transistor internal resistance. Importantly, the pull-up/down resistance is a linear and fixed resistance if the source/sink current is not saturated to 5A/5A, however, it will be nonlinear if the source/sink current is saturated. Therefore, P_{GDO} is different in these two scenarios.

Case 1 - Linear Pull-Up/Down Resistor:

$$P_{GDO} = \frac{P_{GSW}}{2}\left[\frac{R_{OH}}{R_{OH} + R_{GON} + R_{GFET_{int}}} + \frac{R_{OL}}{R_{OL} + R_{GON} \,||\, R_{GOFF} + R_{GFET_{int}}}\right] \quad (10)$$

In this design example, all the predicted source and sink currents are less than 5A and 5A, therefore, use Equation 10 to estimate the UCC23525 gate-driver loss.

$$P_{GDO} = \frac{18mW}{2}\left[\frac{2.5\Omega}{2.5\Omega + 10\Omega + 0\Omega} + \frac{0.7\Omega}{0.7\Omega + 10\Omega \,||\, 10\Omega + 0\Omega}\right] \quad (11)$$

Case 2 - Nonlinear Pull-Up/Down Resistor:

$$P_{GDO} = f_{sw} \times \left[\int_0^{T_{R_{Sys}}} 5A \times (V_{DD} - V_{OUT}(t))dt + \int_0^{T_{R_{Sys}}} 5A \times V_{OUT}(t)\, dt\right] \quad (12)$$

where

- $V_{OUT(t)}$ is the gate-driver OUT pin voltage during the turnon and turnoff period. In cases where the output is saturated for some time, this value can be simplified as a constant-current source (5A at turnon and 5A at turnoff) charging or discharging a load capacitor. Then, the $V_{OUT(t)}$ waveform will be linear and the T_{R_Sys} and T_{F_Sys} can be easily predicted.

For some scenarios, if only one of the pullup or pulldown circuits is saturated and another one is not, the P_{GDO} is a combination of case 1 and case 2, and the equations can be easily identified for the pullup and pulldown based on this discussion.

Use Equation 13 to calculate the total gate-driver loss dissipated in the UCC23710 gate driver, P_{GD}.

$$P_{GD} = P_{GDQ} + P_{GDO} = 29mW + 2.9mW = 31.9mW \quad (13)$$

7.2.2.5 Selecting V_{DD} Capacitor

Bypass capacitors for V_{DD} is essential for achieving reliable performance. TI recommends choosing low-ESR and low-ESL, surface-mount, multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients, and capacitance tolerances. A 50V, 10µF MLCC and a 50V, 0.22µF MLCC are selected for the C_{VDD} capacitor. If the bias power supply output is located a relatively long distance from the V_{CC} pin, a tantalum or electrolytic capacitor with a value greater than 10µF should be used in parallel with C_{VDD}.

Note

DC bias on some MLCCs impacts the actual capacitance value. For example, a 25V, 1µF X7R capacitor is measured to be only 500nF when a DC bias of 15V_{DC} is applied.

7.2.2.6 Overcurrent and Short Circuit Protection

A standard desaturation circuit can be applied to the DESAT pin. If the voltage of the DESAT pin is higher than the threshold V_{DESAT}, the soft turn-off is initiated. A fault will be reported to the input side to DSP/MCU. The output is held to LOW after the fault is detected, and can only be reset by the Forward current in the opto-emulator input. The state-of-art overcurrent and short circuit detection time helps to ensure a short shutdown time for SiC MOSFET and IGBT.

If DESAT pin is not in use, it must be tied to COM to avoid overcurrent fault false triggering.

- Fast reverse recovery high voltage diode is recommended in the desaturation circuit. A resistor is recommended in series with the high voltage diode to limit the inrush current.
- A Schottky diode is recommended from COM to DESAT to prevent driver damage caused by negative voltage.
- A Zener diode is recommended from COM to DESAT to prevent driver damage caused by positive voltage.

7.2.3 Application Curve

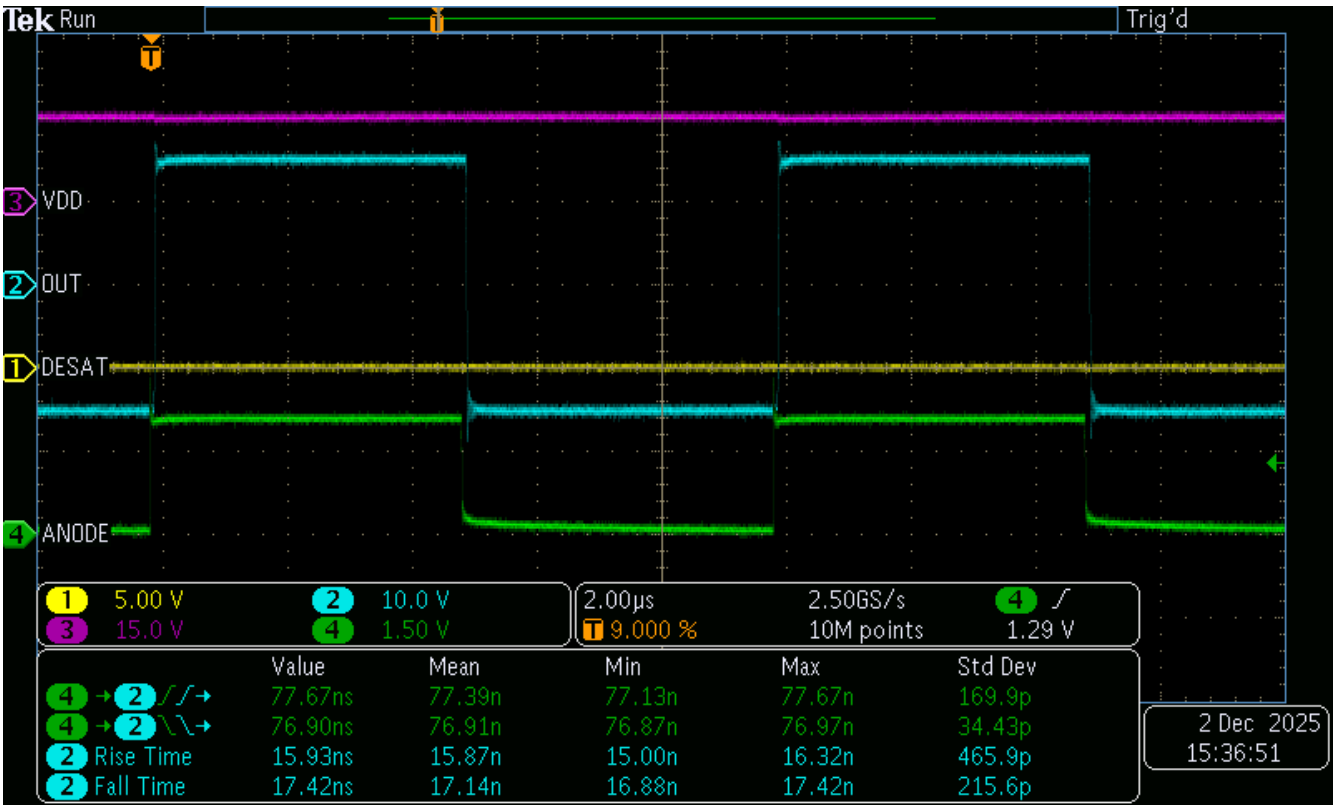


Figure 7-3. UCC23710 Input vs Output Behavior

7.3 Power Supply Recommendations

During the turn on and turn off switching transient, the peak source and sink current is provided by the VDD and VEE power supply. The large peak current is possible to drain the VDD and VEE voltage level and cause a voltage droop on the power supplies. To stabilize the power supply and ensure a reliable operation, a set of decoupling capacitors are recommended at the power supplies.Considering the device has ±5-A peak drive strength and can generate high dV/dt, a 1-µF bypass cap is recommended between VDD and COM, VEE and

COM. A 0.1-µF decoupling cap is also recommended for VCC-GND and VDD-COM to filter out high frequency noise. The decoupling capacitors must be low ESR and ESL to avoid high frequency noise, and should be placed as close as possible to the VCC, VDD and VEE pins to prevent noise coupling from the system parasitics of PCB layout.

To forward bias the e-diode, it is recommended to use a single resistor tied directly to the anode pin, and connect the cathode pin directly to GND.

7.4 Layout

7.4.1 Layout Guidelines

Due to the strong drive strength of the device, careful considerations must be taken in PCB design. Below are some key points:

- The driver should be placed as close as possible to the power semiconductor to reduce the parasitic inductance of the gate loop on the PCB traces.
- The decoupling capacitors of the input and output power supplies should be placed as close as possible to the power supply pins. The peak current generated at each switching transient can cause high dI/dt and voltage spike on the parasitic inductance of PCB traces.
- The driver COM pin should be connected to the Kelvin connection of SiC MOSFET source or IGBT emitter. If the power device does not have a split Kelvin source or emitter, the COM pin should be connected as close as possible to the source or emitter terminal of the power device package to separate the gate loop from the high power switching loop.
- Use a ground plane on the input side to shield the input signals. The input signals can be distorted by the high frequency noise generated by the output side switching transients. The ground plane provides a low-inductance filter for the return current flow.
- If the gate driver is used for the low side switch which the COM pin connected to the dc bus negative, use the ground plane on the output side to shield the output signals from the noise generated by the switch node; if the gate driver is used for the high side switch, which the COM pin is connected to the switch node, ground plane is not recommended.
- If ground plane is not used on the output side, separate the return path of the DESAT and AIN ground loop from the gate loop ground which has large peak source and sink current.
- No PCB trace or copper is allowed under the gate driver. A PCB cutout is recommended to avoid any noise coupling between the input and output side which can contaminate the isolation barrier.

7.4.2 Layout Example

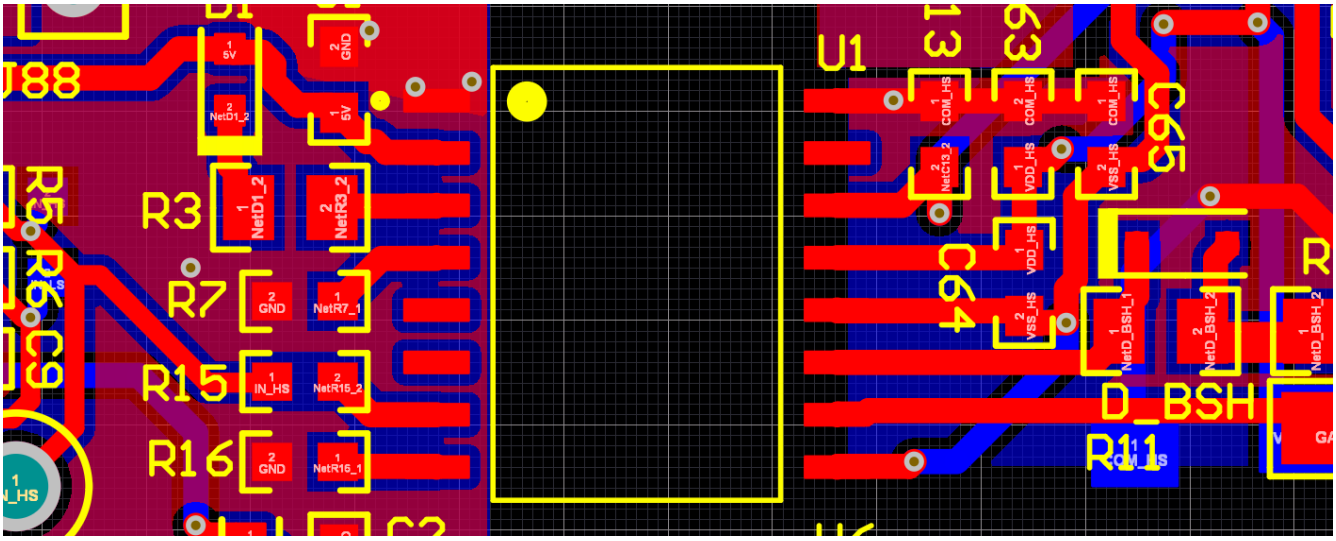


Figure 7-4. Layout Example

8 Device and Documentation Support

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

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8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- *Isolation Glossary*

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC23710BDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-	UCC23710B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

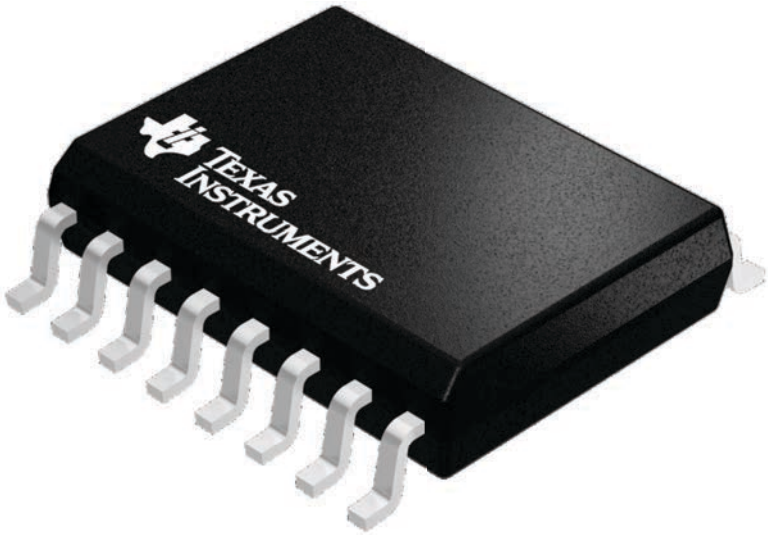
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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Last updated 10/2025