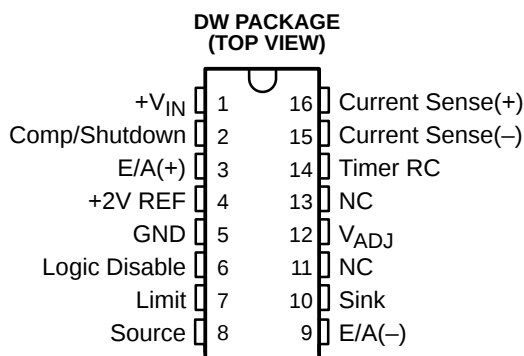


UC2832-EP PRECISION LOW DROPOUT LINEAR CONTROLLER

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- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –40°C to 105°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree[†]**
- **Precision 1% Reference**
- **Over-Current Sense Threshold Accurate to 5%**
- **Programmable Duty-Ratio Over-Current Protection**
- **4.5 V to 36 V Operation**
- **100 mA Output Drive, Source or Sink**
- **Under-Voltage Lockout**
- **Adjustable Current Limit to Current Sense Ratio**
- **Separate +V_{IN} terminal**
- **Programmable Driver Current Limit**
- **Access to VREF and E/A(+)**
- **Logic-Level Disable Input**

[†] Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.



NC = No Connect

description

The UC2832 series of precision linear regulators include all the control functions required in the design of very low dropout linear regulators. Additionally, they feature an innovative duty-ratio current limiting technique which provides peak load capability while limiting the average power dissipation of the external pass transistor during fault conditions. When the load current reaches an accurately programmed threshold, a gated-astable timer is enabled, which switches the regulator's pass device off and on at an externally programmable duty-ratio. During the on-time of the pass element, the output current is limited to a value slightly higher than the trip threshold of the duty-ratio timer. The constant-current-limit is programmable on the UC2832 to allow higher peak current during the on-time of the pass device. With duty-ratio control, high initial load demands and short circuit protection may both be accommodated without extra heat sinking or foldback current limiting. Additionally, if the timer pin is grounded, the duty-ratio timer is disabled, and the IC operates in constant-voltage/constant-current regulating mode.

These IC's include a 2 Volt ($\pm 1\%$) reference, error amplifier, UVLO, and a high current driver that has both source and sink outputs, allowing the use of either NPN or PNP external pass transistors. Safe operation is assured by the inclusion of under-voltage lockout (UVLO) and thermal shutdown.

ORDERING INFORMATION[‡]

T _A	PACKAGE [§]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	SOP – DW	Tape and reel	UC2832TDWREP	UC2832TEP
–40°C to 105°C	SOP – DW	Tube	UC2832TDWEP	UC2832TEP

[‡] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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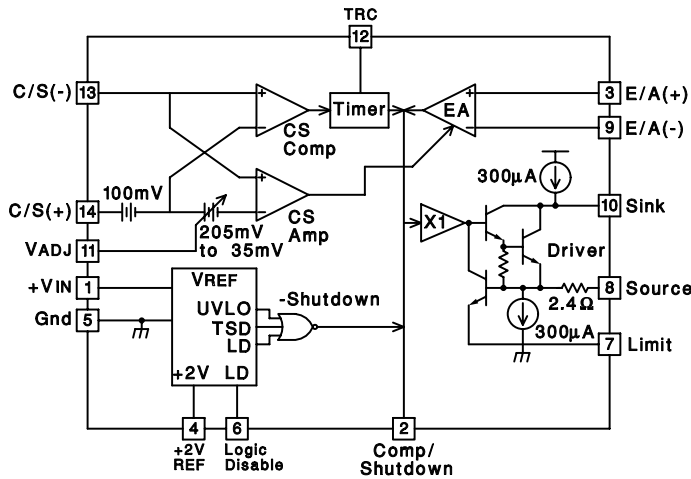
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UC2832-EP

PRECISION LOW DROPOUT LINEAR CONTROLLER

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block diagram



Ordering Information

UC 283	2	T	DW	R	EP	
						ENHANCED PLASTIC INDICATOR
						TAPE and REEL INDICATOR
						PACKAGE
						DW = Plastic SOIC
						TEMPERATURE INDICATOR
						T = -40°C to 105°C
						PRODUCT OPTION

UC2832-EP

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)^{†‡}

V_{IN} supply voltage	40 V
Driver output current (sink or source), I_O	450 mA
Driver sink to source voltage	40 V
TRC pin voltage	–0.3 V to 3.2 V
Other input voltages	–0.3 V to supply voltage
Operating junction temperature range, T_J	–55°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds	300°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] Unless otherwise indicated, voltages are reference to ground and currents are positive into and negative out of the specified terminals.

electrical characteristics, $T_A = -40^\circ\text{C}$ to 105°C for the UC2832T-EP, $+V_{IN} = 15\text{ V}$, Driver sink = $+V_{IN}$, C/S(+) voltage = $+V_{IN}$, and $T_A = T_J$ (unless otherwise stated)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply						
Supply current	+V _{IN} = 6 V		6.5	10	mA	
	+V _{IN} = 36 V		9.5	15		
	Logic Disable = 2 V		3.3	10		
Reference Section						
Output voltage	I _{DRIVER} = 10 mA	T _J = 25°C	1.98	2	2.02	V
		T _J = Full range	1.96	2	2.04	
Load regulation voltage	I _{OUT} = 0 to 10 mA		−10	−5	10	mV
Line regulation	+V _{IN} = 4.5 V to 36 V, I _{DRIVER} = 10 mA		0.033		0.5	mV/V
Under-voltage lockout threshold			3.6		4.5	V
Logic Disable Input						
Threshold voltage			1.3	1.4	1.5	V
Input bias current	Logic Disable = 0 V		−5	−1	0.1	μA
Current Sense Section						
Comparator offset	T _J = 25°C		95	100	105	mV
	T _J = Full range		93	100	107	
Amplifier offset	V _{ADJ} = Open		110	135	170	mV
	V _{ADJ} = 1 V		180	235	290	
	V _{ADJ} = 0 V		250	305	360	
Input bias current	V _{CM} = +V _{IN}		65	100	135	μA
Input offset current	V _{CM} = +V _{IN}		−10		10	μA
Amplifier CMRR	V _{CM} = 4.1 V to +V _{IN} + 0.3 V		80			dB
Transconductance	I _{COMP} = ±100 μA		65			ms
V _{ADJ} input current	V _{ADJ} = 0 V		−10	−1		μA



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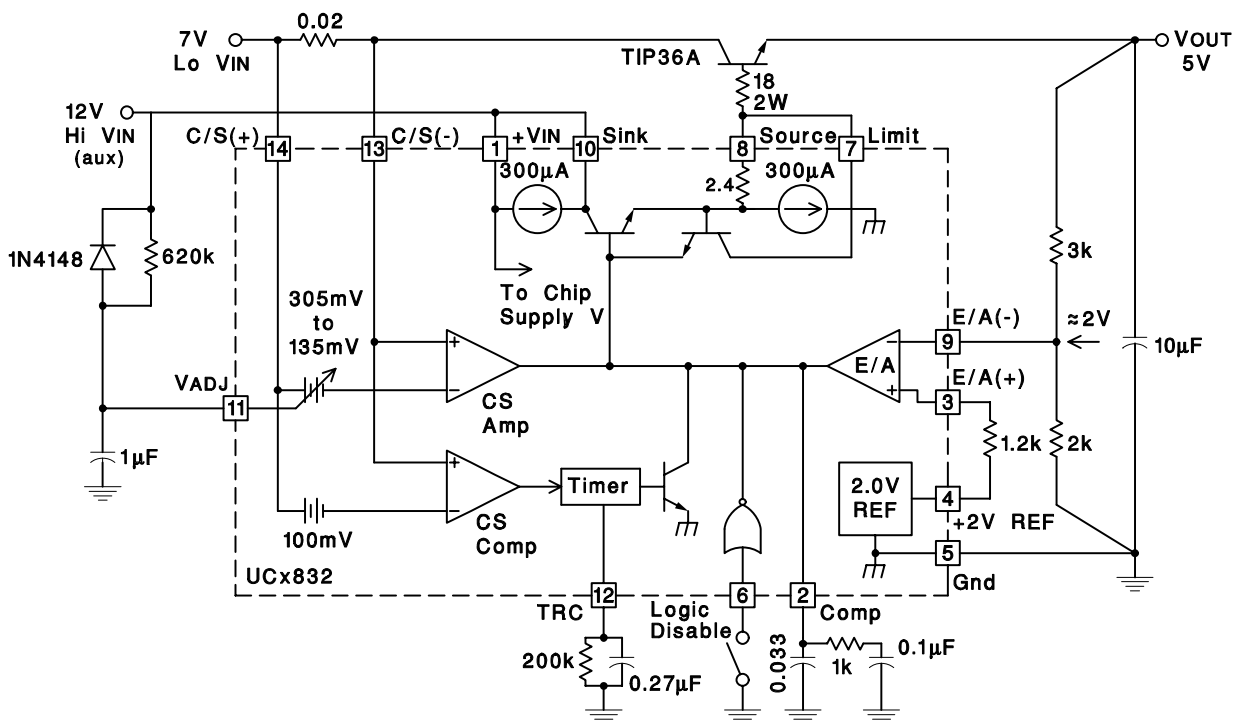
electrical characteristics, $T_A = -40^\circ\text{C}$ to 105°C for the UC2832T-EP, $+V_{IN} = 15\text{ V}$, Driver sink = $+V_{IN}$, C/S(+) voltage = $+V_{IN}$, and $T_A = T_J$ (unless otherwise stated)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Timer						
Inactive leakage current	C/S(+) = C/S(−) = +V _{IN} , TRC pin = 2 V		0.25		1	μA
Active pull-up current	C/S(+) = +V _{IN} , TRC pin = 0 V C/S(−) = +V _{IN} − 0.4 V,		−345	−270	−175	μA
Duty ratio (See Note 1)	ontime/period, R _T = 200 kΩ, C _T = 0.27 μF		4.8			%
Period (See Notes 1 and 2)	ontime + offtime, R _T = 200 kΩ, C _T = 0.27 μF		36			ms
Upper trip threshold (V _U)			1.8			V
Lower trip threshold (V _L)			0.9			V
Trip threshold ratio	V _U / V _L		2.0			V/V
Error Amplifier Section						
Input offset voltage	V _{CM} = V _{COMP} = 2 V		−8		8	mV
Input bias current	V _{CM} = V _{COMP} = 2 V		−4.5	−1.1		μA
Input offset current	V _{CM} = V _{COMP} = 2 V		−1.5		1.5	μA
Open loop voltage gain (A _{VOL})	V _{COMP} = 1 V to 13 V		50	70		dB
Common mode rejection ratio (CMRR)	V _{CM} = 0 V to +V _{IN} − 3 V		60	80		dB
PSRR	V _{CM} = 2 V, +V _{IN} = 4.5 V to 36 V		90			dB
Transconductance	I _{COMP} = ± 10 μA		4.3			ms
High-level output voltage (V _{OH})	I _{COMP} = 0, Volts below +V _{IN}		0.95		1.3	V
Low-level output voltage (V _{OL})	I _{COMP} = 0		4.5		0.7	V
Output high current (I _{OH})	V _{COMP} = 2 V		−700	−500	−100	μA
Output low current (I _{OL})	V _{COMP} = 2 V	C/S(−) = +V _{IN}	100	500	700	μA
		C/S(−) = +V _{IN} − 0.4 V	2	6		mA

NOTES: 1. These parameters are first-order supply-independent, however, both may vary with supply for $+V_{IN}$ less than about 4 V. This supply variation will cause a slight change in the timer period and duty cycle, although a high off-time/on-time ratio will be maintained.
2. With recommended R_T value of 200 k Ω , $T_{OFF} \approx R_T C_T \cdot \ln(V_U/V_L) \pm 10\%$.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Driver Section						
Maximum current	Driver limit and source pins common	T _J = 25°C	200	300	400	mA
		T _J = Full range	100	300	450	
Limiting voltage	Driver limit to source voltage at current limit, I _{SOURCE} = -10 mA, T _J = 25°C, See Note 3		0.72			V
Internal current sense resistance	T _J = 25°C, See Note 3		2.4			Ω
Pull-up current at driver sink	Compensation/Shutdown = 0.4 V	Driver sink = +V _{IN} - 1 V	-800	-300	-100	μA
		+V _{IN} = 36 V, Driver sink = 35 V	-1000	-300	-75	
Pull-down current at driver source	Compensation/Shutdown = 0.4 V, Driver source = 1 V		150	300	700	μA
Saturation voltage sink to source	Driver source = 0 V, Driver current = 100 mA		1.5			V
Maximum source voltage	Driver sink = +V _{IN} , Driver current = 100 mA, Volts below +V _{IN}		3			V
UVLO sink leakage	+V _{IN} = C/S(+) = C/S(-) = 2.5 V, Driver sink = 15 V, Driver source = 0 V, T _A = 25°C		25			μA
Maximum reverse source voltage	Compensation/Shutdown = 0 V, I _{SOURCE} = 100 μA, (+)V _{IN} = 3 V		1.6			V
Thermal shutdown			160			°C

APPLICATION AND OPERATION INFORMATION



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APPLICATION AND OPERATION INFORMATION

Estimating Maximum Load Capacitance

For any power supply, the rate at which the total output capacitance can be charged depends on the maximum output current available and on the nature of the load. For a constant-current current-limited power supply, the output will come up if the load asks for less than the maximum available short-circuit limit current.

To ensure recovery of a duty-ratio current-limited power supply from a short-circuited load condition, there is a maximum total output capacitance which can be charged for a given unit ON time. The design value of ON time can be adjusted by changing the timing capacitor. Nominally, $T_{ON} = 0.693 \times 10 \text{ k}\Omega \times C_T$.

Typically, the IC regulates output current to a maximum of $I_{MAX} = K \times I_{TH}$, where I_{TH} is the timer trip-point current, and

$$K = \frac{\text{Current Sense Amplifier Offset Voltage}}{100 \text{ mA}}$$

and is variable from 1.35 to 3.05 with V_{ADJ} .

For a worst-case constant-current load of value just less than I_{TH} , C_{MAX} can be estimated from:

$$C_{MAX} = \left(\frac{K - 1}{I_{TH}} \right) \times \left(\frac{T_{ON}}{V_{OUT}} \right)$$

where V_{OUT} is the nominal regulator output voltage.

For a resistive load of value R_L , the value of C_{MAX} can be estimated from:

$$C_{MAX} = \frac{T_{ON}}{R_L} \times \frac{1}{\ln \left[\left(1 - \frac{V_{OUT}}{K \times I_{TH} \times R_L} \right)^{-1} \right]}$$

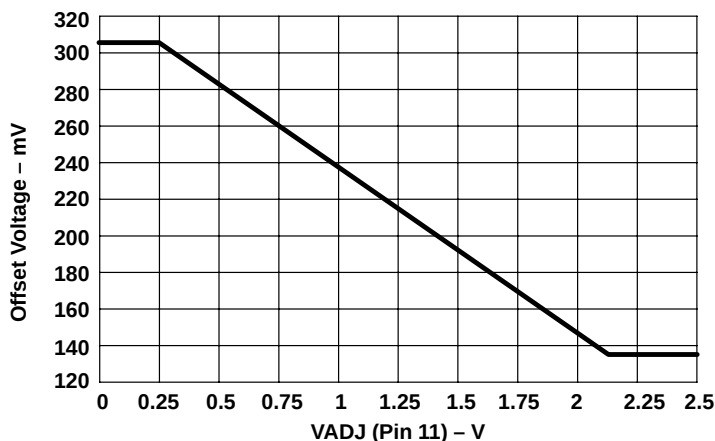


Figure 2. Current Sense Amplifier Offset Voltage vs V_{ADJ}

APPLICATION AND OPERATION INFORMATION

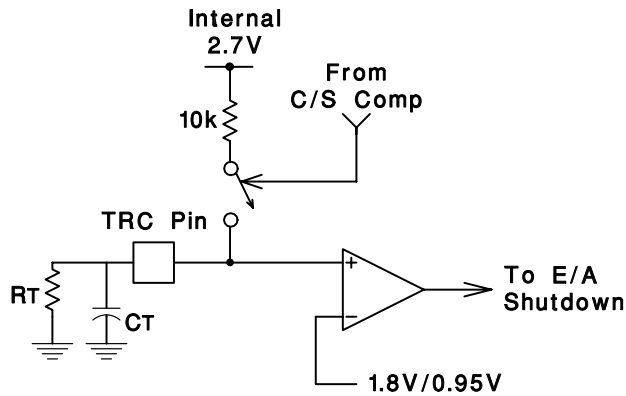
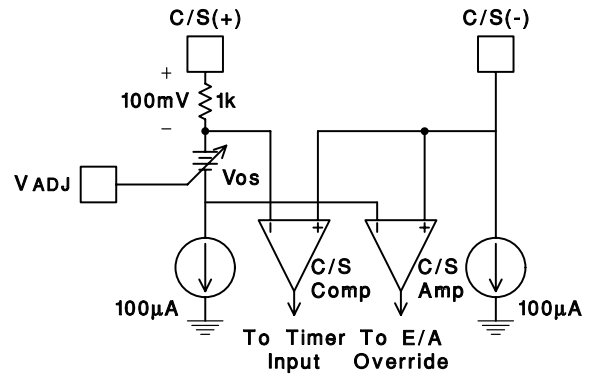


Figure 3. Timer Function



NOTE A: $V_{OS} = 205 \text{ mV to } 35 \text{ mV}$

Figure 4. Current Sense Input Configuration

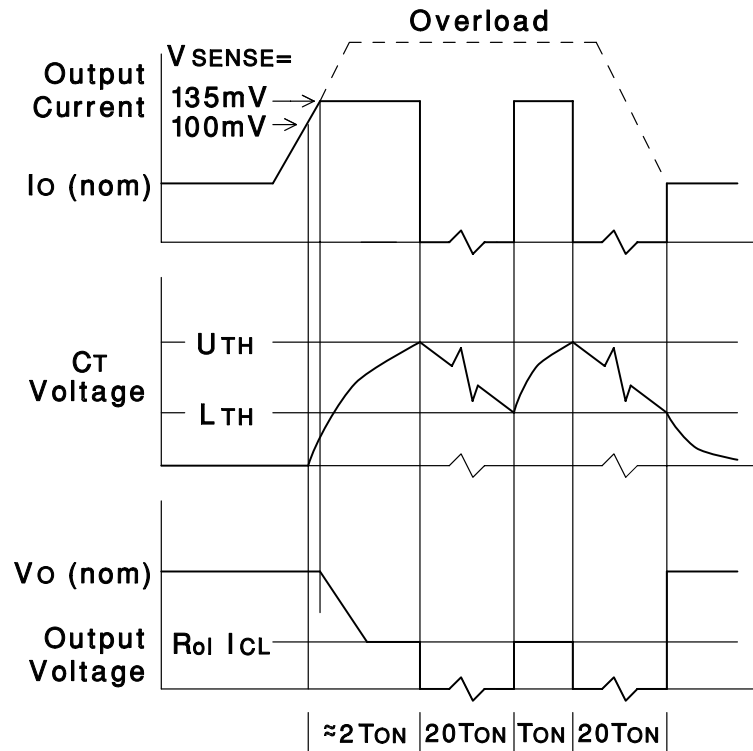


Figure 5. Load Current, Timing Capacitor Voltage, and Output Voltage of the Regulator Under Fault Conditions

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APPLICATION AND OPERATION INFORMATION

UCx832 Error Amplifier

AVOL vs Frequency and Cc

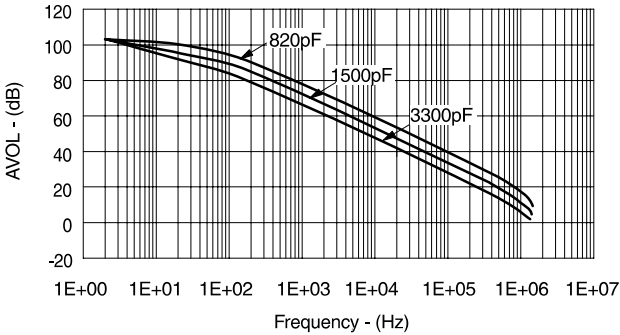


Figure 6. UCx832 Error Amplifier

UCx832 Current Sense Amplifier

AVOL vs Frequency and Cc

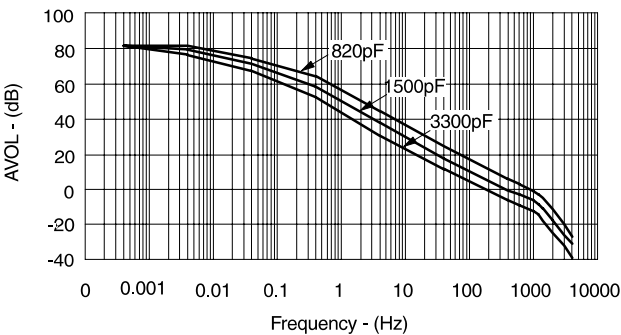


Figure 7. UCx832 Current Sense Amplifier

UCx832 Error Amplifier

Transconductance and Phase vs Frequency

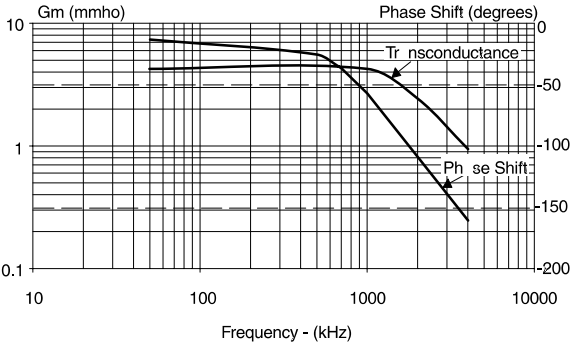


Figure 8. UCx832 Error Amplifier

UCx832 Current Sense Amplifier

Transconductance and Phase vs Frequency

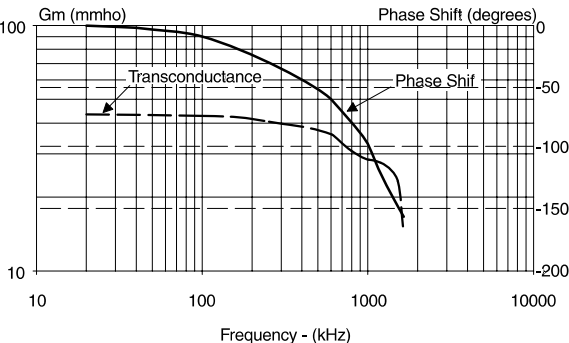


Figure 9. UCx832 Current Sense Amplifier

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UC2832TDWEP	Active	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UC2832TEP
UC2832TDWEP.A	Active	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UC2832TEP

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF UC2832-EP :

- Catalog : [UC2832](#)

- Military : [UC2832M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
UC2832TDWEP	DW	SOIC	16	40	507	12.83	5080	6.6
UC2832TDWEP.A	DW	SOIC	16	40	507	12.83	5080	6.6

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