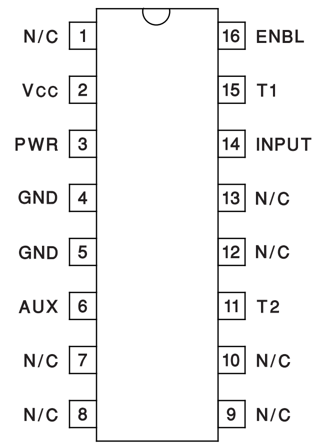
COMPLIMENTARY SWITCH FET DRIVERS

Check for Samples: UC1715-SP

FEATURES

- **Single Input (PWM and TTL Compatible)**
- **High Current Power FET Driver, 1-A Source/2-A Sink**
- **Auxiliary Output FET Driver, 0.5-A Source/1-A Sink**
- **Time Delays Between Power and Auxiliary Outputs Independently Programmable from 50 ns to 700 ns**
- **Time Delay or True Zero-Voltage Operation Independently Configurable for Each Output**
- **Switching Frequency to 1 MHz**
- **Typical 50-ns Propagation Delays**
- **ENBL Pin Activates 220-μA Sleep Mode**
- **Power Output is Active Low in Sleep Mode**
- **Synchronous Rectifier Driver**

W PACKAGE
(TOP VIEW)



DESCRIPTION

The UC1715 is a high speed driver designed to provide drive waveforms for complementary switches. Complementary switch configurations are commonly used in synchronous rectification circuits and active clamp/reset circuits, which can provide zero voltage switching. In order to facilitate the soft switching transitions, independently programmable delays between the two output waveforms are provided on this driver. The delay pins also have true zero voltage sensing capability which allows immediate activation of the corresponding switch when zero voltage is applied. This device requires a PWM-type input to operate and can be interfaced with commonly available PWM controllers.

ORDERING INFORMATION(1)

T_J	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	CFP (W)	5962-0052102VFA	5962-0052102VFA

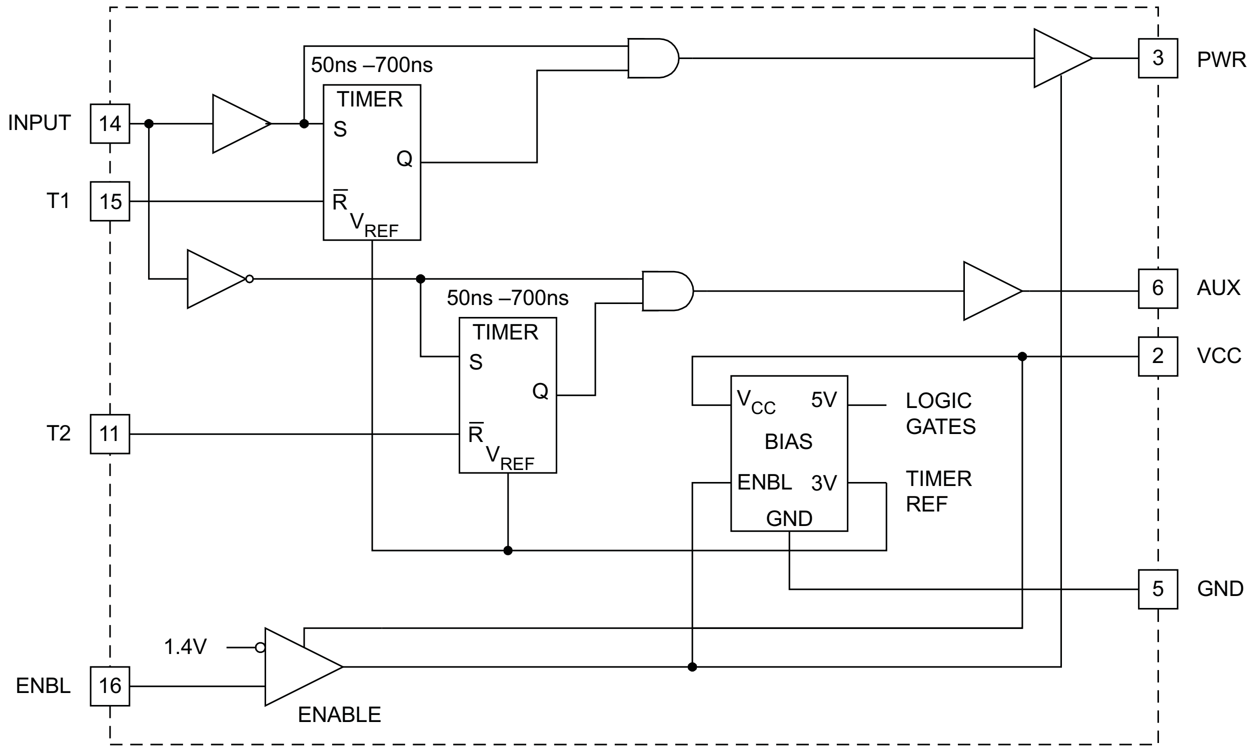
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

DEVICE INFORMATION

PIN FUNCTIONS

PIN NAME	PIN NO.	I/O	DESCRIPTION
N/C	1, 7, 8, 9, 10, 12, 13	-	N/C pins are not bonded out. External connections will not affect device functionality.
V_{CC}	2	I	The V_{CC} input range is from 7 V to 20 V. This pin should be bypassed with a capacitor to GND consistent with peak load current demands.
PWR	3	O	The PWR output waits for the T1 delay after the INPUT's rising edge before switching on, but switches off immediately at INPUT's falling edge (neglecting propagation delays). This output is capable of sourcing 1-A and sinking 2-A of peak gate drive current. PWR output includes a passive, self-biased circuit which holds this pin active low, when ENBL ≥ 0.8 V regardless of VCC's voltage.
GND	4, 5	-	This is the reference pin for all input voltages and the return point for all device currents. It carries the full peak sinking current from the outputs. Any tendency for the outputs to ring below GND voltage must be damped or clamped such that GND remains the most negative potential.
AUX	6		The AUX switches immediately at INPUT's rising edge but waits through the T2 delay after INPUT's falling edge before switching. AUX is capable of sourcing 0.5-A and sinking 1-A of drive current. During sleep mode, AUX is inactive with a high impedance.
T2	11		This pin functions in the same way as T1 but controls the time delay between PWR turn-off and activation of the AUX switch. The resistor on this pin sets the charging current on internal timing capacitors to provide independent time control. The nominal voltage level at this pin is 3 V and the current is internally limited to 1 mA. The total delay from INPUT to output includes a propagation delay in addition to the programmable timer but since the propagation delays are approximately equal, the relative time delay between the two outputs can be assumed to be solely a function of the programmed delays. The relationship of the time delay vs. RT is shown in the Typical Characteristics curves.
INPUT	14	I	The input switches at TTL logic levels (approximately 1.4 V) but the allowable range is from 0 V to 20 V, allowing direct connection to most common IC PWM controller outputs. The rising edge immediately switches the AUX output, and initiates a timing delay, T1, before switching on the PWR output. Similarly, the INPUT falling edge immediately turns off the PWR output and initiates a timing delay, T2, before switching the AUX output. It should be noted that if the input signal comes from a controller with FET drive capability, this signal provides another option. INPUT and PWR provide a delay only at the leading edge while INPUT and AUX provide the delay at the trailing edge.
T1	15		A resistor to ground programs the time delay between AUX switch turn-off and PWR turn-on. The resistor on this pin sets the charging current on internal timing capacitors to provide independent time control. The nominal voltage level at this pin is 3 V and the current is internally limited to 1 mA. The total delay from INPUT to output includes a propagation delay in addition to the programmable timer but since the propagation delays are approximately equal, the relative time delay between the two outputs can be assumed to be solely a function of the programmed delays. The relationship of the time delay vs. RT is shown in the Typical Characteristics curves.
ENBL	16	I	The ENBL input switches at TTL logic levels (approximately 1.2 V), and its input range is from 0 V to 20 V. The ENBL input will place the device into sleep mode when it is a logical low. The current into VCC during the sleep mode is typically 220 µA.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

V_{CC}	Supply voltage		20 V
I_{OH}	Power driver	Continuous	-100 mA
		Peak(3)	-1 A
	Auxiliary driver	Continuous	-100 mA
		Peak(3)	-500 mA
I_{OL}	Power driver	Continuous	100 mA
		Peak(3)	2 A
	Auxiliary driver	Continuous	100 mA
		Peak(3)	1 A
V_I	Input voltage range (INPUT, ENBL)		–0.3 V to 20 V
T_J	Maximum operating junction temperature		150°C
T_{stg}	Storage temperature range		–65°C to 150°C
T_{lead}	Maximum lead temperature (soldering, 10 seconds)		300°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal.
(3) RMS drive current on any pin to be restricted to 672 mA.

THERMAL INFORMATION

THERMAL METRIC[1]		UC1715-SP W 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance[2]	72.9	°C/W
θ_{JC}	Junction-to-case thermal resistance[3]	8.25	
θ_{JB}	Junction-to-board thermal resistance[4]	43.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

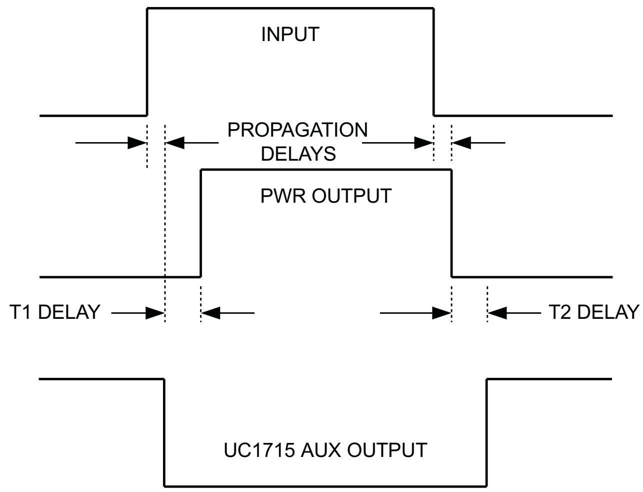
ELECTRICAL CHARACTERISTICS

V_{CC} = 15 V, ENBL ≥ 2 V, R_T1 = 100 kΩ from T1 to GND, R_T2 = 100 kΩ from T2 to GND, $T_A = T_J$ = –55°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overall					
V_{CC}		7		18	V
I_{CC}, nominal	ENBL = 3 V			25	mA
I_{CC}, sleep mode	ENBL = 0.8 V			300	µA
Power Driver (PWR)					
Pre turn-on PWR output, low	V_{CC} = 0 V, I_{OUT} = 10 mA, ENBL ≤ 0.8 V			2	V
PWR output low, sat. (V_{PWR})	INPUT = 0.8 V, I_{OUT} = 40 mA			1	V
	INPUT = 0.8 V, I_{OUT} = 100 mA			1.5	
PWR output high, sat. ($V_{CC} - V_{PWR}$)	INPUT = 3 V, I_{OUT} = −40 mA			3	V
	INPUT = 3 V, I_{OUT} = −100 mA			3	
Rise time	C_L = 2200 pF			60	ns
Fall time	C_L = 2200 pF			60	ns
T1 delay, AUX to PWR(1)	INPUT rising edge, R_T1 = 10 kΩ, see (2)	45		200	ns
T1 delay, AUX to PWR(1)	INPUT rising edge, R_T1 = 100 kΩ, see (2)	250		1300	ns
PWR prop delay	INPUT falling edge, 50%, see (3)			300	ns
Auxiliary Driver (AUX)					
AUX pre turn-on AUX output low (V_{PAUX})	V_{CC} = 0 V, ENBL ≤ 0.8 V, I_{OUT} = 10 mA			2	V
AUX output low, sat. (V_{AUX})	V_{IN} = 3 V, I_{OUT} = 40 mA			1	V
	V_{IN} = 3 V, I_{OUT} = 100 mA			1.5	
AUX output high, sat. ($V_{CC} – V_{AUX}$)	V_{IN} = 0.8 V, I_{OUT} = -40 mA			3	V
	V_{IN} = 0.8 V, I_{OUT} = -100 mA			3	
Rise time	C_L = 2200 pF			60	ns
Fall time	C_L = 2200 pF			60	ns
T2 delay, PWR to AUX(1)	INPUT falling edge, R_T2 = 10 kΩ, see (2)	45		130	ns
T2 delay, PWR to AUX(1)	INPUT falling edge, R_T2 = 100 kΩ, see (2)	200		700	ns
AUX prop delay	INPUT rising edge, 50%, see (3)			185	ns
Enable (ENBL)					
Input threshold				2.8	V
Input current, I_{IH}	ENBL = 15 V	-10		10	µA
Input current, I_{IL}	ENBL = 0 V	-15		15	µA
T1					
Current limit	T1 = 0 V	-2		-0.5	mA
Nominal voltage at T1		2.7		3.3	V
Minimum T1 delay	T1 = 2.5 V, see (2)			80	ns
T2					
Current limit	T2 = 0 V	-2		-0.5	mA
Nominal voltage at T12		2.7		3.3	V
Minimum T2 delay	T2 = 2.5 V, see (2)			80	ns
Input (INPUT)					
Input threshold				2.8	V
Input current, I_{IH}	ENBL = 15 V	-10		10	µA
Input current, I_{IL}	ENBL = 0 V	-20		20	µA

(1) The parameter is guaranteed to the limit specified by characterization, but not production tested.
(2) T1 and T2 delay is defined as the time between the 50% transition point of AUX (PWR) and the 50% transition point of PWR (AUX) with no capacitive load on either output.
(3) Propagation delays are measured from the 50% point of the input signal to the 50% point of the output signal's transition with no load on outputs.

TYPICAL CHARACTERISTICS



A. T1 delay is defined from the 50% point of the transition edge of AUX to the 10% of the rising edge of PWR. T2 delay is defined from the 90% of the falling edge of PWR to the 50% point of the transition edge of AUX.

B. Propagation delay times are measured from the 50% point of the input signal to the 10% point of the output signal's transition with no load on outputs.

Figure 1. Time Relationships

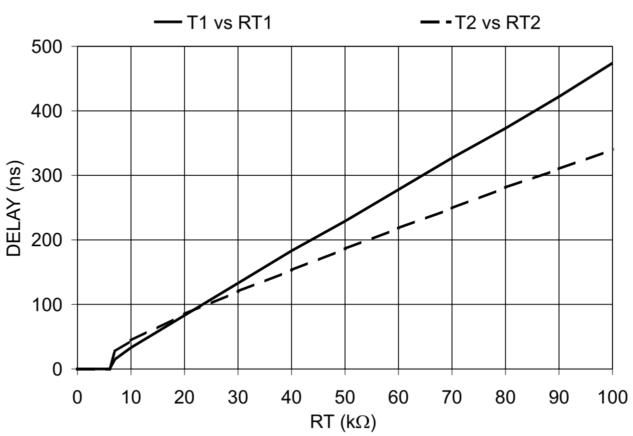


Figure 2. T1 Delay, T2 Delay vs. R_T

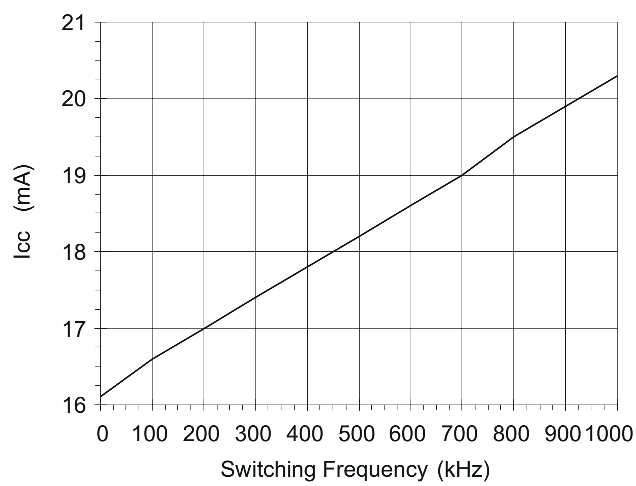


Figure 3. I_{CC} vs Switching Frequency With No Load and 50% Duty Cycle $R_T1 = R_T2 = 50$ kΩ

TYPICAL CHARACTERISTICS (continued)

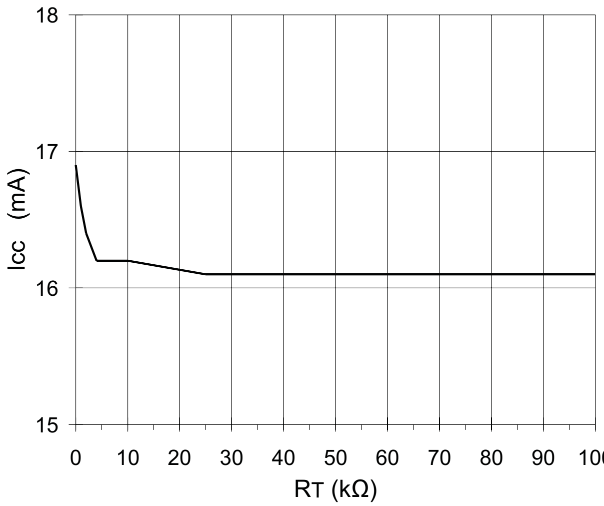


Figure 4. I_{CC} vs R_T With Opposite R_T = 50 kΩ

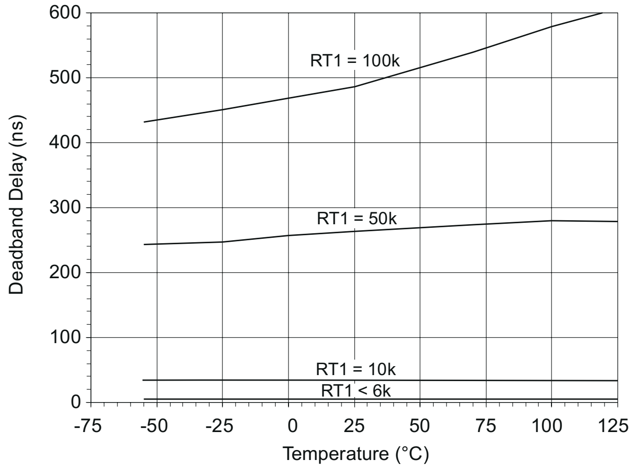


Figure 5. T1 Deadband vs. Temperature
AUX to PWR

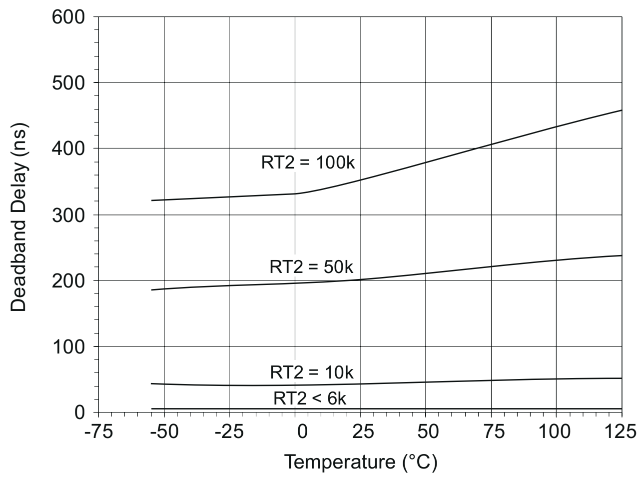


Figure 6. T2 Deadband vs. Temperature
PWR to AUX

TYPICAL APPLICATIONS

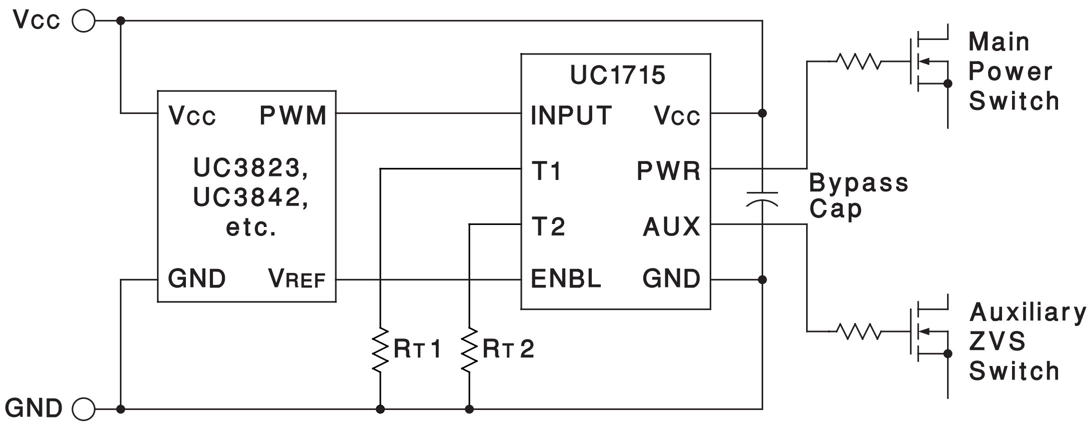


Figure 7. Typical Application With Timed Delays

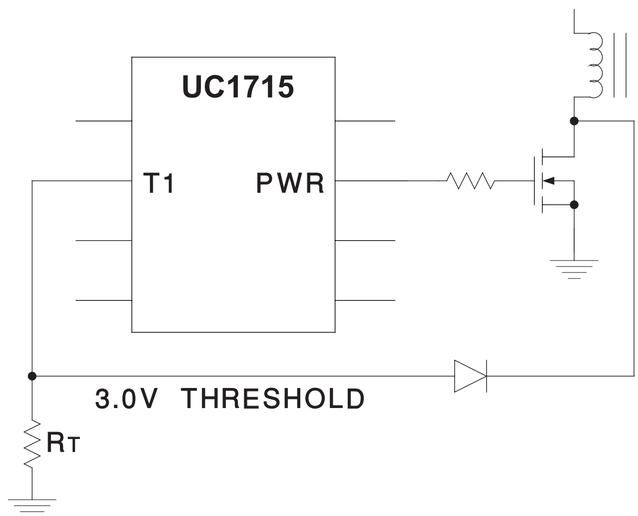


Figure 8. Using the Timer Input for Zero-Voltage Sensing

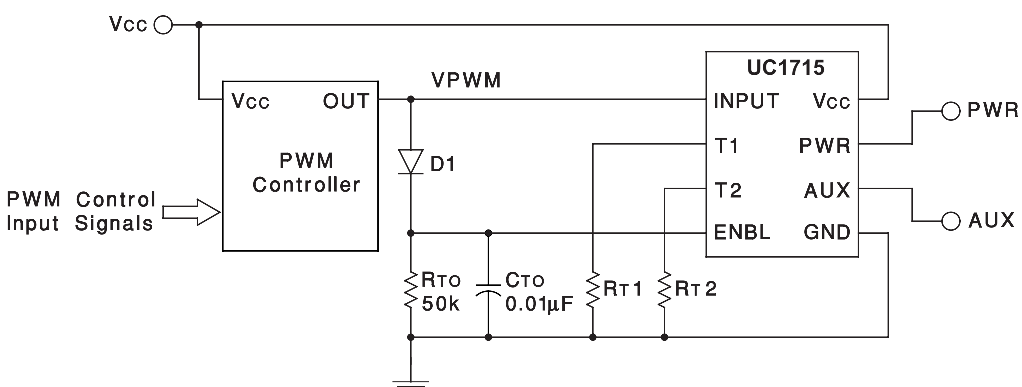


Figure 9. Self-Actuated Sleep Mode With Absence of Input PWM Signal. Wake Up Occurs With First Pulse While Turn-Off is Determined by the (RTO CTO) Time Constant

TYPICAL APPLICATIONS (continued)

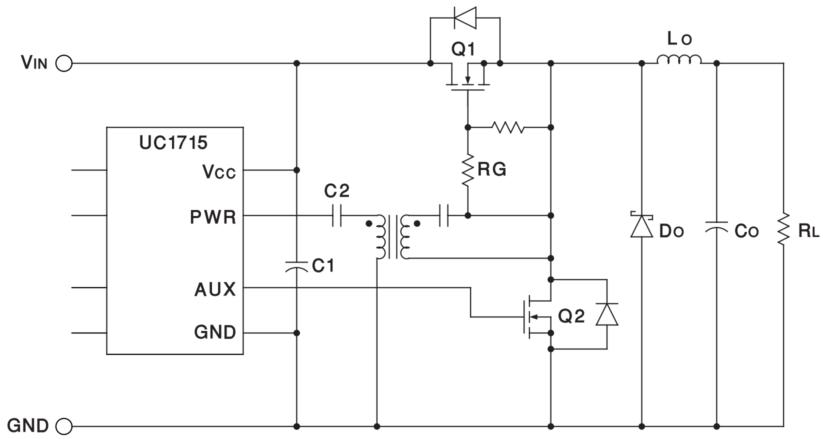


Figure 10. Using the UC1715 as a Complementary Synchronous Rectifier Switch Driver With N-Channel FETs

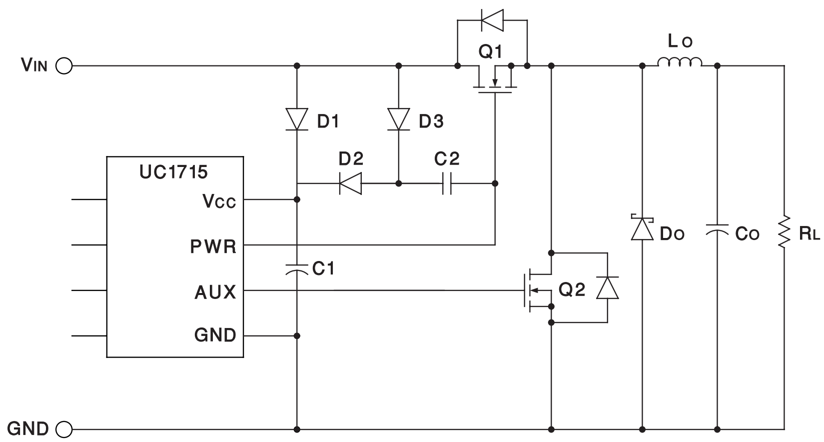


Figure 11. Synchronous Rectifier Application With Charge Pump to Drive High-Side N-Channel Buck Switch. V_{IN} is Limited to 10 V as V_{CC} Will Rise to Approximately $2V_{IN}$

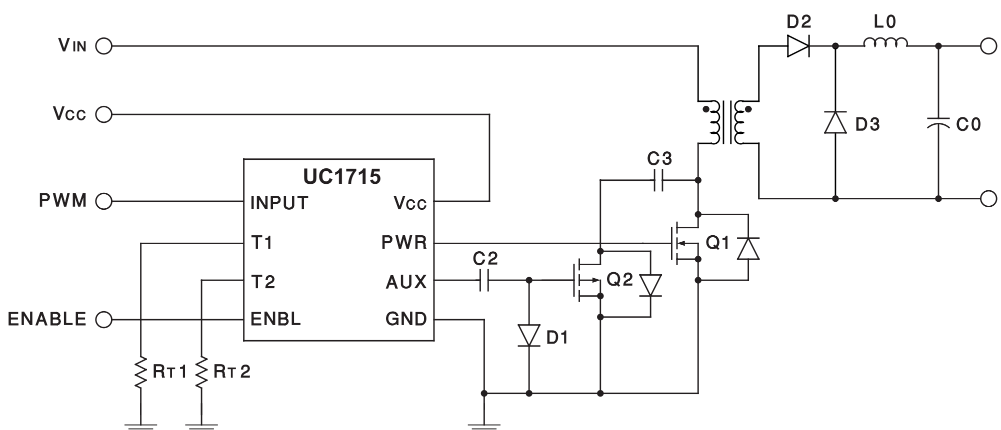


Figure 12. Typical Forward Converter Topology With Active Reset Provided by the UC1714 Driving N-channel switch (Q1) and P-Channel Auxilliary Switch (Q2)

TYPICAL APPLICATIONS (continued)

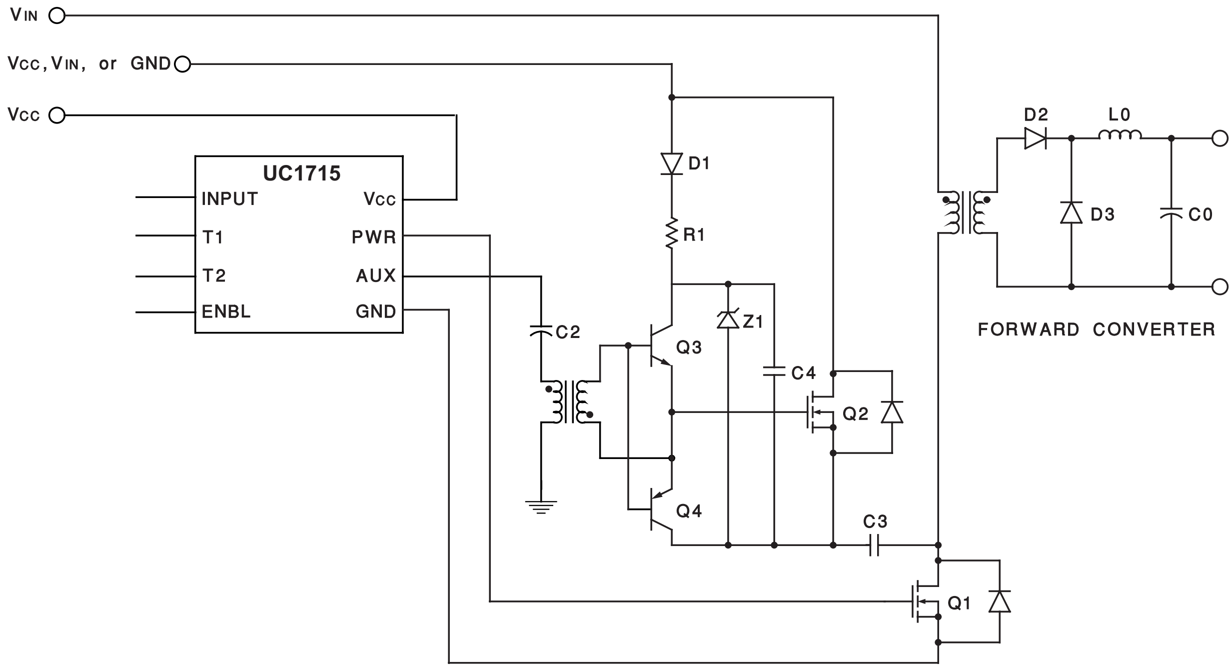


Figure 13. Using N-Channel Active Reset Switch With Floating Drive Command

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-0052102VFA	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-0052102VF A UC1715W-SP
5962-0052102VFA.A	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-0052102VF A UC1715W-SP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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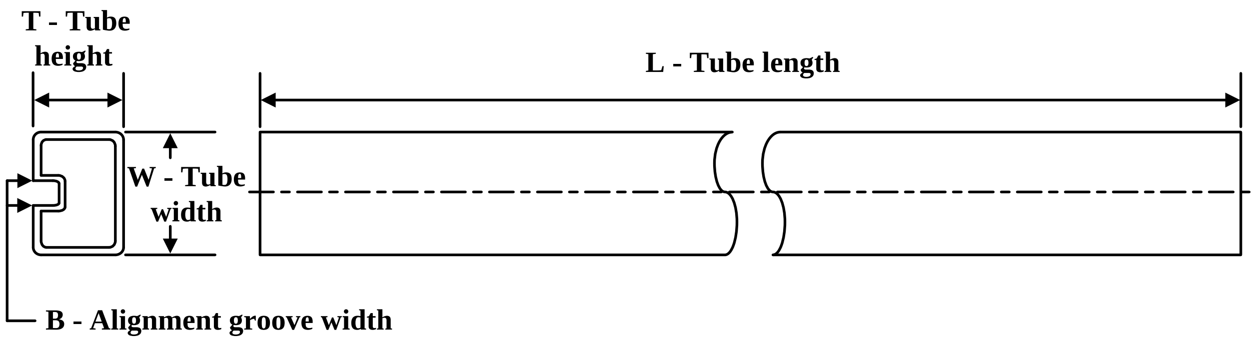
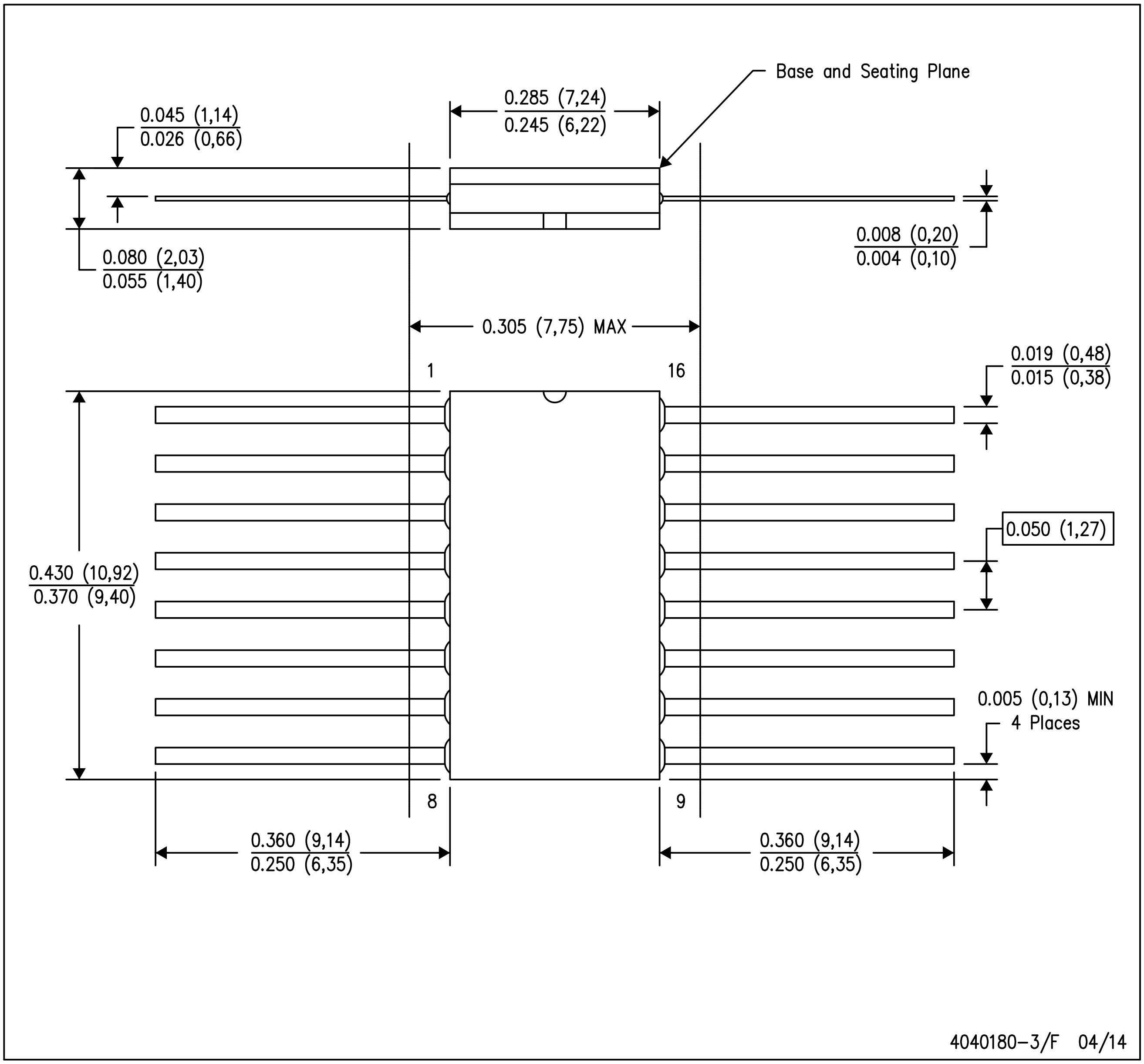
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-0052102VFA	W	CFP	16	25	506.98	26.16	6220	NA
5962-0052102VFA.A	W	CFP	16	25	506.98	26.16	6220	NA

W (R–GDFP–F16) CERAMIC DUAL FLATPACK



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP2–F16