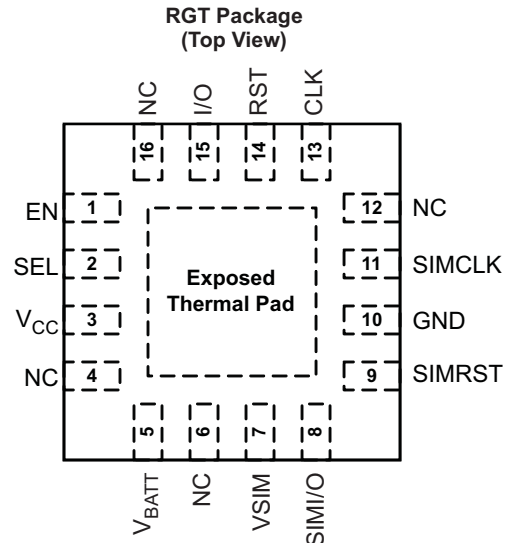


1.8V/3V SIM Card Power Supply With Level Translator

Check for Samples: [TXS4555](#)

FEATURES

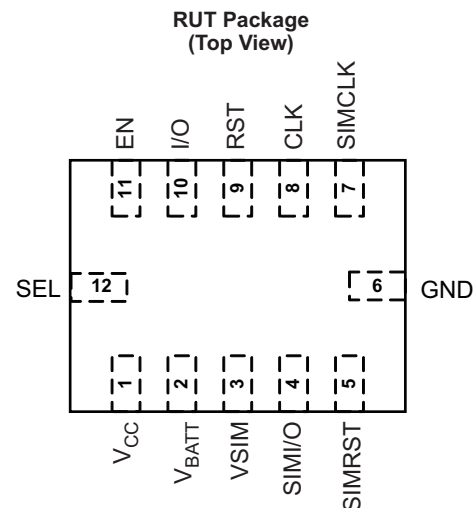
- **Level Translator**
 - V_{CC} Range of 1.65 V to 3.3 V
 - V_{BATT} Range from 2.3 to 5.5V
- **Low-Dropout (LDO) Regulator**
 - 50-mA LDO Regulator With Enable
 - 1.8-V or 2.95-V Selectable Output Voltage
 - 2.3-V to 5.5-V Input Voltage Range
 - Very Low Dropout: 100mV (Max) at 50mA
- **Incorporates Shutdown Feature for the SIM Card Signals According to ISO-7816-3**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-B)
 - 500-V Charged-Device Model (C101)
 - 8kV HBM for SIM Pins
- **Package**
 - 16-Pin QFN (3 mm x 3 mm)
 - 12-Pin QFN (2mm x 1.7mm)



Note: The Exposed center thermal pad must be connected to Ground

DESCRIPTION

The TXS4555 is a complete Smart Identity Module (SIM) card solution for interfacing wireless baseband processors with a SIM card to store I/O for mobile handset applications. The device complies with ISO/IEC Smart-Card Interface requirements as well as GSM and 3G mobile standards. It includes a high-speed level translator capable of supporting Class-B (2.95 V) and Class-C (1.8 V) interfaces, a low-dropout (LDO) voltage regulator that has output voltages that are selectable between 2.95-V Class-B and 1.8-V Class-C interfaces.



The device has two supply voltage pins. V_{CC} can be operated over the full range of 1.65 V to 3.3 V and V_{BATT} from 2.3 to 5.5 V. V_{PWR} is set to either 1.8 V or 2.95 V and is supplied by an internal LDO. The integrated LDO accepts input voltages as high as 5.5 V and outputs either 1.8 V or 2.95 V at 50 mA to the B-side circuitry and to the external SIM card. The TXS4555 enables system designers to easily interface low-voltage microprocessors to SIM cards operating at 1.8 V or 2.95 V.

The TXS4555 also incorporates shutdown sequence for the SIM card pins based on the ISO 7816-3 specification for SIM cards. Proper shutdown of the SIM card signals helps in prevention of corruption of data during accidental shutdown of the phone. The device also has 8kV HBM protection for the SIM pins and standard 2kV HBM protection for all the other pins.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

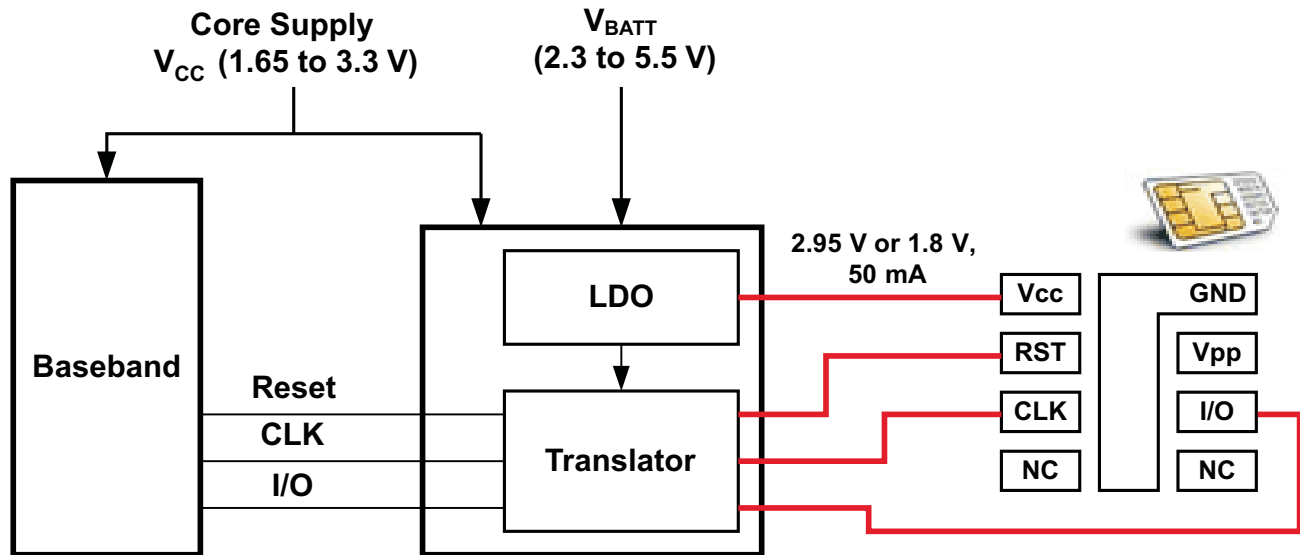


Figure 1. Interfacing with SIM Card

PIN FUNCTIONS

PIN NAME	PIN NO.		TYPE ⁽¹⁾	DESCRIPTION
	RGT	RUT		
EN	1	11	I	Enable/disable control input. Pull EN low to place all outputs in Hi-Z state and to disable the LDO. Referenced to VCC.
SEL	2	12	I	Pin to program VSIM value (Low = 1.8V, High = 2.95V)
Vcc	3	1	P	Power supply voltage which powers all A-port I/Os and control inputs
VBATT	5	2	P	Battery power supply
VSIM	7	3	O	SIM card Power-Supply pin (1.8V or 2.95V)
SIM_I/O	8	4	I/O	Bidirectional SIM I/O pin which connected to I/O pin of the SIM card connector
SIM_RST	9	5	O	SIM Reset pin which connects to RESET pin of the SIM card connector
GND	10	6	G	Ground
SIM_CLK	11	7	O	Clock signal pin which connects to CLK pin of the SIM card connector
CLK	13	8	I	Clock signal pin connected from baseband processor
RST	14	9	I	SIM Reset pin connected from baseband processor
I/O	15	10	I/O	Bidirectional SIM I/O pin which connected from baseband processor
NC	4, 6, 12, 16	–	NC	No Connects

(1) G = Ground, I = Input, O = Output, P = Power

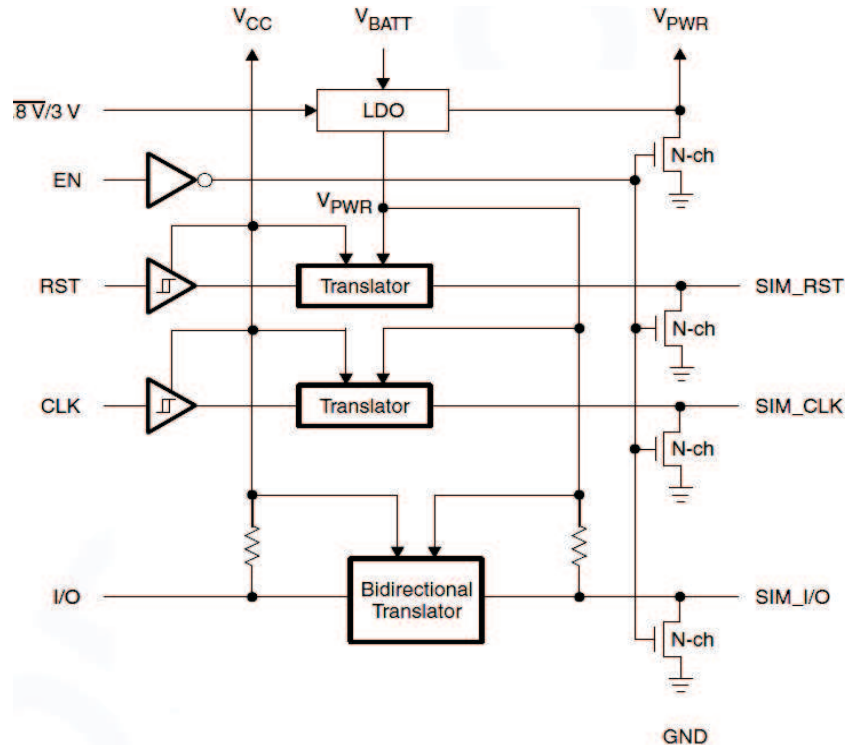


Figure 2. Block Diagram

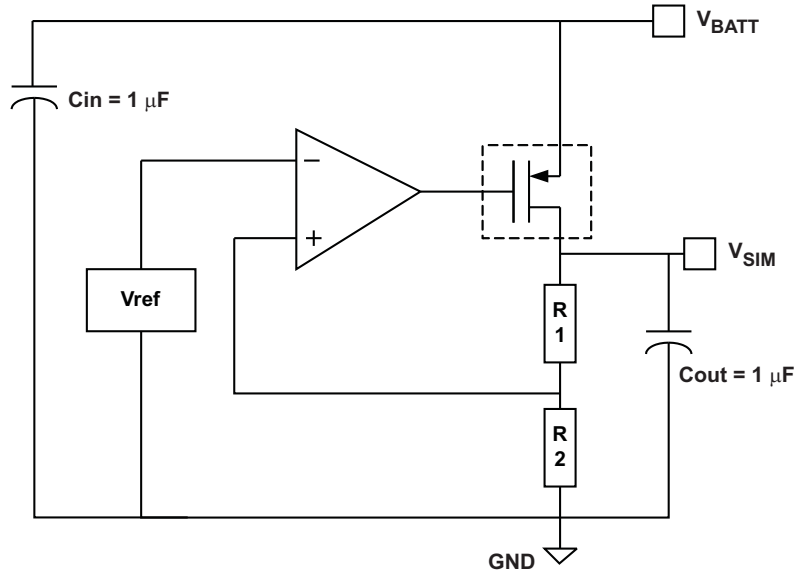


Figure 3. Block Diagram of the LDO

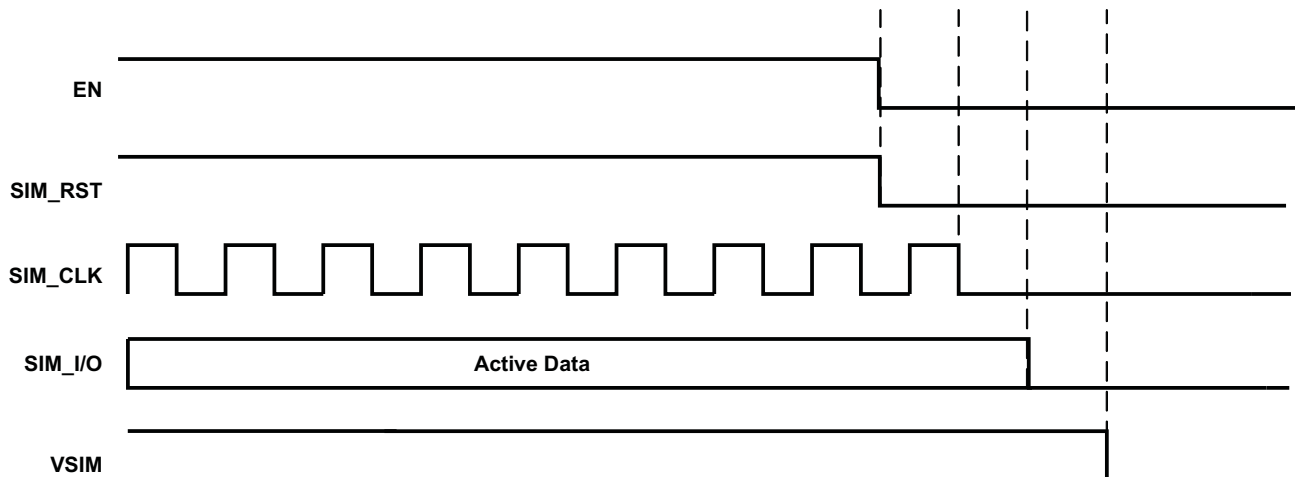


Figure 4. Shutdown Sequence for SIM_RST, SIM_CLK, SIM_IO and VSIM

The shutdown sequence for the SIM signals is based on the ISO 7816-3 specification. The shutdown sequence of these signals helps to properly disable these channels and not have any corruption of data accidentally. Also, this is also helpful when the SIM card is present in a hot swap slot and when pulling out the SIM card, the orderly shutdown of these signals help avoid any improper write/corruption of data.

When EN is taken low, the shutdown sequence happens by powering of the SIM_RST channel. Once that is achieved, SIM_CLK, SIM_I/O and VSIM are powered sequentially one by one. There is an internal 2K pull-down value on the SIM pins and helps to pull these channels low. The shutdown time sequence is in the order of a few microseconds. It is important that EN is taken low before VBAT and VCC supplies go low so that the shutdown sequence can be initiated properly.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			VALUE		UNIT	
			MIN	MAX		
LEVEL TRANSLATOR						
V _{CC}	Supply voltage range			−0.3	4.0	V
V _I	Input voltage range	V _{CC} -port		−0.5	4.6	V
		SIM-port		−0.5	4.6	
		Control inputs		−0.5	4.6	
V _O	Voltage range applied to any output in the high-impedance or power-off state	V _{CC} -port		−0.5	4.6	V
		VSIM-port		−0.5	4.6	
		Control inputs		−0.5	4.6	
V _O	Voltage range applied to any output in the high or low state	V _{CC} -port		−0.5	4.6	V
		SIM-port		−0.5	4.6	
		Control inputs		−0.5	4.6	
I _{IK}	Input clamp current	V _I < 0			−50	mA
I _{OK}	Output clamp current	V _O < 0			−50	mA
I _O	Continuous output current				±50	mA
	Continuous current through VCCA or GND				±100	mA
T _{stg}	Storage temperature range			−65	150	°C
LDO						
VBAT	Input voltage range			−0.3	6	V
V _{OUT}	Output voltage range			−0.3	6	V
	Peak output current			TBD		mA
	Continuous total power dissipation				TBD	
T _J	Junction temperature range			−55	150	°C
T _{stg}	Storage temperature range			−55	150	°C
	ESD rating (host side)	Human-Body Model (HBM)			2	kV
		Charged-Device Model (CDM)			500	V
	ESD rating (SIM side)	Human-Body Model (HBM)			8	kV

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		TXS4555		UNITS
		RGT	RUT	
		16 PINS	12 PINS	
θ _{JA}	Junction-to-ambient thermal resistance	47	87.2	°C/W
θ _{JB}	Junction-to-board thermal resistance	25.12	N/A	
ψ _{JT}	Junction-to-top characterization parameter	1.3	1.7	
θ _{JCbot}	Junction-to-case (bottom) thermal resistance	3.6	n/A	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

				MIN	MAX	UNIT
LEVEL TRANSLATOR						
V _{CC}	Supply voltage			1.65	3.3	V
V _{IH}	High-level input voltage	VCC - port	EN, SEL, RST, CLK, I/O	V _{CC} × 0.7	V _{CC}	V
		SIM - port	SIM_I/O	V _{sim} × 0.7	V _{sim}	
V _{IL}	Low-level input voltage	VCC - port	EN, SEL, RST, CLK, I/O	0	V _{CC} × 0.3	V
		SIM - port	SIM_I/O	0	V _{sim} × 0.3	
Δt/Δv	Input transition rise or fall rate				5	ns/V
T _A	Operating free-air temperature			–40	85	°C

(1) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

ELECTRICAL CHARACTERISTICS – LEVEL TRANSLATOR

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	V _{SIM}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	SIM_RST	I _{OH} = –1mA	1.65 V to 3.3 V	1.8 V / 2.95 V ⁽²⁾	V _{SIM} × 0.8			V
	SIM_CLK	I _{OH} = –1mA			V _{SIM} × 0.8			
	SIM_I/O	I _{OH} = –20 μA			V _{SIM} × 0.8			
	I/O	I _{OH} = –20 μA			V _{CC} × 0.8			
V _{OL}	SIM_RST	I _{OL} = 1 mA	1.65 V to 3.3 V	1.8 V / 2.95 V ⁽²⁾		V _{SIM} × 0.2		V
	SIM_CLK	I _{OL} = 1mA				V _{SIM} × 0.2		
	SIM_I/O	I _{OL} = 1 mA				0.3		
	I/O	I _{OL} = 1 mA				0.3		
I _I	Control inputs	V _I = EN, 1.8V/3V	1.65 V to 3.3 V	1.8 V / 2.95 V ⁽²⁾			±1	μA
I _{CC}	I/O	V _I = V _{CCI} , I _O = 0	1.65 V to 3.3 V	1.8 V / 2.95 V ⁽²⁾			±5	μA
C _{IO}	I/O port					8		pF
	SIM ports					4		
C _I	Control inputs	V _I = V _{CC} or GND				4		pF

(1) All typical values are at T_A = 25°C.

(2) (Supplied by LDO)

LDO ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{BAT}	Input voltage			2.3		5.5	V
V _{SIM}	Output voltage	Class-B Mode (SEL = V _{CC})		2.85	2.95	3.05	V
		Class-C Mode (SEL = 0)		1.7	1.8	1.9	
V _{DO}	Dropout voltage	I _{OUT} = 50 mA				100	mV
I _{GND}	Ground-pin current	I _{OUT} = 0 mA				35	μA
I _{SHDN}	Shutdown current (IGND)	V _{ENx} ≤ 0.4 V, (V _{SIM} + V _{DO}) ≤ V _{BAT} ≤ 5.5 V, T _J = 85°C				3.5	μA
I _{OUT(SC)}	Short-circuit current	R _L = 0 Ω			145		mA
C _{OUT}	Output Capacitor				1		μF
PSRR	Power-supply rejection ratio	V _{BAT} = 3.25 V, V _{SIM} = 1.8 V or 2.95 V, C _{OUT} = 1 μF, I _{OUT} = 50 mA	f = 1 kHz	50			dB
			f = 10 kHz	40			
T _{STR}	Start-up time	V _{SIM} = 1.8 V or 2.95 V, I _{OUT} = 50 mA, C _{OUT} = 1 μF				400	μS
T _J	Operating junction temperature			–40		125	°C

(1) All typical values are at T_A = 25°C.

GENERAL ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R _{I/OPU}	I/O pull-up		16	20	24	kΩ
R _{SIMPU}	SIM_I/O pull-up		10	14	18	kΩ
R _{SIMPD}	SIM_I/O pull-down	Active pull-downs are connected to the VSIM regulator output to the SIM_CLK, SIM_RST, SIM_I/O when EN = 0			3	kΩ

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V		UNIT
			MIN	MAX	
VSIM = 1.8 V or 2.95 V SUPPLIED BY INTERNAL LDO					
t _{rA}	SIM_I/O	C _L = 50 pF	1		μs
t _{rB}	SIM_RST		1		μs
	SIM_CLK		18		ns
	SIM_I/O		1		us
f _{max}	SIM_CLK		25		MHz
Duty Cycle	SIM_CLK		40%	60%	

OPERATING CHARACTERISTICS

T_A = 25°C, V_{SIM} = 1.8 V

PARAMETER		TEST CONDITIONS	V _{CC} TYP	UNIT
			1.8 V	
C _{pdA} ⁽¹⁾	Class B	C _L = 0, f = 5 MHz, t _r = t _f = 1 ns	13	pF
	Class C		11	

(1) Power dissipation capacitance per transceiver.

TYPICAL CHARACTERISTICS

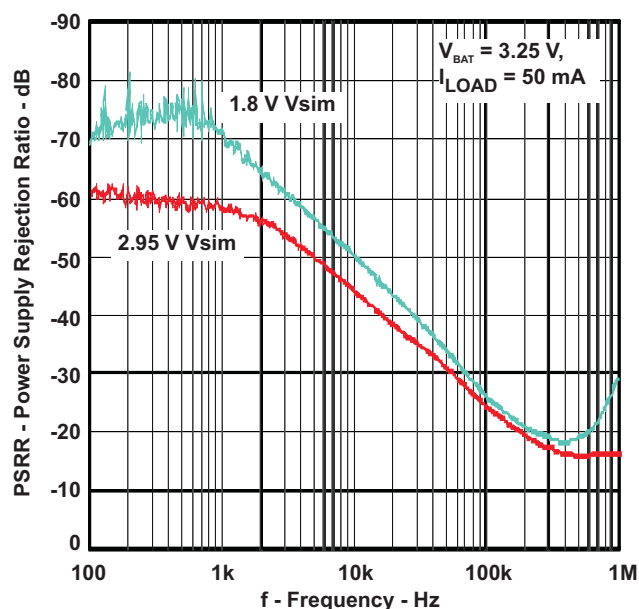


Figure 5. PSRR

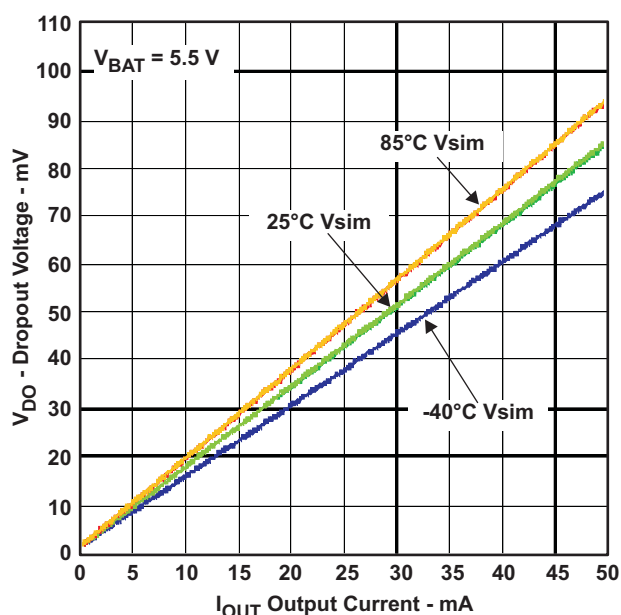


Figure 6. Dropout Voltage vs Output Current

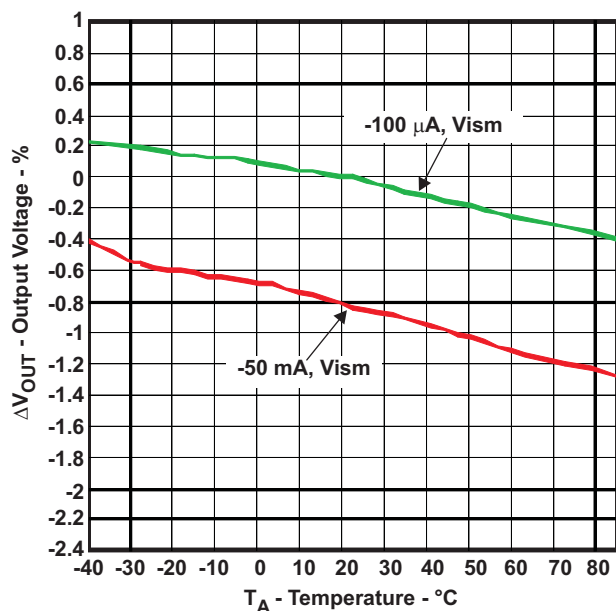
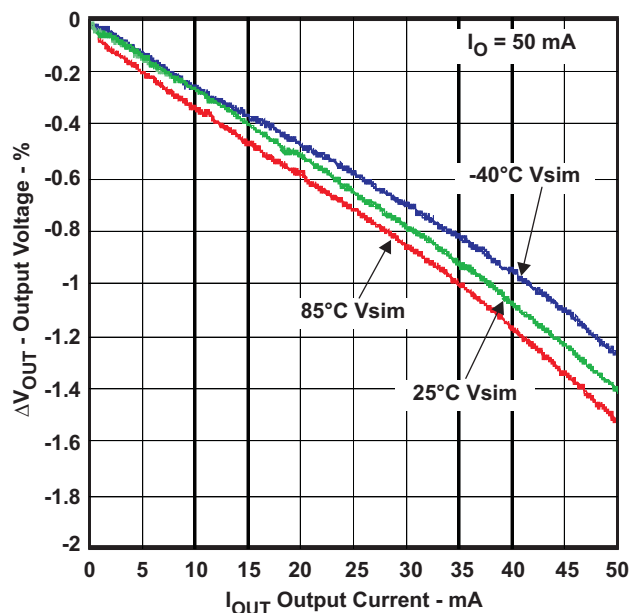


Figure 7. Output Voltage vs Temperature, Class-B/C

Figure 8. Load Regulation, I_{OUT} = 50 mA, Class-C

APPLICATION INFORMATION

The LDO's included on the TXS4555 achieve ultra-wide bandwidth and high loop gain, resulting in extremely high PSRR at very low headroom ($V_{BAT} - V_{SIM}$). The TXS4555 provides fixed regulation at 1.8V or 2.95V. Low noise, enable, low ground pin current make it ideal for portable applications. The device offers sub-bandgap output voltages, current limit and thermal protection, and is fully specified from -40°C to 125°C .

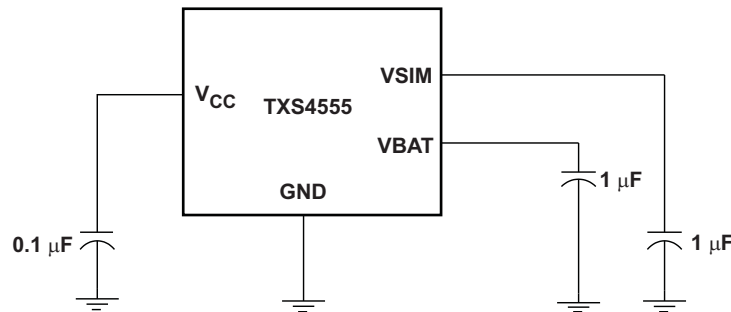


Figure 9. Typical Application Circuit for TXS4555

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

It is good analog design practice to connect a $1.0\ \mu\text{F}$ low equivalent series resistance (ESR) capacitor across the input supply (VBAT) near the regulator. Also, a $0.1\ \mu\text{F}$ is required for the logic core supply (VDDIO).

This capacitor will counteract reactive input sources and improve transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or if the device is located several inches from the power source. The LDO's are designed to be stable with standard ceramic capacitors of values $1.0\ \mu\text{F}$ or larger. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be $< 1.0\ \Omega$.

OUTPUT NOISE

In most LDO's, the bandgap is the dominant noise source. To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT} , with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

INTERNAL CURRENT LIMIT

The TXS4555 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current limit state for extended periods of time.

The PMOS pass element in the TXS4555 has a built-in body diode that conducts current when the voltage at VSIM exceeds the voltage at VBAT. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

DROPOUT VOLTAGE

The TXS4555 uses a PMOS pass transistor to achieve low dropout. When $(V_{BAT} - V_{SIM})$ is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} will approximately scale with output current because the PMOS device behaves like a resistor in dropout.

STARTUP

The TXS4555 uses a quick-start circuit which allows the combination of very low output noise and fast start-up times.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

MINIMUM LOAD

The TXS4555 is stable and well-behaved with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TXS4555 employs an innovative low-current mode circuit to increase loop gain under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current.

THERMAL INFORMATION

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage because of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TXS4555 has been designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the TXS4555 into thermal shutdown will degrade device reliability.

REVISION HISTORY

Changes from Revision A (March 2011) to Revision B	Page
• Removed Ordering Information table.	2
• Updated V_{IH} and V_{IL} to specify additional information.	6

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TXS4555RGTR	Active	Production	VQFN (RGT) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZUT
TXS4555RGTR.B	Active	Production	VQFN (RGT) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZUT
TXS4555RUTR	Active	Production	UQFN (RUT) 12	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	69R
TXS4555RUTR.B	Active	Production	UQFN (RUT) 12	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	69R

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

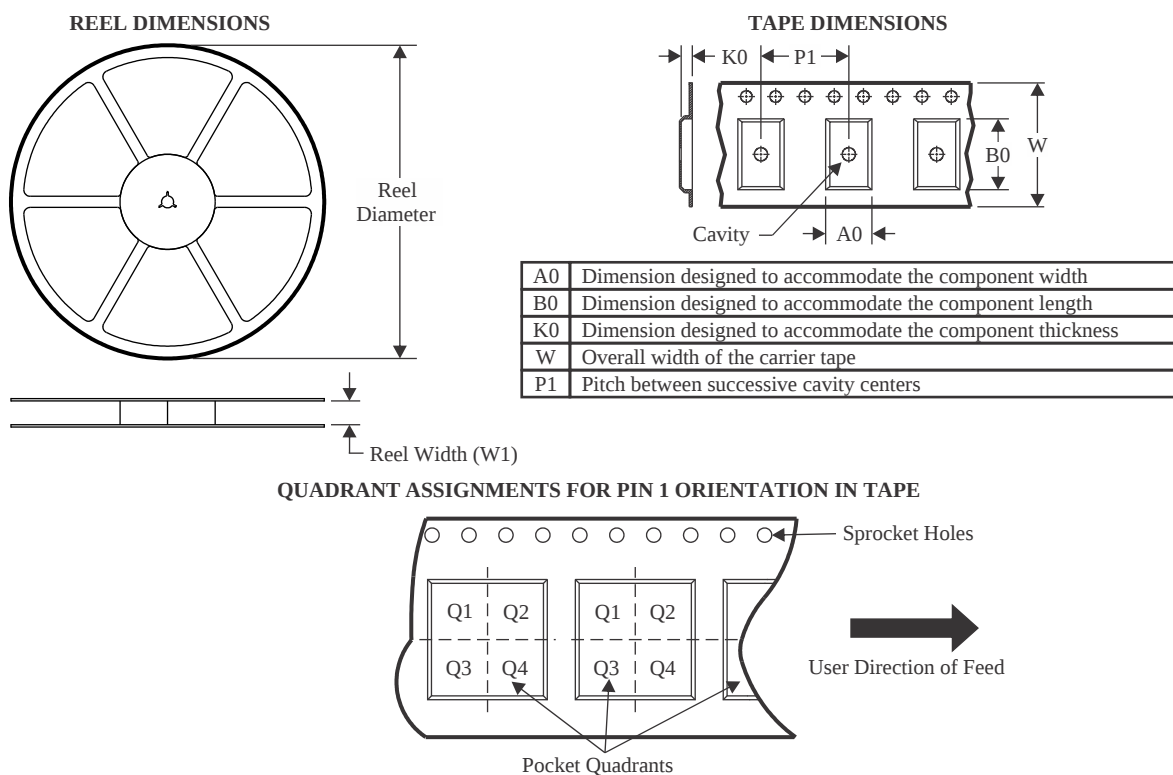
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

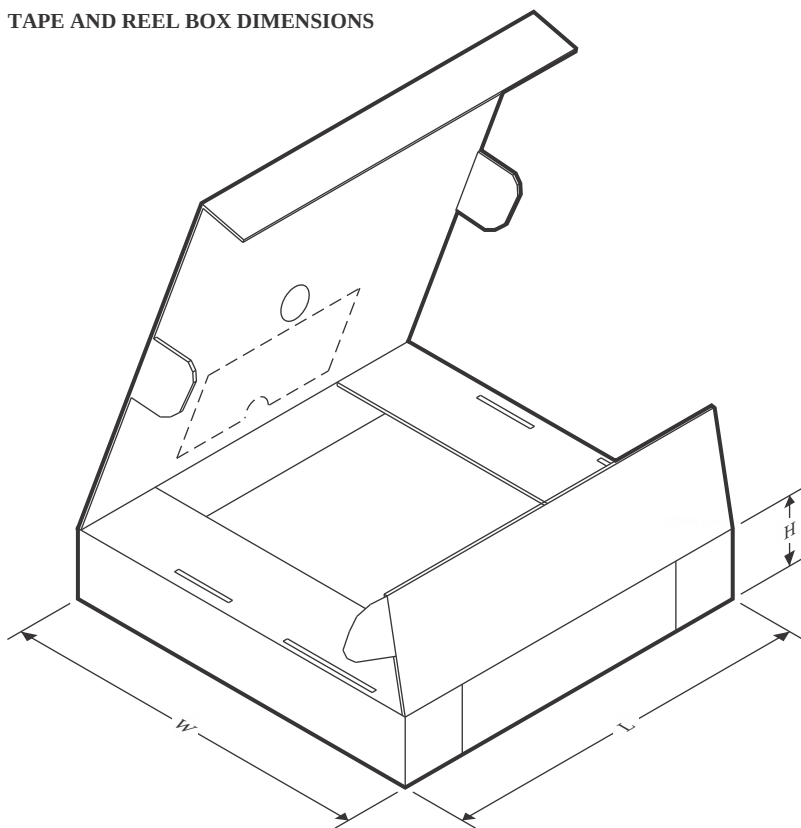
TAPE AND REEL INFORMATION



*All dimensions are nominal

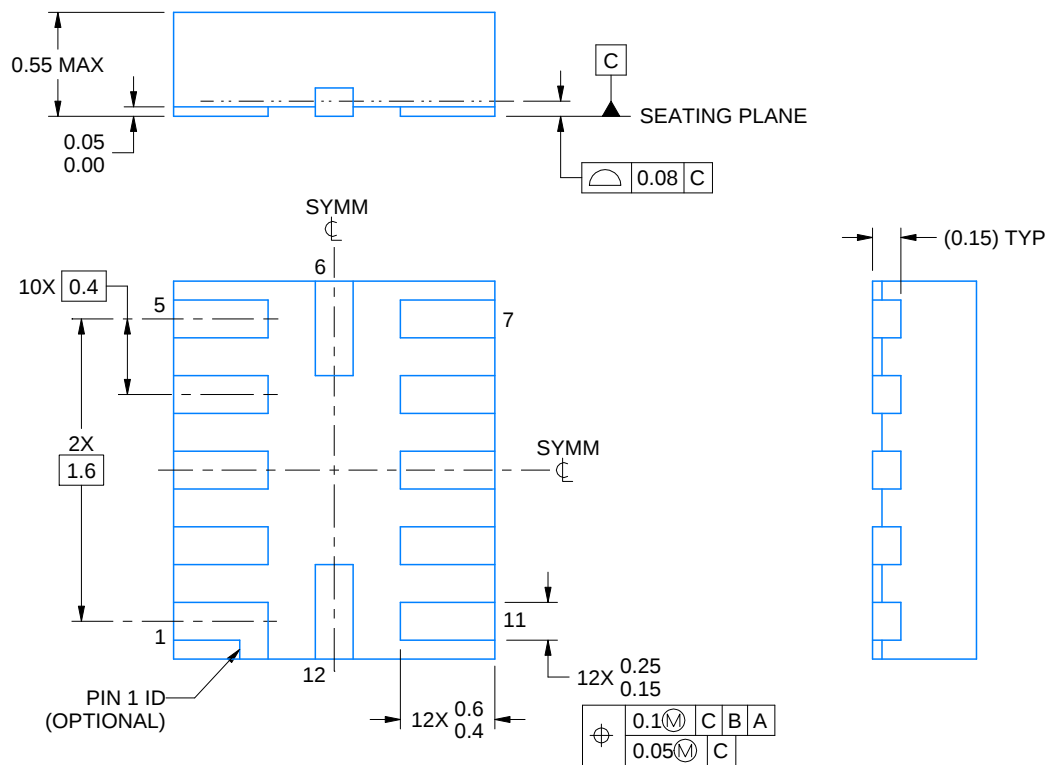
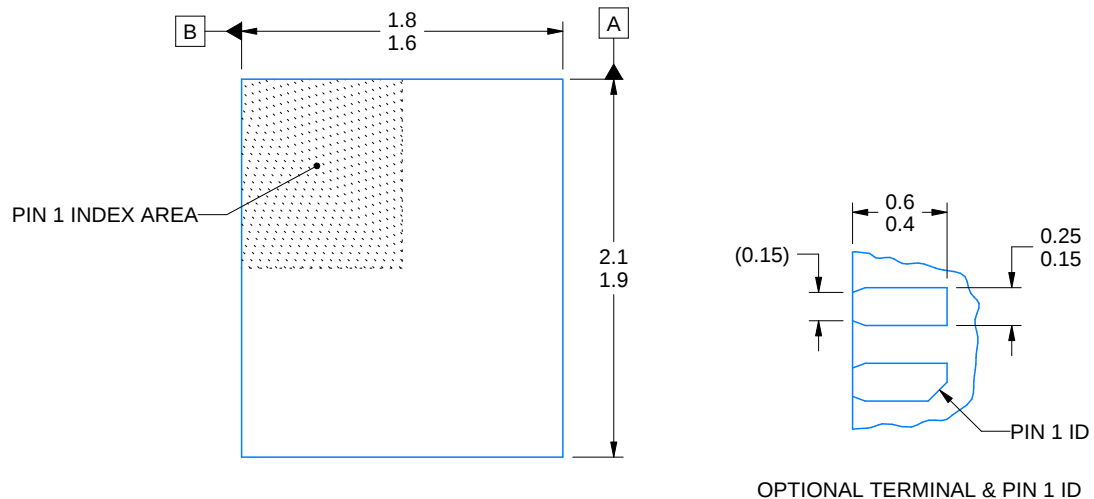
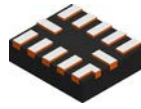
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS4555RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TXS4555RUTR	UQFN	RUT	12	3000	180.0	8.4	1.95	2.3	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS4555RGTR	VQFN	RGT	16	3000	353.0	353.0	32.0
TXS4555RUTR	UQFN	RUT	12	3000	202.0	201.0	28.0



4220310/A 11/2016

NOTES:

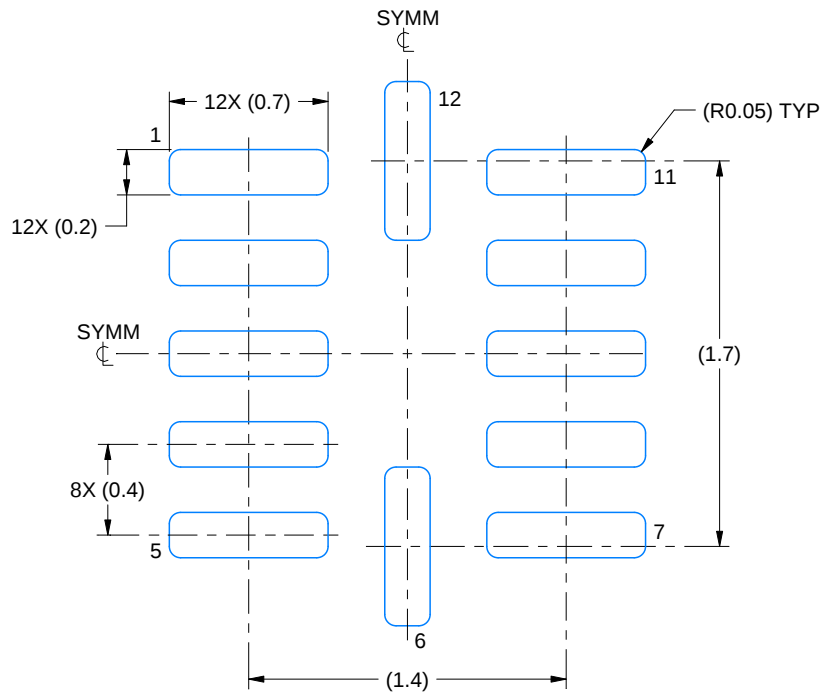
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

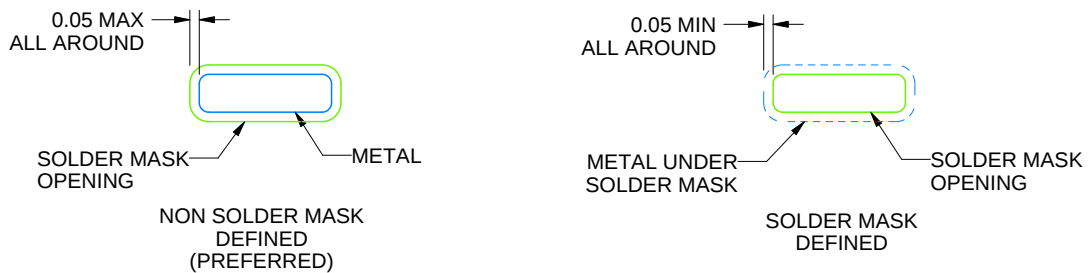
RUT0012A

UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS

4220310/A 11/2016

NOTES: (continued)

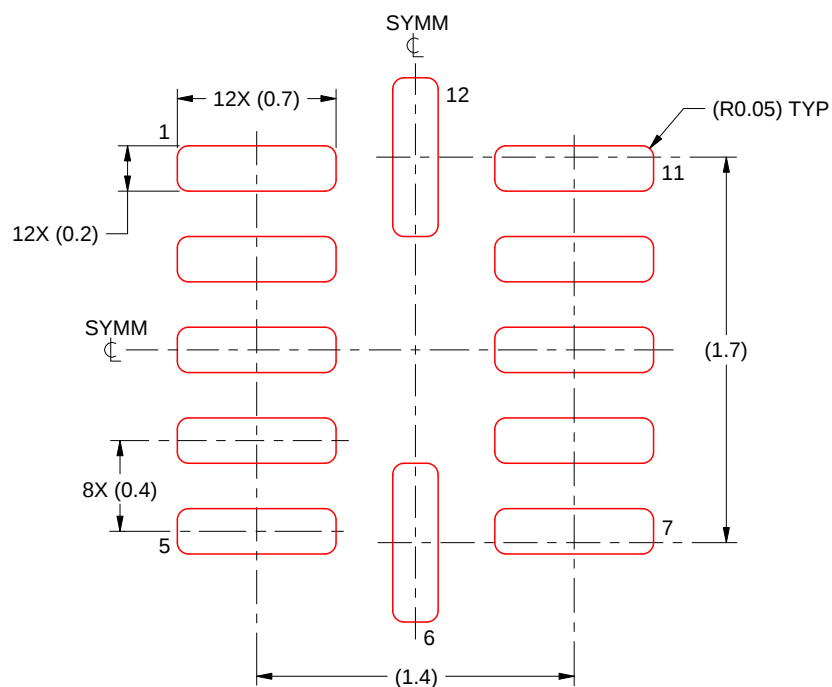
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

RUT0012A

UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

4220310/A 11/2016

NOTES: (continued)

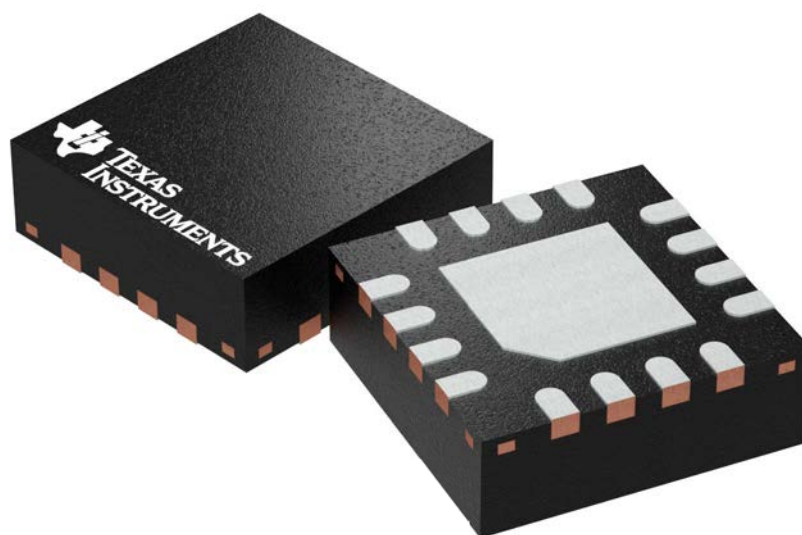
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RGT 16

GENERIC PACKAGE VIEW

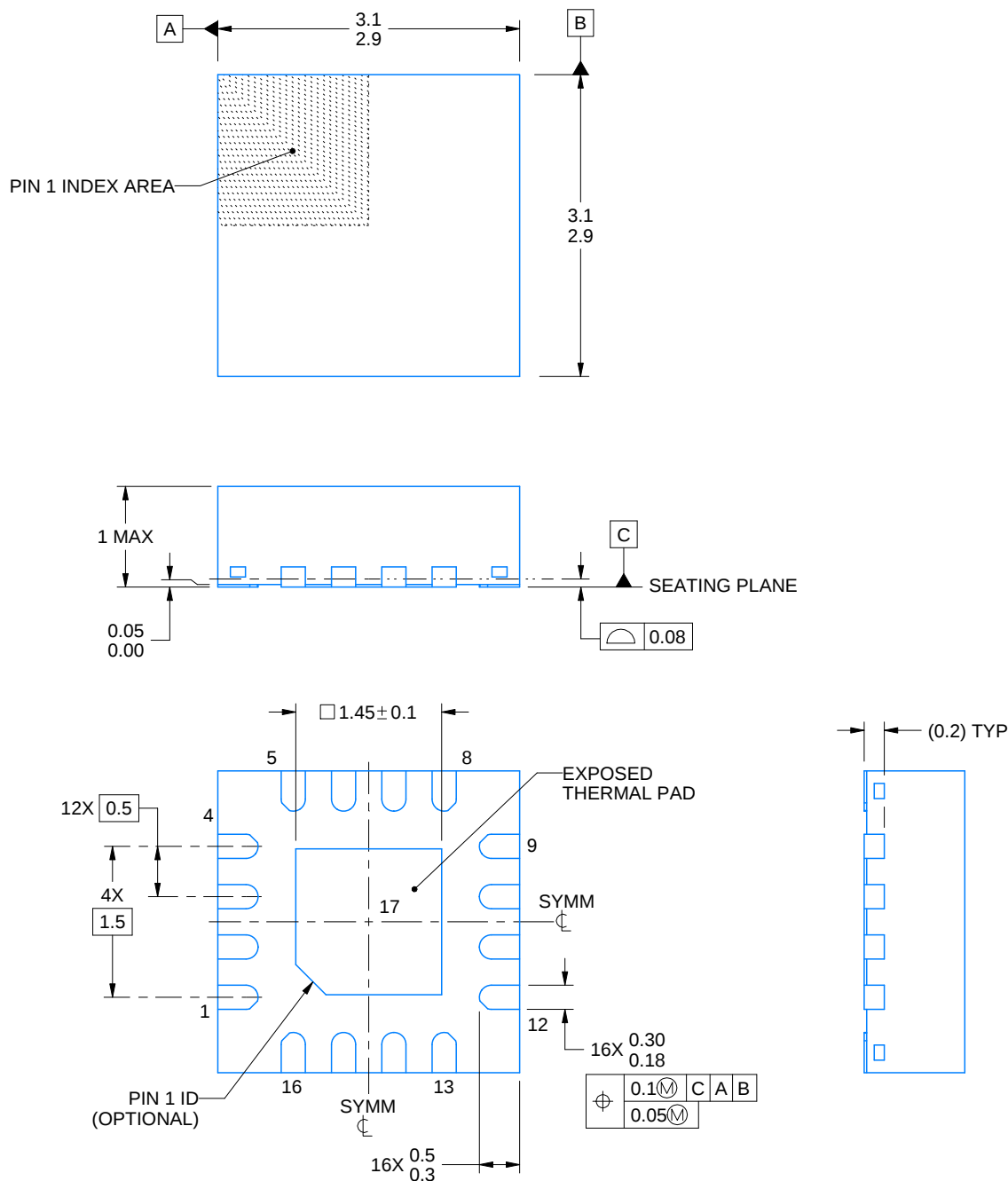
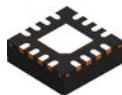
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203495/1



4219032/A 02/2017

NOTES:

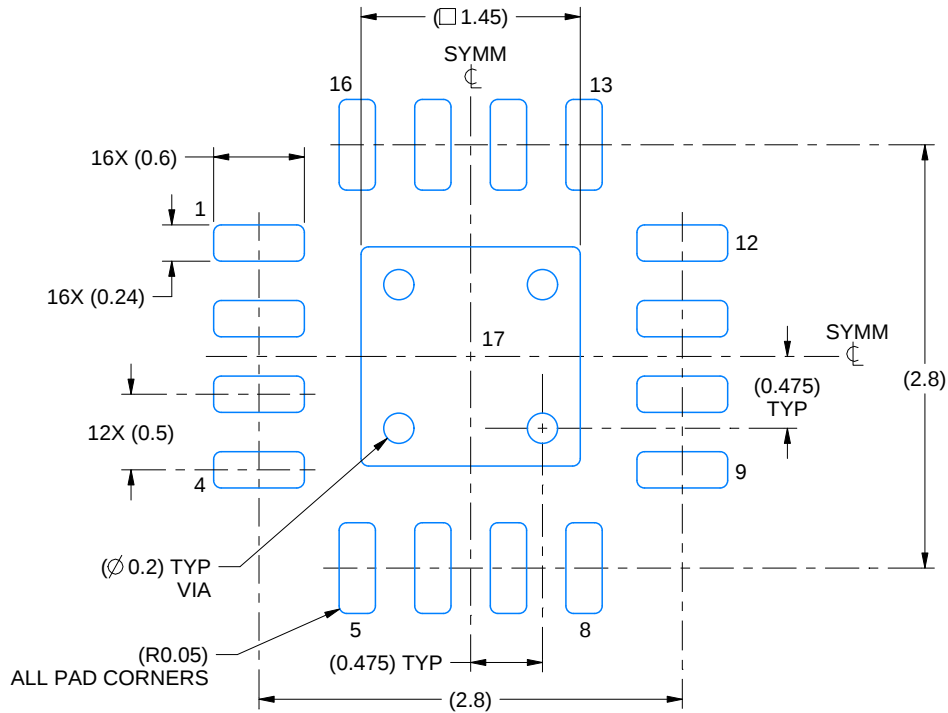
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220

EXAMPLE BOARD LAYOUT

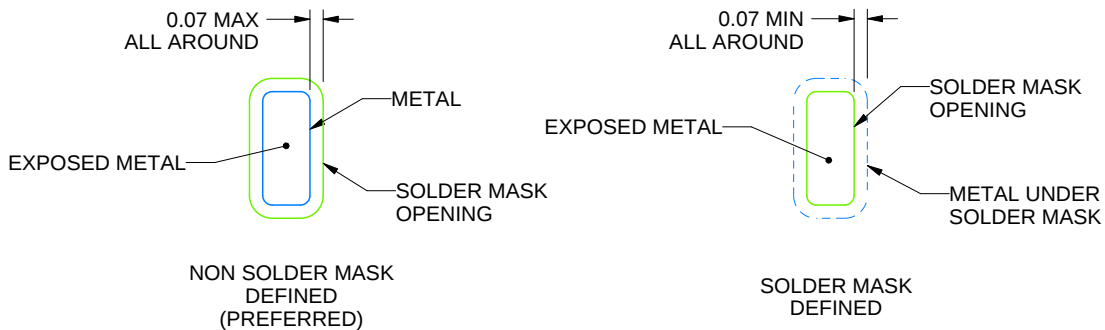
RGT0016A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4219032/A 02/2017

NOTES: (continued)

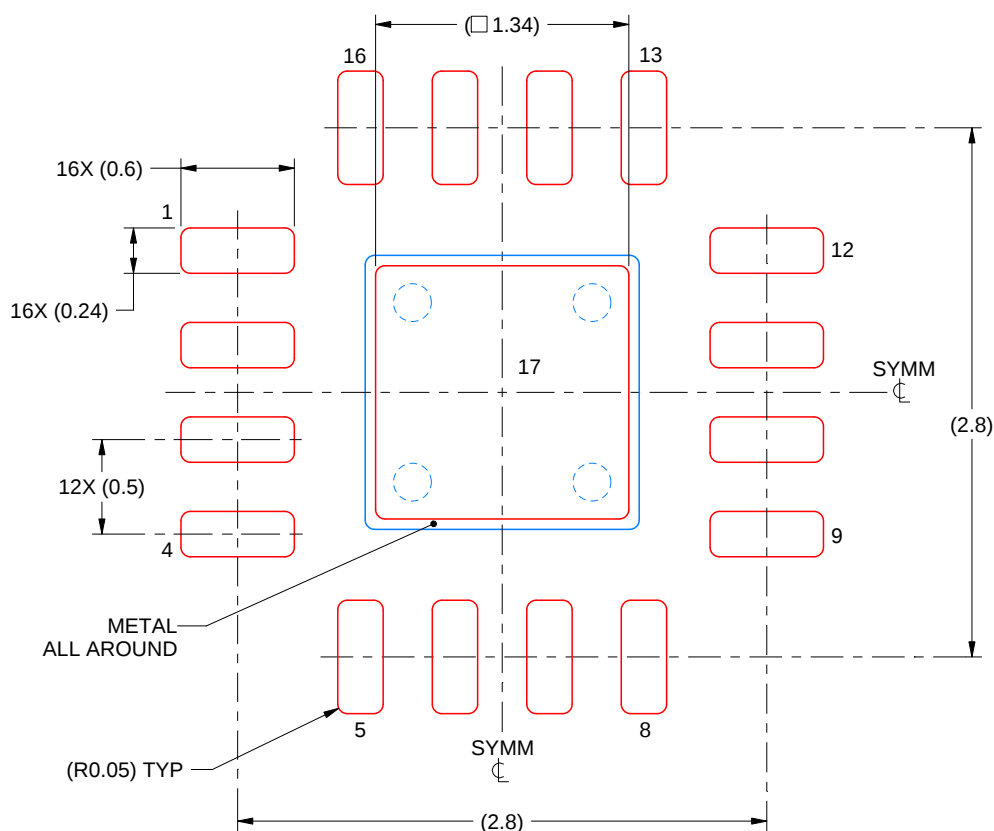
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGT0016A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
 86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
 SCALE:25X

4219032/A 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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