









TXS0104V SCES964 - JUNE 2024

TXS0104V 4-Bit Bi-directional, Level-Shifting, Voltage Translator for Open-Drain and **Push-Pull Applications**

1 Features

- No direction-control signal needed
- Maximum data rates:
 - 24Mbps (push pull)
 - 2Mbps (open drain)
- 1.65V to 3.6V on A port and 2.3V to 5.5V on B port $(V_{CCA} \leq V_{CCB})$
- No power-supply sequencing required V_{CCA} or V_{CCB} can be ramped first
- Latch-up performance exceeds 100mA per JESD 78, class II
- ESD protection exceeds JESD 22:
 - A port:
 - 2000V Human-Body Model (A114-B)
 - 500V Charged-Device Model (C101)
 - B port:
 - 5000V Human-Body Model (A114-B)
 - 500V Charged-Device Model (C101)

2 Applications

- Handset
- **Smartphone**
- **Tablet**
- **Desktop PC**

3 Description

This 4-bit non-inverting translator uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.65V to 3.6V. V_{CCA} must be less than or equal to V_{CCB}. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 2.3V to 5.5V. This allows for low-voltage bidirectional translation between any of the 1.8V, 2.5V, 3.3V, and 5V voltage nodes.

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state.

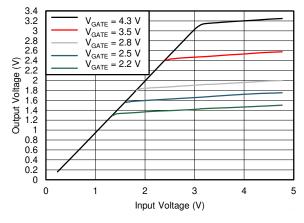
The TXS0104V is designed so that the OE input circuit is supplied by V_{CCA}.

For the high-impedance state during power up or power down, tie OE to GND through a pull-down resistor; the current-sourcing capability of the driver determines the minimum value of the resistor.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
	PW (TSSOP, 14)	5mm × 6.4mm
	BQA (WQFN, 12)	3mm × 2.5mm
TXS0104V	RUT (UQFN, 12)	2mm × 1.7mm
	RGY (VQFN, 14)	3.5mm × 3.5mm
	D (SOIC, 14)	8.65mm × 6mm

- For more information, see Section 11. (1)
- The package size (length × width) is a nominal value and includes pins, where applicable.



Transfer Characteristics of an N-Channel Transistor

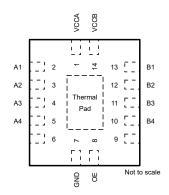


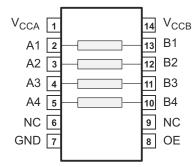
Table of Contents

1 Features1	7.1 Overview1	3
2 Applications 1	7.2 Functional Block Diagram1	
3 Description1	7.3 Feature Description1	
4 Pin Configuration and Functions3	7.4 Device Functional Modes1	
5 Specifications5	8 Application and Implementation1	Ę
5.1 Absolute Maximum Ratings5	8.1 Application Information1	Ę
5.2 ESD Ratings5	8.2 Typical Application1	Ę
5.3 Recommended Operating Conditions5	8.3 Power Supply Recommendations1	7
5.4 Thermal Information (PW, RGY, BQA, RUT, D)6	8.4 Layout1	7
5.5 Electrical Characteristics6	9 Device and Documentation Support1	8
5.6 Switching Characteristics, V _{CCA} = 1.8 ± 0.15V7	9.1 Documentation Support1	8
5.7 Switching Characteristics, V _{CCA} = 2.5 ± 0.2V	9.2 Receiving Notification of Documentation Updates1	8
5.8 Switching Characteristics, V _{CCA} = 3.3 ± 0.3V8	9.3 Support Resources1	8
5.9 Switching Characteristics: T _{sk} , T _{MAX} 9	9.4 Trademarks1	8
5.10 Typical Characteristics9	9.5 Electrostatic Discharge Caution1	8
6 Parameter Measurement Information11	9.6 Glossary1	8
6.1 Load Circuits11	10 Revision History1	
6.2 Voltage Waveforms12	11 Mechanical, Packaging, and Orderable	
7 Detailed Description13	Information1	8



4 Pin Configuration and Functions



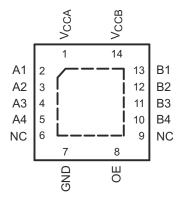


NC - No internal connection

Figure 4-2. D and PW Package, 14-Pin SOIC and TSSOP (Top View)

NC - No internal connection

Figure 4-1. BQA Package, 14-Pin WQFN (Top View)



NC - No internal connection

PIN

Figure 4-3. RGY Package, 14-Pin VQFN (Top View)

Table 4-1. Pin Functions: BQA, PW, D, or RGY

TYPE(1) **DESCRIPTION** NAME NO. Α1 2 I/O Input/output A1. Referenced to V_{CCA}. A2 Input/output A2. Referenced to V_{CCA}. 3 I/O А3 4 I/O Input/output A3. Referenced to V_{CCA}. A4 I/O 5 Input/output A4. Referenced to V_{CCA}. Input/output B1. Referenced to V_{CCB}. В1 13 I/O

B2	12	I/O	Input/output B2. Referenced to V _{CCB} .
В3	11	I/O	Input/output B3. Referenced to V _{CCB} .
B4	10	I/O	Input/output B4. Referenced to V _{CCB} .
GND	7	_	Ground
OE	8	I	3-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA} .
V _{CCA}	1	_	A-port supply voltage. $1.65V \le V_{CCA} \le 3.6V$ and $V_{CCA} \le V_{CCB}$.
V _{CCB}	14	_	B-port supply voltage. $2.3V \le V_{CCB} \le 5.5V$.
Thermal Pa	ad	_	For the RGY package, the exposed center thermal pad must be connected to ground

(1) I = input, O = output



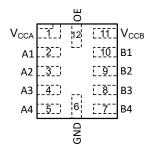


Figure 4-4. RUT Package, 12-Pin UQFN (Transparent Top View)

Table 4-2. Pin Functions: RUT

Р	IN	TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.	ITPE(*)	DESCRIPTION
A1	2	I/O	Input/output A1. Referenced to V _{CCA} .
A2	3	I/O	Input/output A2. Referenced to V _{CCA} .
A3	4	I/O	Input/output A3. Referenced to V _{CCA} .
A4	5	I/O	Input/output A4. Referenced to V _{CCA} .
B1	10	I/O	Input/output B1. Referenced to V _{CCB} .
B2	9	I/O	Input/output B2. Referenced to V _{CCB} .
В3	8	I/O	Input/output B3. Referenced to V _{CCB} .
B4	7	I/O	Input/output B4. Referenced to V _{CCB} .
GND	6	_	Ground
OE	12	I	3-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA} .
V _{CCA}	1	_	A-port supply voltage. $1.65 \text{V} \le \text{V}_{\text{CCA}} \le 3.6 \text{V}$ and $\text{V}_{\text{CCA}} \le \text{V}_{\text{CCB}}$.
V _{CCB}	11	_	B-port supply voltage. $2.3V \le V_{CCB} \le 5.5V$.

⁽¹⁾ I = input, O = output



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CCA}	Supply voltage A		-0.5	4.6	V
V _{CCB}	Supply voltage B		-0.5	6.5	V
		I/O Ports (A Port)	-0.5	4.6	
V _I	Input Voltage ⁽²⁾	I/O Ports (B Port)	-0.5	6.5	V
		OE	-0.5	4.6	
V	V-14	A Port	-0.5	4.6	V
Vo	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾	B Port	-0.5	6.5	, v
V	V-16	A Port	-0.5	V _{CCA} + 0.5	
Vo	Voltage applied to any output in the high or low state ^{(2) (3)}	B Port	-0.5	V _{CCB} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current		-50	50	mA
	Continuous current through V _{CC} or GND		-100	100	mA
Tj	Junction Temperature			150	°C
T _{stg}	Storage temperature		-65	150	°C

- (1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 6.5V maximum if the output current rating is observed.

5.2 ESD Ratings

				VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	A Port	±2000	
\ <u></u>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC 33-00 TV	B Port	±5000	.,
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	A Port	±500	V
		Charged device model (CDIVI), per ANSI/ESDA/JEDEC 35-002	B Port	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

		,	V _{CCA}	V _{CCB}	MIN	MAX	UNIT
V _{CCA}	Supply voltage A			•	1.65	3.6	V
V _{CCB}	Supply voltage B				2.3	5.5	V
		A-port I/O's	1.65V to 1.95V	2.3V to 5.5V	V _{CCI} - 0.2	V _{CCI}	
	High-level input voltage	A-port 1/O's	2.3V to 3.6V	2.3V to 5.5V	V _{CCI} - 0.4	V _{CCI}	V
V _{IH}	I lightever input voltage	B-port I/O's	1.65V to 3.6V	2.3V to 5.5V	V _{CCI} - 0.4	V _{CCI}	
		OE Input	1.65V to 3.6V	2.3V to 5.5V	V _{CCA} x 0.65	5.5	
		A-port I/O's	1.65V to 3.6V	2.3V to 5.5V		0.2	
V _{IL}	Low-level input voltage	B-port I/O's	1.65V to 3.6V	2.3V to 5.5V		0.2	V
		OE Input	1.65V to 3.6V	2.3V to 5.5V		V _{CCA} x 0.35	
Δt/Δν	Input transition rise and fall time	Push-Pull Driving	1.65V to 3.6V	2.3V to 5.5V		10	ns/V
T _A	Operating free-air temperature	•			-40	85	°C

- (1) V_{CCI} is the V_{CC} associated with the input port.
- V_{CCO} is the V_{CC} associated with the output port.



All control inputs and data I/Os of this device have weak pulldowns to ensure the line is not floating when undefined external to the device. The input leakage from these weak pulldowns is defined by the I_I specification indicated under Electrical Characteristics.

5.4 Thermal Information (PW, RGY, BQA, RUT, D)

				TXS0104V			
	THERMAL METRIC(1)	PW (TSSOP)	RGY (VQFN)	BQA (WQFN)	RUT (UQFN)	D (SOIC)	UNIT
		14 PINS	14 PINS	14 PINS	12 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.2	52.9	73.5	150.4	93.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	46.2	54.3	76.9	68.6	53.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.9	28.4	43.0	76.3	52.0	°C/W
Y _{JT}	Junction-to-top characterization parameter	3.4	2.7	4.7	2.4	13.4	°C/W
Y _{JB}	Junction-to-board characterization parameter	70.2	28.3	42.9	76.2	51.6	°C/W
R _θ JC(bottom)	Junction-to-case (bottom) thermal resistance	N/A	12.0	19.6	N/A	N/A	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1) (2)

					0	perating	free-aiı	temperati	ure (T _A)		
	PARAMETER	TEST CONDITIONS	V _{CCA}	V _{CCB}		25°C		-40°	C to 85°	С	UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{OHA}	Port A output high voltage (3)	I _{OH} = -20μA	1.65V to 3.6V	2.3V to 5.5V	V _{CCA} x 0.8			V _{CCA} x 0.8			V
V _{OLA}	Low-level output voltage (4)	I _{OL} = 1mA	1.65V to 3.6V	2.3V to 5.5V			0.4			0.4	V
V _{OHB}	Port B output high voltage	I _{OH} = -20μA	1.65V to 3.6V	2.3V to 5.5V	V _{CCB} x 0.8			V _{CCB} x 0.8			V
V _{OLB}	Low-level output voltage (4)	I _{OL} = 1mA	1.65V to 3.6V	2.3V to 5.5V			0.4			0.4	V
I	Input leakage current	OE V _I = V _{CC} or GND	1.65V to 3.6V	2.3V to 5.5V	-2		2	-10		10	μA
I _{OZ}	Tri-state output current	A or B Port: $V_I = V_{CCI}$ or GND $V_O = V_{CCO}$ or GND OE = GND	1.65V to 3.6V	2.3V to 5.5V	-1		1	-10		10	μA
			1.65V to V _{CCB}	2.3V to 5.5V			2.4			3.3	
I _{CCA}	V _{CCA} supply current	$V_I = V_{CCI}$ or GND $I_O = 0$	0V	5.5V	-3			-3			μA
	Current	10 - 0	3.6V	0V			2.2			2.2	
			1.65V to V _{CCB}	2.3V to 5.5V			12			12	
I _{CCB}	V _{CCB} supply current	$V_I = V_{CCI}$ or GND $I_O = 0$	0V	5.5V			5			5	μA
	Garrent	10 - 0	3.6V	0V	-1			-1			
I _{CCA} + I _{CCB}	Combined supply current	V _I = V _{CCI} or GND I _O = 0	1.65V to V _{CCB}	2.3V to 5.5V			15			15	μA
C _i	Control Input Capacitance	V _I = 3.3V or GND	3.3V	3.3V			6			6	pF
C _{io}	Data I/O Capacitance	A or B Port	3.3V	3.3V		5	6.5		12	16.5	pF

⁽¹⁾

 V_{CCI} is the V_{CC} associated with the input port V_{CCO} is the V_{CC} associated with the output port (2)

Tested at $V_I = V_{T+(MAX)}$ (3)



(4) Tested at V_I = V_{T-(MIN)}

5.6 Switching Characteristics, $V_{CCA} = 1.8 \pm 0.15V$

over operating free-air temperature range (unless otherwise noted)

							B-l	Port Sup	ply Volta	age (V _C	ов)			
	PARAMETER	FROM	то	Test Conditions	2	.5 ± 0.2V	'	3	.3 ± 0.3V	,	5	.0 ± 0.5V	'	UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t _{PHL}	Propagation Delay (Hight-to-Low)			Push-Pull		4			4			5		ns
t _{PHL}	Propagation Delay (Hight-to-Low)		В	Open-Drain		8.8			9.6			10		ns
t _{PLH}	Propagation Delay (Low-to-High)	A	В	Push-Pull		6			6			6		ns
t _{PLH}	Propagation Delay (Low-to-High)			Open-Drain		200			160			120		ns
t _{PHL}	Propagation Delay (Hight-to-Low)			Push-Pull		4			4		4			ns
t _{PHL}	Propagation Delay (Hight-to-Low)			Open-Drain	5.3		4.4			4.1			ns	
t _{PLH}	Propagation Delay (Low-to-High)	– B	A	Push-Pull		5		4			4			ns
t _{PLH}	Propagation Delay (Low-to-High)			Open-Drain		173		120		9/		90		ns
t _{en}	Enable Time	OE	A or B	-40°C to 85°C		200			200			200		ns
t _{dis}	Disable Time	OE	A or B	-40°C to 85°C		250			250			250		ns
t _{rA}	Ouput Rise Time	В	^	Push-Pull		9			9			7		ns
t _{rA}	Ouput Rise Time	В	A	Open-Drain		150			120			80		ns
t _{rB}	Ouput Rise Time	_	В	Push-Pull		10			9			7		ns
t _{rB}	Ouput Rise Time	A	В	Open-Drain	145			106			58		ns	
t _{fA}	Output Fall Time	_		Push-Pull		5			5			5		ns
t _{fA}	Output Fall Time	В	A	Open-Drain	6		6				6		ns	
t _{fB}	Output Fall Time	1	Б	Push-Pull		7			7			8		ns
t _{fB}	Output Fall Time	A	В	Open-Drain		13			16			16		ns

5.7 Switching Characteristics, $V_{CCA} = 2.5 \pm 0.2V$

over operating free-air temperature range (unless otherwise noted)

		B-Port Supply Voltage (V _{CCB})												
	PARAMETER	FROM	то	Test Conditions	2.5 ± 0.2V			3	3.3 ± 0.3V	'	5	.0 ± 0.5V	'	UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t _{PHL}	Propagation Delay (Hight-to-Low)			Push-Pull		3			3.4			5		ns
t _{PHL}	Propagation Delay (Hight-to-Low)		В	Open-Drain		6.3			6			5.8		ns
t _{PHL}	Propagation Delay (Hight-to-Low)	A	В	Push-Pull		3			4			4		ns
t _{PHL}	Propagation Delay (Hight-to-Low)			Open-Drain		200		160			120			ns
t _{PHL}	Propagation Delay (Hight-to-Low)			Push-Pull		3			3			4		ns
t _{PHL}	Propagation Delay (Hight-to-Low)	В	A	Open-Drain		4.7			4.2			4		ns
t _{PHL}	Propagation Delay (Hight-to-Low)			Push-Pull	2.1		2.1 2		2			1.9		ns
t _{PHL}	Propagation Delay (Hight-to-Low)			Open-Drain		173			120			90		ns
t _{en}	Enable Time	OE	A or B	-40°C to 85°C		200			200			200		ns



5.7 Switching Characteristics, $V_{CCA} = 2.5 \pm 0.2V$ (continued)

over operating free-air temperature range (unless otherwise noted)

							B-l	Port Sup	ply Volt	age (V _{CC}	:в)			
	PARAMETER	FROM	то	Test Conditions	2	.5 ± 0.2V	'	3	.3 ± 0.3\	′	5	.0 ± 0.5V	,	UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t _{dis}	Disable Time	OE	A or B	-40°C to 85°C		250			250			250		ns
t _{rA}	Ouput Rise Time	В	^	Push-Pull		7			6			5		ns
t _{rA}	Ouput Rise Time]	Α	Open-Drain		149			101			63		ns
t _{rB}	Ouput Rise Time	^	В	Push-Pull		8			7			6		ns
t _{rB}	Ouput Rise Time	A		Open-Drain		150			101			63		ns
t _{fA}	Output Fall Time	В	^	Push-Pull		5.1			5.2			5		ns
t _{fA}	Output Fall Time]	Α	Open-Drain		6			6			5		ns
t _{fB}	Output Fall Time	^	В	Push-Pull		7			6.4			8.7		ns
t _{fB}	Output Fall Time	A		Open-Drain		8			9			10		ns

5.8 Switching Characteristics, $V_{CCA} = 3.3 \pm 0.3V$

over operating free-air temperature range (unless otherwise noted)

	perating nee-all tempe			,		B-Por	t Supply	Voltage (V	ссв)		
	PARAMETER	FROM	то	Test Conditions	3	3.3 ± 0.3V		5	.0 ± 0.5V		UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t _{PHL}	Propagation Delay (Hight-to-Low)			Push-Pull		2.4			3.1		
t _{PHL}	Propagation Delay (Hight-to-Low)	A	В	Open-Drain		4.2			4.6		no
t _{PLH}	Propagation Delay (Low-to-High)		Б	Push-Pull		4.2		4.4			ns
t _{PLH}	Propagation Delay (Low-to-High)			Open-Drain		160		120			ı
t _{PHL}	Propagation Delay (Hight-to-Low)			Push-Pull		2.5			3.3		ns
t _{PHL}	Propagation Delay (Hight-to-Low)	В	A	Open-Drain		4.5		4			ns
t _{PLH}	Propagation Delay (Low-to-High)	B		Push-Pull		2.5			2.6		ns
t _{PLH}	Propagation Delay (Low-to-High)			Open-Drain		139			105		ns
t _{en}	Enable Time	OE	A or B	-40°C to 85°C		200		200		200	
t _{dis}	Disable Time	OE	A or B	-40°C to 85°C		250			250		ns
t _{rA}	Ouput Rise Time	В	Α	Push-Pull		5			4		ns
t _{rA}	Ouput Rise Time] D	A	Open-Drain		116			85		ns
t _{rB}	Ouput Rise Time	_	В	Push-Pull		6			7		ns
t _{rB}	Ouput Rise Time	A	В	Open-Drain		116		116			ns
t _{fA}	Output Fall Time	В	Α	Push-Pull		8			7.6		ns
t _{fA}	Output Fall Time]	^	Open-Drain		6		5			ns
t _{fB}	Output Fall Time	_	В	Push-Pull		8.2			10.8		ns
t _{fB}	Output Fall Time	A	D	Open-Drain		7			8		ns

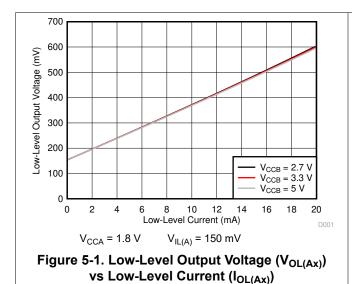


5.9 Switching Characteristics: T_{sk} , T_{MAX}

over operating free-air temperature range (unless otherwise noted)

			V _{CCA}			Operating free-air temperature (T _A) -40°C to 85°C			
PARAMETER	TEST CON	DITIONS		V _{CCB}	-40°				
					MIN	TYP	MAX		
		Push-Pull Driving	1.8 ± 0.15V	2.5V ± 0.2V			18		
TMAX - Maximum Data Rate	50% Duty Cycle Input One channel switching	Push-Pull Driving	1.8 ± 0.15V	3.3V ± 0.3V			21	Mbps	
	one ename enmening	Push-Pull Driving	1.8 ± 0.15V	5V ± 0.5V			23		
		Push-Pull Driving	2.5V ± 0.2V	2.5V ± 0.2V			20		
TMAX - Maximum Data Rate	50% Duty Cycle Input One channel switching	Push-Pull Driving	2.5V ± 0.2V	3.3V ± 0.3V			22	Mbps	
raio	One onamer switching	Push-Pull Driving	2.5V ± 0.2V	5V ± 0.5V		24			
TMAX - Maximum Data	50% Duty Cycle Input	Push-Pull Driving	3.3V ± 0.3V	3.3V ± 0.3V			22	N 41	
Rate	One channel switching	Push-Pull Driving	3.3V ± 0.3V	5V ± 0.5V	5V ± 0.5V		24	Mbps	
		Open-Drain Driving	1.8 ± 0.15V	2.5V ± 0.2V			2		
TMAX - Maximum Data Rate	50% Duty Cycle Input One channel switching	Open-Drain Driving	1.8 ± 0.15V	3.3V ± 0.3V		2		Mbps	
T tato	- Cine cinaminer emiterining	Open-Drain Driving	1.8 ± 0.15V	5V ± 0.5V		2			
		Open-Drain Driving	2.5V ± 0.2V	2.5V ± 0.2V			2		
TMAX - Maximum Data Rate	50% Duty Cycle Input One channel switching	Open-Drain Driving	2.5V ± 0.2V	3.3V ± 0.3V		2		Mbps	
T tato		Open-Drain Driving	2.5V ± 0.2V	5V ± 0.5V			2		
TMAX - Maximum Data	50% Duty Cycle Input	Open-Drain Driving	3.3V ± 0.3V	3.3V ± 0.3V			2	N 41	
Rate	One channel switching	Open-Drain Driving	3.3V ± 0.3V	5V ± 0.5V			2	Mbps	
	Pulse Duration, Data	Push-Pull Driving	1.65V to 3.3V	2.3V to 5.5V	500				
t _w	Inputs	Open-Drain Driving	1.65V to 3.3V	2.3V to 5.5V				ns	
t Output skow	Skew between any two outputs of the same			2.3V to 5.5V		1			
t _{sk} - Output skew	package switching in the same direction	Open-Drain Driving	1.65V to 3.3V	2.3V to 5.5V			1	ns	

5.10 Typical Characteristics



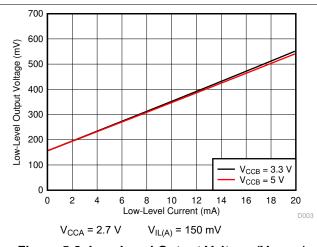
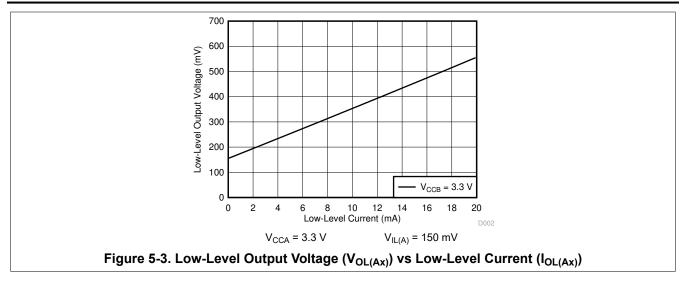


Figure 5-2. Low-Level Output Voltage $(V_{OL(Ax)})$ vs Low-Level Current $(I_{OL(Ax)})$





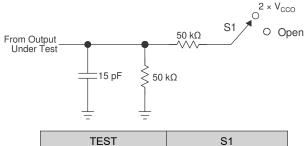
6 Parameter Measurement Information

6.1 Load Circuits



Figure 6-1. Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Propagation Delay, Output Rise-Time and Fall-Time Measurement Using a Push-Pull Driver

Figure 6-2. Data Rate, Pulse Duration, Measurement Using an Open-Drain Driver



TEST	S1
t _{PZL} / t _{PLZ} (t _{dis})	2 × V _{CCO}
t _{PHZ} / t _{PZH} (t _{en})	Open

Figure 6-3. Load Circuit for Enable-Time and Disable-Time Measurement

- 1. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- 2. $\,\,t_{PZL}$ and t_{PZH} are the same as $t_{en}.$
- 3. V_{CCI} is the V_{CC} associated with the input port.
- 4. V_{CCO} is the V_{CC} associated with the output port.



6.2 Voltage Waveforms

The outputs are measured one at a time, with one transition per measurement. All input pulses are supplied by generators that have the following characteristics:

- PRR ≤ 10MHz
- $Z_O = 50\Omega$
- dv/dt ≥ 1V/ns

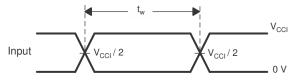


Figure 6-4. Pulse Duration

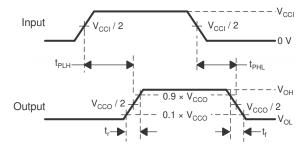
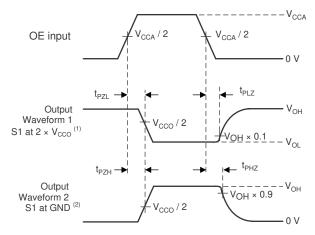


Figure 6-5. Propagation Delay Times



- A. Waveform 1 is for an output with internal such that the output is high, except when OE is high (see Figure 6-3).
- B. Waveform 2 is for an output with conditions such that the output is low, except when OE is high.

Figure 6-6. Enable and Disable Times

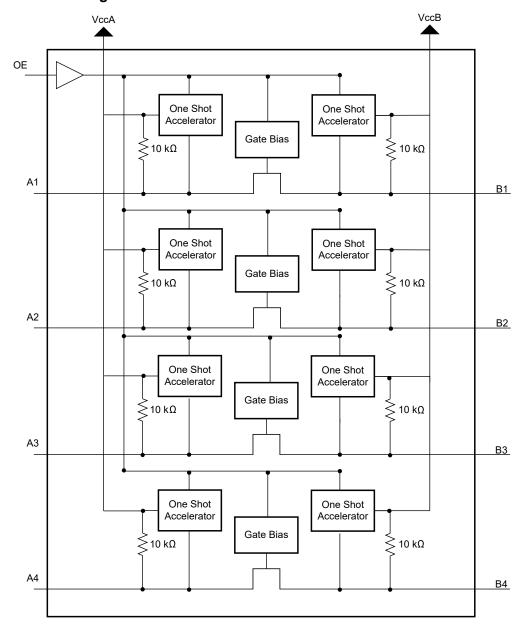


7 Detailed Description

7.1 Overview

The TXS0104V device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.65V to 3.6V, while the B port can accept I/O voltages from 2.3V to 5.5V. The device is a pass gate architecture with edge rate accelerators (one shots) to improve the overall data rate. $10k\Omega$ pullup resistors, commonly used in open drain applications, have been conveniently integrated so that an external resistor is not needed. While this device is designed for open drain applications, the device can also translate push-pull CMOS logic outputs.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Architecture

The TXS0104V architecture (see Figure 7-1) does not require a direction-control signal to control the direction of data flow from A to B or from B to A.

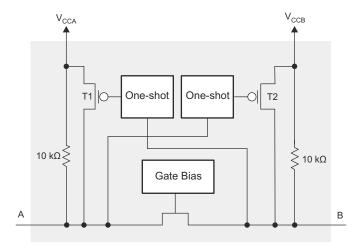


Figure 7-1. Architecture of a TXS0104V Cell

Each A-port I/O has an internal $10k\Omega$ pullup resistor to V_{CCA} , and each B-port I/O has an internal $10k\Omega$ pullup resistor to V_{CCB}. The output one-shots detect rising edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1 and T2) for a short duration which speeds up the low-to-high transition.

7.3.2 Input Driver Requirements

The fall time (t_{fA} and t_{fB}) of a signal depends on the output impedance of the external device driving the data I/Os of the TXS0104V device. Similarly, the t_{PHL} and maximum data rates also depend on the output impedance of the external driver. The values for tfA, tfB, tPHL, and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50Ω .

7.3.3 Power Up

During operation, ensure that $V_{CCA} \le V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \ge V_{CCB}$ does not damage the device, so any power supply can be ramped up first.

7.3.4 Enable and Disable

The TXS0104V device has an OE input that disables the device by setting OE low, which places all I/Os in the high-impedance state. The disable time (t_{dis}) indicates the delay between the time when the OE pin goes low and when the outputs actually enter the high-impedance state. The enable time (ten) indicates the amount of time the user must allow for the one-shot circuitry to become operational after the OE pin is taken high.

7.3.5 Pullup and Pulldown Resistors on I/O Lines

Each A-port I/O has an internal $10k\Omega$ pullup resistor to V_{CCA} , and each B-port I/O has an internal $10k\Omega$ pullup resistor to V_{CCB}. If a smaller value of pullup resistor is required, an external resistor must be added from the I/O to V_{CCA} or V_{CCB} (in parallel with the internal $10k\Omega$ resistors).

7.4 Device Functional Modes

The TXS0104V device has two functional modes: enabled and disabled. To disable the device set the OE input low, which places all I/Os in a high impedance state. Setting the OE input high will enable the device.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TXS0104V device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The TXS0104V device is an excellent choice for applications where an open-drain driver is connected to the data I/Os. The TXS0104V device can also be used in applications where a push-pull driver is connected to the data I/Os, but the TXB0104 device might be a better option for such push-pull applications.

8.2 Typical Application

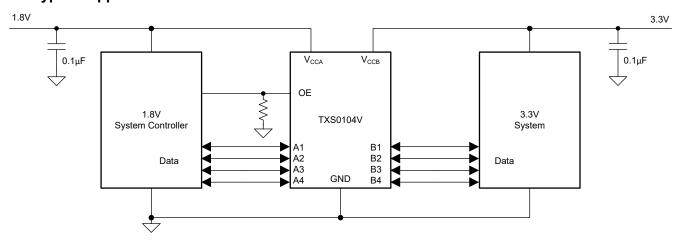


Figure 8-1. Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.65 to 3.6V
Output voltage range	2.3 to 5.5V

Copyright © 2024 Texas Instruments Incorporated

Product Folder Links: TXS0104V



8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
 - Use the supply voltage of the device that is driving the TXS0104V device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
 - Use the supply voltage of the device that the TXS0104V device is driving to determine the output voltage range.
 - The TXS0104V device has 10kΩ internal pullup resistors. External pullup resistors can be added to reduce the total RC of a signal trace if necessary.
- An external pull down resistor decreases the output V_{OH} and V_{OL}. Use Equation 1 to calculate the V_{OH} as a
 result of an external pull down resistor.

$$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 10 \, k\Omega) \tag{1}$$

where

 V_{CCx} is the supply voltage on either V_{CCA} or V_{CCB} R_{PD} is the value of the external pull down resistor

8.2.3 Application Curve

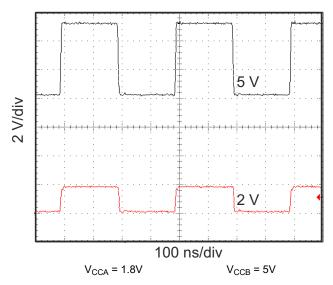


Figure 8-2. Level-Translation of a 2.5MHz Signal

8.3 Power Supply Recommendations

The TXS0104V device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB} . V_{CCB} accepts any supply voltage from 2.3V to 5.5V and V_{CCA} accepts any supply voltage from 1.65V to 3.6V as long as Vs is less than or equal to V_{CCB} . The A port and B port are designed to track V_{CCA} and V_{CCB} respectively allowing for low-voltage bidirectional translation between any of the 1.8V, 2.5V, 3.3V, and 5V voltage nodes.

The TXS0104V device does not require power sequencing between V_{CCA} and V_{CCB} during power-up so the power-supply rails can be ramped in any order. A V_{CCA} value greater than or equal to V_{CCB} ($V_{CCA} \ge V_{CCB}$) does not damage the device, but during operation, V_{CCA} must be less than or equal to V_{CCB} ($V_{CCA} \le V_{CCB}$) at all times.

The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. For the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The current-sourcing capability of the driver determines the minimum value of the pulldown resistor to ground.

8.4 Layout

8.4.1 Layout Guidelines

For device reliability, it is recommended to follow common printed-circuit board layout guidelines such as follows:

- Bypass capacitors should be used on power supplies.
- · Short trace lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one shot duration, approximately 30ns, and encounters low impedance at the source driver.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements

8.4.2 Layout Example

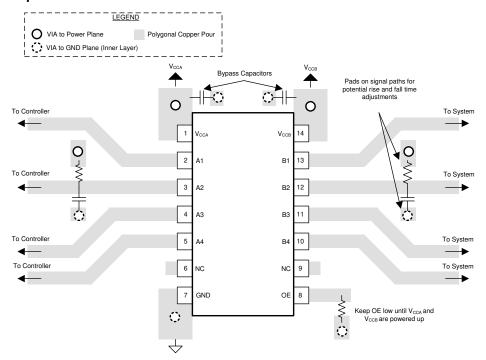


Figure 8-3. TXS0104V Layout Example



9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, Effects of External Pullup and Pulldown Resistors on TXS and TXB Devices application report
- Texas Instruments, Basics of Voltage Translation application report
- Texas Instruments, A Guide to Voltage Translation With TXS-Type Translators application report

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

DATE	REVISION	NOTES
June 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com 8-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
	(1)	(2)			(3)	(4)	(5)		(0)
TXS0104VBQAR	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YF04V
TXS0104VBQAR.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YF04V
TXS0104VDR	Active	Production	SOIC (D) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TXS0104V
TXS0104VDR.A	Active	Production	SOIC (D) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TXS0104V
TXS0104VPWR	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YF04V
TXS0104VPWR.A	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YF04V
TXS0104VRGYR	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YF04V
TXS0104VRGYR.A	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YF04V
TXS0104VRUTR	Active	Production	UQFN (RUT) 12	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1SV
TXS0104VRUTR.A	Active	Production	UQFN (RUT) 12	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1SV

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

www.ti.com 8-Nov-2025

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TXS0104V:

Automotive: TXS0104V-Q1

NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

www.ti.com 18-Jul-2025

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0104VBQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
TXS0104VDR	SOIC	D	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TXS0104VPWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TXS0104VRGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TXS0104VRUTR	UQFN	RUT	12	3000	180.0	8.4	2.0	2.3	0.75	4.0	8.0	Q1

www.ti.com 18-Jul-2025



*All dimensions are nominal

7 till dillitorioriorio di o mominar							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0104VBQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
TXS0104VDR	SOIC	D	14	3000	340.5	336.1	32.0
TXS0104VPWR	TSSOP	PW	14	3000	353.0	353.0	32.0
TXS0104VRGYR	VQFN	RGY	14	3000	360.0	360.0	36.0
TXS0104VRUTR	UQFN	RUT	12	3000	210.0	185.0	35.0

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



INSTRUMENTS www.ti.com





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
 The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.





NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).





NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



www.ti.com



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.





NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



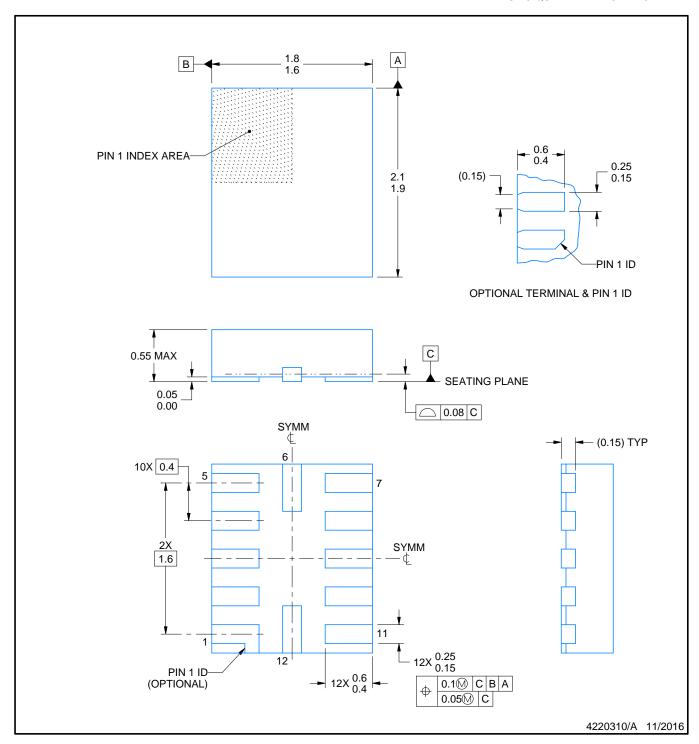


NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



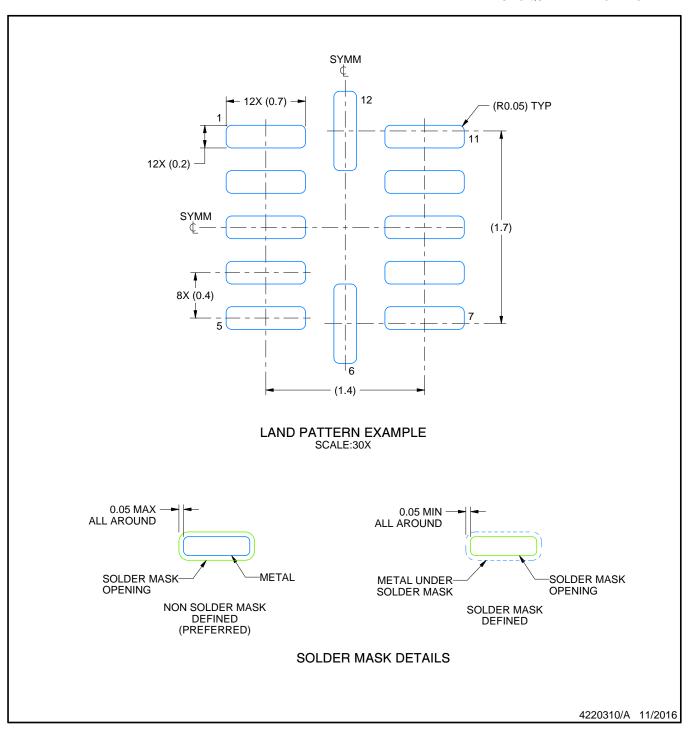




NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 This drawing is subject to change without notice.

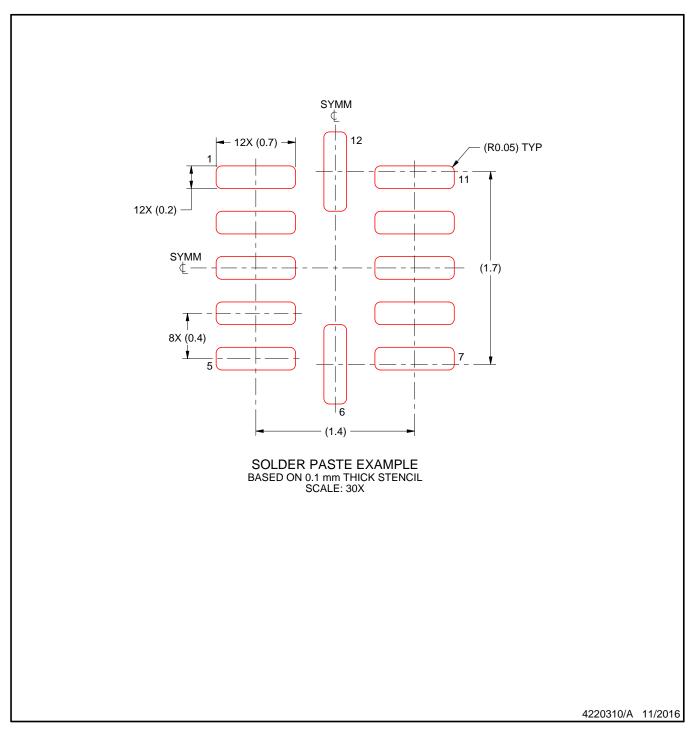




NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).





NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025