

TXS0102 2-Bit Bidirectional Voltage-Level Translator for Open-Drain and Push-Pull **Applications**

1 Features

- No direction-control signal needed
- Maximum data rates:
 - 24Mbps (push pull)
 - 2Mbps (open drain)
- Available in the Texas Instruments NanoStar™ integrated circuit package
- 1.65V to 3.6V on A port and 2.3V to 5.5V on B port $(V_{CCA} \le V_{CCB})$
- V_{CC} isolation feature: if either V_{CC} input is at GND, both ports are in the High-Impedance state
- No power-supply sequencing required: either V_{CCA} or V_{CCB} can be ramped first
- I_{off} supports partial-power-down mode operation
- Latch-up performance exceeds 100mA per JESD 78, Class II
- ESD protection exceeds JESD 22:
 - A port:
 - 2500V Human-Body Model (A114-B)
 - 250V Machine Model (A115-A)
 - 1500V Charged-Device Model (C101)
 - B port:
 - 8kV Human-Body Model (A114-B)
 - 250V Machine Model (A115-A)
 - 1500V Charged-Device Model (C101)

2 Applications

- I²C / SMBus
- **UART**
- **GPIO**

3 Description

This two-bit non-inverting translator is a bidirectional voltage-level translator and can be used to establish digital switching compatibility between mixed-voltage systems. It uses two separate configurable powersupply rails, with the A ports supporting operating voltages from 1.65V to 3.6V while it tracks the V_{CCA} supply, and the B ports supporting operating voltages from 2.3V to 5.5V while it tracks the V_{CCB} supply. This allows the support of both lower and higher logic signal levels while providing bidirectional translation capabilities between any of the 1.8V, 2.5V, 3.3V, and 5V voltage nodes.

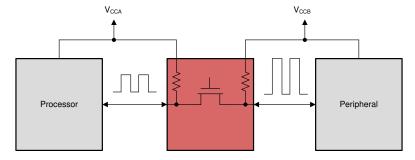
When the output-enable (OE) input is low, all I/Os are placed in the high-impedance state, which significantly reduces the power-supply quiescent current consumption.

To put the device in the high-impedance state during power up or power down, tie OE to GND through a pulldown resistor; the current-sourcing capability of the driver determines the minimum value of the resistor.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE(2)
PART NOWBER	FACRAGE	PACKAGE SIZE
	DCT (SSOP, 8)	2.95mm × 4mm
	DCU (VSSOP, 8)	2mm × 3.1mm
TXS0102	DQE (X2SON, 8)	1.4mm × 1mm
17/30/102	DQM (SON, 8)	1.8mm × 1.2mm
	YZP (DSBGA, 8)	1.9mm x 0.9mm
	DTT (DSBGA, 8)	1.95mm × 1mm

- For more information, see Section 11
- The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Block Diagram for TXS0102



Table of Contents

1 Features1	7.1 Overview	14
2 Applications1	7.2 Functional Block Diagram	
3 Description1	7.3 Feature Description	
4 Pin Configuration and Functions3	7.4 Device Functional Modes	16
5 Specifications4	8 Application and Implementation	. 17
5.1 Absolute Maximum Ratings4	8.1 Application Information	
5.2 ESD Ratings4	8.2 Typical Application	
5.3 Recommended Operating Conditions5	8.3 Power Supply Recommendations	18
5.4 Thermal Information5	8.4 Layout	. 19
5.5 Electrical Characteristics6	9 Device and Documentation Support	20
5.6 Switching Characteristics, V _{CCA} = 1.8 ± 0.15V7	9.1 Documentation Support	. 20
5.7 Switching Characteristics, V _{CCA} = 2.5 ± 0.2V7	9.2 Receiving Notification of Documentation Updates	20
5.8 Switching Characteristics, V _{CCA} = 3.3 ± 0.3V8	9.3 Support Resources	. 20
5.9 Switching Characteristics: T _{sk} , T _{MAX} 9	9.4 Trademarks	20
5.10 Operating Characteristics: V _{CCA} = 1.5V to 3.3V,	9.5 Electrostatic Discharge Caution	20
V _{CCB} = 1.5V to 3.3V10	9.6 Glossary	20
5.11 Typical Characteristics11	10 Revision History	. 20
Parameter Measurement Information12	11 Mechanical, Packaging, and Orderable	
7 Detailed Description14	Information	. 21



4 Pin Configuration and Functions



Figure 4-1. YZP Package, 8-Pin DSBGA (Bottom View)

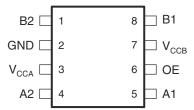


Figure 4-2. DCT or DCU Package, 8-Pin SSOP and VSSOP (Top View)

V_{CCA}	[[]	ı_8_	V _{CCE}
A1	_2_I	1_7_	B1
A2	3_1	ı <u>_</u> 6_	B2
GND	<u>-4</u> 1	1_5_	OE

Figure 4-3. DQE or DQM Package, 8-Pin X2SON (Top View)

B2 (1) (8) B1 GND (2) (7) V_{CCB} V_{CCA} (3) (6) OE A2 (4) (5) A1

Figure 4-4. DTT Package, 8-Pin SOP (Top View)

Table 4-1. Pin Functions

		PIN									
		NO.		TYPE(1)	DESCRIPTION						
NAME	DCT, DCU, DTT	DQE, DQM	YZP								
A1	5	2	D2	I/O	Input/output A. Referenced to V _{CCA} .						
A2	4	3	D1	I/O	Input/output A. Referenced to V _{CCA} .						
B1	8	8 7 A2			Input/output B. Referenced to V _{CCB} .						
B2	1	6	A1	I/O	Input/output B. Referenced to V _{CCB} .						
GND	2	4	B1	_	Ground						
OE	6	5	C2	I	Output enable (active High). Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA} .						
V_{CCA}	3	1	C1	Р	A-port supply voltage. 1.65V ≤ V _{CCA} ≤ 3.6V and V _{CCA} ≤ V _{CCB}						
V _{CCB}	7	8	B2	Р	B-port supply voltage. 2.3V ≤ V _{CCB} ≤ 5.5V						

⁽¹⁾ I = input, O = output, I/O = input and output, P = power



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CCA}	Supply voltage A		-0.5	4.6	V
V _{CCB}	Supply voltage B		-0.5	6.5	V
V	Input Voltage ⁽²⁾	A Port	-0.5	4.6	V
V _I	input voitage	B Port	-0.5	6.5	v
.,	Voltage applied to any output in the high-impedance or power-off	A Port	-0.5	4.6	V
Vo	state ⁽²⁾	B Port	-0.5	6.5	V
V	Valtage applied to any output in the high or law state(2) (3)	A Port	-0.5	V _{CCA} + 0.5	V
Vo	Voltage applied to any output in the high or low state ^{(2) (3)}	B Port	-0.5	$V_{\text{CCA}} + 0.5$ $V_{\text{CCB}} + 0.5$	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current	,		±50	mA
	Continuous current through V _{CC} or GND			±100	mA
Tj	Junction Temperature			150	°C
T _{stg}	Storage temperature		-65	150	°C

⁽¹⁾ Stresses beyond those listed under <u>Section 5.1</u> may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under <u>Section 5.3</u> Exposure beyond the limits listed in <u>Section 5.3</u> may affect device reliability.

5.2 ESD Ratings

				VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	A Port	±2500	
	Electrostatic	Truman body moder (Tibin), per ANSI/ESDA/JEDEC 33-001	B Port	±8000	\/
V _(ESD)	discharge	Charried device model (CDM) ner ANSI/ESDA/JEDEC IS 002	A Port	±1500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002	B Port	±1500	

⁽²⁾ The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The output positive-voltage rating may be exceeded up to 6.5V maximum if the output current rating is observed.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1) (2) (3) (4) (5)

			V _{CCA}	V _{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage A				1.65	3.6	V
V_{CCB}	Supply voltage B				2.3	5.5	V
		A-port I/O's	1.65V to 1.95V		V _{CCI} - 0.2 V _{CI}		
	Himb Invalinguit valtage		2.3V to 3.6V	0.00/45 5.50/	V _{CCI} - 0.4	V _{CCI}	V
V_{IH}	High-level input voltage	B-port I/O's	1.65V to 3.6V	2.3V to 5.5V	V _{CCI} - 0.4	V _{CCI}	V
		OE Input	1.65V to 3.6V		V _{CCA} x 0.65	5.5	
		A-port I/O's			0	0.15	
V_{IL}	Low-level input voltage	B-port I/O's	1.65V to 3.6V	2.3V to 5.5V	0	0.15	V
* IL	Low total input valuage	OE Input	1.007 to 0.07	2.07 10 0.07	0	V _{CCA} x 0.35	·
		A-port I/O's				10	ns/V
Δt/Δν	Input transition rise and fall time	B-port I/O's	1.65V to 3.6V	2.3V to 5.5V		10	ns/V
		OE Input				10	ns/V
T _A	Operating free-air temperature			1	-40	85	°C

- (1) V_{CCI} is the V_{CC} associated with the input port.
- (2) V_{CCO} is the V_{CC} associated with the output port.
- (3) The maximum V_{IL} value is provided to ensure that a valid V_{OL} is maintaned. The V_{OL} value is V_{IL} plus the voltage drop across the pass-gate transistor.
- (4) V_{CCA} must be less than or equal to V_{CCB} , and V_{CCA} must not exceed 3.6V.
- (5) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application note, Implications of Slow or Floating CMOS Inputs.

5.4 Thermal Information

					TXS0102			
Т	HERMAL METRIC(1)	DCU	DQE	DCT	DTT	YZT	DQM	UNIT
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	239.8	229.6	168.5	219.8	105.8	212.8	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	88.5	89.1	84.6	139.0	1.6	84.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	151.6	128.0	96.1	122.3	10.8	118.1	°C/W
Y _{JT}	Junction-to-top characterization parameter	30.9	2.8	15.1	17.5	3.1	2.8	°C/W
Y_{JB}	Junction-to-board characterization parameter	150.5	127.7	94.7	122.2	10.8	117.8	°C/W
R_{θ} JC(bottom)	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	N/A	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.



5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

					Оре	erating 1	free-ai	r tempera	ature (T	A)	
P	ARAMETER	TEST CONDITIONS	V _{CCA}	V _{CCB}		25°C		-40°	C to 85	°C	UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{OHA}	Port A output high voltage	$I_{OH} = -20uA$ $V_{IB} \ge V_{CCB} - 0.4V$	1.65V to 3.6V	2.3V to 5.5V				V _{CCA} x 0.67			
V _{OLA}	Port A output low voltage	$I_{OL} = 1mA$ $V_{IB} \le 0.15V$	1.65V to 3.6V	2.3V to 5.5V						0.4	V
V _{OHB}	Port B output high voltage	$I_{OH} = -20uA$ $V_{IB} \ge V_{CCB} - 0.4V$	1.65V to 3.6V	2.3V to 5.5V				V _{CCB} x 0.67			
V _{OLB}	Port B output low voltage	$I_{OL} = 1mA$ $V_{IB} \le 0.15V$	1.65V to 3.6V	2.3V to 5.5V						0.4	
I	Input leakage current	OE V _I = V _{CC} or GND	1.65V to 3.6V	2.3V to 5.5V			±1			±2	
	Partial power down current	A port	0V	0V to 5.5V			±1			±2	μA
I _{off}	Partial power down current	B port	0V to 3.6V	0V			±1			±2	
I _{OZ}	Tri-state output current	A or B Port: $V_1 = V_{CC1}$ or GND $V_0 = V_{CCO}$ or GND OE = GND	1.65V to 3.6V	2.3V to 5.5V	-1		1	-2		2	μА
I _{CCA}	V _{CCA} supply current	$V_I = V_{CCI}$ or GND $I_O = 0$	1.65V to V _{CCB}	2.3V to 5.5V						2.4	μA
I _{CCA}	V _{CCA} supply current	$V_I = V_{CCI}$ or GND $I_O = 0$	3.6V	0V						2.2	μA
I _{CCA}	V _{CCA} supply current	$V_I = V_{CCI}$ or GND $I_O = 0$	0V	5.5V				-2			μA
I _{CCB}	V _{CCB} supply current	$V_I = V_{CCI}$ or GND $I_O = 0$	1.65V to V _{CCB}	2.3V to 5.5V						12	μA
I _{CCB}	V _{CCB} supply current	$V_I = V_{CCI}$ or GND $I_O = 0$	3.6V	0V				-1			μA
I _{CCB}	V _{CCB} supply current	$V_I = V_{CCI}$ or GND $I_O = 0$	0V	5.5V						3	μA
I _{CCA} +	Combined supply current	$V_I = V_{CCI}$ or GND $I_O = 0$	1.65V to V _{CCB}	2.3V to 5.5V						14.4	μA
C _i	Input Capacitance	OE	3.3V	3.3V		2.5				3.5	pF
C _{io}	Input-to-output internal capacitance	A or B port	3.3V	3.3V		10					pF
C _{io}	Input-to-output internal capacitance	A port	3.3V	3.3V		5			6		pF
C _{io}	Input-to-output internal capacitance	B port	3.3V	3.3V		6			7.5		pF

 $[\]begin{array}{ll} \hbox{(1)} & V_{CCI} \text{ is the } V_{CC} \text{ associated with the input port} \\ \hbox{(2)} & V_{CCA} \text{ must be less than or equal to } V_{CCB}, \text{ and } V_{CCA} \text{ must not exceed 3.6V.} \\ \hbox{(3)} & V_{CCO} \text{ is the } V_{CC} \text{ associated with the output port} \\ \end{array}$



5.6 Switching Characteristics, $V_{CCA} = 1.8 \pm 0.15V$

								B-Poi	rt Sup	ply Vo	Itage (V _{CCB})			
ı	PARAMETER	FROM	то	Test C	onditions	2.	.5 ± 0.2	2V	3.	.3 ± 0.3	3V	5.	.0 ± 0.	5V	UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t _{PHL}	Propagation Delay (Hight-to- Low)	A	В	Push-Pull	-40°C to 85°C			5.3			5.4			6.8	ns
t _{PHL}	Propagation Delay (Hight-to- Low)	A	В	Open-Drain	-40°C to 85°C	2.3		8.8	2.4		9.6	2.6		10	ns
t _{PLH}	Propagation Delay (Low-to- High)	A	В	Push-Pull	-40°C to 85°C			6.8			7.1			7.5	ns
t _{PLH}	Propagation Delay (Low-to- High)	А	В	Open-Drain	-40°C to 85°C	45		260	36		208	27		198	ns
t _{PHL}	Propagation Delay (Hight-to- Low)	В	A	Push-Pull	-40°C to 85°C			4.4			4.5			4.7	ns
t _{PHL}	Propagation Delay (Hight-to- Low)	В	A	Open-Drain	-40°C to 85°C	1.9		5.3	1.1		4.4	1.2		4	ns
t _{PLH}	Propagation Delay (Low-to- High)	В	A	Push-Pull	-40°C to 85°C			5.3			4.5			0.5	ns
t _{PLH}	Propagation Delay (Low-to- High)	В	A	Open-Drain	-40°C to 85°C	45		175	36		140	27		102	ns
t _{en}	Enable Time	OE	A or B		-40°C to 85°C			200			200			200	ns
t _{dis}	Disable Time	OE	A or B		-40°C to 85°C			200			200			200	ns
t _{rA}	Ouput Rise Time	В	А	Push-Pull	-40°C to 85°C	3.2		9.5	2.3		9.3	2		7.6	ns
t _{rA}	Ouput Rise Time	В	Α	Open-Drain	-40°C to 85°C	38		165	30		132	22		95	ns
t _{rB}	Ouput Rise Time	Α	В	Push-Pull	-40°C to 85°C	4		10.8	2.7		9.1	2.7		7.6	ns
t _{rB}	Ouput Rise Time	Α	В	Open-Drain	-40°C to 85°C	34		145	23		106	10		58	ns
t _{fA}	Output Fall Time	В	Α	Push-Pull	-40°C to 85°C	2		5.9	1.9		6	1.7		13.3	ns
t_{fA}	Output Fall Time	В	А	Open-Drain	-40°C to 85°C	4.4		6.9	4.3		6.4	4.2		6.1	ns
t _{fB}	Output Fall Time	А	В	Push-Pull	-40°C to 85°C	2.9		13.8	2.8		16.2	2.8		16.2	ns
t _{fB}	Output Fall Time	Α	В	Open-Drain	-40°C to 85°C	6.9		13.8	7.5		16.2	7		16.2	ns

5.7 Switching Characteristics, $V_{CCA} = 2.5 \pm 0.2V$

					B-Port Supply Voltage (V _{CCB})										
ı	PARAMETER	FROM	то	Test Conditions		2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t _{PHL}	Propagation Delay (Hight-to- Low)	A	В	Push-Pull	-40°C to 85°C			3.2			3.7			3.8	ns
t _{PHL}	Propagation Delay (Hight-to- Low)	A	В	Open-Drain	-40°C to 85°C	1.7		6.3	2		6	2.1		5.8	ns
t _{PLH}	Propagation Delay (Low-to- High)	A	В	Push-Pull	-40°C to 85°C			3.5			4.1			4.4	ns

Copyright © 2025 Texas Instruments Incorporated

Submit Document Feedback



								B-Poi	rt Sup	ply Vo	Itage (V _{CCB})			
ı	PARAMETER	FROM	то	Test Co	onditions	2.	5 ± 0.2	2V	3.	3 ± 0.3	3V	5.	0 ± 0.5	δV	UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t _{PLH}	Propagation Delay (Low-to- High)	A	В	Open-Drain	-40°C to 85°C	43		250	36		206	27		190	ns
t _{PHL}	Propagation Delay (Hight-to- Low)	В	A	Push-Pull	-40°C to 85°C			3			3.6			4.3	ns
t _{PHL}	Propagation Delay (Hight-to- Low)	В	А	Open-Drain	-40°C to 85°C	1.8		4.7	2.6		4.2	1.2		4	ns
t _{PLH}	Propagation Delay (Low-to- High)	В	A	Push-Pull	-40°C to 85°C			2.5		,	1.6			1	ns
t _{PLH}	Propagation Delay (Low-to- High)	В	А	Open-Drain	-40°C to 85°C	44		170	37		140	27		103	ns
t _{en}	Enable Time	OE	A or B		-40°C to 85°C			200			200			200	ns
t _{dis}	Disable Time	OE	A or B		-40°C to 85°C			200			200			200	ns
t _{rA}	Ouput Rise Time	В	Α	Push-Pull	-40°C to 85°C	2.8		7.4	2.6		6.6	1.8		5.6	ns
t _{rA}	Ouput Rise Time	В	Α	Open-Drain	-40°C to 85°C	3		149	28		121	24		89	ns
t _{rB}	Ouput Rise Time	Α	В	Push-Pull	-40°C to 85°C	3.2		8.3	2.9		7.2	2.4		6.1	ns
t _{rB}	Ouput Rise Time	Α	В	Open-Drain	-40°C to 85°C	35		151	24		112	12		64	ns
t _{fA}	Output Fall Time	В	Α	Push-Pull	-40°C to 85°C	1.9		5.7	1.9		5.5	1.8		5.3	ns
t _{fA}	Output Fall Time	В	Α	Open-Drain	-40°C to 85°C	4.4	,	6.9	4.3		6.2	4.2		5.8	ns
t _{fB}	Output Fall Time	Α	В	Push-Pull	-40°C to 85°C	2.2		7.8	2.4		6.7	2.6		6.6	ns
t _{fB}	Output Fall Time	Α	В	Open-Drain	-40°C to 85°C	5.1		8.8	5.4		9.4	5.4		10.4	ns

5.8 Switching Characteristics, $V_{CCA} = 3.3 \pm 0.3 V$

							B-Port	Supply	Voltage	(V _{CCB})		
	PARAMETER	FROM	то	Test Conditions		3	.3 ± 0.3	V	5.	0 ± 0.5	V	UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
t _{PHL}	Propagation Delay (Hight-to-Low)	А	В	Push-Pull	-40°C to 85°C			2.4			3.1	ns
t _{PHL}	Propagation Delay (Hight-to-Low)	А	В	Open-Drain	-40°C to 85°C	1.3		4.2	1.4		4.6	ns
t _{PLH}	Propagation Delay (Low-to-High)	А	В	Push-Pull	-40°C to 85°C			4.2			4.4	ns
t _{PLH}	Propagation Delay (Low-to-High)	А	В	Open-Drain	-40°C to 85°C	36		204	28		165	ns
t _{PHL}	Propagation Delay (Hight-to-Low)	В	А	Push-Pull	-40°C to 85°C			2.5			3.3	ns
t _{PHL}	Propagation Delay (Hight-to-Low)	В	A	Open-Drain	-40°C to 85°C	1		124	1		97	ns
t _{PLH}	Propagation Delay (Low-to-High)	В	A	Push-Pull	-40°C to 85°C			2.5			2.6	ns
t _{PLH}	Propagation Delay (Low-to-High)	В	A	Open-Drain	-40°C to 85°C	3		139	3		105	ns
t _{en}	Enable Time	OE	A or B		-40°C to 85°C			200			200	ns
t _{dis}	Disable Time	OE	A or B		-40°C to 85°C			200		,	200	ns
t _{rA}	Ouput Rise Time	В	Α	Push-Pull	-40°C to 85°C	2.3		5.6	1.9		4.8	ns



	PARAMETER FROM			FROM TO Test Conditions				5	UNIT		
						MIN	TYP MAX	MIN	TYP	MAX	
t _{rA}	Ouput Rise Time	В	Α	Open-Drain	-40°C to 85°C	25	116	19		85	ns
t _{rB}	Ouput Rise Time	Α	В	Push-Pull	-40°C to 85°C	2.5	6.4	2.1		7.4	ns
t _{rB}	Ouput Rise Time	Α	В	Open-Drain	-40°C to 85°C	26	116	14	,	72	ns
t _{fA}	Output Fall Time	В	Α	Push-Pull	-40°C to 85°C	2	5.4	1.9		5	ns
t _{fA}	Output Fall Time	В	Α	Open-Drain	-40°C to 85°C	4.3	6.1	4.2		5.7	ns
t _{fB}	Output Fall Time	Α	В	Push-Pull	-40°C to 85°C	2.3	7.4	2.4		7.6	ns
t _{fB}	Output Fall Time	A	В	Open-Drain	-40°C to 85°C	5	7.6	4.8		8.3	ns

5.9 Switching Characteristics: T_{sk} , T_{MAX}

over operating free-air temperature range (unless otherwise noted)

					Opera tempe	ting fre erature		
PARAMETER	TEST CON	DITIONS	V _{CCA}	V _{CCB}	-40°0	to 12	5°C	UNIT
					MIN	TYP	MAX	
			1.8 ± 0.15V	2.5V ± 0.2V			21	
			1.8 ± 0.15V	$3.3V \pm 0.3V$			22	
			1.8 ± 0.15V	5V ± 0.5V			24	
		Push-Pull Driving	2.5V ± 0.2V	2.5V ± 0.2V			20	
		Push-Puli Driving	2.5V ± 0.2V	3.3V ± 0.3V			22	
			2.5V ± 0.2V	5V ± 0.5V			24	
			3.3V ± 0.3V	3.3V ± 0.3V			23	
	50% Duty Cycle		3.3V ± 0.3V	5V ± 0.5V			24	
T _{MAX} - Maximum Data Rate	Input One channel		1.8 ± 0.15V	1.8 ± 0.15V		2	Mbps	
Bata Nate	switching		1.8 ± 0.15V	2.5V ± 0.2V			2	
			1.8 ± 0.15V	3.3V ± 0.3V			2	
			1.8 ± 0.15V	5V ± 0.5V			2	
		Open-Drain Driving	2.5V ± 0.2V	2.5V ± 0.2V			2	
		Bilving	2.5V ± 0.2V	3.3V ± 0.3V			2	
			2.5V ± 0.2V	5V ± 0.5V			2	
			3.3V ± 0.3V	3.3V ± 0.3V			2	
			3.3V ± 0.3V	5V ± 0.5V			2	
	Dulas Dunation Data	Push-Pull Driving	1.65V to 3.6V	2.3V to 5.5V	20	-		
t _w	Pulse Duration, Data Inputs	Open-Drain Driving	1.65V to 3.6V	2.3V to 5.5V	500	,		ns
t _{sk} - Output skew	Skew between any tw same package switch direction		1.65V to 3.6V	2.3V to 5.5V			0.7	ns

Copyright © 2025 Texas Instruments Incorporated



5.10 Operating Characteristics: $V_{CCA} = 1.5V$ to 3.3V, $V_{CCB} = 1.5V$ to 3.3V

 $T_A = 25^{\circ}C^{(1)}$

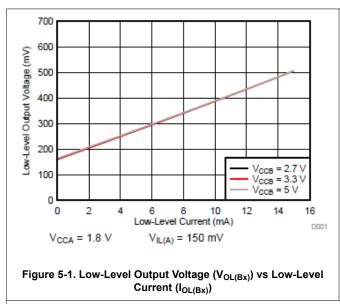
			Supply Voltage (V	CCA = V _{CCB} ,unl noted)	ess otherwise	
	PARAMETER	Test Conditions	1.8 ± 0.15V	2.5 ± 0.2V	3.3 ± 0.3V	UNIT
			TYP	TYP	TYP	
C _{pdA} (2)	A-port input, B-port output to B: outputs enabled		4.1	4.2	4.7	
O _{pd} A V	B-port input, A-port output to B: outputs enabled	A Port CL = 0, RL = Open	9.0	7.3	7.8	pF
C (3)	A-port input, B-port output to B: outputs enabled	f = 10MHz t _{rise} = t _{fall} = 1ns	11.0	9.9	9.2	рг
C _{pdB} (3)	B-port input, A-port output to B: outputs enabled		5.6	7.1	7.4	
C (2)	A-port input, B-port output to B: outputs disabled		0.1	0.1	0.1	
C _{pdA} ⁽²⁾	B-port input, A-port output to B: outputs disabled	B Port CL = 0, RL = Open	0.1	0.1	0.1	pF
C (3)	A-port input, B-port output to B: outputs disabled	f = 10MHz t _{rise} = t _{fall} = 1ns	0.2	0.2	0.2	рΓ
C _{pdB} (3)	B-port input, A-port output to B: outputs disabled		0.2	0.2	0.18	

For additional information about how power dissipation capacitance affects power consumption, see the CMOS Power Consumption (1) and C_{pd} Calculation application note.

A-Port power dissipation capacitance per transceiver.

⁽³⁾ B-Port power dissipation capacitance per transceiver.

5.11 Typical Characteristics



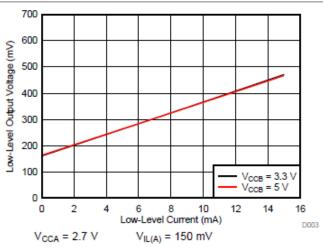


Figure 5-2. Low-Level Output Voltage $(V_{OL(Bx)})$ vs Low-Level Current $(I_{OL(Bx)})$

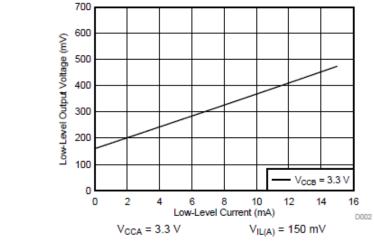


Figure 5-3. Low-Level Output Voltage $(V_{OL(Bx)})$ vs Low-Level Current $(I_{OL(Bx)})$



6 Parameter Measurement Information

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- PRR 10MHz
- $Z_{\rm O} = 50\Omega$
- dv/dt ≥ 1V/ns

Note

All parameters and waveforms are not applicable to all devices.

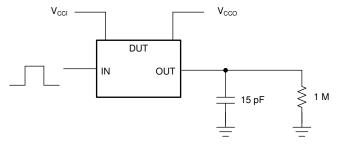


Figure 6-1. Data Rate, Pulse Duration, Propagation Delay, Output Rise And Fall Time Measurement Using A Push-Pull Driver

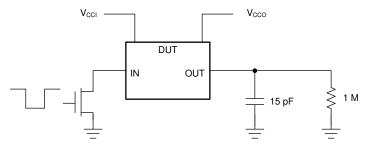


Figure 6-2. Data Rate, Pulse Duration, Propagation Delay, Output Rise And Fall Time Measurement Using An Open-Drain Driver

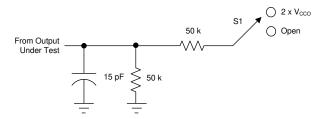


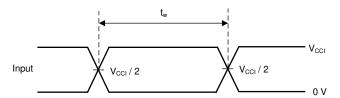
Figure 6-3. Load Circuit For Enable / Disable Time Measurement

Table 6-1. Switch Configuration For Enable / Disable Timing

TEST	S1
t _{PZL} ⁽²⁾ , t _{PLZ} ⁽¹⁾	2 × V _{CCO}
t _{PHZ} ⁽¹⁾ , t _{PZH} ⁽²⁾	Open

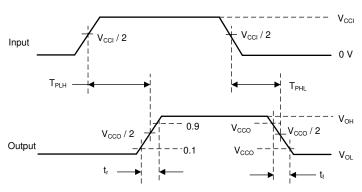
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en}.





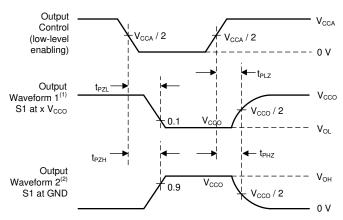
(1) All input pulses are measured one at a time, with one transition per measurement.

Figure 6-4. Voltage Waveforms Pulse Duration



(1) All input pulses are measured one at a time, with one transition per measurement.

Figure 6-5. Voltage Waveforms Propagation Delay Times



- (1) Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
- (2) Waveform 2 is for an output with internal conditions such that the ouput is high, except when disabled by the output control.

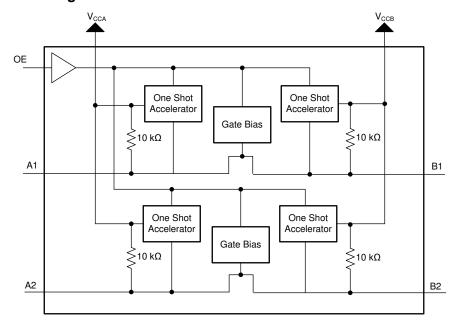
Figure 6-6. Voltage Waveforms Enable And Disable Times

7 Detailed Description

7.1 Overview

The TXS0102 device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.65V to 3.6V, while the B port can accept I/O voltages from 2.3V to 5.5V. The device is a pass-gate architecture with edge-rate accelerators (one-shots) to improve the overall data rate. $10k\Omega$ pullup resistors, commonly used in open-drain applications, have been conveniently integrated so that an external resistor is not needed. While this device is designed for open-drain applications, the device can also translate push-pull CMOS logic outputs.

7.2 Functional Block Diagram



Copyright © 2025 Texas Instruments Incorporated Product Folder Links: *TXS0102*

7.3 Feature Description

7.3.1 Architecture

The TXS0102 architecture (see Figure 7-1) is an auto-direction-sensing based translator that does not require a direction-control signal to control the direction of data flow from A to B or from B to A.

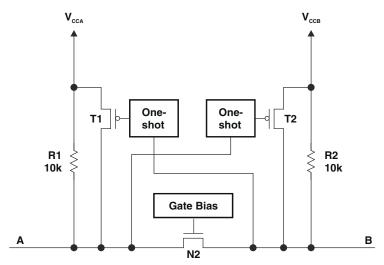


Figure 7-1. Architecture of a TXS0102 Cell

These two bidirectional channels independently determine the direction of data flow without a direction-control signal. Each I/O pin can be automatically reconfigured as either an input or an output, which is how this auto-direction feature is realized.

The TXS0102 device is part of TI's *Switch* type voltage translator family and employs two key circuits to enable this voltage translation:

- An N-channel pass-gate transistor topology that ties the A-port to the B-port
- Output one-shot (O.S.) edge-rate accelerator circuitry to detect and accelerate rising edges on the A or B ports

For bidirectional voltage translation, pull-up resistors are included on the device for dc current sourcing capability. The V_{GATE} gate bias of the N-channel pass transistor is set at approximately one threshold voltage (V_T) above the V_{CC} level of the low-voltage side. Data can flow in either direction without guidance from a control signal.

The O.S. rising-edge rate accelerator circuitry speeds up the output slew rate by monitoring the input edge for transitions, helping maintain the data rate through the device. During a low-to-high signal rising edge, the O.S. circuits turn on the PMOS transistors (T1, T2) to increase the current drive capability of the driver for approximately 30ns or 95% of the input edge, whichever occurs first.

This edge-rate acceleration provides high ac drive by bypassing the internal $10k\Omega$ pull-up resistors during the low-to-high transition to speed up the signal. The output resistance of the driver is decreased to approximately 50Ω to 70Ω during this acceleration phase. To minimize dynamic I_{CC} and the possibility of signal contention, the user should wait for the O.S. circuit to turn off before applying a signal in the opposite direction. The worst-case duration is equal to the minimum pulse-width number provided in the *Table 6-1* section of this data sheet.

Copyright © 2025 Texas Instruments Incorporated

7.3.2 Input Driver Requirements

The continuous dc-current sinking capability is determined by the external system-level open-drain (or push-pull) drivers that are interfaced to the TXS0102 I/O pins. Since the high bandwidth of these bidirectional I/O circuits is used to facilitate this fast change from an input to an output and an output to an input, they have a modest dc-current sourcing capability of hundreds of micro-Amps, as determined by the internal $10k\Omega$ pullup resistors.

The fall time (t_{fA}, t_{fB}) of a signal depends on the edge-rate and output impedance of the external device driving TXS0102 data I/Os, as well as the capacitive loading on the data lines.

Similarly, the t_{PHL} and max data rates also depend on the output impedance of the external driver. The values for tfA, tfB, tPHL, and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50Ω .

7.3.3 Output Load Considerations

TI recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper O.S. triggering takes place. PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration, causing any reflection to encounter low impedance at the source driver. The O.S. circuits are designed to stay on for approximately 30ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration.

With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic ICC, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the TXS0102 device output sees, so it is recommended that this lumped-load capacitance be considered to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

7.3.4 Enable and Disable

The TXS0102 device has an OE input that is used to disable the device by setting OE low, which places all I/Os in the Hi-Z state. The disable time (t_{dis}) indicates the delay between the time when OE goes low and when the outputs are disabled (Hi-Z). The enable time (ten) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

7.3.5 Pullup or Pulldown Resistors on I/O Lines

Each A-port I/O has an internal $10k\Omega$ pullup resistor to V_{CCA} , and each B-port I/O has an internal $10k\Omega$ pullup resistor to V_{CCB}. If a smaller value of pullup resistor is required, an external resistor must be added from the I/O to V_{CCA} or V_{CCB} (in parallel with the internal $10k\Omega$ resistors). Adding lower value pull-up resistors will effect V_{OL} levels, however. The internal pull-ups of the TXS0102 are disabled when the OE pin is low.

7.4 Device Functional Modes

The device has two functional modes, enabled and disabled. To disable the device set the OE input low, which places all I/Os in a high impedance state. Setting the OE input high will enable the device.

Product Folder Links: TXS0102

Copyright © 2025 Texas Instruments Incorporated

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TXS0102 device can be used to bridge the digital-switching compatibility gap between two voltage nodes to successfully interface logic threshold levels found in electronic systems. It should be used in a point-to-point topology for interfacing devices or systems operating at different interface voltages with one another. Its primary target application use is for interfacing with open-drain drivers on the data I/Os such as I²C or 1-wire, where the data is bidirectional and no control signal is available. The device can also be used in applications where a push-pull driver is connected to the data I/Os, but the TXB0102 might be a better option for such push-pull applications.

8.2 Typical Application

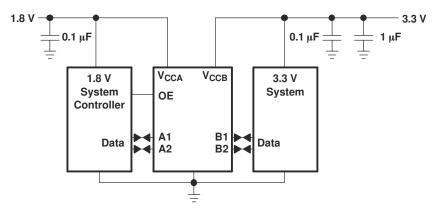


Figure 8-1. Typical Application Circuit

8.2.1 Design Requirements

Copyright © 2025 Texas Instruments Incorporated

For this design example, use the parameters listed in Table 8-1. And make sure the V_{CCA} ≤ V_{CCB}.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.65 to 3.6V
Output voltage range	2.3 to 5.5V

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

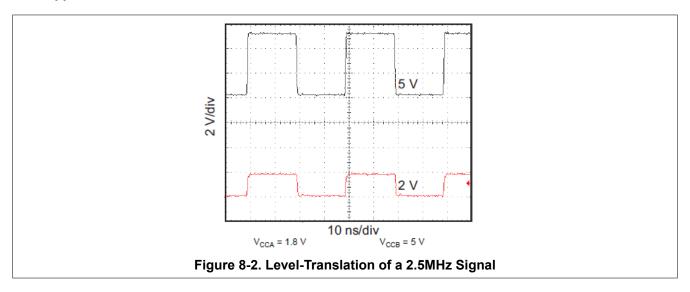
- · Input voltage range:
 - Use the supply voltage of the device that is driving the TXS0102 device to determine the input voltage range. For a valid logic high the value must exceed the VIH of the input port. For a valid logic low the value must be less than the VIL of the input port.
- · Output voltage range:
 - Use the supply voltage of the device that the TXS0102 device is driving to determine the output voltage range.
 - The TXS0102 device has 10kΩ internal pullup resistors. External pullup resistors can be added to reduce the total RC of a signal trace if necessary.
 - An external pull down resistor decreases the output VOH and VOL. Use Equation 1 to calculate the VOH
 as a result of an external pull down resistor.

$$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 10kq) \tag{1}$$

where:

- V_{CCx} is the supply voltage on either V_{CCA} or V_{CCB}
- R_{PD} is the value of the external pull down resistor

8.2.3 Application Curves



8.3 Power Supply Recommendations

During operation, ensure that $V_{CCA} \le V_{CCB}$ at all times. The sequencing of each power supply will not damage the device during the power up operation, so either power supply can be ramped up first. The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. To put the outputs in the high-impedance state during power up or power down, tie the OE input pin to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The current-sourcing capability of the driver determines the minimum value of the pulldown resistor to ground.

8.4 Layout

8.4.1 Layout Guidelines

For device reliability, it is recommended to follow common printed-circuit board layout guidelines such as follows:

- Bypass capacitors should be used on power supplies and should be placed as close as possible to the V_{CCA},
 V_{CCB} pin, and G_{ND} pin.
- · Short trace lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than
 the one-shot duration (approximately 30ns) causing any reflection to encounter low impedance at the source
 driver.

8.4.2 Layout Example

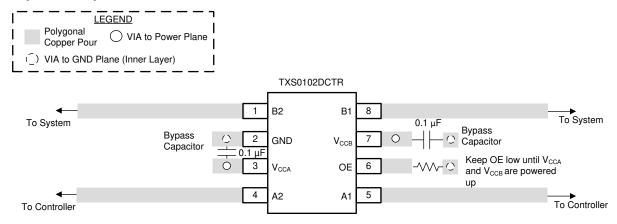


Figure 8-3. TXS0102 Layout Example



9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, A Guide to Voltage Translation With TXS-Type Translators application note
- Texas Instruments, Factors Affecting VOL for TXS and LSF Auto-bidirectional Translation Devices application
- Texas Instruments, Biasing Requirements for TXS, TXB, and LSF Auto-Bidirectional Translators application
- Texas Instruments, Effects of pullup and pulldown resistors on TXS and TXB devices application note
- Texas Instruments, Introduction to logic application note
- Texas Instruments, TI Logic and Linear Products Guide selection and solution guides
- Texas Instruments, Washing Machine Solutions Guide selection and solution guides
- Texas Instruments, TI Smartphone Solutions Guide selection and solution guides

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on Notifications to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

NanoStar[™] is a trademark of Texas Instruments Incorporated.

TI E2E[™] is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (July 2023) to Revision K (August 2025) **Page** Updated thermals for all packages, removed YZP package thermal information, and added DTT thermal Updated degradation of I_{CCA}/ I_{CCB}6



Changes from Revision I (August 2018) to Revision J (July 2023)

Page

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com

7-Oct-2025

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
TXS0102DCTR	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(35UT, NFE) (R, Z)
TXS0102DCTR.A	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(35UT, NFE) (R, Z)
TXS0102DCTR.B	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(35UT, NFE) (R, Z)
TXS0102DCTRE4	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFE (R, Z)
TXS0102DCTRE4.A	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFE (R, Z)
TXS0102DCTRE4.B	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFE (R, Z)
TXS0102DCTT	Active	Production	SSOP (DCT) 8	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(35UT, NFE) (R, Z)
TXS0102DCTT.B	Active	Production	SSOP (DCT) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(35UT, NFE) (R, Z)
TXS0102DCTTE4	Active	Production	SSOP (DCT) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFE (R, Z)
TXS0102DCTTE4.B	Active	Production	SSOP (DCT) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFE (R, Z)
TXS0102DCTTG4	Active	Production	SSOP (DCT) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFE (R, Z)
TXS0102DCTTG4.B	Active	Production	SSOP (DCT) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFE (R, Z)
TXS0102DCUR	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(35ST, FE, NFEQ, N FER) NZ
TXS0102DCUR.A	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(35ST, FE, NFEQ, N FER) NZ
TXS0102DCUR.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(35ST, FE, NFEQ, N FER) NZ
TXS0102DCURG4	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFER





7-Oct-2025 www.ti.com

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
TXS0102DCURG4.A	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFER
TXS0102DCURG4.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFER
TXS0102DCUT	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(FE, NFEQ, NFER) NZ
TXS0102DCUT.A	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(FE, NFEQ, NFER) NZ
TXS0102DCUT.B	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(FE, NFEQ, NFER) NZ
TXS0102DCUTG4	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFER
TXS0102DCUTG4.A	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFER
TXS0102DCUTG4.B	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFER
TXS0102DQER	Active	Production	X2SON (DQE) 8	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2H
TXS0102DQER.A	Active	Production	X2SON (DQE) 8	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2H
TXS0102DQER.B	Active	Production	X2SON (DQE) 8	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2H
TXS0102DQMR	Active	Production	X2SON (DQM) 8	3000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2H (2H7, 2HR) (2HG, 2HH)
TXS0102DQMR.A	Active	Production	X2SON (DQM) 8	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2H (2H7, 2HR) (2HG, 2HH)
TXS0102DQMR.B	Active	Production	X2SON (DQM) 8	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2H (2H7, 2HR) (2HG, 2HH)
TXS0102DQMRG4	Active	Production	X2SON (DQM) 8	3000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2H (2H7, 2HR) (2HG, 2HH)
TXS0102DQMRG4.A	Active	Production	X2SON (DQM) 8	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2H (2H7, 2HR) (2HG, 2HH)
TXS0102DQMRG4.B	Active	Production	X2SON (DQM) 8	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2H (2H7, 2HR) (2HG, 2HH)
TXS0102DTTR	Active	Production	X1SON (DTT) 8	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ЗНОН
TXS0102YZPR	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	2H
TXS0102YZPR.B	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	2H

PACKAGE OPTION ADDENDUM

7-Oct-2025

www.ti.com

- (1) Status: For more details on status, see our product life cycle.
- (2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TXS0102:

Automotive: TXS0102-Q1

NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



www.ti.com 11-Aug-2025

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0102DCTR	SSOP	DCT	8	3000	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
TXS0102DCTR	SSOP	DCT	8	3000	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
TXS0102DCTRE4	SSOP	DCT	8	3000	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
TXS0102DCTT	SSOP	DCT	8	250	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
TXS0102DCTTE4	SSOP	DCT	8	250	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
TXS0102DCTTG4	SSOP	DCT	8	250	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
TXS0102DCUR	VSSOP	DCU	8	3000	180.0	9.0	2.25	3.4	1.0	4.0	8.0	Q3
TXS0102DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TXS0102DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
TXS0102DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TXS0102DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TXS0102DQER	X2SON	DQE	8	5000	180.0	8.4	1.2	1.6	0.55	4.0	8.0	Q1
TXS0102DQMR	X2SON	DQM	8	3000	180.0	9.5	1.4	2.0	0.5	4.0	8.0	Q1
TXS0102DQMR	X2SON	DQM	8	3000	180.0	8.4	1.57	2.21	0.59	4.0	8.0	Q1
TXS0102DQMRG4	X2SON	DQM	8	3000	180.0	9.5	1.4	2.0	0.5	4.0	8.0	Q1
TXS0102DQMRG4	X2SON	DQM	8	3000	180.0	8.4	1.57	2.21	0.59	4.0	8.0	Q1



PACKAGE MATERIALS INFORMATION

www.ti.com 11-Aug-2025

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0102DTTR	X1SON	DTT	8	5000	180.0	8.4	1.15	2.1	0.48	4.0	8.0	Q1
TXS0102YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1



www.ti.com 11-Aug-2025



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0102DCTR	SSOP	DCT	8	3000	183.0	183.0	20.0
TXS0102DCTR	SSOP	DCT	8	3000	190.0	190.0	30.0
TXS0102DCTRE4	SSOP	DCT	8	3000	183.0	183.0	20.0
TXS0102DCTT	SSOP	DCT	8	250	190.0	190.0	30.0
TXS0102DCTTE4	SSOP	DCT	8	250	183.0	183.0	20.0
TXS0102DCTTG4	SSOP	DCT	8	250	183.0	183.0	20.0
TXS0102DCUR	VSSOP	DCU	8	3000	182.0	182.0	20.0
TXS0102DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
TXS0102DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
TXS0102DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
TXS0102DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
TXS0102DQER	X2SON	DQE	8	5000	202.0	201.0	28.0
TXS0102DQMR	X2SON	DQM	8	3000	184.0	184.0	19.0
TXS0102DQMR	X2SON	DQM	8	3000	202.0	201.0	28.0
TXS0102DQMRG4	X2SON	DQM	8	3000	184.0	184.0	19.0
TXS0102DQMRG4	X2SON	DQM	8	3000	202.0	201.0	28.0
TXS0102DTTR	X1SON	DTT	8	5000	210.0	185.0	35.0
TXS0102YZPR	DSBGA	YZP	8	3000	182.0	182.0	20.0





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-187 variation CA.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

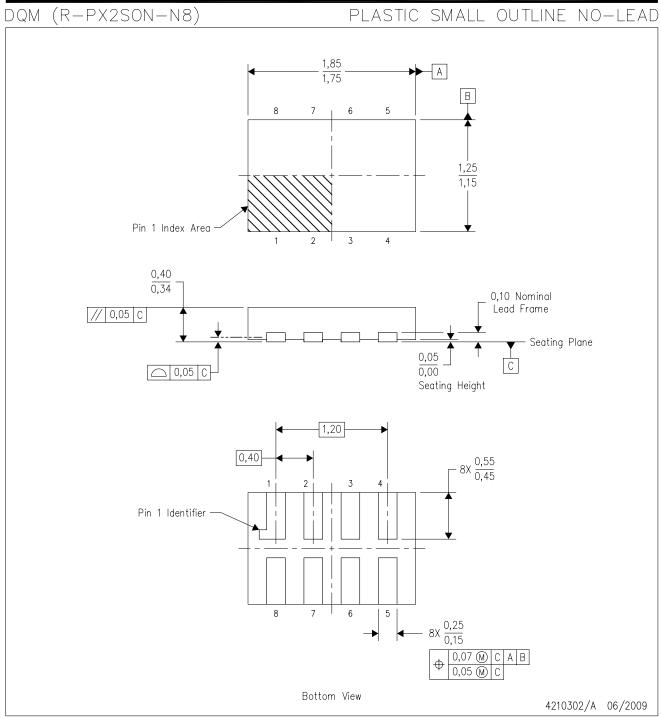




NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.





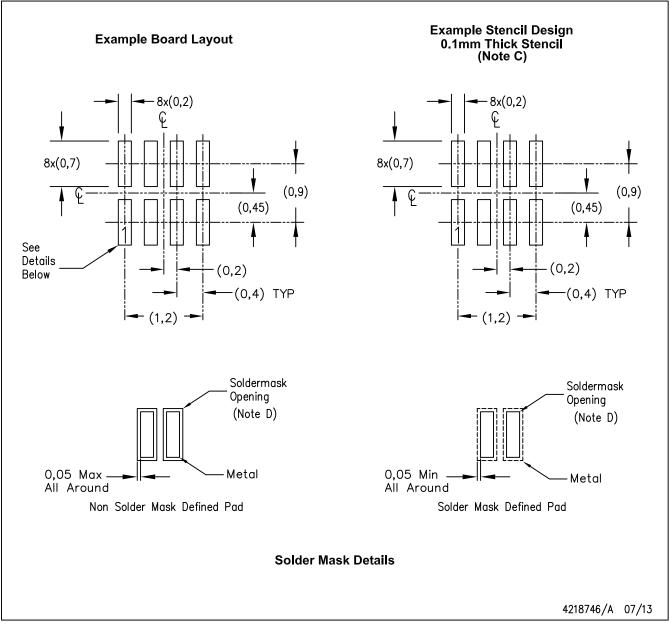
NOTES: All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.C. SON (Small Outline No-Lead) package configuration.



DQM (R-PX2SON-N8)

PLASTIC SMALL OUTLINE NO-LEAD

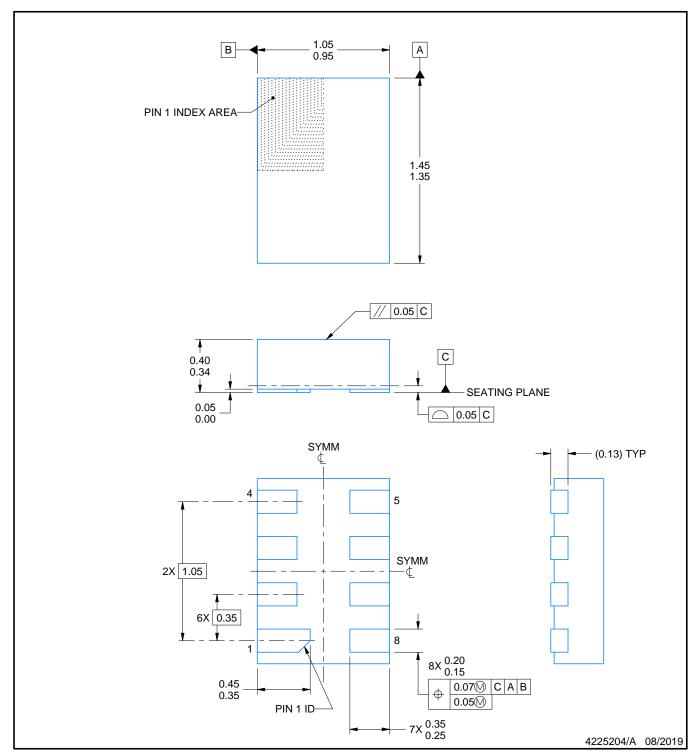


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- D. Customers should contact their board fabrication site for recommended solder mask tolerances.







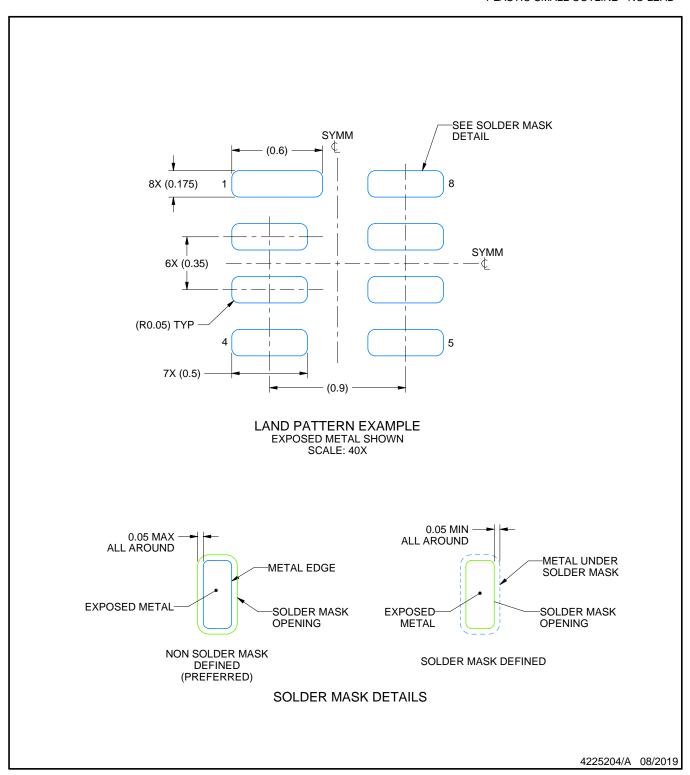
NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This package complies to JEDEC MO-287 variation X2EAF.

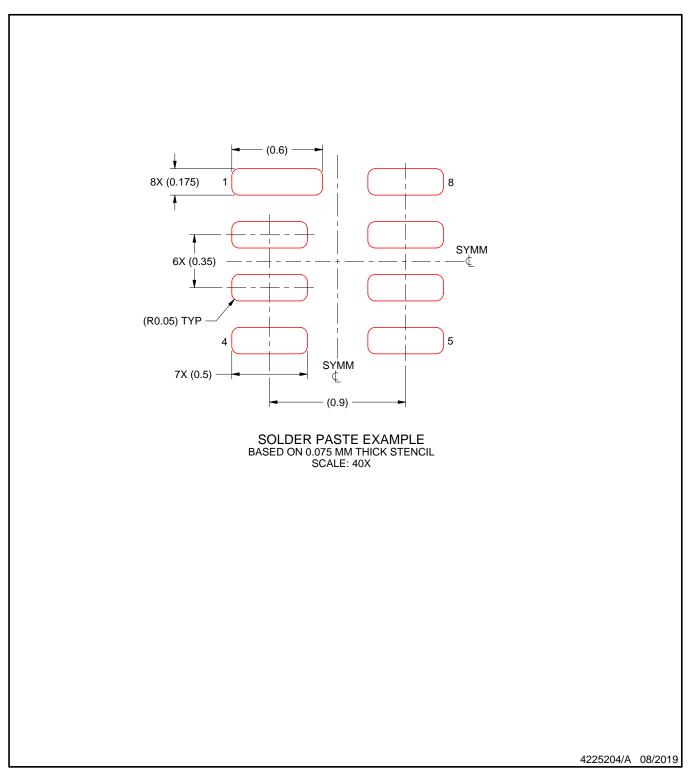




NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



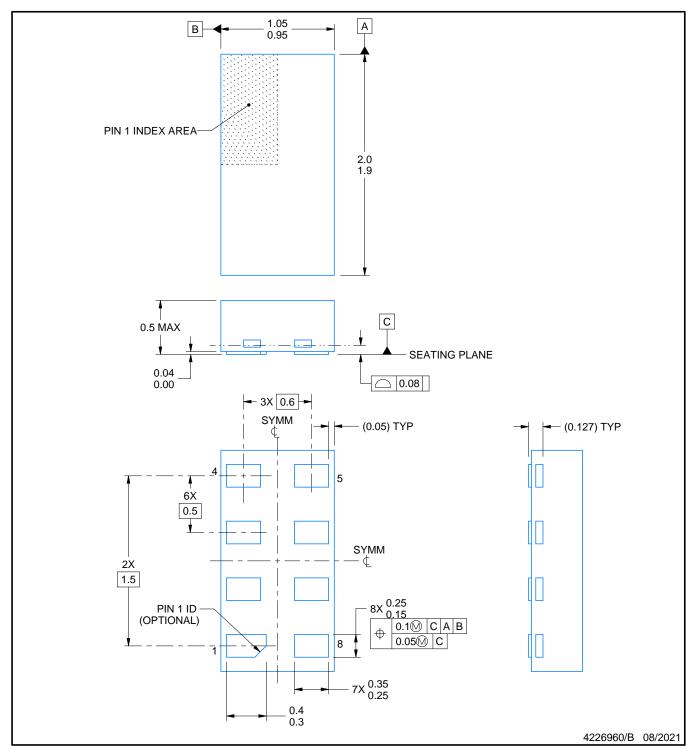


NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





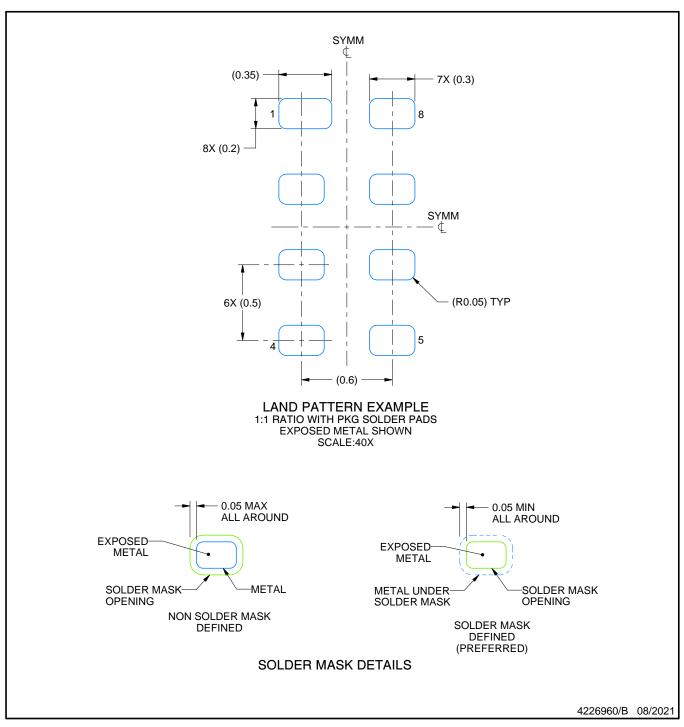


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

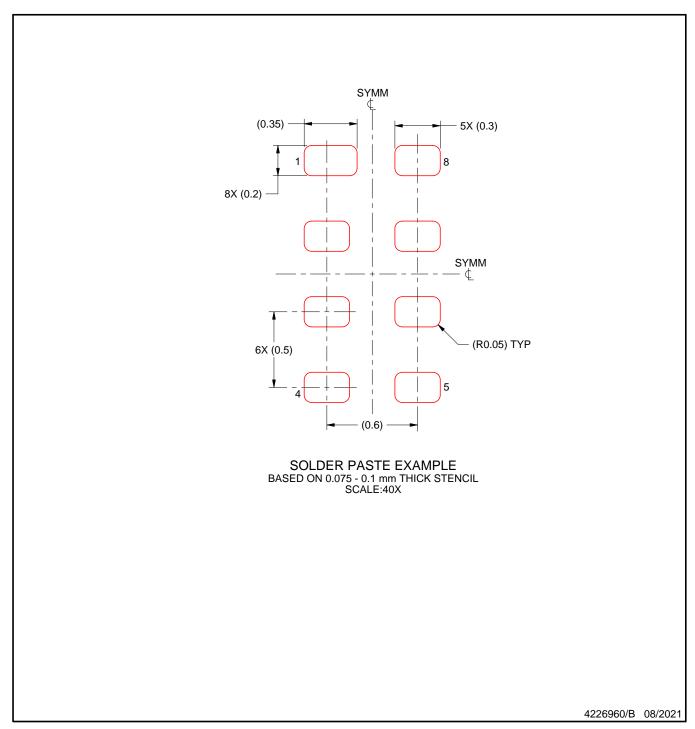




NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).





NOTES: (continued)

Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





DIE SIZE BALL GRID ARRAY



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2025. Texas Instruments Incorporated