

TXG102x 2-bit, $\pm 10V$ Ground-Level Translator

1 Features

- Supports DC shifts up to $\pm 10V$
- AC Noise Rejection of $20V_{PP}$ up to 45MHz
- CMTI of $1kV/\mu s$
- Low Prop Delay (<5ns) and Ch-Ch Skew (<0.20ns)
- Greater than 250Mbps
- Low power consumption (0.8mA per channel at 1Mbps, 1.8V)
- Fully configurable dual-rail design allows each port to operate from 1.71V to 5.5V
- 4, 2, 1 channel devices with multiple configurations will be available
- Two device variants:
 - TXG1020: 2 forward
 - TXG1021: 1 forward, 1 reverse
- Supports V_{CC} disconnect feature (I/Os are forced into high-Z)
- Schmitt-trigger inputs allows for slow and noisy signals
- Inputs with integrated static pull-down resistors prevent channels from floating
- Operating temperature from $-40^{\circ}C$ to $+125^{\circ}C$
- Latch-up performance exceeds 100mA per JESD 78, class II
 - ESD protection exceeds JESD 22
 - 2500V human-body model
 - 500V charged-device model
- Package options provided:
 - DSG (WSON-8)
 - DDF (SOT-8)
 - D (SOIC-8)

2 Applications

- Test and Measurement
- Industrial Automation
- Appliances
- Robotics

- Avionics

3 Description

The TXG102x is a 2-bit, fixed direction, non-galvanic based voltage and ground-level translator that can support both logic-level shifting between 1.71V to 5.5V and ground-level shifting up to $\pm 10V$. Compared to traditional level shifters, the TXG102x family can solve the challenges of voltage translation across different ground levels. The [Simplified Diagram](#) shows a common use case where DC shift occurs between GNDA to GNDB due to parasitic resistance or capacitance.

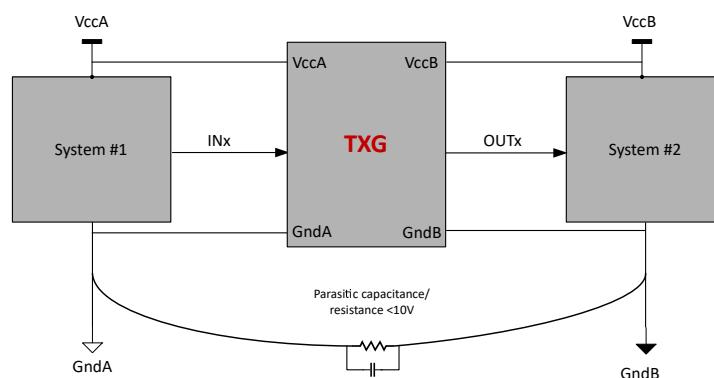
V_{CCA} is referenced to GNDA and V_{CCB} is referenced to GNDB. Ax pins are referenced to V_{CCA} logic level while Bx pins are referenced to V_{CCB} logic levels. Both A port and B port can accept voltages from 1.71V to 5.5V. The leakage between GNDA and GNDB is <40nA when V_{CC} to GND is shorted.

The TXG102x device helps improve noise immunity and power sequencing across different ground domains while providing low power consumption, latency and channel-to-channel skew. It can suppress noise levels of $20V_{PP}$ up to 45MHz ([Figure 8-3](#)). This device can support multiple interfaces such as UART, GPIO, and JTAG.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
TXG1020 TXG1021	DSG (WSON-8)	2.0mm \times 2.00mm
	DDF (SOT-8)	2.90mm \times 1.60mm
	D (SOIC-8)	4.90mm \times 3.90mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Diagram



An **IMPORTANT NOTICE** at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. **PRODUCTION DATA**.

Table of Contents

1 Features	1	8.1 Overview.....	23
2 Applications	1	8.2 Functional Block Diagram.....	23
3 Description	1	8.3 Feature Description.....	24
4 Pin Configuration and Functions	3	8.4 Device Functional Modes.....	27
5 Specifications	7	9 Application and Implementation	28
5.1 Absolute Maximum Ratings.....	7	9.1 Application Information.....	28
5.2 ESD Ratings.....	7	9.2 Typical Application.....	28
5.3 Recommended Operating Conditions.....	8	9.3 Power Supply Recommendations.....	30
5.4 Thermal Information.....	8	9.4 Layout.....	30
5.5 Electrical Characteristics.....	9	10 Device and Documentation Support	31
5.6 Supply Current.....	11	10.1 Device Support.....	31
5.7 Switching Characteristics, $V_{CCA} = 1.8 \pm 0.15V$	13	10.2 Documentation Support.....	31
5.8 Switching Characteristics, $V_{CCA} = 2.5 \pm 0.2V$	14	10.3 Receiving Notification of Documentation Updates.....	31
5.9 Switching Characteristics, $V_{CCA} = 3.3 \pm 0.3V$	15	10.4 Support Resources.....	31
5.10 Switching Characteristics, $V_{CCA} = 5.0 \pm 0.5V$	16	10.5 Trademarks.....	31
5.11 Switching Characteristics: T_{sk}, T_{MAX}	17	10.6 Electrostatic Discharge Caution.....	31
6 Typical Characteristics	19	10.7 Glossary.....	31
7 Parameter Measurement Information	21	11 Revision History	32
7.1 Load Circuit and Voltage Waveforms.....	21	12 Mechanical, Packaging, and Orderable Information	32
8 Detailed Description	23		

4 Pin Configuration and Functions

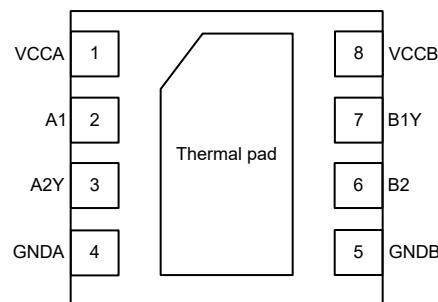


Figure 4-1. TXGx021DSG Package 8-Pin WSON Top View

Table 4-1. TXGx021 DSG Pin Functions

PIN		I/O	DESCRIPTION
Name	TXGx021		
A1	2	I	Input A1. Referenced to V_{CCA}
A2Y	3	O	Output A2. Referenced to V_{CCA}
B1Y	7	O	Output B1. Referenced to V_{CCB}
B2	6	I	Input B2. Referenced to V_{CCB}
V_{CCA}	1	—	A side supply voltage. $1.71V \leq V_{CCA} \leq 5.5V$
V_{CCB}	8	—	B side supply voltage. $1.71V \leq V_{CCB} \leq 5.5V$
GNDA	4	—	Ground reference for V_{CCA}
GNDB	5	—	Ground reference for V_{CCB}
—	Thermal pad	—	Keep thermal pad floating.

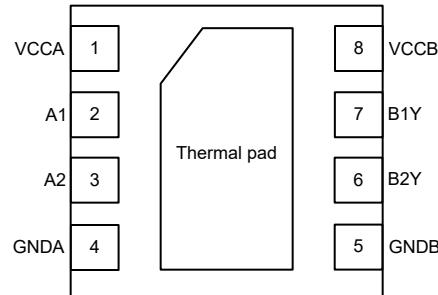


Figure 4-2. TXGx020DSG Package 8-Pin WSON Top View

Table 4-2. TXGx020 DSG Pin Functions

PIN		I/O	DESCRIPTION
Name	TXGx020		
A1	2	I	Input A1. Referenced to V_{CCA}
A2	3	I	Input A2. Referenced to V_{CCA}
B1Y	7	O	Output B1. Referenced to V_{CCB}
B2Y	6	O	Output B2. Referenced to V_{CCB}
V_{CCA}	1	—	A side supply voltage. $1.71V \leq V_{CCA} \leq 5.5V$
V_{CCB}	8	—	B side supply voltage. $1.71V \leq V_{CCB} \leq 5.5V$
GNDA	4	—	Ground reference for V_{CCA}
GNDB	5	—	Ground reference for V_{CCB}
—	Thermal pad	—	Keep thermal pad floating.

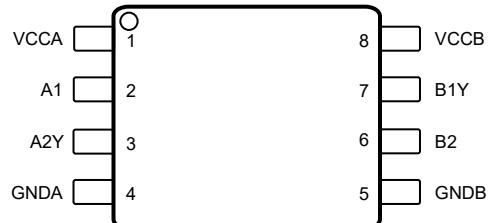


Figure 4-3. TXGx021DDF 8-Pin SOT and TXGx021D 8-pin SOIC Top View

Table 4-3. TXGx021 DDF and D Pin Functions

PIN		I/O	DESCRIPTION
Name	TXGx021		
A1	2	I	Input A1. Referenced to V_{CCA}
A2Y	3	O	Output A2. Referenced to V_{CCA}
B1Y	7	O	Output B1. Referenced to V_{CCB}
B2	6	I	Input B2. Referenced to V_{CCB}
V_{CCA}	1	—	A side supply voltage. $1.71V \leq V_{CCA} \leq 5.5V$
V_{CCB}	8	—	B side supply voltage. $1.71V \leq V_{CCB} \leq 5.5V$
GNDA	4	—	Ground reference for V_{CCA}
GNDB	5	—	Ground reference for V_{CCB}

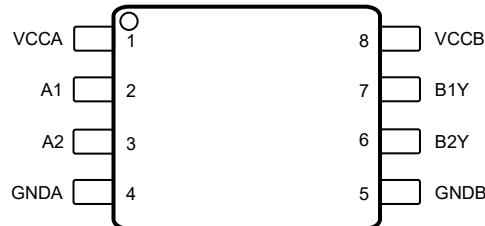


Figure 4-4. TXGx020DDF 8-Pin SOT and TXGx020D 8-pin SOIC Top View

Table 4-4. TXGx020 DDF and D Pin Functions

PIN		I/O	DESCRIPTION
Name	TXGx020		
A1	2	I	Input A1. Referenced to V_{CCA}
A2	3	I	Input A2. Referenced to V_{CCA}
B1Y	7	O	Output B1. Referenced to V_{CCB}
B2Y	6	O	Output B2. Referenced to V_{CCB}
V_{CCA}	1	—	A side supply voltage. $1.71V \leq V_{CCA} \leq 5.5V$
V_{CCB}	8	—	B side supply voltage. $1.71V \leq V_{CCB} \leq 5.5V$
GNDA	4	—	Ground reference for V_{CCA}
GNDB	5	—	Ground reference for V_{CCB}

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CCA} to V_{GNDA}	Supply voltage A to Ground voltage A		-0.5	6.5	V
V_{CCB} to V_{GNDB}	Supply voltage B to Ground voltage B		-0.5	6.5	V
V_{GNDA} to V_{GNDB}	Voltage between GNDA and GNDB	Voltage between GNDA and GNDB	-15	15	V
V_I	Input Voltage ⁽²⁾	I/O Ports (A Port) to V_{GNDA}	-0.5	6.5	V
		I/O Ports (B Port) to V_{GNDB}	-0.5	6.5	
V_O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾	A Port to V_{GNDA}	-0.5	6.5	V
		B Port to V_{GNDB}	-0.5	6.5	
V_O	Voltage applied to any output in the high or low state ^{(2) (3)}	A Port to V_{GNDA}	-0.5 $V_{CCA} + 0.5$		V
		B Port to V_{GNDB}	-0.5 $V_{CCB} + 0.5$		
I_{IK}	Input clamp current	$V_I < 0$	-20		mA
I_{OK}	Output clamp current	$V_O < 0$	-20		mA
I_O	Continuous output current		-25	25	mA
	Continuous current through V_{CC} or GND		-100	100	mA
T_j	Junction Temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under [Section 5.1](#) may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Section 5.3](#) Exposure beyond the limits listed in [Section 5.3](#) may affect device reliability.

(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The output positive-voltage rating may be exceeded up to 6.5V maximum if the output current rating is observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) ^{(1) (2) (3)}

				MIN	TYP	MAX	UNIT
V_{CCA}	Supply voltage A - Relative to GNDA			1.71		5.5	V
V_{CCB}	Supply voltage B - Relative to GNDB			1.71		5.5	V
V_{GNDA} to V_{GNDB}	Voltage between GNDA and GNDB	Voltage between GNDA and GNDB	Voltage between GNDA and GNDB	-10		10	V
I_{OH}	High-level output current		$V_{CCO} = 1.71V$	-4.5			mA
			$V_{CCO} = 2.3V$	-8			
			$V_{CCO} = 3V$	-10			
			$V_{CCO} = 4.5V$	-12			
I_{OL}	Low-level output current		$V_{CCO} = 1.71V$		4.5		mA
			$V_{CCO} = 2.3V$		8		
			$V_{CCO} = 3V$		10		
			$V_{CCO} = 4.5V$		12		
V_I	Input voltage - Relative to GNDA			0		5.5	V
V_O	Output voltage - Relative to GNDB			0		V_{CCO}	V
T_A	Operating free-air temperature			-40		125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.

(2) V_{CCO} is the V_{CC} associated with the output port.

(3) All control inputs and data I/Os of this device have weak pulldowns to ensure the line is not floating when undefined external to the device. The input leakage from these weak pulldowns is defined by the I_I specification indicated under [Section 5.5](#).

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TXG802x	UNIT
		D (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	122.0	°C/W
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	60.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.8	°C/W
Y_{JT}	Junction-to-top characterization parameter	11.5	°C/W
Y_{JB}	Junction-to-board characterization parameter	68.8	°C/W
$R_{\theta JC(\text{bottom})}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

PARAMETER	TEST CONDITIONS	V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)			UNIT	
				–40°C to 125°C				
				MIN	TYP	MAX		
V_{OH}	High-level output voltage ⁽³⁾	$I_{OH} = -4.5\text{mA}$	1.71V	1.71V	1.5		V	
		$I_{OH} = -8\text{mA}$	2.3V	2.3V	2.0			
		$I_{OH} = -10\text{mA}$	3V	3V	2.7			
		$I_{OH} = -12\text{mA}$	4.5V	4.5V	4.1			
V_{OL}	Low-level output voltage ⁽⁴⁾	$I_{OL} = 4.5\text{mA}$	1.71V	1.71V		0.16	V	
		$I_{OL} = 8\text{mA}$	2.3V	2.3V		0.27		
		$I_{OL} = 10\text{mA}$	3V	3V		0.34		
		$I_{OL} = 12\text{mA}$	4.5V	4.5V		0.41		
V_{T+}	Positive-going input-threshold voltage	Data Inputs (Ax, Bx) (Referenced to V_{CCI})	1.71V	1.71V		1.11	V	
			2.3V	2.3V		1.40		
			3V	3V		1.73		
			4.5V	4.5V		2.45		
			5.5V	5.5V		3.0		
V_{T-}	Negative-going input-threshold voltage	Data Inputs (Ax, Bx) (Referenced to V_{CCI})	1.71V	1.71V	0.56		V	
			2.3V	2.3V	0.80			
			3V	3V	1.14			
			4.5V	4.5V	1.59			
			5.5V	5.5V	2.0			
ΔV_T	Input-threshold hysteresis ($V_{T+} - V_{T-}$)	Data Inputs (Ax, Bx) (Referenced to V_{CCI})	1.71V	1.71V	0.3	0.55	V	
			2.3V	2.3V	0.36	0.60		
			3V	3V	0.38	0.54		
			4.5V	4.5V	0.41	0.86		
ΔV_T	Input-threshold hysteresis ($V_{T+} - V_{T-}$)	Data Inputs (Ax, Bx) (Referenced to V_{CCI})	5.5V	5.5V	0.40	0.96	V	
I_I	Input leakage current	Data Inputs (Ax, Bx) $V_I = V_{CCI}$ or GND	1.71V – 5.5V	1.71V – 5.5V	0.2	1.6	μA	
$I_{off\text{-float}}$	Floating supply Partial power down current	A Port or B Port $V_I = V_{CC}$	Floating ⁽⁵⁾	0V - 5.5V	0.26	1.55	μA	
			0V - 5.5V	Floating ⁽⁵⁾	0.26	1.55		

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

PARAMETER		TEST CONDITIONS	V _{CCA}	V _{CCB}	Operating free-air temperature (T _A)			UNIT	
					−40°C to 125°C				
					MIN	TYP	MAX		
I _{off-float}	Floating supply Partial power down current	A Port or B Port V _I = GND	Floating ⁽⁵⁾	0V - 5.5V			0.06	nA	
I _{off-float}	Floating supply Partial power down current		0V - 5.5V	Floating ⁽⁵⁾			0.39	nA	
C _i	Control Input Capacitance	V _I = 3.3V or V _{GNDA}	3.3V	3.3V			2	pF	
C _{io}	Data I/O Capacitance	V _O = 1.71V DC +1MHz -16dBm sine wave	3.3V	3.3V	1.3		2.6	pF	
C _{GND}	Cap between grounds	All channels combined (V _{CC} both sides are powered on)					46	pF	
		All channels combined (V _{CC} to GND shorted)					53	pF	
Leakage	Current Leakage between GndA to GndB	All channels combined (V _{CC} both sides are powered on and inputs are all low)	1.71V – 5.5V	1.71V – 5.5V			0.06	µA	
		All channels combined (V _{CC} both sides are powered on and inputs are all high)	1.71V – 5.5V	1.71V – 5.5V			32	µA	
		All channels combined (V _{CC} to GND shorted)	1.71V – 5.5V	1.71V – 5.5V			0.04	µA	
CMTI	Common Mode Transient Immunity	Input toggling at 100Mbps Ground shift up to 10V	1.71V – 5.5V	1.71V – 5.5V	1			kV/µs	
V _{UVLO+}	Positive-Going Undervoltage Lockout Voltage	A Supply	1.71V – 5.5V				1.64	V	
		B Supply		1.71V – 5.5V			1.64	V	
V _{UVLO-}	Negative-Going Undervoltage Lockout Voltage	A Supply	1.71V – 5.5V		1.2			V	
		B Supply		1.71V – 5.5V	1.2			V	
V _{UVLO_Hys}	Undervoltage Lockout Hysteresis	A Supply	1.71V – 5.5V		58			mV	
		B Supply		1.71V – 5.5V	58			mV	

 (1) V_{CCI} is the V_{CC} associated with the input port and referenced to GND_A

 (2) V_{CCO} is the V_{CC} associated with the output port and referenced to GND_B

 (3) Tested at V_I = V_{T+(MAX)}

 (4) Tested at V_I = V_{T-(MIN)}

(5) Floating is defined as a node that is both not actively driven by an external device and has leakage not exceeding 10nA

5.6 Supply Current

over operating free-air temperature range (unless otherwise noted)⁽¹⁾ ⁽²⁾

PARAMETER	TEST CONDITIONS	V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)		UNIT	
				-40°C to 125°C			
				MIN	TYP	MAX	
TXGx021							
I_{CCA}	V_{CCA} supply current	$V_I = V_{CCI}$ or GND $I_O = 0$	1.71V – 5.5V	1.71V – 5.5V	300	747	μA
			0V	5.5V	-2	12.5	
			5.5V	0V	349	589	
	V_{CCB} supply current	$V_I = GND$ $I_O = 0$	5.5V	Floating ⁽³⁾	347	577	
			1.71V – 5.5V	1.71V – 5.5V	497	1077	
			0V	5.5V	546	919	
$I_{CCA} + I_{CCB}$	Supply Current - DC Signal	$V_I = V_{CCI}$	5.5V	0V	-2	24.5	μA
			Floating ⁽³⁾	5.5V	548	919	
			1.8V	1.8V	0.7	1.6	
			2.5V	2.5V	0.8	1.6	
			3.3V	3.3V	0.8	1.7	
	$V_I = GND$		5V	5V	0.8	1.9	mA
			1.8V	1.8V	0.7	1.6	
			2.5V	2.5V	0.8	1.6	
			3.3V	3.3V	0.8	1.7	
			5V	5V	0.8	1.9	

over operating free-air temperature range (unless otherwise noted)⁽¹⁾ ⁽²⁾

PARAMETER	TEST CONDITIONS	V _{CCA}	V _{CCB}	Operating free-air temperature (T _A)			UNIT	
				-40°C to 125°C				
				MIN	TYP	MAX		
I _{CCA} + I _{CCB}	Supply Current - AC Signal	All channels switching with square wave clock input; CL = 15pF, 1Mbps	1.8V	1.8V	0.9	1.6	mA	
			2.5V	2.5V	0.9	1.6		
			3.3V	3.3V	0.9	1.7		
			5V	5V	1.1	2		
		All channels switching with square wave clock input; CL = 15pF, 50Mbps	1.8V	1.8V	4.6	6.3	mA	
			2.5V	2.5V	5.5	7.3		
			3.3V	3.3V	6.8	8.2		
			5V	5V	8.7	10.7		
		All channels switching with square wave clock input; CL = 15pF, 100Mbps	1.8V	1.8V	8.5	10.6	mA	
			2.5V	2.5V	10	13		
			3.3V	3.3V	12	14.7		
			5V	5V	16.6	20.2		
TXGx020								
I _{CCA}	V _{CCA} supply current	V _I = V _{CCI} or GND I _O = 0	1.71V – 5.5V	1.71V – 5.5V	299	602	µA	
			0V	5.5V	-2.5	1.2	µA	
			5.5V	0V	302	602	µA	
I _{CCB}	V _{CCB} supply current	V _I = V _{CCI} or GND I _O = 0	1.71V – 5.5V	1.71V – 5.5V	504	1225	µA	
			0V	5.5V	486	906	µA	
			5.5V	0V	-2	24.5	µA	
		V _I = GND I _O = 0	Floating ⁽³⁾	5.5V	486	906	µA	
			Floating ⁽³⁾	5.5V	486	906	µA	
I _{CCA} + I _{CCB}	Supply Current - DC Signal	V _I = V _{CCI}	1.8V	1.8V	0.7	1.6	mA	
			2.5V	2.5V	0.8	1.6	mA	
			3.3V	3.3V	0.8	1.7	mA	
			5V	5V	0.8	1.9	mA	
		V _I = GND	1.8V	1.8V	0.7	1.6	mA	
			2.5V	2.5V	0.8	1.6	mA	
			3.3V	3.3V	0.8	1.7	mA	
			5V	5V	0.8	1.9	mA	
			1.8V	1.8V	0.7	1.6	mA	
			2.5V	2.5V	0.8	1.6	mA	

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

PARAMETER		TEST CONDITIONS	V _{CCA}	V _{CCB}	Operating free-air temperature (T _A)			UNIT	
					−40°C to 125°C				
					MIN	TYP	MAX		
I _{CCA} + I _{CCB}	Supply Current - AC Signal	All channels switching with square wave clock input; CL = 15pF, 1Mbps	1.8V	1.8V	0.9	1.6	mA	mA	
			2.5V	2.5V	0.9	1.6	mA		
			3.3V	3.3V	0.9	1.7	mA		
			5V	5V	1.1	2	mA		
		All channels switching with square wave clock input; CL = 15pF, 50Mbps	1.8V	1.8V	4.5	6.3	mA		
			2.5V	2.5V	5.5	7.3	mA		
			3.3V	3.3V	6.3	8	mA		
			5V	5V	8.4	10.7	mA		
		All channels switching with square wave clock input; CL = 15pF, 100Mbps	1.8V	1.8V	8.5	10.7	mA		
			2.5V	2.5V	10	13	mA		
			3.3V	3.3V	12	14.7	mA		
			5V	5V	16.6	20.2	mA		

(1) V_{CCI} is the V_{CC} associated with the input port and referenced to GND_A

(2) V_{CCO} is the V_{CC} associated with the output port and referenced to GND_B

(3) Floating is defined as a node that is both not actively driven by an external device and has leakage not exceeding 10nA

5.7 Switching Characteristics, V_{CCA} = 1.8 ± 0.15V

PARAMETER		TEST CONDITIONS	FROM	TO	TEMPERATURE	B-Port Supply Voltage (V _{CCB})								UNIT	
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t _{pd}	Propagation delay	1Mbps all 4 channels toggling	A	B	-40°C to 85°C	2.8	7.3	2.8	2.8	7.4	2.8	7.5	2.9	7.8	ns
			A	B	-40°C to 125°C	2.8	7.6	2.8	2.8	7.8	2.8	7.9	2.9	8.3	
			B	A	-40°C to 85°C	2.8	7.3	2.7	5.7	2.6	5.1	2.6	4.8		
			B	A	-40°C to 125°C	2.8	7.7	2.7	6	2.6	5.3	2.6	5.1		
PWD	Pulse width distortion	t _{phl} - t _{plh}	A	B	-40°C to 85°C	0.7	1.5	0.6	1.5	0.5	1.4	0.5	1.2		ns
			A	B	-40°C to 125°C	0.7	1.5	0.6	1.5	0.5	1.4	0.5	1.2		
			B	A	-40°C to 85°C	0.7	1.5	0.6	1.5	0.5	1.4	0.5	1.2		
			B	A	-40°C to 125°C	0.7	1.5	0.6	1.5	0.5	1.4	0.4	1.2		

PARAMETER		TEST CONDITIONS	FROM	TO	TEMPERATURE	B-Port Supply Voltage (V _{CCB})												UNIT	
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V				
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t _r	Output signal rise time		A	B	-40°C to 85°C	0.5	1.3	0.5	1.35	0.5	1.4	0.5	1.6					ns	
			A	B	-40°C to 125°C	0.5	1.3	0.5	1.4	0.5	1.4	0.5	1.7						
			B	A	-40°C to 85°C	0.5	1.2	0.5	1.3	0.5	1.2	0.5	1.3						
			B	A	-40°C to 125°C	0.5	1.3	0.5	1.4	0.5	1.3	0.5	1.3						
t _f	Output signal fall time		A	B	-40°C to 85°C	0.4	1.3	0.4	1.3	0.4	1.5	0.5	1.7					ns	
			A	B	-40°C to 125°C	0.4	1.5	0.4	1.5	0.4	1.6	0.5	2						
			B	A	-40°C to 85°C	0.4	1.3	0.4	1.4	0.4	1.3	0.4	1.3						
			B	A	-40°C to 125°C	0.4	1.4	0.4	1.45	0.4	1.4	0.4	1.35						
t _{DO}	Default output delay time from input power loss	Measured from the time V _{CC} goes below 1.2V			-40°C to 85°C	6.1	10.6	6.1	10.4	6	10.3	5.9	9.9					μs	
					-40°C to 125°C	6.1	10.6	6.1	10.4	6	10.3	5.9	9.9						
t _{PU}	Time from ULVO to valid output data				-40°C to 85°C	21.1	64.3	4.3	69.1	4.5	76.6	55.3	99.4					μs	
					-40°C to 125°C	19.9	64.3	4.3	69.1	4.5	76.6	53.9	99.4						

5.8 Switching Characteristics, V_{CCA} = 2.5 ± 0.2V

PARAMETER		TEST CONDITIONS	FROM	TO	TEMPERATURE	B-Port Supply Voltage (V _{CCB})												UNIT	
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V				
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t _{pd}	Propagation delay	1Mbps all 4 channels toggling	A	B	-40°C to 85°C	2.7	5.7	2.7	5.8	2.7	5.9	2.8	6.3					ns	
			A	B	-40°C to 125°C	2.7	6	2.7	6.1	2.7	6.2	2.8	6.6						
			B	A	-40°C to 85°C	2.8	7.4	2.7	5.8	2.6	5.1	2.6	4.9						
			B	A	-40°C to 125°C	2.8	7.7	2.7	6.1	2.6	5.5	2.6	5.2						
PWD	Pulse width distortion	t _{phl} - t _{plh}	A	B	-40°C to 85°C	0.1	1	0.1	0.8	0	0.7	-0.14	0.6					ns	
			A	B	-40°C to 125°C	0.1	1	0.1	0.8	0	0.7	-0.15	0.6						
			B	A	-40°C to 85°C	0.1	1	0.1	0.8	0	0.7	-0.14	0.6						
			B	A	-40°C to 125°C	0.1	1	0.1	0.8	0	0.7	-0.15	0.6						
t _r	Output signal rise time		A	B	-40°C to 85°C	0.5	1.3	0.5	1.3	0.5	1.4	0.5	1.6					ns	
			A	B	-40°C to 125°C	0.5	1.3	0.5	1.4	0.5	1.4	0.5	1.7						
			B	A	-40°C to 85°C	0.5	1.3	0.4	1.3	0.5	1.3	0.4	1.3						
			B	A	-40°C to 125°C	0.5	1.3	0.4	1.3	0.5	1.3	0.4	1.4						

PARAMETER		TEST CONDITIONS	FROM	TO	TEMPERATURE	B-Port Supply Voltage (V _{CCB})										UNIT		
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t _f	Output signal fall time		A	B	-40°C to 85°C	0.4	1.4	0.4	1.3	0.4	1.5	0.5	1.7				ns	
			A	B	-40°C to 125°C	0.4	1.4	0.4	1.5	0.4	1.6	0.5	2					
			B	A	-40°C to 85°C	0.4	1.3	0.4	1.3	0.4	1.35	0.4	1.3					
			B	A	-40°C to 125°C	0.4	1.5	0.4	1.5	0.4	1.4	0.4	1.5					
t _{DO}	Default output delay time from input power loss	Measured from the time V _{CC} goes below 1.2V			-40°C to 85°C	6.1	10.6	6.1	10.4	5.6	10.4	5.4	9.9				μs	
					-40°C to 125°C	6.1	10.6	6.1	10.4	5.6	10.4	5.4	9.9					
t _{PU}	Time from ULVO to valid output data				-40°C to 85°C	21.1	64.3	4.3	69.1	4.5	76.6	55.3	99.4				μs	
					-40°C to 125°C	19.9	64.3	4.3	69.1	4.5	76.6	53.9	99.4					

5.9 Switching Characteristics, V_{CCA} = 3.3 ± 0.3V

PARAMETER		TEST CONDITIONS	FROM	TO	TEMPERATURE	B-Port Supply Voltage (V _{CCB})										UNIT		
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t _{pd}	Propagation delay	1Mbps all 4 channels toggling	A	B	-40°C to 85°C	2.6	5.1	2.7	5.2	2.7	5.3	2.8	5.8				ns	
			A	B	-40°C to 125°C	2.6	5.3	2.7	5.5	2.7	5.7	2.8	6.3					
			B	A	-40°C to 85°C	2.8	7.5	2.7	5.9	2.7	5.3	2.6	5.1					
			B	A	-40°C to 125°C	2.8	7.9	2.7	6.2	2.7	5.7	2.6	5.4					
PWD	Pulse width distortion	t _{phl} - t _{plh}	A	B	-40°C to 85°C	-0.03	0.6	-0.09	0.5	-0.13	0.5	-0.3	0.4				ns	
			A	B	-40°C to 125°C	-0.11	0.6	-0.13	0.5	-0.18	0.5	-0.4	0.4					
			B	A	-40°C to 85°C	-0.03	0.6	-0.09	0.5	-0.13	0.5	-0.3	0.4					
			B	A	-40°C to 125°C	-0.11	0.6	-0.13	0.5	-0.18	0.5	-0.4	0.4					
t _r	Output signal rise time		A	B	-40°C to 85°C	0.5	1.3	0.5	1.3	0.5	1.4	0.5	1.6				ns	
			A	B	-40°C to 125°C	0.5	1.3	0.5	1.4	0.5	1.4	0.5	1.6					
			B	A	-40°C to 85°C	0.5	1.3	0.5	1.3	0.5	1.4	0.5	1.4					
			B	A	-40°C to 125°C	0.5	1.35	0.5	1.4	0.5	1.4	0.5	1.5					
t _f	Output signal fall time		A	B	-40°C to 85°C	0.4	1.3	0.4	1.4	0.4	1.5	0.5	1.7				ns	
			A	B	-40°C to 125°C	0.4	1.5	0.4	1.6	0.4	1.6	0.5	2					
			B	A	-40°C to 85°C	0.4	1.4	0.4	1.4	0.4	1.4	0.4	1.4					
			B	A	-40°C to 125°C	0.4	1.7	0.4	1.6	0.4	1.6	0.4	1.7					

PARAMETER		TEST CONDITIONS	FROM	TO	TEMPERATURE	B-Port Supply Voltage (V _{CCB})												UNIT	
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V				
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t _{DO}	Default output delay time from input power loss	Measured from the time V _{CC} goes below 1.2V			-40°C to 85°C	6	10.6	5.8	10.4	5.8	10.3	5.8	10.3	5.8	10.3	5.8	10	μs	
					-40°C to 125°C	6	10.6	5.8	10.4	5.8	10.3	5.8	10.3	5.8	10.3	5.8	10	μs	
t _{PU}	Time from ULVO to valid output data				-40°C to 85°C	21.1	64.3	4.3	69.1	4.5	76.6	57.8	99.4	57.8	99.4	57.8	99.4	μs	
					-40°C to 125°C	19.9	64.3	4.3	69.1	4.5	76.6	53.9	99.4	53.9	99.4	53.9	99.4	μs	

5.10 Switching Characteristics, V_{CCA} = 5.0 ± 0.5V

PARAMETER		TEST CONDITIONS	FROM	TO	TEMPERATURE	B-Port Supply Voltage (V _{CCB})												UNIT	
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V				
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t _{pd}	Propagation delay	1Mbps all 4 channels toggling	A	B	-40°C to 85°C	2.6	4.8	2.6	5	2.7	5.1	2.8	5.6	2.8	5.6	2.8	5.6	ns	
					-40°C to 125°C	2.6	5.1	2.6	5.3	2.7	5.4	2.8	5.9	2.8	5.9	2.8	5.9		
			B	A	-40°C to 85°C	3	7.9	2.8	6.2	2.7	5.9	2.7	5.6	2.7	5.6	2.7	5.6		
					-40°C to 125°C	3	8.4	2.8	6.6	2.7	6.2	2.7	6.2	2.7	6.2	2.7	6		
PWD	Pulse width distortion	t _{phl} - t _{plh}	A	B	-40°C to 85°C	-0.22	0.4	-0.27	0.3	-0.32	0.3	-0.50	0.2	-0.50	0.2	-0.50	0.2	ns	
					-40°C to 125°C	-0.33	0.4	-0.37	0.3	-0.42	0.3	-0.60	0.2	-0.60	0.2	-0.60	0.2		
			B	A	-40°C to 85°C	-0.22	0.4	-0.27	0.3	-0.32	0.3	-0.5	0.2	-0.5	0.2	-0.5	0.2		
					-40°C to 125°C	-0.33	0.4	-0.37	0.3	-0.42	0.3	-0.60	0.2	-0.60	0.2	-0.60	0.2		
t _r	Output signal rise time		A	B	-40°C to 85°C	0.5	1.3	0.5	1.3	0.5	1.4	0.5	1.6	0.5	1.6	0.5	1.6	ns	
					-40°C to 125°C	0.5	1.3	0.5	1.4	0.5	1.4	0.5	1.6	0.5	1.6	0.5	1.6		
			B	A	-40°C to 85°C	0.6	1.6	0.6	1.6	0.6	1.6	0.6	1.6	0.5	1.6	0.5	1.6		
					-40°C to 125°C	0.6	1.75	0.6	1.7	0.6	1.7	0.6	1.7	0.5	1.6	0.5	1.6		
tf	Output signal fall time		A	B	-40°C to 85°C	0.4	1.3	0.4	1.4	0.4	1.5	0.5	1.7	0.5	1.7	0.5	1.7	ns	
					-40°C to 125°C	0.4	1.4	0.4	1.5	0.4	1.6	0.5	1.8	0.4	1.8	0.4	1.8		
			B	A	-40°C to 85°C	0.4	1.8	0.5	1.8	0.4	1.8	0.4	1.8	0.4	1.8	0.4	1.8		
					-40°C to 125°C	0.4	2.5	0.5	2	0.4	2	0.4	2	0.4	2	0.4	2		
t _{DO}	Default output delay time from input power loss	Measured from the time V _{CC} goes below 1.2V			-40°C to 85°C	5.5	10.7	5.6	10.5	5.7	10.6	5.9	10	5.9	10	5.9	10	μs	
					-40°C to 125°C	5.5	10.7	5.6	10.5	5.7	10.6	5.9	10	5.9	10	5.9	10		
t _{PU}	Time from ULVO to valid output data				-40°C to 85°C	21.1	64.3	4.3	69.1	4.5	76.6	55.3	99.4	55.3	99.4	55.3	99.4	μs	
					-40°C to 125°C	19.9	64.3	4.3	69.1	4.5	76.6	53.9	99.4	53.9	99.4	53.9	99.4		

5.11 Switching Characteristics: T_{sk} , T_{MAX}

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC1}	V_{CC0}	Operating free-air temperature (T_A)			UNIT	
				-40°C to 125°C				
				MIN	TYP	MAX		
T_{MAX} - Maximum Data Rate	50% Duty Cycle Input One channel switching 20% of pulse > 0.7* V_{CC0} 20% of pulse < 0.3* V_{CC0}	No Translation	1.65V - 1.95V	1.65V - 1.95V	264		Mbps	
			2.3V - 2.7V	2.3V - 2.7V	220			
			3.0V - 3.6V	3.0V - 3.6V	220			
			4.5V - 5.5V	4.5V - 5.5V	176			
T_{MAX} - Maximum Data Rate	50% Duty Cycle Input One channel switching 20% of pulse > 0.7* V_{CC0} 20% of pulse < 0.3* V_{CC0}	Up Translation	1.65V - 1.95V	2.3V - 2.7V	264		Mbps	
			1.65V - 1.95V	3.0V - 3.6V	264			
			1.65V - 1.95V	4.5V - 5.5V	264			
			2.3V - 2.7V	3.0V - 3.6V	220			
			2.3V - 2.7V	4.5V - 5.5V	220			
			3.0V - 3.6V	4.5V - 5.5V	176			
T_{MAX} - Maximum Data Rate	50% Duty Cycle Input One channel switching 20% of pulse > 0.7* V_{CC0} 20% of pulse < 0.3* V_{CC0}	Down Translation	2.3V - 2.7V	1.65V - 1.95V	264		Mbps	
			3.0V - 3.6V	2.3V - 2.7V	220			
			3.0V - 3.6V	1.65V - 1.95V	220			
			4.5V - 5.5V	3.0V - 3.6V	176			
			4.5V - 5.5V	1.65V - 1.95V	220			
			4.5V - 5.5V	1.65V - 1.95V	220			
t_{sk} - Output skew	Timing skew between any switching outputs on the rising or falling edge (same direction channels)	No Translation	1.65V - 1.95V	1.65V - 1.95V		0.02	ns	
			2.3V - 2.7V	2.3V - 2.7V		0.02		
			3.0V - 3.6V	3.0V - 3.6V		0.02		
			4.5V - 5.5V	4.5V - 5.5V		0.04		
t_{sk} - Output skew	Timing skew between any switching outputs on the rising or falling edge (same direction channels)	Up Translation	1.65V - 1.95V	2.3V - 2.7V		0.02	ns	
			1.65V - 1.95V	3.0V - 3.6V		0.02		
			1.65V - 1.95V	4.5V - 5.5V		0.02		
			2.3V - 2.7V	3.0V - 3.6V		0.02		
			2.3V - 2.7V	4.5V - 5.5V		0.02		
			3.0V - 3.6V	4.5V - 5.5V		0.02		

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CCI}	V _{CCO}	Operating free-air temperature (T _A)			UNIT	
				-40°C to 125°C				
				MIN	TYP	MAX		
t _{sk} - Output skew	Timing skew between any switching outputs on the rising or falling edge (same direction channels)	Down Translation	2.3V - 2.7V	1.65V - 1.95V		0.02	ns	
			3.0V - 3.6V	2.3V - 2.7V		0.02		
			3.0V - 3.6V	1.65V - 1.95V		0.02		
			4.5V - 5.5V	3.0V - 3.6V		0.04		
			4.5V - 5.5V	2.3V - 2.7V		0.04		
			4.5V - 5.5V	1.65V - 1.95V		0.04		

6 Typical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

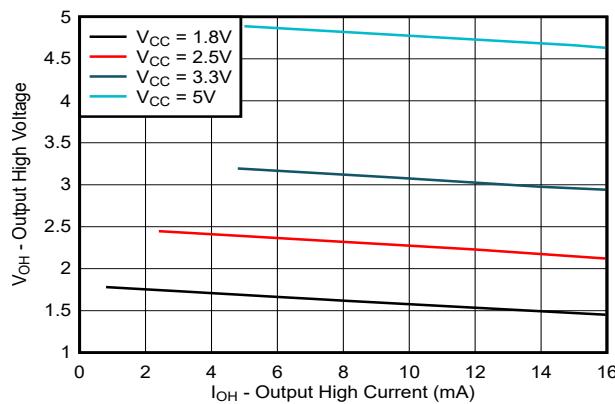


Figure 6-1. Output High Voltage ($V_{O\bar{H}}$) vs Source Current ($I_{O\bar{H}}$)

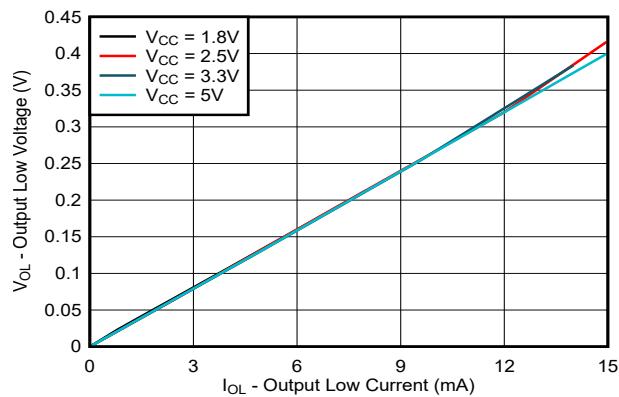


Figure 6-2. Output Low Voltage ($V_{O\bar{L}}$) vs Sink Current ($I_{O\bar{L}}$)

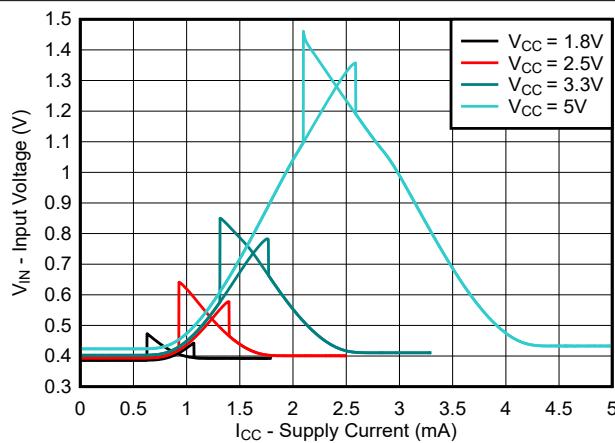


Figure 6-3. Supply Current (I_{CC_A}) vs Input Voltage (V_{IN}) [TXG0x021]

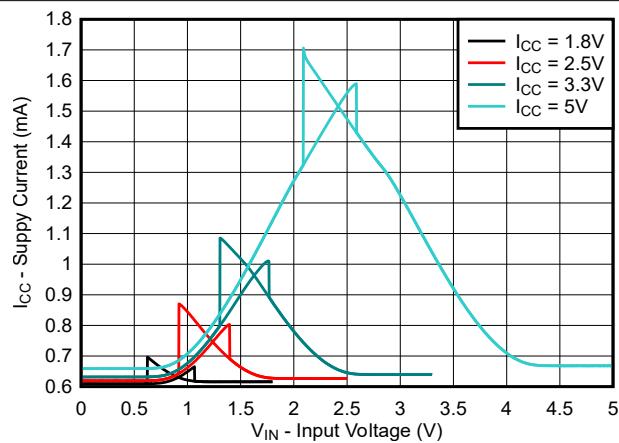


Figure 6-4. Supply Current (I_{CC_B}) vs Input Voltage (V_{IN}) [TXG0x021]

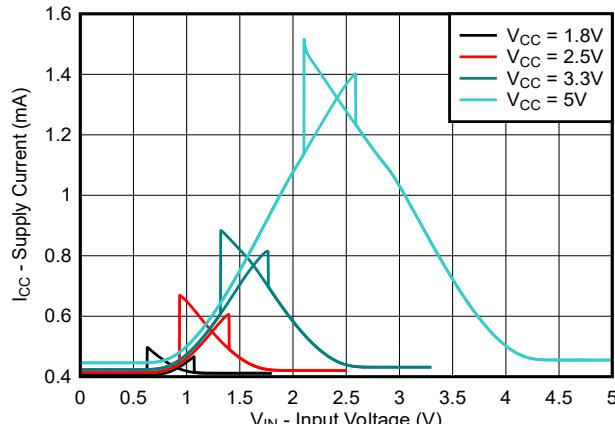


Figure 6-5. Supply Current (I_{CC_A}) vs Input Voltage (V_{IN}) [TXGx020]

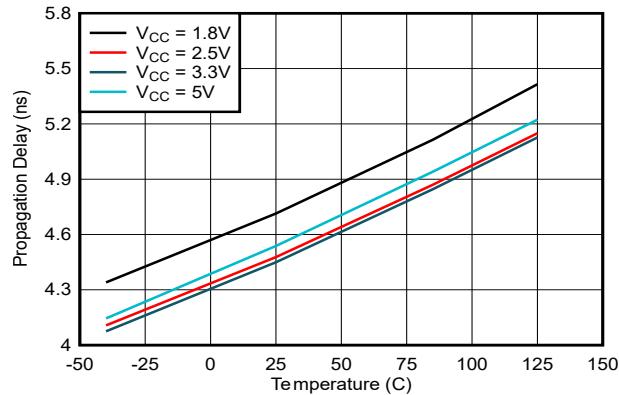


Figure 6-6. Propagation Delay, T_{PLH} , vs Temperature

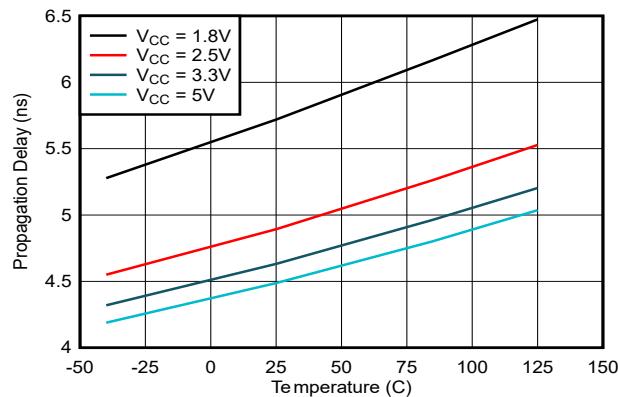


Figure 6-7. Propagation Delay, T_{PHL} , vs Temperature

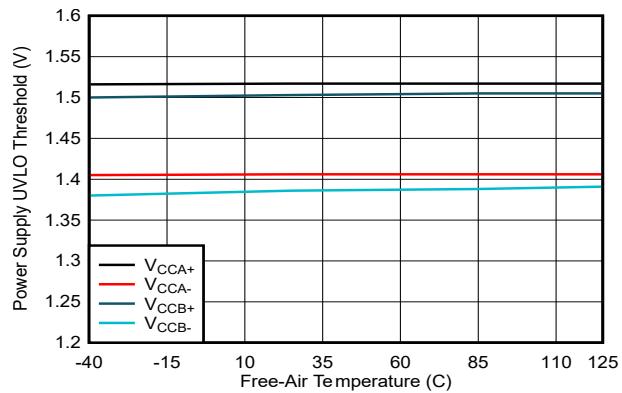


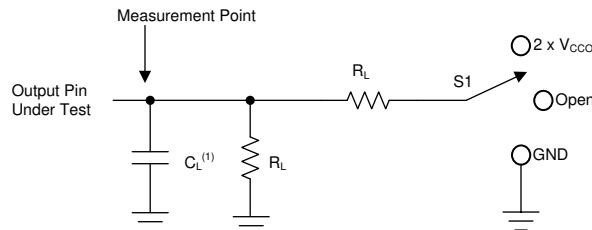
Figure 6-8. Power Supply Undervoltage Threshold vs Free-Air Temperature

7 Parameter Measurement Information

7.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, generators supply all input pulses that have the following characteristics:

- $f = 1\text{MHz}$
- $Z_O = 50\Omega$
- $\Delta t / \Delta V \leq 1\text{ns/V}$

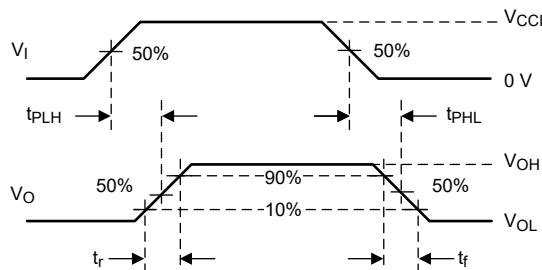


A. C_L includes probe and jig capacitance.

Figure 7-1. Load Circuit

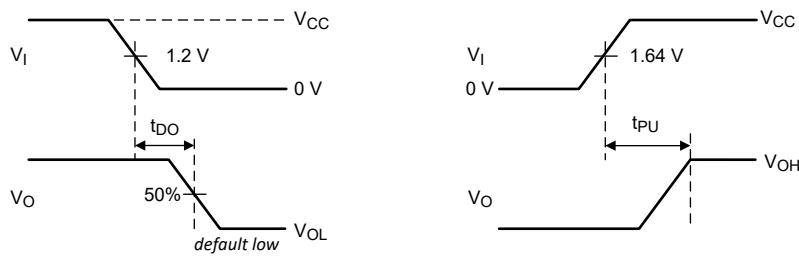
Table 7-1. Load Circuit Conditions

Parameter	V _{CCO}	R _L	C _L	S ₁	V _{TP}	
t _{pd}	Propagation (delay) time	1.71V – 5.5V	10kΩ	15pF	Open	N/A



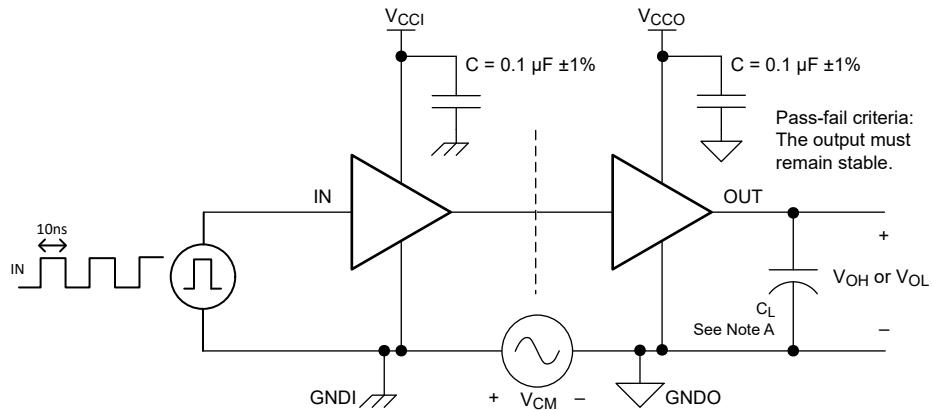
1. V_{CC1} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L , C_L , and S_1 .

Figure 7-2. Switching Characteristics Voltage Waveforms



1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L , C_L , and S_1

Figure 7-3. Default Output Delay Time & Time from UVLO to Valid Output Voltage Waveform



1. $C_L = 15\text{pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 7-4. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

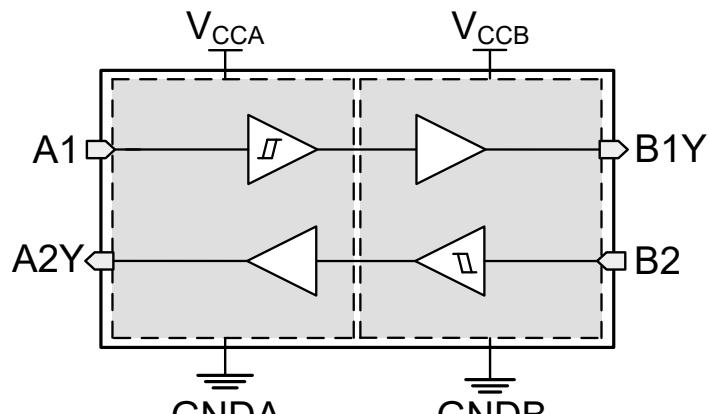
The TXG102x is a 2-bit ground-level translator that uses two individually configurable power-supply rails which allows it to translate across two different power domains. The device is operational with V_{CCA} and V_{CCB} supplies as low as 1.71V and as high as 5.5V. The A port is designed to track V_{CCA} and the B port is designed to track V_{CCB} . In addition to I/O level shifting, this translator can support a difference of -10V to +10V between GNDA and GNDB. V_{CCA} is referenced to GNDA and V_{CCB} is referenced to GNDB.

The TXG102x device is designed for asynchronous communication between data buses, and transmits data with fixed direction from the A bus to the B bus on some channels and from the B bus to the A bus on the remaining channels.

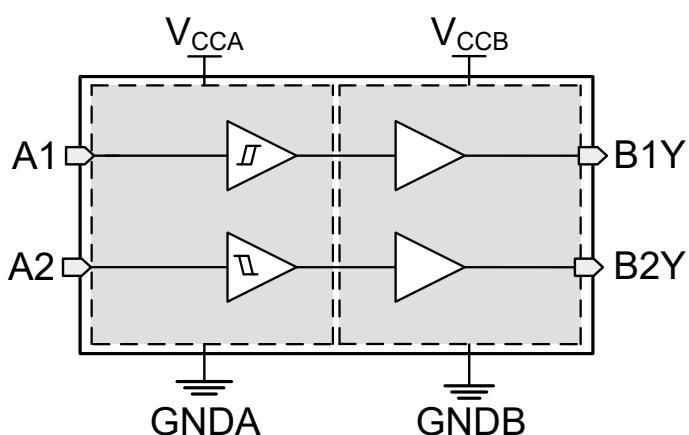
The V_{CC} disconnect feature ensures that if V_{CC} is disconnected with the complementary supply within recommended operating conditions, outputs are disabled and set to the high-impedance state while the supply current is maintained. The $I_{off\cdot float}$ circuitry ensures that no excessive current is drawn from or sourced into an input or output while the supply is floating.

Glitch-free power supply sequencing allows either supply rail to be powered on or off in any order while providing robust power sequencing performance.

8.2 Functional Block Diagram



TXG1021 Functional Block Diagram



TXG1020 Functional Block Diagram

8.3 Feature Description

8.3.1 CMOS Schmitt-Trigger Inputs with Integrated Pulldowns

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the [Section 5.5](#). The worst case resistance is calculated with the maximum input voltage, given in the [Section 5.1](#), and the maximum input leakage current, given in the [Section 5.5](#), using ohm's law ($R = V \div I$).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the [Section 5.5](#), which makes this device extremely tolerant to slow or noisy inputs. Driving the inputs slowly will increase dynamic current consumption of the device. See [Understanding Schmitt Triggers](#) for additional information regarding Schmitt-trigger inputs.

8.3.1.1 Inputs with Integrated Static Pull-Down Resistors

This device has $5\text{M}\Omega$ typical integrated weak pull-downs for each input. This feature allows all inputs to be left floating without the concern for unstable outputs or increased current consumption. This also helps to reduce external component count for applications where not all channels are used or need to be fixed low. If an external pull-up is required, it should be no larger than $1\text{M}\Omega$ to avoid contention with the $5\text{M}\Omega$ internal pull-down.

8.3.2 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. [Section 5.1](#) defines the electrical and thermal limits that must be followed at all times.

8.3.3 V_{CC} Disconnect

The outputs for this device are disabled and enter a high-impedance state when either supply is left floating (disconnected), and with the complementary supply within recommended operating conditions. It is recommended that the inputs are kept low before floating (disconnecting) either supply.

The $I_{CCx(\text{floating})}$ in the [Section 5.5](#) specifies the maximum supply current. The $I_{off(\text{float})}$ in the [Section 5.5](#) specifies the maximum leakage into or out of any input or output pin on the device.

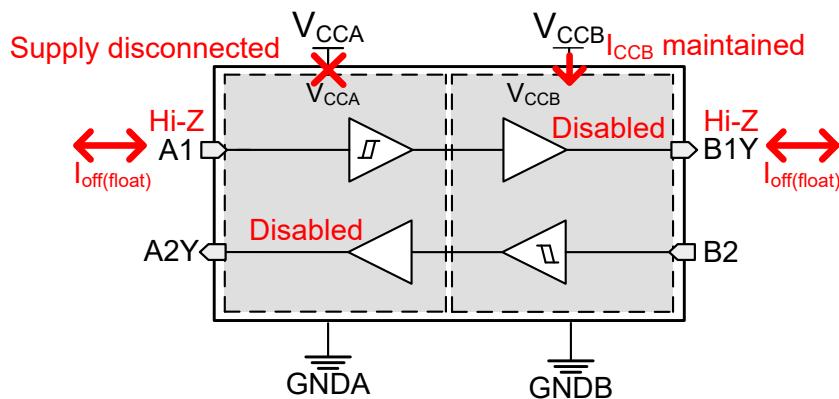


Figure 8-1. V_{CC} Disconnect Feature

8.3.4 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the [Section 5.3](#).

8.3.5 Glitch-Free Power Supply Sequencing

Either supply rail may be powered on or off in any order without producing a glitch on the inputs or outputs (that is, where the output erroneously transitions to V_{CC} when it should be held low or vice versa). Glitches of this

nature can be misinterpreted by a peripheral as a valid data bit, which could trigger a false device reset of the peripheral, a false device configuration of the peripheral, or even a false data initialization by the peripheral.

8.3.6 Negative Clamping Diodes

Figure 8-2 depicts the inputs and outputs to this device that have negative clamping diodes.

CAUTION

Voltages beyond the values specified in the [Section 5.1](#) table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

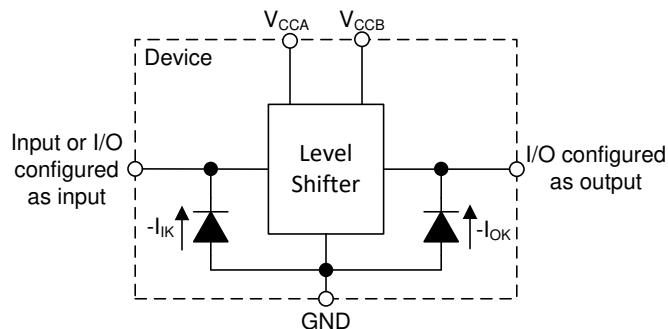


Figure 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.7 Fully Configurable Dual-Rail Design

The V_{CCA} and V_{CCB} pins can be supplied at any voltage from 1.71V to 5.5V, making the device suitable for translating between any of the voltage nodes (1.8V, 2.5V, 3.3V, and 5.0V).

8.3.8 Supports High-Speed Translation

The TXG102x device can support high data-rate applications. The translated signal data rate can be greater than 250Mbps when the signal is translated from 1.71V to 5.5V.

8.3.9 AC Noise Rejection

TXG102x supports I/O voltage translation in environments with noisy grounds. The plot below illustrates the amount of noise that GNDA and GNDB can reject in terms peak-to-peak voltage over frequency without disrupting communication between two systems. As an example, Figure 8-4 below shows GNDA with a ground bounce of $2V_{PP}$ at 10kHz but still effectively translating 5V to 2.5V without any degradation.

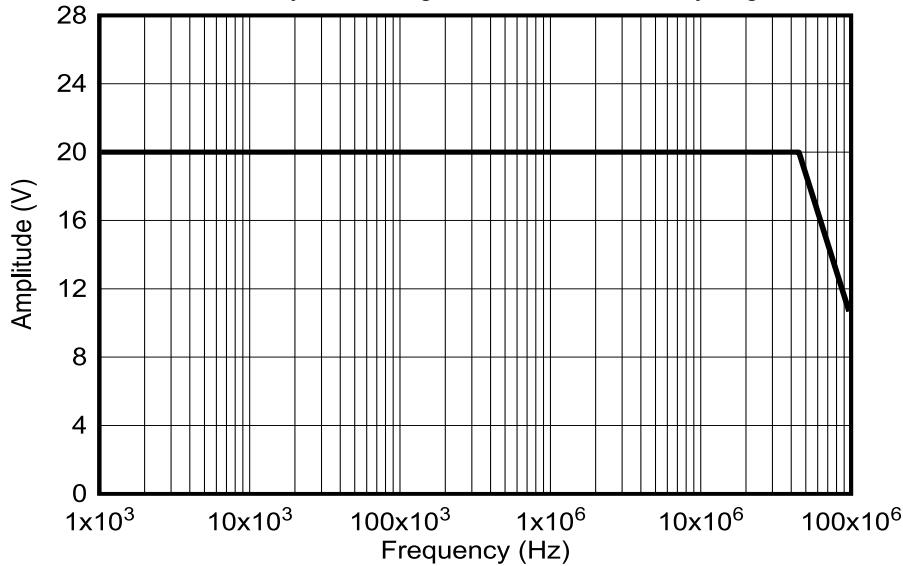


Figure 8-3. AC Noise Rejection Plot

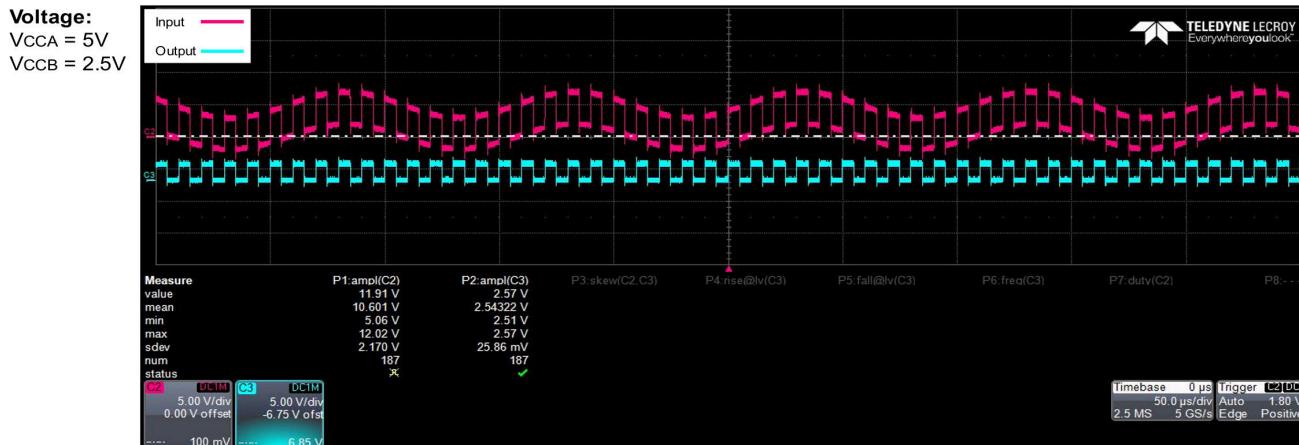


Figure 8-4. Waveform showing 5V to 2.5V I/O translation with AC Ground Noise of $2V_{PP}$ at 10kHz

8.4 Device Functional Modes

Table 8-1. Function Table

Power Supply ⁽¹⁾		Port Status	
VCCI	VCCO	Input	Output
PU	PU	H	H
PU	PU	L	L
PU	PU	Open	L
PD	PU	X	L

(1) In the table above: PU = Powered Up; PD = Powered Down; X = Irrelevant; H = High Level; L = Low Level; Open = Floating

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TXG102x is used for level translation, enabling communication between devices or systems operating at different interface and ground voltages. The TXG102x device is ideal for use in applications where a push-pull driver is connected to the data inputs. [Figure 9-1](#) is an example of two systems that translate from 1.8V to 3.3V across a SPI interface while also seeing a ground shift of -3V on GNDB while GNDA is at 0V. The ground shift of 3V is from the noisy power ground of the Digital-to-Analog Converter (DAC).

9.2 Typical Application

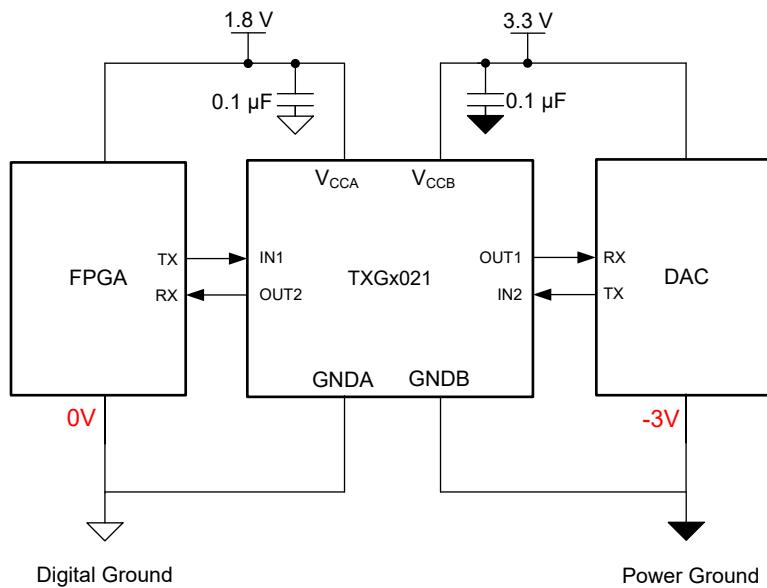


Figure 9-1. TXG1021 in Test and Measurement

9.2.1 Design Requirements

Use the parameters listed in [Table 9-1](#) for this design example.

Table 9-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	1.71V to 5.5V
Output voltage range	1.71V to 5.5V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
 - Use the supply voltage of the device that is driving the TXG102x device to determine the input voltage range. For a valid logic-high, the value must exceed the positive-going input-threshold voltage (V_{T+}) of the

input port. For a valid logic low the value must be less than the negative-going input-threshold voltage (V_{T^-}) of the input port.

- Output voltage range
 - Use the supply voltage of the device that the TXG102x device is driving to determine the output voltage range.

9.2.3 Application Curves

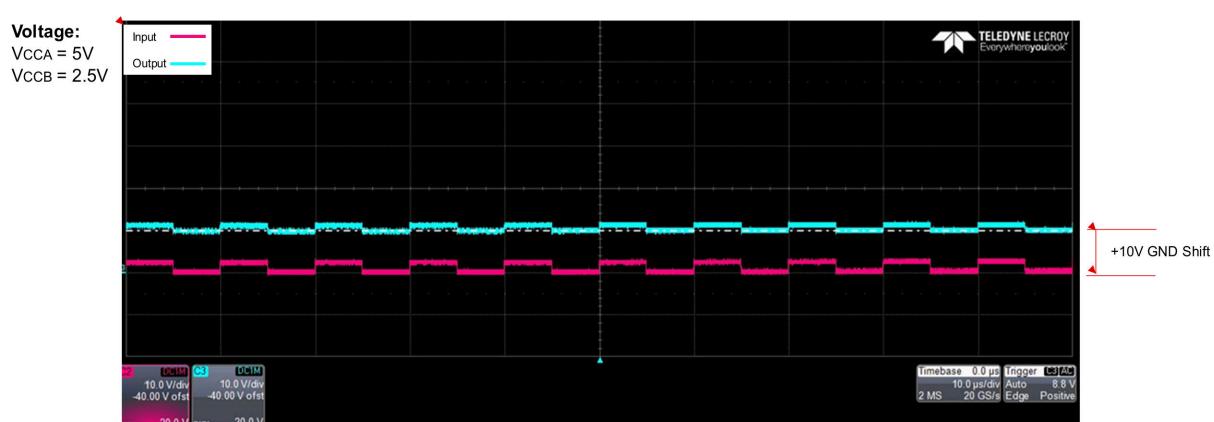
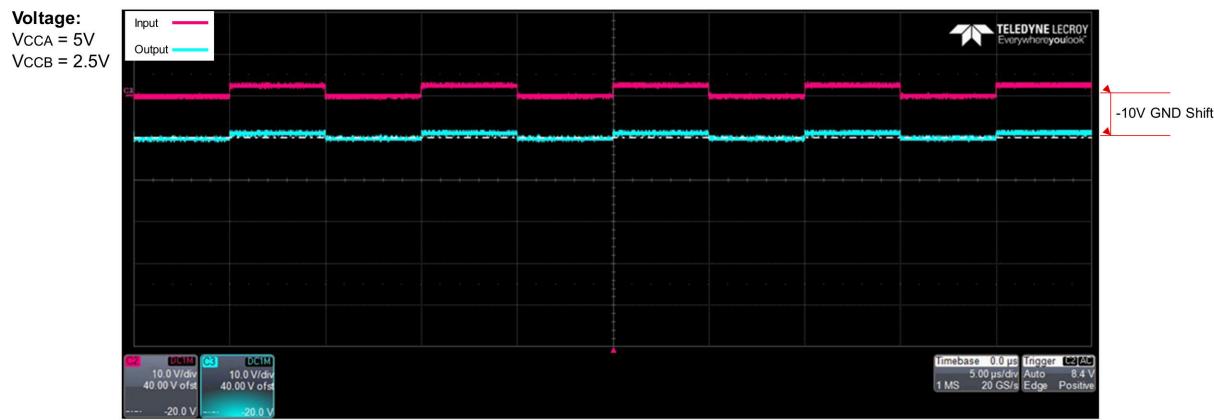


Figure 9-2. Waveform showing -10V (top) and +10V (bottom) Ground Shift with 5V to 2.5V I/O Translation

9.3 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch free power sequencing without any supply sequencing requirements such as ramp order or ramp rate. Please make sure the difference between V_{CC} and GND remains at 6.5V max at all times.

9.4 Layout

9.4.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Use bypass capacitors on the power supply pins and place them as close to the device as possible. A 0.1 μ F capacitor is recommended, but transient performance can be improved by having 1 μ F and 0.1 μ F capacitors in parallel as bypass capacitors.
- The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing.
- A 0.1 μ F capacitor can be added between GNDA and GNDB to improve performances of CMTI.

9.4.2 Layout Example

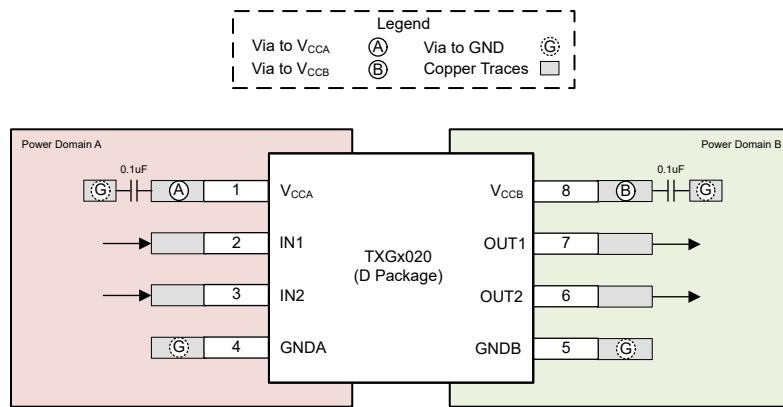


Figure 9-3. D Layout Example

10 Device and Documentation Support

10.1 Device Support

10.1.1 Regulatory Requirements

No statutory or regulatory requirements apply to this device.

There are no special characteristics for this product.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Understanding Schmitt Triggers](#) application report
- Texas Instruments, [CMOS Power Consumption and \$C_{pd}\$ Calculation](#) application report

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

10.5 Trademarks

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10.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

[TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2025) to Revision A (November 2025)	Page
• Updated data sheet status from <i>Advanced Information</i> to <i>Production Data</i>	1
• Updated CMTI minimum specification.....	9
• Added Typical Characteristics plots.....	19
• Added Functional Block Diagram for TXG1020.....	23
• Added Table 8-1	27

DATE	REVISION	NOTES
June 2025	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTXG1020DR	Active	Preproduction	SOIC (D) 8	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTXG1021DR	Active	Preproduction	SOIC (D) 8	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	
TXG1020DDFR	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1020
TXG1020DR	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TG1020
TXG1021DDFR	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1021
TXG1021DR	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TG1021

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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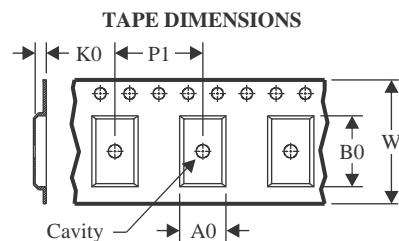
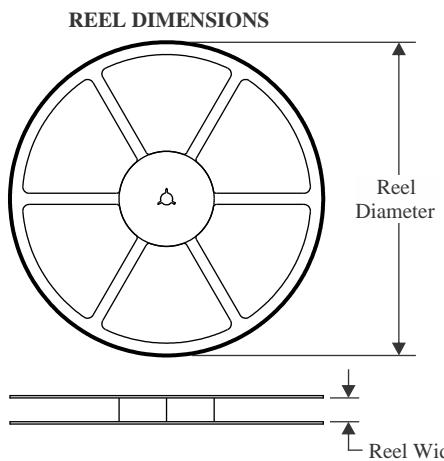
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TXG1020, TXG1021 :

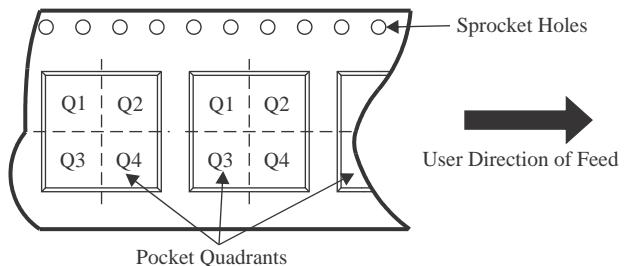
- Automotive : [TXG1020-Q1](#), [TXG1021-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

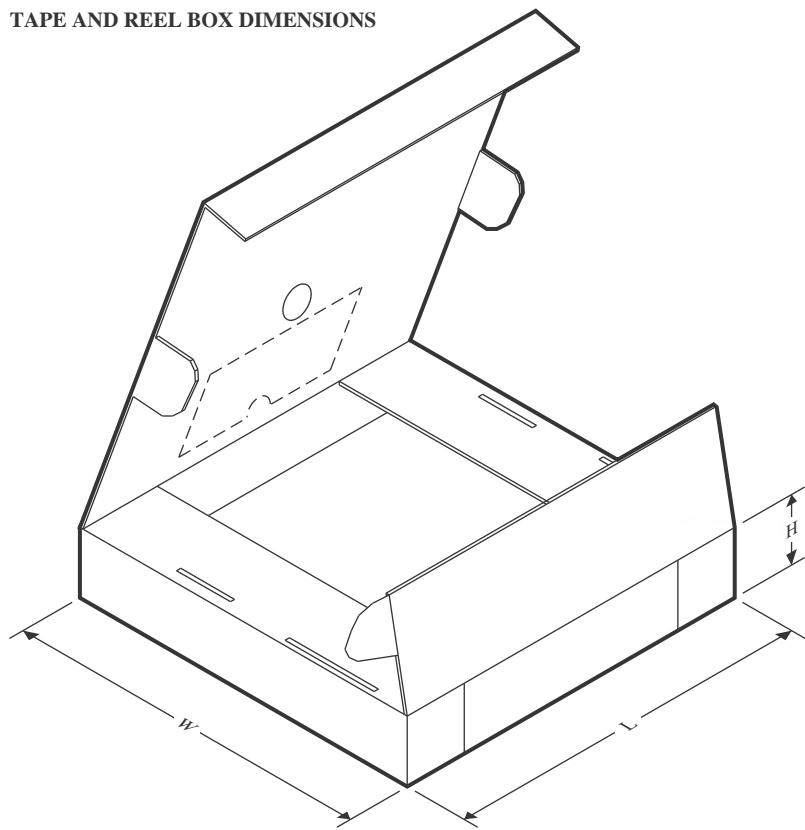
TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXG1020DR	SOIC	D	8	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TXG1021DDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TXG1021DR	SOIC	D	8	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXG1020DR	SOIC	D	8	3000	340.5	336.1	32.0
TXG1021DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TXG1021DR	SOIC	D	8	3000	340.5	336.1	32.0

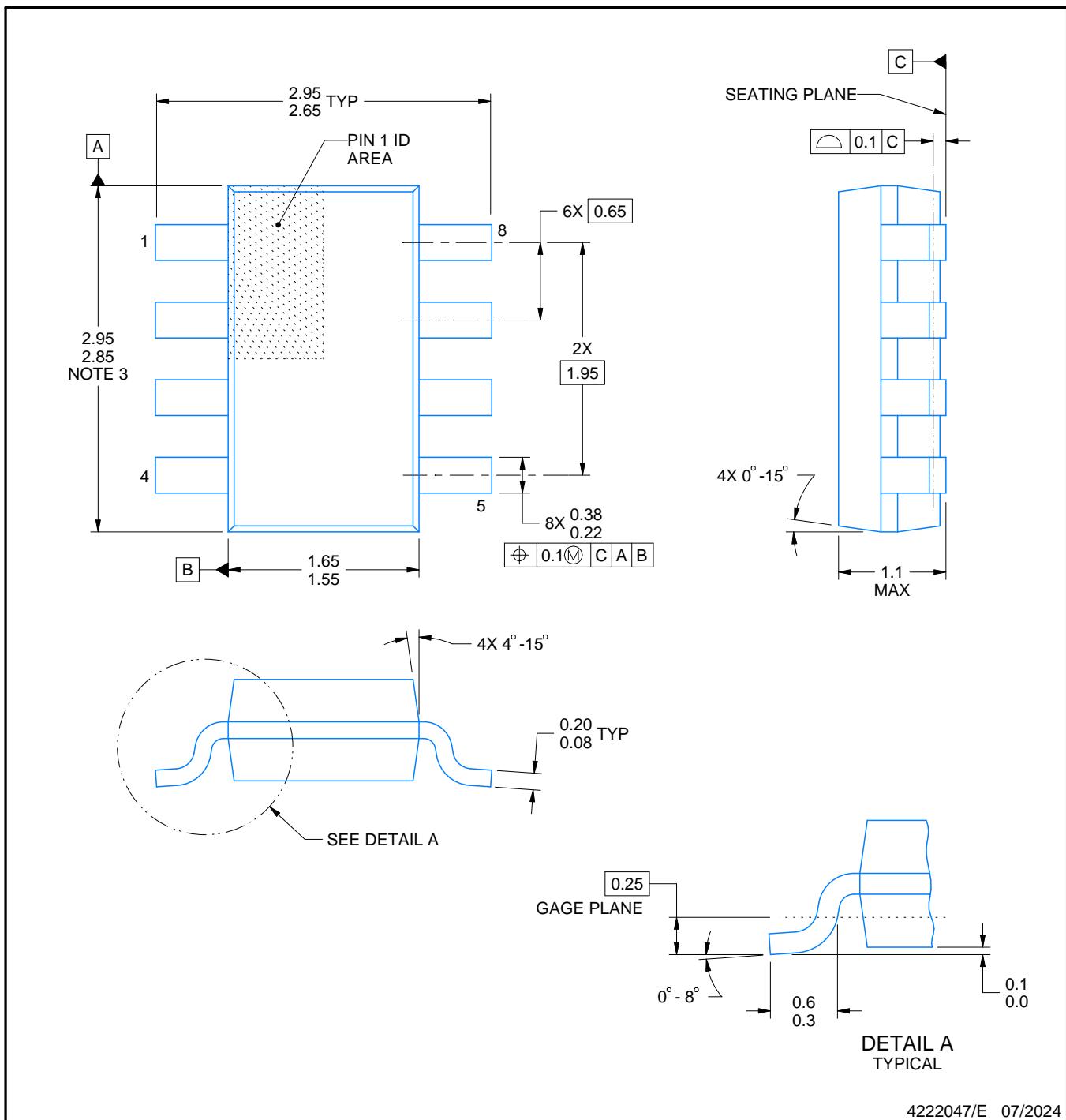
PACKAGE OUTLINE

DDF0008A



SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



4222047/E 07/2024

NOTES:

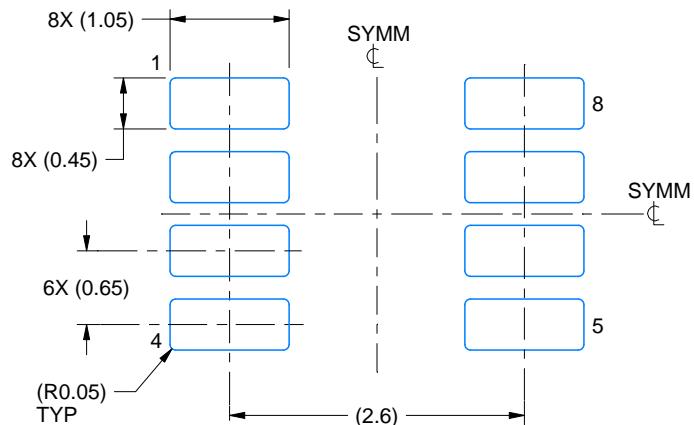
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

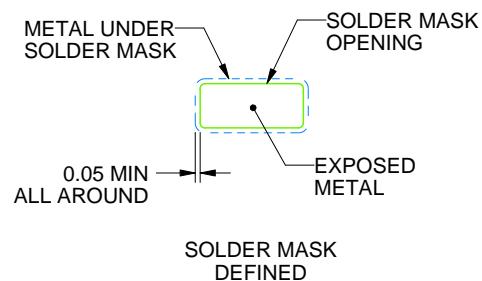
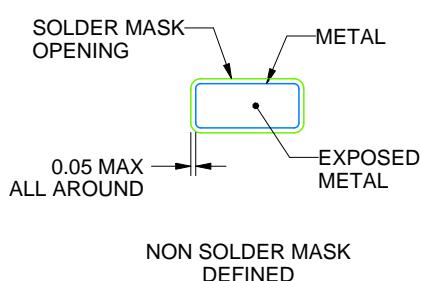
DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

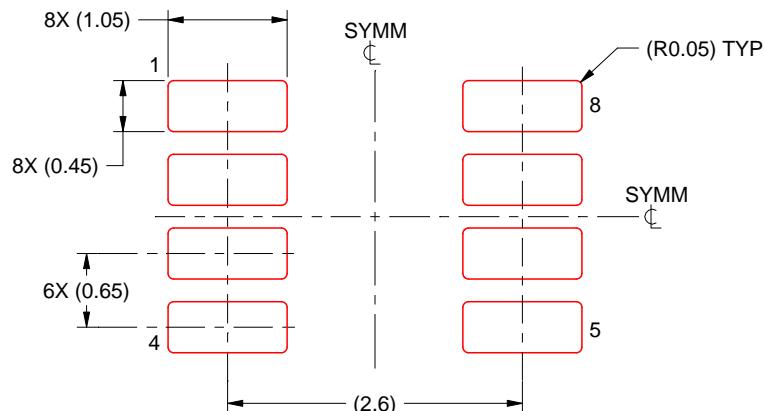
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

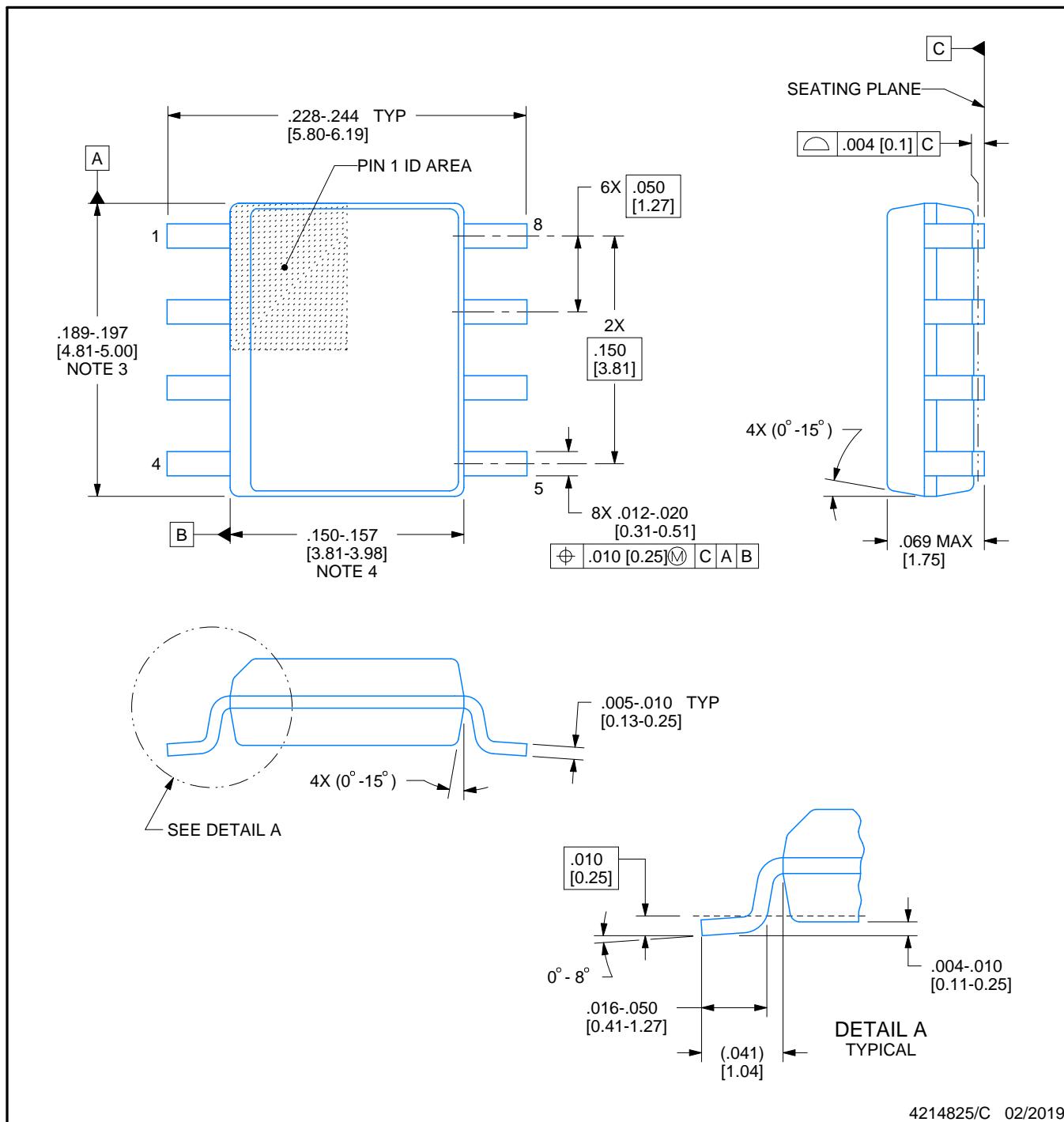


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

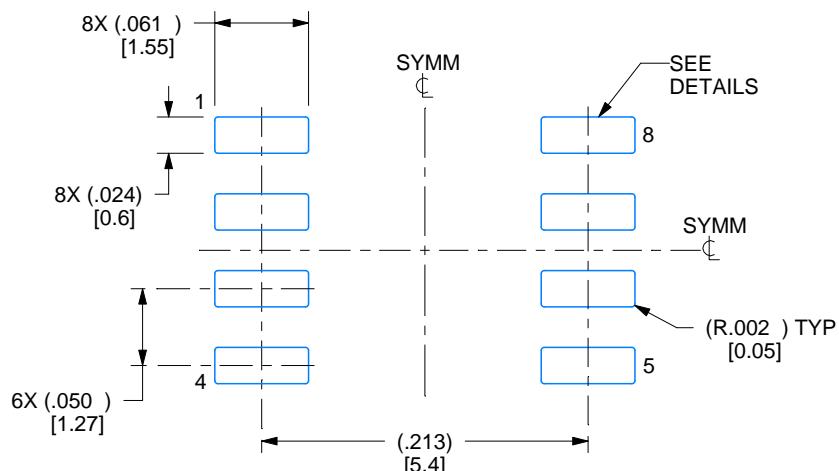
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

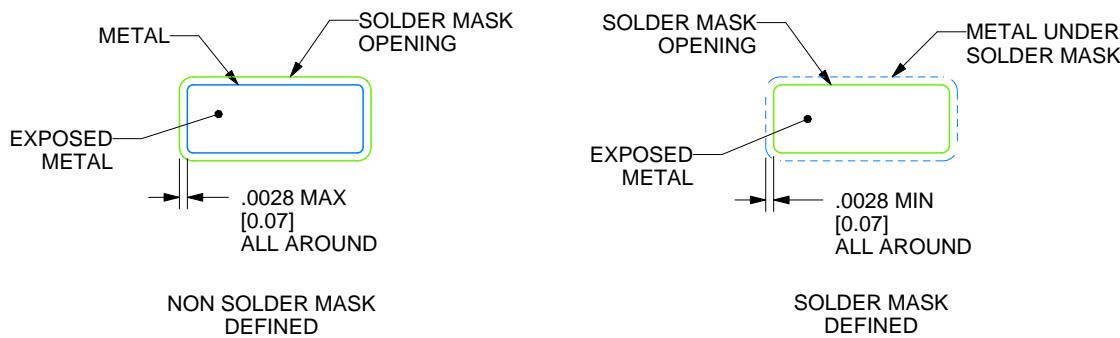
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

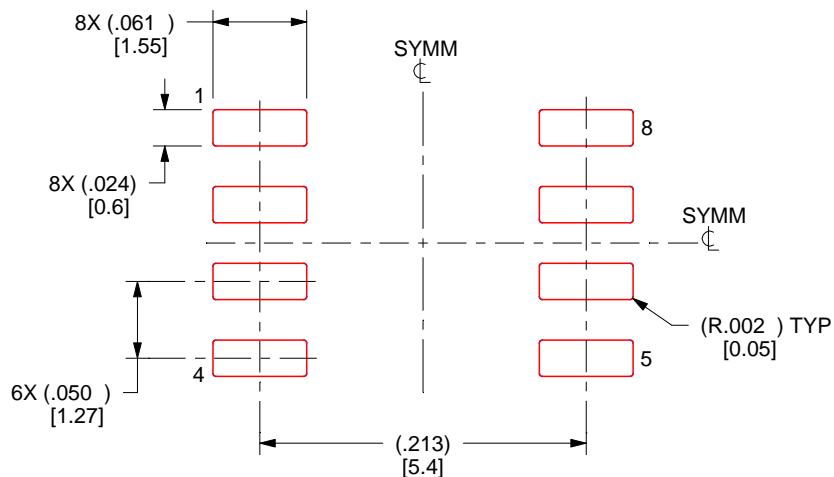
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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