TUSB564-Q1 Automotive USB Type-C® DP Alt Mode 8.1Gbps Sink-Side Linear Redriver Crosspoint Switch

1 Features

- USB Type-C® crosspoint switch supporting
  - USB 3.25Gbps + 2 DP 1.4 lanes
  - 4 DP 1.4 lanes
- USB 3.2 up to 5Gbps
- DisplayPort™ 1.4 up to 8.1Gbps (HBR3)
- VESA® DisplayPort™ alt mode UFP_D redriving crosspoint switch supporting C, D, and E pin assignments
- Ultra-low-power architecture
- Linear redriver with up to 11.6dB equalization
- Transparent to DisplayPort™ link training
- Configuration through GPIO or I^2C
- Hot-plug capable
- Automotive Grade 2 temperature range: –40°C to 105°C
- Package: 5mm × 7mm, 0.5mm pitch VQFN

2 Applications

- Automotive infotainment and cluster
- Rear seat entertainment
- Automotive head units

3 Description

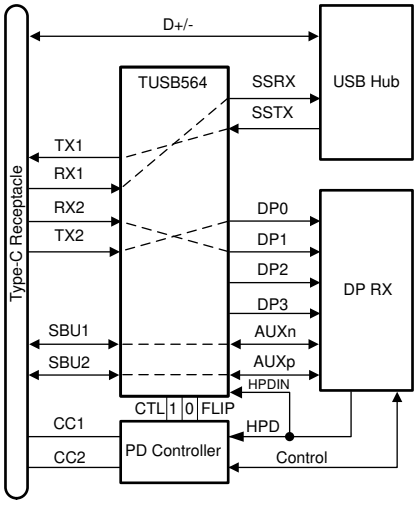
The TUSB564-Q1 is a VESA® DisplayPort™ Alt Mode over USB-C® redriving switch that supports USB 3.2 data rates up to 5Gbps and DisplayPort 1.4 up to 8.1Gbps for upstream facing port (Sink). The device is used for UFP_D pin assignments C, D, and E from the VESA® DisplayPort™ Alt Mode over USB Type-C® Standard.

The TUSB564-Q1 provides several levels of receive linear equalization to compensate for inter symbol interference (ISI) due to cable and board trace loss. The TUSB564-Q1 operates on a single 3.3V supply and comes in an automotive grade 2 temperature range.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TUSB564-Q1	RGF (VQFN, 40)	7mm × 5mm

(1) For all available packages, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematics

Table of Contents

4 Pin Configuration and Functions

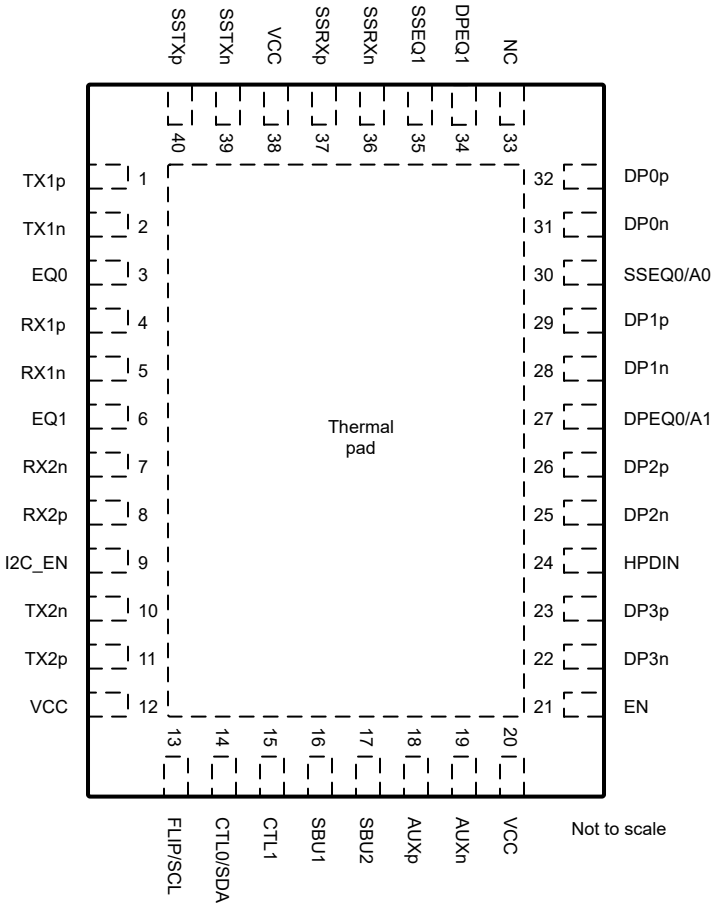


Figure 4-1. RGF Package, 40-Pin (VQFN) (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
DP0p	32	Diff O	DP differential positive output for DisplayPort Lane 0.
DP0n	31	Diff O	DP differential negative output for DisplayPort Lane 0.
DP1p	29	Diff O	DP differential positive output for DisplayPort Lane 1.
DP1n	28	Diff O	DP differential negative output for DisplayPort Lane 1.
DP2p	26	Diff O	DP differential positive output for DisplayPort Lane 2.
DP2n	25	Diff O	DP differential negative output for DisplayPort Lane 2.
DP3p	23	Diff O	DP differential positive output for DisplayPort Lane 3.
DP3n	22	Diff O	DP differential negative output for DisplayPort Lane 3.
TX1n	2	Diff I/O	Differential negative input for DisplayPort or differential negative output for USB3.2 upstream facing port.
TX1p	1	Diff I/O	Differential positive input for DisplayPort or differential positive output for USB3.2 upstream facing port.
RX1n	5	Diff I	Differential negative input for DisplayPort or USB3 upstream facing port.
RX1p	4	Diff I	Differential positive input for DisplayPort or USB3 upstream facing port.
RX2p	8	Diff I	Differential positive input for DisplayPort or USB3 upstream facing port.
RX2n	7	Diff I	Differential negative input for DisplayPort or USB3 upstream facing port.

Table 4-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
TX2p	11	Diff I/O	Differential positive input for DisplayPort or differential positive output for USB3 upstream Facing port.
TX2n	10	Diff I/O	Differential negative input for DisplayPort or differential negative output for USB3 upstream Facing port.
SSTXp	40	Diff I	Differential positive input for USB3 downstream facing port.
SSTXn	39	Diff I	Differential negative input for USB3 downstream facing port.
SSRXp	37	Diff O	Differential positive output for USB3 downstream facing port.
SSRXn	36	Diff O	Differential negative output for USB3 downstream facing port.
EQ1	6	4 Level I	This pin along with EQ0 sets the USB receiver equalizer gain for upstream facing RX1 and RX2 when USB used. Up to 11dB of EQ available.
EQ0	3	4 Level I	This pin along with EQ1 sets the USB receiver equalizer gain for upstream facing RX1 and RX2 when USB used. Up to 11dB of EQ available.
EN	21	2 Level I (PD)	Device Enable. For normal operation pull up this pin to 3.3V through a 10k to 50kΩ resistor.
HPDIN	24	2 Level I	Hot Plug Detect. This pin is an input for Hot Plug Detect received from DisplayPort sink. When HPDIN is Low for greater than 2ms, all DisplayPort lanes are disabled while the AUX to SBU switch remains closed.
I2C_EN	9	4 Level I	I^2C Programming Mode or GPIO Programming Select. I^2C is only disabled when this pin is "0". 0 = GPIO mode (I^2C disabled) R = TI Test Mode (I^2C enabled at 3.3V) F = I^2C enabled at 1.8 V 1 = I^2C enabled at 3.3V.
SBU1	16	I/O, CMOS	SBU1. DC couple this pin to the SBU1 pin on the Type-C receptacle. A 2MΩ resistor to GND is also recommended.
SBU2	17	I/O, CMOS	SBU2. DC couple this pin to the SBU2 pin on the Type-C receptacle. A 2MΩ resistor to GND is also recommended.
AUXp	18	I/O, CMOS	AUXp. DisplayPort AUX positive I/O connected to the DisplayPort sink through a AC-coupling capacitor. In addition to AC-coupling capacitor, this pin also requires a 1M resistor to DP_PWR (3.3V). This pin along with AUXN is used by the TUSB564-Q1 for AUX snooping and is routed to SBU1/2 based on the orientation of the Type-C.
AUXn	19	I/O, CMOS	AUXn. DisplayPort AUX negative I/O connected to the DisplayPort sink through a AC-coupling capacitor. In addition to AC-coupling capacitor, this pin also requires a 1M resistor to GND. This pin along with AUXP is used by the TUSB564-Q1 for AUX snooping and is routed to SBU1/2 based on the orientation of the Type-C.
DPEQ1	34	4 Level I	DisplayPort Receiver EQ. The DPEQ1 and DPEQ0 pins select the DisplayPort receiver equalization gain.
DPEQ0/A1	27	4 Level I	DisplayPort Receiver EQ. The DPEQ0 and DPEQ1 pins select the DisplayPort receiver equalization gain. When I2C_EN ≠ "0", the DPEQ0 pin also sets the TUSB564-Q1 I^2C address.
SSEQ1	35	4 Level I	The SSEQ1 and SSEQ0 pins set the USB receiver equalizer gain for downstream facing SSTXP/N.
SSEQ0/A0	30	4 Level I	The SSEQ0 and SSEQ1 pins set the USB receiver equalizer gain for downstream facing SSTXP/N. When I2C_EN ≠ "0", the SSEQ0 pin also sets the TUSB564-Q1 I^2C address. If I2C_EN = "F", then the SSEQ0 pin must be set to "F" or "0".
FLIP/SCL	13	2 Level I (Failsafe) (PD)	When I2C_EN = "0" this pin is Flip control, otherwise this pin is I^2C clock. When used for the I^2C clock, pull up to the VCC I^2C supply on the I^2C controller through an external resistor.
CTL0/SDA	14	2 Level I (Failsafe) (PD)	When I2C_EN = "0" this pin is USB3 switch control, otherwise this pin is I^2C data. When used for I^2C data, pull up to the VCC I^2C supply on the I^2C controller through an external resistor.

Table 4-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
CTL1	15	2 Level I (Failsafe) (PD)	DP Alt mode Switch Control Pin. When I2C_EN = "0", this pin can enable or disable DisplayPort functionality. Otherwise, when I2C_EN ≠ "0", DisplayPort functionality is enabled and disabled through I^2C registers. L = DisplayPort Disabled. H = DisplayPort Enabled.
VCC	12	P	3.3V Power Supply
VCC	20	P	3.3V Power Supply
VCC	38	P	3.3V Power Supply
NC	33	NC	No connect pin. Leave open.
GND	Thermal Pad	G	Ground

(1) I = input, O = output, Diff = differential, P = power, NC = no connection, G = ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature and voltage range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.3	4	V
V_{IN_DIFF}	Differential voltage at differential inputs		±2.5	V
V_{IN_SE}	Input voltage at differential Inputs	–0.5	4	V
V_{IN_CMOS}	Input voltage at CMOS inputs	–0.3	4	V
T_J	Junction temperature		125	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1), all pins	±4000	V
		Charged device model (CDM), per AEC Q100-011, all pins	±1500	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature and voltage range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{CC_RAMP}	Power supply ramp	0.1		100	ms
V_{I2C}	Supply that external resistors on SDA and SCL are pulled up too	1.7		3.6	V
V_{PSN}	Power supply noise on VCC			100	mV
T_A	Ambient temperature	–40		105	°C
T_{PCB}	PCB temperature (1mm away from the device)	–40		112	°C

5.4 Thermal Information

THERMAL METRIC(1)		Device RGF (VQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	10.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power						
$P_{CC-ACTIVE-USB}$	Average active power in USB-only mode while in U0	CTL1 = L; CTL0 = H; Link in U0 at 5Gbps;		340		mW
$P_{CC-ACTIVE-USB-DP}$	Average active power in USB + 2 lane DP mode	CTL1 = H; CTL0 = H; USB in U0 at 5Gbps; DP at 8.1Gbps;		670		mW
$P_{CC-ACTIVE-DP}$	Average active power in 4 lane DP mode	CTL1 = H; CTL0 = L; Four DP lanes at 8.1Gbps		640		mW
$P_{CC-NC-USB}$	Average power in USB mode while in disconnect state.	CTL1 = L; CTL0 = H; No USB device detected;		2.5		mW
$P_{CC-U2U3}$	Average power in USB mode while in U2/U3 state	CTL1 = L; CTL0 = H; Link in U2 or U3;		2.5		mW
$P_{CC-SHUTDOWN}$	Average power in shutdown mode.	CTL1 = L; CTL0 = L; I2C_EN = "0";		0.7		mW
4-State CMOS Inputs(EQ[1:0], SSEQ[1:0], DPEQ[1:0], I2C_EN)						
I_{IH}	High-level input current	V_{CC} = 3.6V; V_{IN} = 3.6V	20		80	µA
I_{IL}	Low-level input current	V_{CC} = 3.6V; V_{IN} = 0V	–160		–40	µA
4-Level V_{TH}	Threshold 0 / R	V_{CC} = 3.3V		0.59		V
	Threshold R/ Float	V_{CC} = 3.3V		1.65		V
	Threshold Float / 1	V_{CC} = 3.3V		2.7		V
R_{PU}	Internal pullup resistance			45		kΩ
R_{PD}	Internal pulldown resistance			95		kΩ
2-State CMOS Input (EN, FLIP, CTL0, CTL1, HPDIN) CTL1, CTL0 and FLIP are Failsafe						
V_{IH}	High-level input voltage		2.2		3.6	V
V_{IL}	Low-level input voltage		0		0.8	V
R_{PD}	Internal pull-down resistance for FLIP, CTL0, and EN.			500		kΩ
$R_{PD-CTL1}$	Internal pull-down resistance for CTL1			395		kΩ
I_{IH-EN}	High-level input current for EN pin	V_{IN} = 3.6V	4		12	µA
I_{IL-EN}	Low-level input current for EN pin	V_{IN} = GND, V_{CC} = 3.6V	–1		1	µA
$I_{IH-FLIP}$	High-level input current for FLIP pin	V_{IN} = 3.6V	4		12	µA
$I_{IL-FLIP}$	Low-level input current for FLIP pin	V_{IN} = GND, V_{CC} = 3.6V	–1		1	µA
$I_{IH-CTL0}$	High-level input current for CTL0 pin	V_{IN} = 3.6V	4		12	µA
$I_{IL-CTL0}$	Low-level input current for CTL0 pin	V_{IN} = GND, V_{CC} = 3.6V	–1		1	µA
$I_{IH-CTL1}$	High-level input current for CTL1 pin	V_{IN} = 3.6V	4		12	µA
$I_{IL-CTL1}$	Low-level input current for CTL1 pin	V_{IN} = GND, V_{CC} = 3.6V	–1		1	µA
$I_{IH-HPDIN}$	High-level input current for HPD pin	V_{IN} = 3.6V	0.5		5	µA
$I_{IL-HPDIN}$	Low-level input current for HPD pin	V_{IN} = GND, V_{CC} = 3.6V	–1		1	µA
I2C Control Pins SCL, SDA						
V_{IH}	High-level input voltage	I2C_EN = "1" or "R" (3.3V I2C levels)	2.2		3.6	V
V_{IL}	Low-level input voltage	I2C_EN = "1" or "R" (3.3V I2C levels)	0		0.8	V
V_{IH}	High-level input voltage	I2C_EN = "F" (1.8V I2C levels)	1.2		3.6	V
V_{IL}	Low-level input voltage	I2C_EN = "F" (1.8V I2C levels)	0		0.4	V
V_{OL}	Low-level output voltage	I2C_EN ! = "0"; I_{OL} = 3mA	0		0.4	V
I_{OL}	Low-level output current	I2C_EN ! = "0"; V_{OL} = 0.4V	20			mA

5.5 Electrical Characteristics (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{i_I2C}	Input current on SDA pin	0.1 × V_{I2C} < Input voltage < 3.3V	–10		10	µA
C_{i_I2C}	Input capacitance				10	pF
USB Differential Receiver (RX1P/N, RX2P/N, SSTXP/N)						
$V_{RX-DIFF-PP}$	Input differential peak-peak voltage swing linear dynamic range	AC-coupled differential peak-to-peak signal measured post CTLE through a reference channel		1200		mVppd
$V_{RX-DC-CM}$	Common-mode voltage bias in the receiver (DC)			0		V
$R_{RX-DIFF-DC}$	Differential input impedance (DC)	Present after a USB3 device is detected on TXP/TXN	72		120	Ω
$R_{RX-CM-DC}$	Receiver DC common mode impedance	Present after a USB3 device is detected on TXP/TXN	18		30	Ω
$Z_{RX-HIGH-IMP-DC-POS}$	Common-mode input impedance with termination disabled (DC)	Present when no USB3 device is detected on TXP/TXN. Measured over the range of 0V to 500mV with respect to GND.	25			kΩ
$V_{SIGNAL-DET-DIFF-PP}$	Input differential peak-to-peak signal detect assert level	At 5Gbps, No loss and bit rate PRBS7 pattern		80		mVppd
$V_{RX-IDLE-DET-DIFF-PP}$	Input differential peak-to-peak signal detect de-assert level	At 5Gbps, No loss and bit rate PRBS7 pattern		60		mVppd
$V_{RX-LFPS-DET-DIFF-PP}$	Low-frequency periodic signaling (LFPS) detect threshold	25℃ ≤ T_A ≤ 105℃; Below the minimum is squelched. Tested at 25MHz and 300mVppd VIN.	100		300	mVppd
$RL_{RX-DIFF}$	Differential return loss	50MHz to 1.25GHz at 90Ω; Lowest EQ setting; FLIP = L;		–23		dB
$RL_{RX-DIFF}$	Differential return loss	2.5GHz at 90Ω; Lowest EQ setting; FLIP = L;		–22		dB
RL_{RX-CM}	Common-mode return loss	50MHz to 2.5GHz at 90Ω; Lowest EQ setting; FLIP = L;		–13		dB
EQ_{SS}	Receiver equalization for RX1/2 receivers at maximum setting	At 2.5GHz; FLIP = L;		11.6		dB
EQ_{SS}	Receiver equalization for SSTX receiver at maximum setting	At 2.5GHz; FLIP = L;		10		dB
USB Differential Transmitter (TX1P/N, TX2P/N, SSRXP/N)						
$V_{TX-DIFF-PP}$	Transmitter dynamic differential voltage swing range.			1300		mVppd
$V_{TX-RCV-DETECT}$	Amount of voltage change allowed during Receiver Detection	At 3.3V			600	mV
$V_{TX-CM-IDLE-DELTA}$	Transmitter idle common-mode voltage change while in U2/U3 and not actively transmitting LFPS	Measured at the connector side of the AC-coupling capacitor with 50Ω load	–600		600	mV
$V_{TX-DC-CM}$	Common-mode voltage bias in the transmitter (DC)	In U0;	1.5		2.1	V
$V_{TX-CM-AC-PP-ACTIVE}$	TX AC common-mode voltage active	At 3.3V; Maximum mismatch from Txp+Txn for both time and amplitude			100	mVpp
$V_{TX-IDLE-DIFF-AC-PP}$	AC electrical idle differential peak-to-peak output voltage	At package pins after high-pass filter (HPF) to remove DC component; HPF = 1/LPF; No AC or DC signals are applied at RX terminals;	0		10	mV

5.5 Electrical Characteristics (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{TX-IDLE-DIFF-DC}$	DC electrical idle differential output voltage	At package pins after low-pass filter (LPF) to remove AC component; LPF = 1/HPF; No AC or DC signals are applied at RX terminals;	0		10	mV
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute DC common-mode voltage between U1 and U0	At package pin			200	mV
$R_{TX-DIFF}$	Differential impedance of the driver		75		120	Ω
R_{TX-CM}	Common-mode impedance of the driver	Measured with respect to AC ground over 0V to 500mV	18		30	Ω
$C_{AC-COUPLING}$	External AC-coupling capacitor		75		265	nF
$I_{TX-SHORT}$	TX short-circuit current	TX+/- shorted to GND			67	mA
$RL_{TX-DIFF}$	Differential return loss (SDD22)	50MHz to 1.25GHz at 90Ω; Lowest EQ setting; FLIP = L;		–25		dB
$RL_{TX-DIFF-2.5G}$	Differential return loss (SDD22)	2.5GHz at 90Ω; Lowest EQ setting; FLIP = L;		–12		dB
RL_{TX-CM}	Common-mode return loss (SCC22)	50MHz to 2.5GHz at 90Ω; Lowest EQ setting; FLIP = L;		–14		dB
AC Electrical Characteristics						
Crosstalk	Differential crosstalk between TX and RX signal pairs	At 2.5GHz; FLIP = L;		–45		dB
G_{LF}	Low-frequency voltage gain.	At 100MHz, 600mVpp V_{ID}	–0.25	0.6	1.5	dB
$G_{LF\_LFPS\_TX1/2}$	Low-frequency voltage gain for SSTX –> TX1/TX2 path	At 10MHz to 50MHz sine wave; 1.0Vpp V_{ID}; EQ = 0; FLIP = 0 and 1;	–0.5	0.8	1.6	dB
$CP_{1\ dB-LF}$	Low-frequency –1dB compression point	At 100MHz, 200mVpp < V_{ID} < 2000mVpp		1000		mVpp
$CP_{1\ dB-HF}$	High-frequency –1dB compression point	At 2.5GHz, 200mVpp < V_{ID} < 2000mVpp		1000		mVpp
D_{J_5G}	TX output deterministic jitter	200mVpp < V_{ID} < 2000mVpp, PRBS7, 5Gbps, 10dB pre-channel and 1dB post-channel, Optimal EQ setting		0.025		UIpp
$D_{J\_8.1G}$	TX output deterministic jitter	200mVpp < V_{ID} < 2000mVpp, PRBS7, 8.1Gbps, 10dB pre-channel and 1dB post-channel, Optimal EQ setting		0.03		UIpp
DisplayPort Receiver (TX1P/N, TX2P/N, RX1P/N, RX2P/N)						
V_{ID_PP}	Peak-to-peak input differential dynamic voltage range			1400		mVppd
V_{IC}	Input common-mode voltage			0		V
C_{AC}	External AC-coupling capacitor		75		265	nF
EQ_{DP}	Receiver equalizer at maximum setting	At 4.05GHz;		13.7		dB
d_R	Data rate	HBR3			8.1	Gbps
R_{tx}	Input termination resistance		80	100	120	Ω
DisplayPort Transmitter (DP[3:0]P/N)						
$V_{TX-DIFFPP}$	VOD dynamic range			1300		mVppd
$I_{TX-SHORT}$	TX short-circuit current	TX+/- shorted to GND			67	mA
$V_{DPTX-DC-CM}$	Common-mode voltage bias in the transmitter (DC)		1.5		2.2	V
R_{DPTX}	Differential impedance of the driver		75		120	Ω
AUXP/N and SBU1/2						

5.5 Electrical Characteristics (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{ON}	Output ON resistance	V_{CC} = 3.3V; V_{IN} = 0V to 0.4V for AUXP; V_{IN} = 2.7V to 3.6V for AUXN		5	10	Ω
$R_{ON-MISMATCH}$	ΔON resistance mismatch within pair	V_{CC} = 3.3V; V_{IN} = 0V to 0.4V for AUXP; V_{IN}= 2.7V to 3.6V for AUXN			1.5	Ω
R_{ON_FLAT}	ON resistance flatness (RONmax–RON min) measured at identical VCC and temperature	V_{CC} = 3.3V; V_{IN} = 0V to 0.4V for AUXP; V_{IN} = 2.7V to 3.6V for AUXN			2	Ω
$V_{AUXP\_DC\_CM}$	AUX channel DC common-mode voltage for AUXP and SBU2.	V_{CC} = 3.3V	0		0.4	V
$V_{AUXN\_DC\_CM}$	AUX channel DC common-mode voltage for AUXN and SBU1	V_{CC} = 3.3V	2.7		3.6	V
C_{AUX_ON}	ON-state capacitance	V_{CC} = 3.3V; CTL1 = 1; V_{IN} = 0V or 3.3V		4	7	pF
C_{AUX_OFF}	OFF-state capacitance	V_{CC} = 3.3V; CTL1 = 0; V_{IN} = 0V or 3.3V		3	6	pF

5.6 Timing Requirements

		MIN	NOM	MAX	UNIT
USB3					
$t_{IDLEEntry}$,	Delay from U0 to electrical idle		10		ns
$t_{IDLEExit\_U1}$	U1 exit time: break in electrical idle to the transmission of LFPS		6		ns
$t_{IDLEExit\_U2U3}$	U2/U3 exit time: break in electrical idle to transmission of LFPS		10		µs
t_{RXDET_INTVL}	RX detect interval while in disconnect			12	ms
$t_{IDLEExit\_DISC}$	Disconnect exit time		10		µs
t_{Exit_SHTDN}	Shutdown exit time (CTL0 = V_{CC}/2 to U2/U3)		1		ms
t_{DIFF_DLY}	Differential propagation delay (20% to 80% of differential voltage measured 1.7 inch from the output pin)			300	ps
$t_{PWRUPACTIVE}$	Time when Vcc reaches 70% to device active			1	ms
t_R, t_F	Output rise/fall time		40		ps
t_{RF-MM}	Output rise/fall time mismatch (20% to 80% of differential voltage measured 1.7 inch from the output pin)			5	ps

5.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUXp/n and SBU1/2						
T_{AUX_PD}	Switch propagation delay	CTL1 = H			1400	ps
$T_{AUX\_SW\_OFF}$	Switching on time	CTL1 = H to L			7500	ns
$T_{AUX\_SW\_ON}$	Switching off time	CTL1 = L to H			3000	ns
T_{AUX_INTRA}	Intra-pair output skew	CTL1 = H			400	ps
USB and DisplayPort mode transition requirement (GPIO mode)						

5.7 Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{GP\_USB\_4DP}$	Min overlap of CTL0 and CTL1 when transitioning from USB 3.1 only mode to 4-Lane DisplayPort mode or vice versa		4			µs
$T_{HPDIN\_DEBOUNCE}$	HPDIN debounce time when transitioning from H to L	Less than minimum is ignored by device	1.5		4	ms
I²C (SDA and SCL)						
f_{SCL}	I²C clock frequency				1	MHz
t_{BUF}	Bus free time between START and STOP conditions		0.5			µs
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock pulse is generated		0.26			µs
t_{LOW}	Low period of the I²C clock		0.5			µs
t_{HIGH}	High period of the I²C clock		0.26			µs
t_{SUSTA}	Setup time for a repeated START condition		0.26			µs
t_{HDDAT}	Data hold time		0.004			µs
t_{SUDAT}	Data setup time		50			ns
t_R	Rise time of both SDA and SCL signals				120	ns
t_F	Device output fall time for SDA	30pF load	0.7		5	ns
t_{SUSTO}	Setup time for STOP condition		0.26			µs
C_b	Capacitive load for each bus line				100	pF

5.8 Typical Characteristics

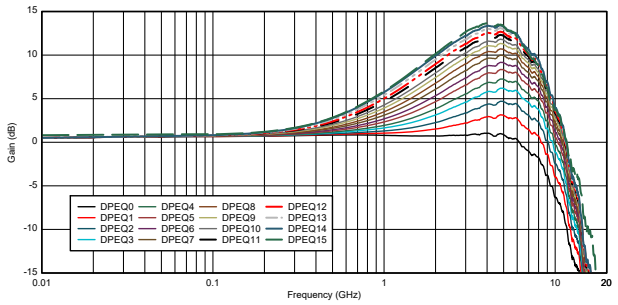


Figure 5-1. DisplayPort EQ Settings Curves at Nominal Conditions

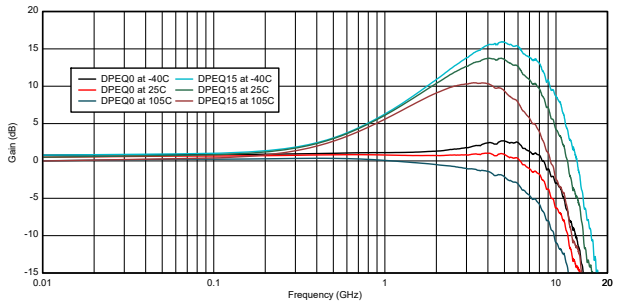


Figure 5-2. DisplayPort DPEQ0 and DPEQ15 Across Temperature

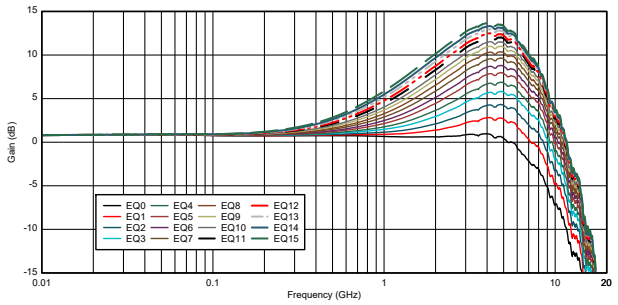


Figure 5-3. USB3 RX1 EQ Settings Curves

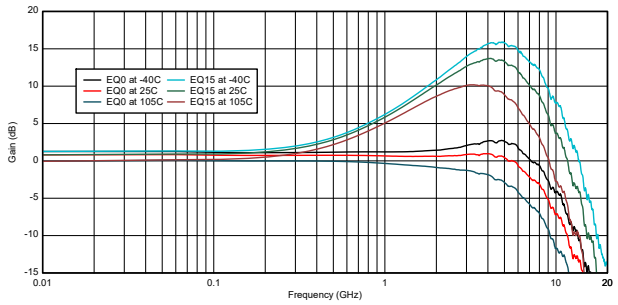


Figure 5-4. USB3 RX1 EQ0 and EQ15 Across Temperature

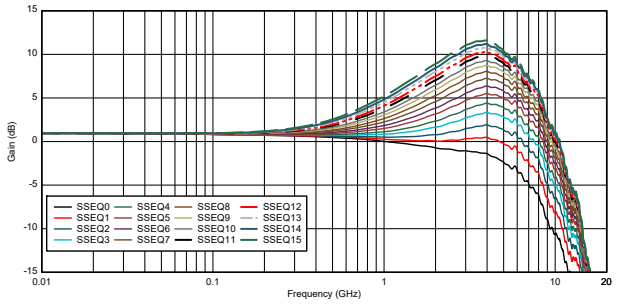


Figure 5-5. USB3 SSTX EQ Settings Curves

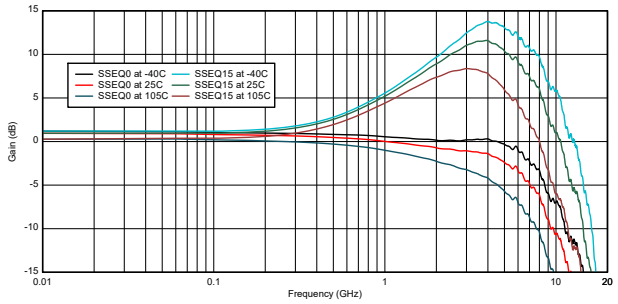


Figure 5-6. USB3 SSTX SSEQ0 and SSEQ15 Across Temperature

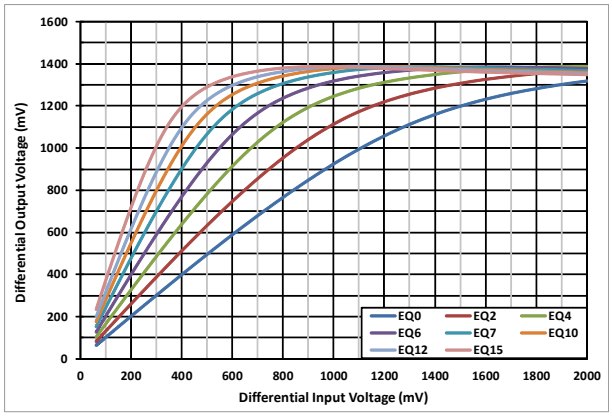


Figure 5-7. DisplayPort Linearity Curves at 4.05GHz

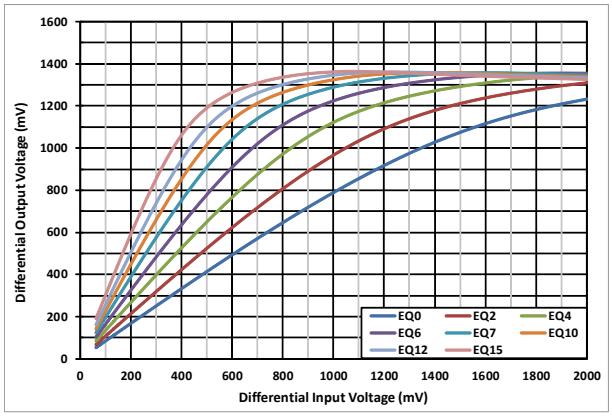


Figure 5-8. USB TX (DFP) Linearity Curves at 2.5GHz

5.8 Typical Characteristics (continued)

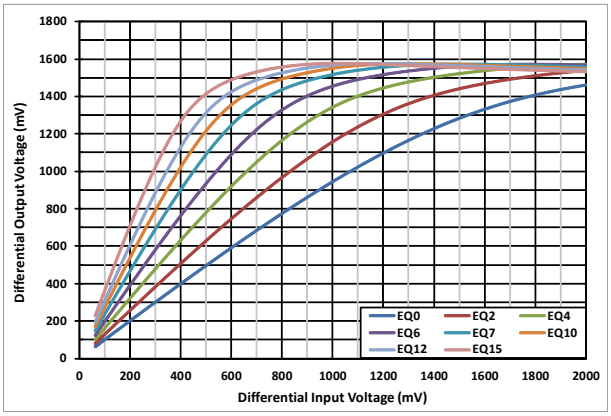


Figure 5-9. USB RX (UFP) Linearity Curves at 2.5GHz

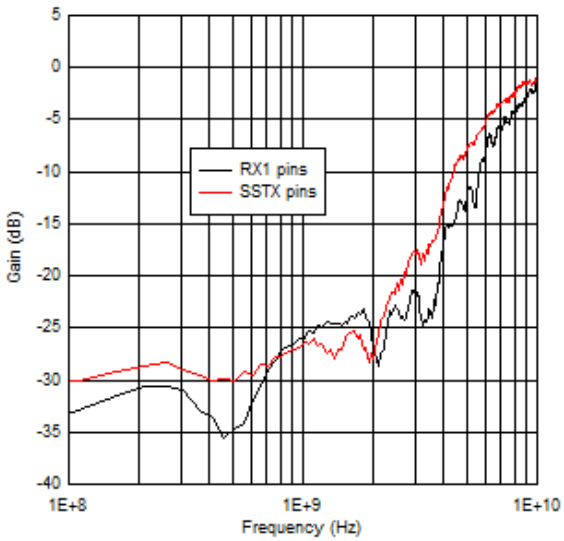


Figure 5-10. Input Return Loss Performance

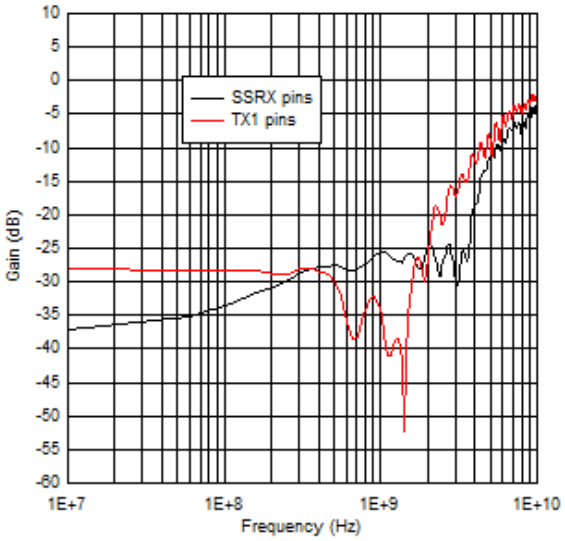


Figure 5-11. Output Return Loss Performance

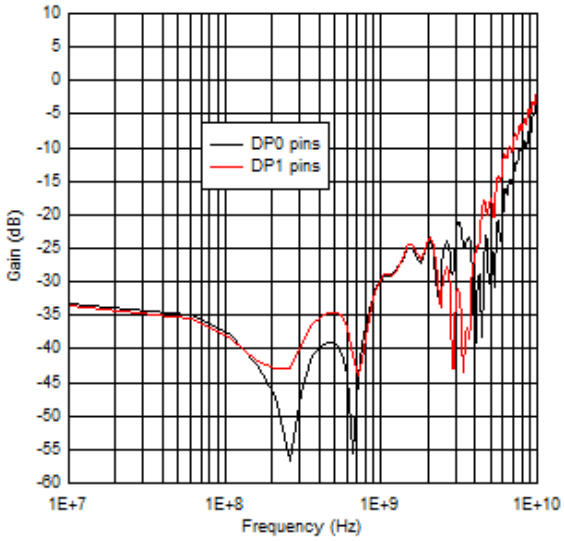


Figure 5-12. DisplayPort Output Return Loss Performance

5.8 Typical Characteristics (continued)

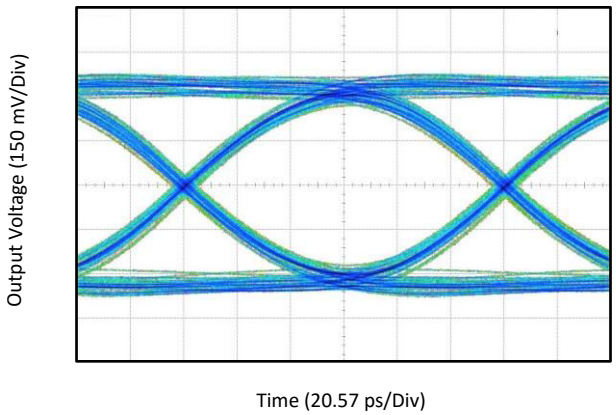


Figure 5-13. DisplayPort HBR3 Eye-Pattern Performance with 12-Inch Input PCB Trace at 8.1Gbps

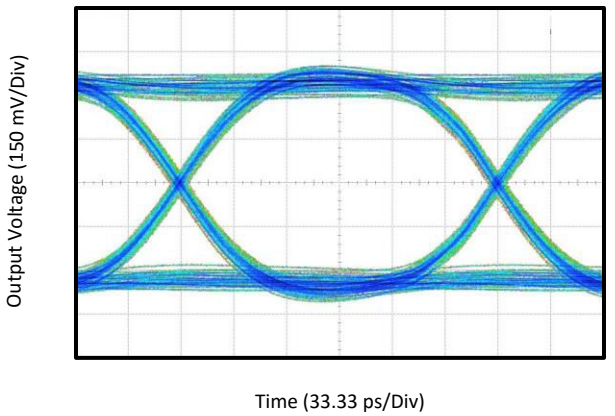


Figure 5-14. USB 3.1 Gen1 Eye-Pattern Performance with 12-Inch Input PCB Trace at 5Gbps

6 Parameter Measurement Information

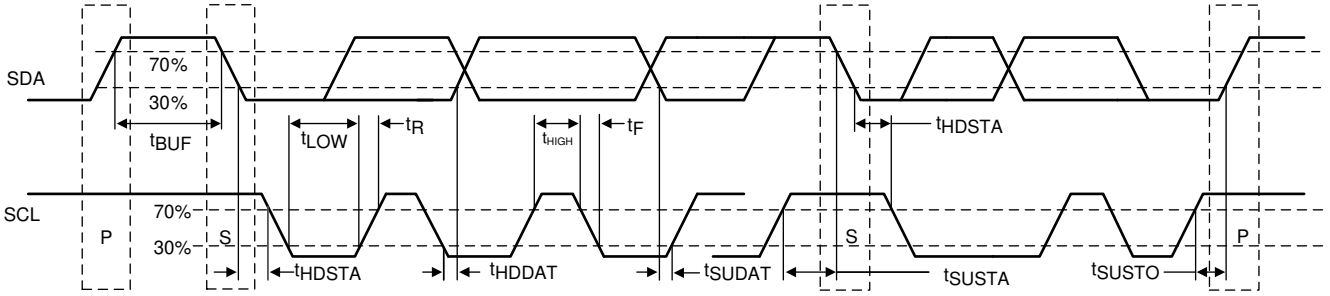


Figure 6-1. I²C Timing Diagram Definitions

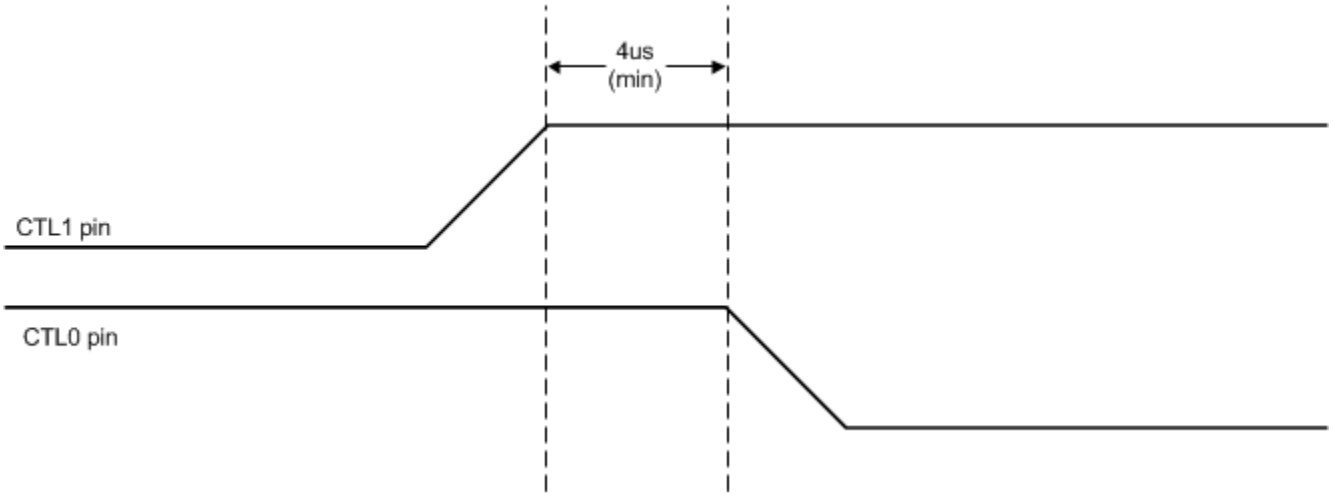


Figure 6-2. USB3.1 to 4-Lane DisplayPort in GPIO Mode

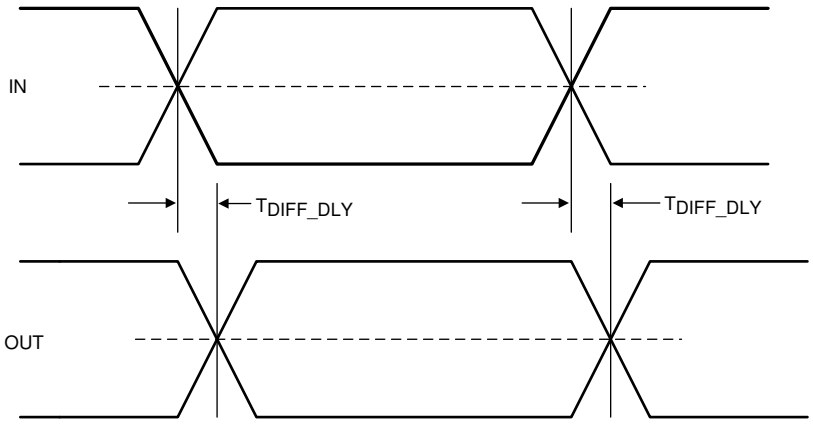


Figure 6-3. Propagation Delay

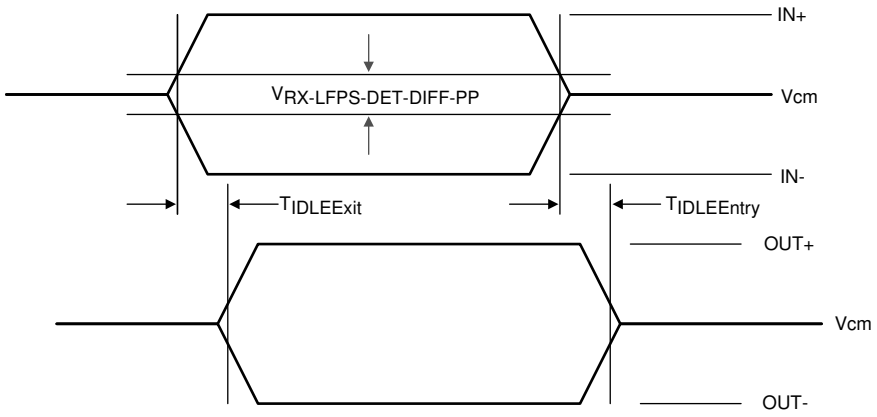


Figure 6-4. Electrical Idle Mode Exit and Entry Delay

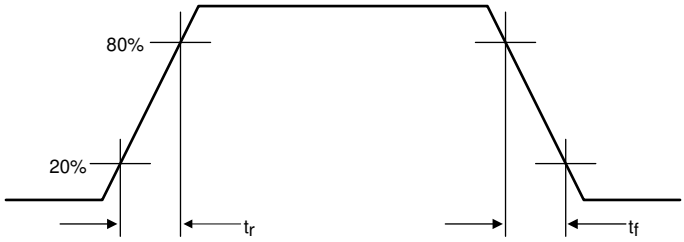


Figure 6-5. Output Rise and Fall Times

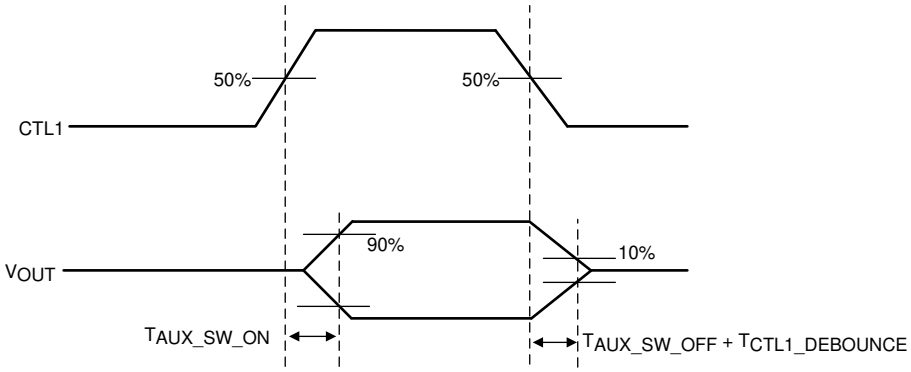


Figure 6-6. AUX and SBU Switch ON and OFF Timing Diagram

7 Detailed Description

7.1 Overview

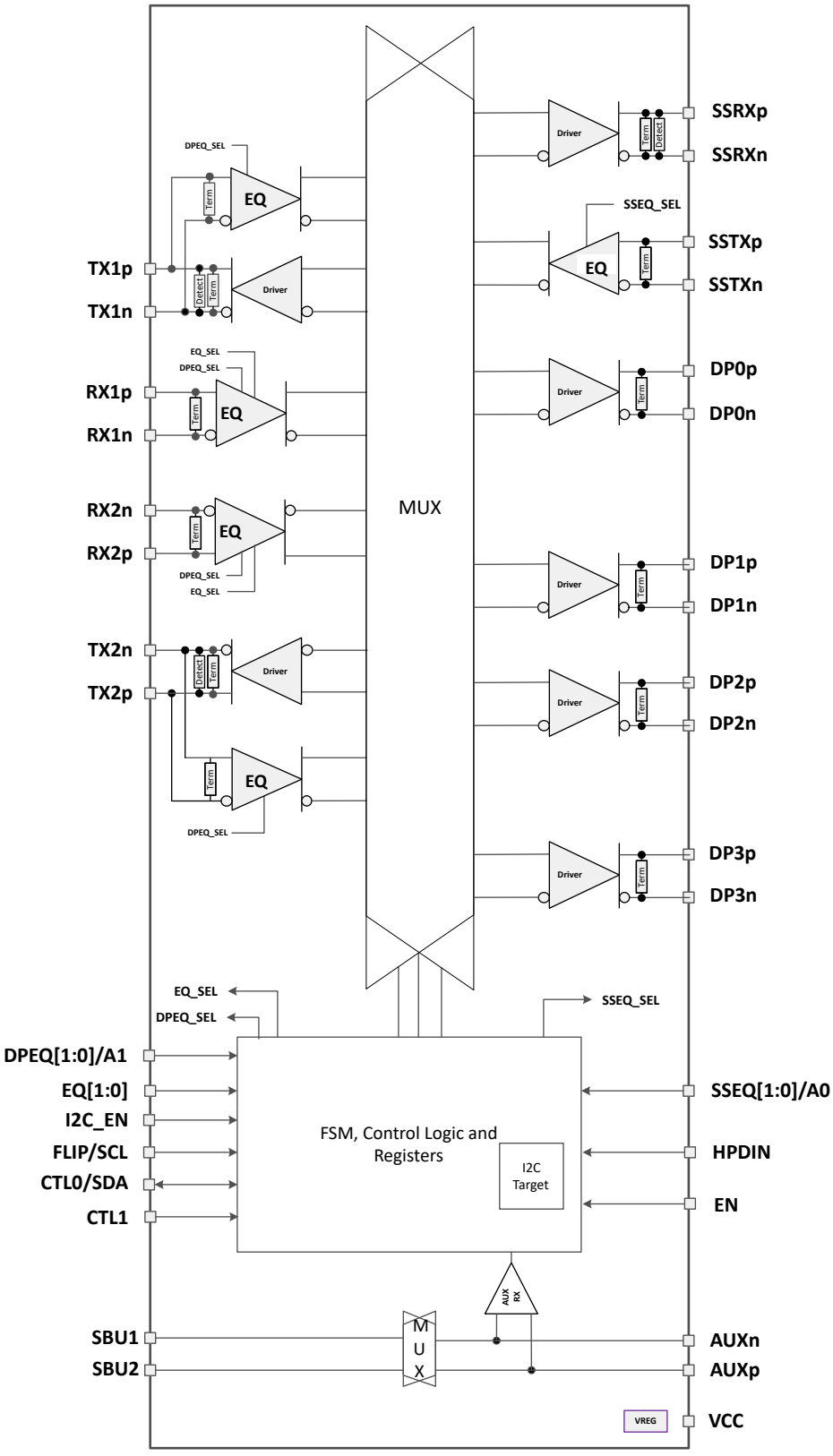
The TUSB564-Q1 is a VESA USB Type-C Alt Mode redriving switch that supports data rates up to 8.1Gbps for upstream facing port. This device uses 5th generation USB redriver technology. The device is used for UFP pin assignments C and D from the VESA DisplayPort Alt Mode on USB Type-C Standard.

The TUSB564-Q1 provides several levels of receive equalization to compensate for cable and board trace loss which if not equalized causes inter-symbol interference (ISI) when USB 3.2 or DisplayPort 1.4 signals travel across a PCB or cable. This device requires a 3.3V power supply. The device comes in an automotive grade 2 temperature range.

For a sink application, the TUSB564-Q1 enables the system to pass both transmitter compliance and receiver jitter tolerance tests for USB 3.2 up to 5Gbps and DisplayPort version 1.4 HBR3. The redriver recovers incoming data by applying equalization that compensates for channel loss, and drives out signals with a high differential voltage. Each channel has a receiver equalizer with selectable gain settings. Set the equalization based on the amount of insertion loss in the channels connected to the TUSB564-Q1. Independent equalization control for each channel can be set using EQ[1:0], SSEQ[1:0], and DPEQ[1:0] pins.

The TUSB564-Q1 advanced state machine makes the device transparent to hosts and devices. After power up, the TUSB564-Q1 periodically performs receiver detection on the TX pairs. If the TUSB564-Q1 detects a USB 3.2 receiver, the RX termination is enabled, and the TUSB564-Q1 is ready to re-drive.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 USB 3.2

The TUSB564-Q1 supports USB 3.2 datarates up to 5Gbps. The TUSB564-Q1 supports all the USB defined power states (U0, U1, U2, and U3). The TUSB564-Q1 is a linear redriver, therefore the device cannot decode USB3.2 physical layer traffic. The TUSB564-Q1 monitors the actual physical layer conditions like receiver termination, electrical idle, LFPS, and SuperSpeed signaling rate to determine the USB power state of the USB 3.2 interface.

The TUSB564-Q1 features an intelligent low-frequency periodic signaling (LFPS) detector. The LFPS detector automatically senses the low-frequency signals and disables receiver equalization functionality. When not receiving LFPS, the TUSB564-Q1 enables receiver equalization based on the EQ[1:0] and SSEQ[1:0] pins or values programmed into EQ1_SEL, EQ2_SEL, and SSEQ_SEL registers.

7.3.2 DisplayPort

The TUSB564-Q1 supports up to four DisplayPort lanes at datarates up to 8.1Gbps (HBR3). When configured in DisplayPort mode, the TUSB564-Q1 monitors the native AUX traffic as the device traverses between DisplayPort source and DisplayPort sink. For the purposes of reducing power, the TUSB564-Q1 manages the number of active DisplayPort lanes based on the content of the AUX transactions. The TUSB564-Q1 snoops native AUX writes to DPCD registers 0x00101 (LANE_COUNT_SET) and 0x00600 (SET_POWER_STATE) of the DisplayPort sink. The TUSB564-Q1 disables or enables lanes based on value written to LANE_COUNT_SET. The TUSB564-Q1 disables all lanes when SET_POWER_STATE is in the D3. Otherwise, active lanes are based on value of LANE_COUNT_SET.

DisplayPort AUX snooping is enabled by default but can be disabled by changing the AUX_SNOOP_DISABLE register. After AUX snoop is disabled, management of TUSB564-Q1 DisplayPort lanes are controlled through various configuration registers.

Note

AUX snooping feature is only supported when TUSB564-Q1 is configured for I^2C mode. When TUSB564-Q1 is configured for GPIO mode, the AUX snoop feature is disabled and all four DP lanes are enabled if HPDIN is asserted high.

When the TUSB564-Q1 AUX snoop feature is enabled, the syncs defined by the DisplayPort standard must be received for AUX snoop feature to function properly. AUX writes to the DPCD address 0x00600 and 0x00101 of the panel can result in SET_POWER_STATE and LANE_COUNT_SET fields at TUSB564-Q1 offset 0x12 to get set to the appropriate value. If these fields do not get set correctly, then incoming AUX may not be compliant. If this is the case, then it is best to disable AUX snoop by setting the AUX_SNOOP_DISABLE field at offset 0x13.

7.3.3 4-Level Inputs

The TUSB564-Q1 has (I2C_EN, EQ[1:0], DPEQ[1:0], and SSEQ[1:0]) 4-level inputs pins that are used to control the equalization gain and place TUSB564-Q1 into different modes of operation. These 4-level inputs use a resistor divider to help set the four valid levels and provide a wider range of control settings. There is an internal 35kΩ pullup and a 95kΩ pulldown. These resistors, together with the external resistor connection combine to achieve the desired voltage level.

Table 7-1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Tie 1kΩ 5% to GND
R	Tie 20kΩ 5% to GND
F	Float (leave pin open)
1	Tie 1kΩ 5% to V_{CC}

Note

All 4-level inputs are latched after the rising edge of internal reset. After t_{cfg_hd}, the internal pullup and pulldown resistors are isolated to save power.

7.3.4 Receiver Linear Equalization

The purpose of receiver equalization is to compensate for channel insertion loss and the resulting inter-symbol interference in the system before the input or after the output of the TUSB564-Q1. The receiver overcomes these losses by attenuating the low-frequency components of the signals with respect to the high-frequency components. Select the proper gain setting to match the channel insertion loss. Two 4-level input pins enable up to 16 possible equalization settings. The USB3.2 upstream path, USB3.2 downstream path, and DisplayPort each have two 4-level inputs. The TUSB564-Q1 also provides the flexibility of adjusting settings through I^2C registers.

7.4 Device Functional Modes

7.4.1 Device Configuration in GPIO Mode

The TUSB564-Q1 is in GPIO configuration when I2C_EN = "0". The TUSB564-Q1 supports the following configurations: USB only, 2 DisplayPort lanes + USB, or 4 DisplayPort lanes (no USB). The CTL1 pin controls whether DisplayPort is enabled. The combination of CTL1 and CTL0 selects between USB only, 2 lanes of DisplayPort, or 4-lanes of DisplayPort as detailed in Table 7-2. The AUXp or AUXn to SBU1 or SBU2 mapping is controlled based on Table 7-3.

After power up (V_{CC} from 0V to 3.3V), the TUSB564-Q1 defaults to USB mode. The USB PD controller upon detecting no device attached to Type-C port must take TUSB564-Q1 out of USB mode by transitioning the CTL0 pin from L to H and back to L.

Table 7-2. GPIO Configuration Control

CTL1 PIN	CTL0 PIN	FLIP PIN	CONFIGURATION	VESA DisplayPort ALT MODE UFP_D CONFIGURATION
L	L	L	Power Down	—
L	L	H	Power Down	—
L	H	L	One Port USB – No Flip	—
L	H	H	One Port USB – With Flip	—
H	L	L	4 Lane DP – No Flip	C
H	L	H	4 Lane DP – With Flip	C
H	H	L	One Port USB + 2 Lane DP – No Flip	D
H	H	H	One Port USB + 2 Lane DP – With Flip	D

Table 7-3. GPIO AUXp or AUXn to SBU1 or SBU2 Mapping

CTL1 PIN	FLIP PIN	MAPPING
H	L	SBU1 → AUXn SBU2 → AUXp
H	H	SBU2 → AUXn SBU1 → AUXp
L > 2ms	X	Open

Table 7-4 details the TUSB564-Q1 MUX routing. This table is valid for both I^2C and GPIO configuration modes.

Table 7-4. INPUT to OUTPUT Mapping

CTL1 PIN	CTL0 PIN	FLIP PIN	FROM	TO
			INPUT PIN	OUTPUT PIN
L	L	L	NA	NA
L	L	H	NA	NA
L	H	L	RX1p	SSRXp
			RX1n	SSRXn
			SSTXp	TX1p
			SSTXn	TX1n
L	H	H	RX2p	SSRXp
			RX2n	SSRXn
			SSTXp	TX2p
			SSTXn	TX2n
H	L	L	TX2p	DP0p
			TX2n	DP0n
			RX2p	DP1p
			RX2n	DP1n
			RX1p	DP2p
			RX1n	DP2n
			TX1p	DP3p
			TX1n	DP3n
H	L	H	TX1p	DP0p
			TX1n	DP0n
			RX1p	DP1p
			RX1n	DP1n
			RX2p	DP2p
			RX2n	DP2n
			TX2p	DP3p
			TX2n	DP3n
H	H	L	RX1p	SSRXp
			RX1n	SSRXn
			SSTXp	TX1p
			SSTXn	TX1n
			TX2p	DP0p
			TX2n	DP0n
			RX2p	DP1p
			RX2n	DP1n
H	H	H	RX2p	SSRXp
			RX2n	SSRXn
			SSTXp	TX2p
			SSTXn	TX2n
			TX1p	DP0p
			TX1n	DP0n
			RX1p	DP1p
			RX1n	DP1n

7.4.2 Device Configuration In I²C Mode

The TUSB564-Q1 is in I²C mode when I2C_EN is not equal to 0. The same configurations defined in GPIO mode are also available in I²C mode. The TUSB564-Q1 USB and DisplayPort configuration is controlled based on Table 7-5. The AUXp or AUXn to SBU1 or SBU2 mapping control is based on Table 7-6.

Table 7-5. I²C Configuration Control

REGISTERS			CONFIGURATION	VESA DisplayPort ALT MODE UFP_D CONFIGURATION
CTLSEL1	CTLSEL0	FLIPSEL		
0	0	0	Power Down	—
0	0	1	Power Down	—
0	1	0	One Port USB – No Flip	—
0	1	1	One Port USB – With Flip	—
1	0	0	4 Lane DP – No Flip	C
1	0	1	4 Lane DP – With Flip	C
1	1	0	One Port USB + 2 Lane DP – No Flip	D
1	1	1	One Port USB– + 2 Lane DP – With Flip	D

Table 7-6. I²C AUXp or AUXn to SBU1 or SBU2 Mapping

REGISTERS			MAPPING
AUX_SBU_OVR	CTLSEL1	FLIPSEL	
00	1	0	SBU1 → AUXn SBU2 → AUXp
00	1	1	SBU2 → AUXn SBU1 → AUXp
00	0	X	Open
01	X	X	SBU1 → AUXn SBU2 → AUXp
10	X	X	SBU2 → AUXn SBU1 → AUXp
11	X	X	Open

7.4.3 DisplayPort Mode

The TUSB564-Q1 supports up to four DisplayPort lanes at datarates up to 8.1Gbps. The TUSB564-Q1 can be enabled for DisplayPort through the GPIO control pin CTL1 or through the I²C register CTLSEL1. When I2C_EN is "0", DisplayPort is controlled based on Table 7-2. When not in GPIO mode, DisplayPort functionality is controlled through I²C registers. Data transfer through the DisplayPort lanes is further controlled by the HPDIN pin. DisplayPort must be enabled using CTL1 pin or CTLSEL1 register and also HPDIN must be pulled high for the DisplayPort data transfer to be enabled through the DisplayPort lanes.

Note

When operating in 4-lane DP mode (CTLSEL[1:0] = 2h) with AUX snoop disabled (AUX_SNOOP_DISABLE = 1), all four DP lanes must be enabled (DP0_DISABLE = DP1_DISABLE = DP2_DISABLE = DP3_DISABLE = "0").

With AUX snoop disabled (AUX_SNOOP_DISABLE = 1) and CTLESEL[1:0] = 2h, the individual DP lane disable/enable for DP0 and DP3 are swapped and DP1 and DP2 are swapped. DP0_DISABLE controls DP3, DP3_DISABLE controls DP0, DP1_DISABLE controls DP2, and DP2_DISABLE controls DP1.

7.4.4 Linear EQ Configuration

Each of the TUSB564-Q1 receiver lanes has individual controls for receiver equalization. The receiver equalization gain value can be controlled either through I^2C registers or through GPIOs. Table 7-7 details the gain value for each available combination when TUSB564-Q1 is in GPIO mode. These same options are also available in I^2C mode by updating registers DP0EQ_SEL, DP1EQ_SEL, DP2EQ_SEL, DP3EQ_SEL, EQ1_SEL, EQ2_SEL, and SSEQ_SEL. Each of the 4-bit EQ configuration registers is mapped to the configuration pins as follows: x_SEL = {x1[1:0],x0[1:0]} where xn[1:0] are the EQ configuration pins with pin levels mapped to 2-bit values as: 0 = 00, R = 01, F = 10, 1 = 11.

Table 7-7. TUSB564-Q1 Receiver Equalization GPIO Control

EQUALIZATION SETTING #	USB3.1 UPSTREAM FACING PORTS			USB 3.1 DOWNSTREAM FACING PORT			ALL DISPLAYPORT LANES		
	EQ1 PIN LEVEL	EQ0 PIN LEVEL	EQ GAIN AT 2.5GHz (dB)	SSEQ1 PIN LEVEL	SSEQ0 PIN LEVEL	EQ GAIN AT 2.5GHz (dB)	DPEQ1 PIN LEVEL	DPEQ0 PIN LEVEL	EQ GAIN AT 4.05GHz (dB)
0	0	0	–0.7	0	0	-0.9	0	0	1.0
1	0	R	1.8	0	R	0.2	0	R	3.0
2	0	F	2.7	0	F	1.1	0	F	4.4
3	0	1	3.7	0	1	2.2	0	1	5.8
4	R	0	4.6	R	0	3.0	R	0	6.8
5	R	R	5.5	R	R	4.0	R	R	8.0
6	R	F	6.3	R	F	4.8	R	F	8.8
7	R	1	7.0	R	1	5.6	R	1	9.6
8	F	0	7.8	F	0	6.4	F	0	10.4
9	F	R	8.5	F	R	7.0	F	R	11.0
10	F	F	9.1	F	F	7.6	F	F	11.6
11	F	1	9.7	F	1	8.2	F	1	12.1
12	1	0	10.1	1	0	8.7	1	0	12.5
13	1	R	10.7	1	R	9.2	1	R	13.0
14	1	F	11.1	1	F	9.7	1	F	13.4
15	1	1	11.6	1	1	10.2	1	1	13.7

7.4.5 USB3 Modes

The TUSB564-Q1 monitors the physical layer conditions like receiver termination, electrical idle, LFPS, and SuperSpeed signaling rate to determine the state of the USB3.1 interface. Depending on the state of the USB 3.2 interface, the TUSB564-Q1 can be in one of four primary modes of operation when USB 3.2 is enabled (CTL0 = H or CTLSEL0 = 1b1): Disconnect, U2/U3, U1, and U0.

The Disconnect mode is the state in which TUSB564-Q1 has not detected far-end termination on upstream facing port (UFP) or downstream facing port (DFP). The disconnect mode is the lowest power mode of each of the four modes. The TUSB564-Q1 remains in this mode until far-end receiver termination has been detected on both UFP and DFP. The TUSB564-Q1 immediately exits this mode and enters U0 after far-end termination is detected.

When in U0 mode, the TUSB564-Q1 redrives all traffic received on UFP and DFP. U0 is the highest power mode of all USB3.1 modes. The TUSB564-Q1 remains in U0 mode until electrical idle occurs on both UFP and DFP. Upon detecting electrical idle, the TUSB564-Q1 immediately transitions to U1.

The U1 mode is the intermediate mode between U0 mode and U2/U3 mode. In U1 mode, the TUSB564-Q1 UFP and DFP receiver termination remains enabled. The UFP and DFP transmitter DC common mode is maintained. The power consumption in U1 is similar to power consumption of U0.

Next to the disconnect mode, the U2/U3 mode is next lowest power state. While in this mode, the TUSB564-Q1 periodically performs far-end receiver detection. Anytime the far-end receiver termination is not detected on either UFP or DFP, the TUSB564-Q1 leaves the U2/U3 mode and transitions to the Disconnect mode. The device also monitors for a valid LFPS. Upon detection of a valid LFPS, the TUSB564-Q1 immediately transitions to the U0 mode. In U2/U3 mode, the TUSB564-Q1 receiver terminations remain enabled but the TX DC common mode voltage is not maintained.

7.4.6 Operation Timing – Power Up

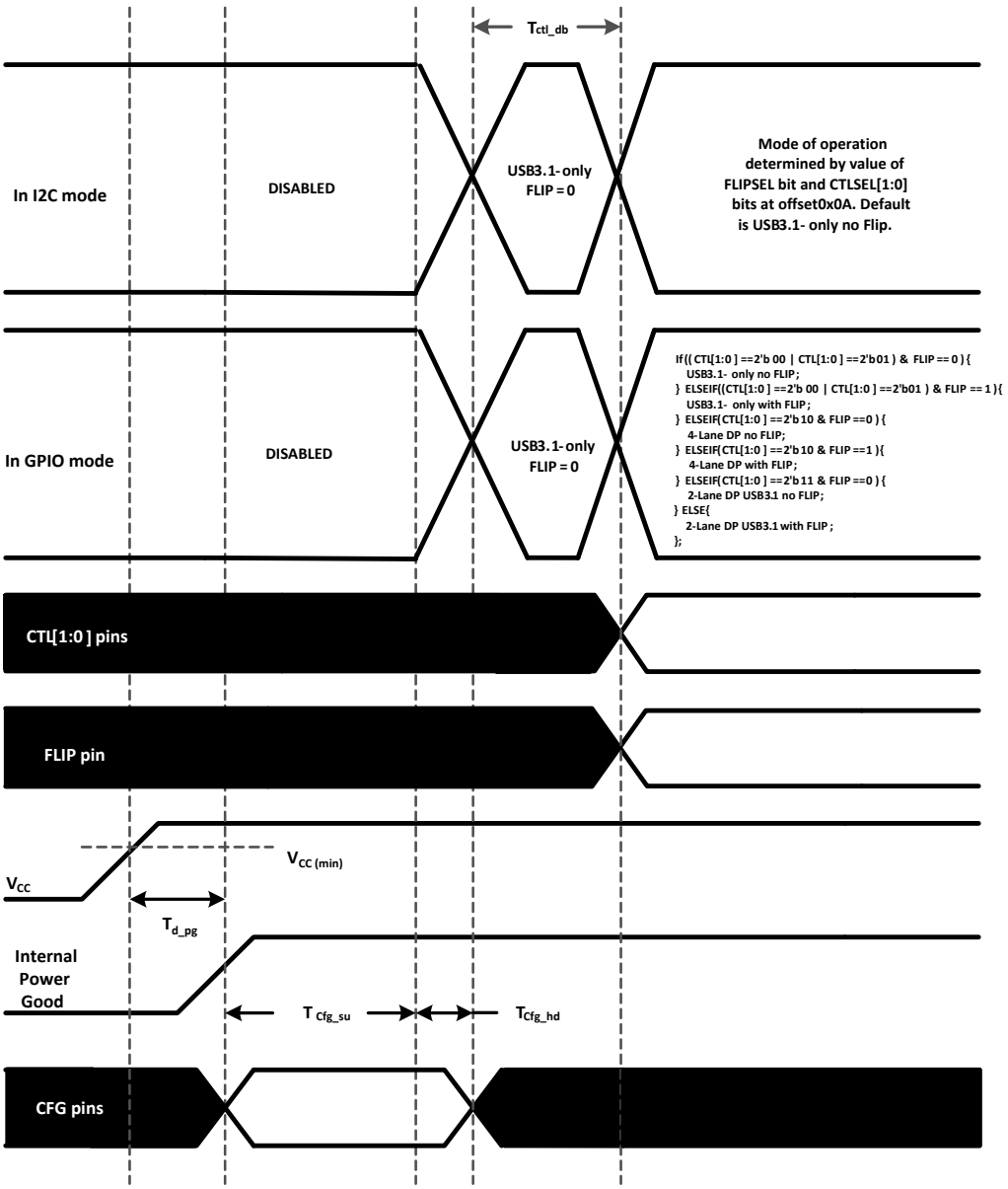


Figure 7-1. Power-Up Timing

Table 7-8. Power-Up Timing (1) (2)

PARAMETER		MIN	MAX	UNIT
t_{d_pg}	V_{CC} (minimum) to Internal Power Good asserted high		500	µs
t_{cfg_su}	CFG(1) pins setup(2)	50		µs
t_{cfg_hd}	CFG(1) pins hold	10		µs
t_{CTL_DB}	CTL[1:0] and FLIP pin debounce		16	ms
t_{VCC_RAMP}	VCC supply ramp requirement	0.1	50	ms

(1) Following pins comprise CFG pins: I2C_EN, EQ[1:0], SSEQ[1:0], and DPEQ[1:0].
(2) Recommend CFG pins are stable when V_{CC} is at minimum value.

7.5 Programming

For further programmability, the TUSB564-Q1 can be controlled using I^2C. The SCL and SDA pins are used for I^2C clock and I^2C data, respectively.

Table 7-9. TUSB564-Q1 I^2C Target Address

DPEQ0/A1 PIN LEVEL	SSEQ0/A0 PIN LEVEL	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (W/R)
0	0	1	0	0	0	1	0	0	0/1
0	R	1	0	0	0	1	0	1	0/1
0	F	1	0	0	0	1	1	0	0/1
0	1	1	0	0	0	1	1	1	0/1
R	0	0	1	0	0	0	0	0	0/1
R	R	0	1	0	0	0	0	1	0/1
R	F	0	1	0	0	0	1	0	0/1
R	1	0	1	0	0	0	1	1	0/1
F	0	0	0	1	0	0	0	0	0/1
F	R	0	0	1	0	0	0	1	0/1
F	F	0	0	1	0	0	1	0	0/1
F	1	0	0	1	0	0	1	1	0/1
1	0	0	0	0	1	1	0	0	0/1
1	R	0	0	0	1	1	0	1	0/1
1	F	0	0	0	1	1	1	0	0/1
1	1	0	0	0	1	1	1	1	0/1

7.5.1 TUSB564-Q1 I²C Target Behavior

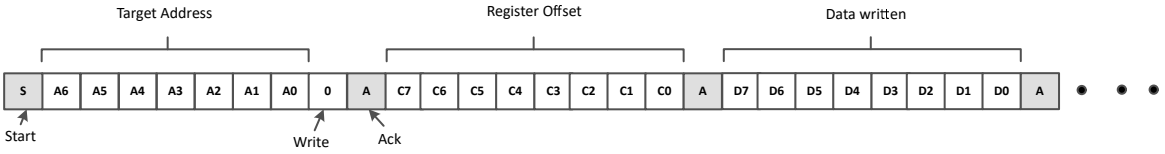


Figure 7-2. I²C Write with Data

Use the following procedure to write data to TUSB564-Q1 I²C registers (refer to Figure 7-2):

1. The controller initiates a write operation by generating a start condition (S), followed by the TUSB564-Q1 7-bit address and a zero-value W/R bit to indicate a write cycle.
2. The TUSB564-Q1 acknowledges the address cycle.
3. The controller presents the register offset within TUSB564-Q1 to be written, consisting of one byte of data, MSB-first.
4. The TUSB564-Q1 acknowledges the sub-address cycle.
5. The controller presents the first byte of data to be written to the I²C register.
6. The TUSB564-Q1 acknowledges the byte transfer.
7. The controller can continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TUSB564-Q1.
8. The controller terminates the write operation by generating a stop condition (P).

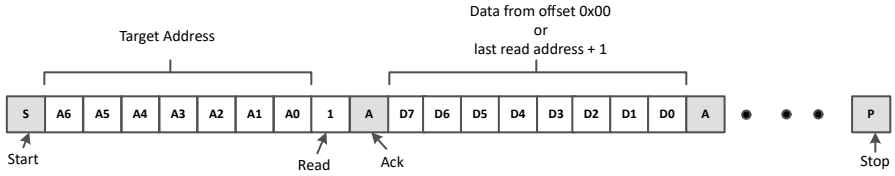


Figure 7-3. I²C Read Without Repeated Start

Use the following procedure to read the TUSB564-Q1 I²C registers without a repeated Start (refer Figure 7-3).

1. The controller initiates a read operation by generating a start condition (S), followed by the TUSB564-Q1 7-bit address and a zero-value W/R bit to indicate a read cycle.
2. The TUSB564-Q1 acknowledges the 7-bit address cycle.
3. Following the acknowledge the controller continues sending clock.
4. The TUSB564-Q1 transmit the contents of the memory registers MSB-first starting at register 00h or last read register offset+1. If a write to the I²C register occurred prior to the read, then the TUSB564-Q1 shall start at the register offset specified in the write.
5. The TUSB564-Q1 waits for either an acknowledge (ACK) or a not-acknowledge (NACK) from the controller after each byte transfer; the I²C controller acknowledges reception of each data byte transfer.
6. If an ACK is received, the TUSB564-Q1 transmits the next byte of data as long as controller provides the clock. If a NAK is received, the TUSB564-Q1 stops providing data and waits for a stop condition (P).
7. The controller terminates the write operation by generating a stop condition (P).

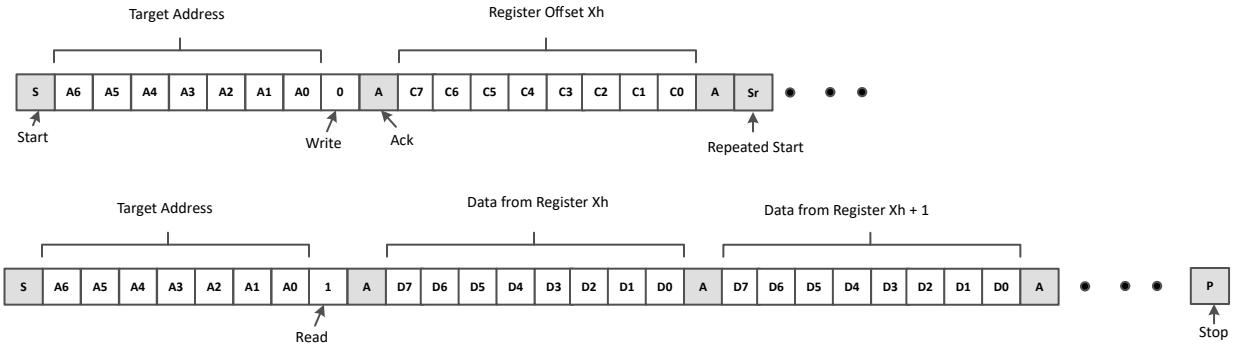


Figure 7-4. I²C Read with Repeated Start

Use the following procedure to read the TUSB564-Q1 I²C registers with a repeated Start (refer Figure 7-4).

1. The controller initiates a read operation by generating a start condition (S), followed by the TUSB564-Q1 7-bit address and a zero-value W/R bit to indicate a write cycle.
2. The TUSB564-Q1 acknowledges the 7-bit address cycle.
3. The controller presents the register offset within TUSB564-Q1 to be written, consisting of one byte of data, MSB-first.
4. The TUSB564-Q1 acknowledges the register offset cycle.
5. The controller presents a repeated start condition (Sr).
6. The controller initiates a read operation by generating a start condition (S), followed by the TUSB564-Q1 7-bit address and a one-value W/R bit to indicate a read cycle.
7. The TUSB564-Q1 acknowledges the 7-bit address cycle.
8. The TUSB564-Q1 transmit the contents of the memory registers MSB-first starting at the register offset.
9. The TUSB564-Q1 shall wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the controller after each byte transfer; the I²C controller acknowledges reception of each data byte transfer.
10. If an ACK is received, the TUSB564-Q1 transmits the next byte of data as long as controller provides the clock. If a NAK is received, the TUSB564-Q1 stops providing data and waits for a stop condition (P).
11. The controller terminates the read operation by generating a stop condition (P).

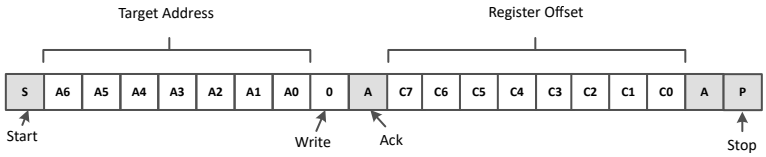


Figure 7-5. I²C Write Without Data

Use the following procedure to set a starting sub-address for I²C reads (refer to Figure 7-5).

1. The controller initiates a write operation by generating a start condition (S), followed by the TUSB564-Q1 7-bit address and a zero-value W/R bit to indicate a write cycle.
2. The TUSB564-Q1 acknowledges the address cycle.
3. The controller presents the register offset within TUSB564-Q1 to be written, consisting of one byte of data, MSB-first.
4. The TUSB564-Q1 acknowledges the register offset cycle.
5. The controller terminates the write operation by generating a stop condition (P).

Note

After initial power up, if no register offset is included for the read procedure (refer to Figure 7-3), then reads start at register offset 00h and continue byte by byte through the registers until the I^2C controller terminates the read operation. During a read operation, the TUSB564-Q1 auto-increments the I^2C internal register address of the last byte transferred independent of whether or not an ACK was received from the I^2C controller.

Software must only access (read or write) addresses detailed in this document. Accessing reserved or undocumented addresses can result in TUSB564-Q1 entering an undefined state.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TUSB564-Q1 is a linear redriver designed specifically to compensation for intersymbol interference (ISI) jitter caused by signal attenuation through a passive medium like PCB traces and cables. Because the TUSB564-Q1 has four independent DisplayPort 1.4 inputs, one upstream facing USB 3.2 Gen 1 input, and two downstream facing USB 3.2 Gen 1 inputs, the TUSB564-Q1 can be optimized to correct ISI on all those seven inputs through 16 different equalization choices. Placing the TUSB564-Q1 between a USB3.2 Host/DisplayPort 1.4 GPU and a USB3.2 Type-C receptacle can correct signal integrity issues resulting in a more robust system.

8.2 Typical Application

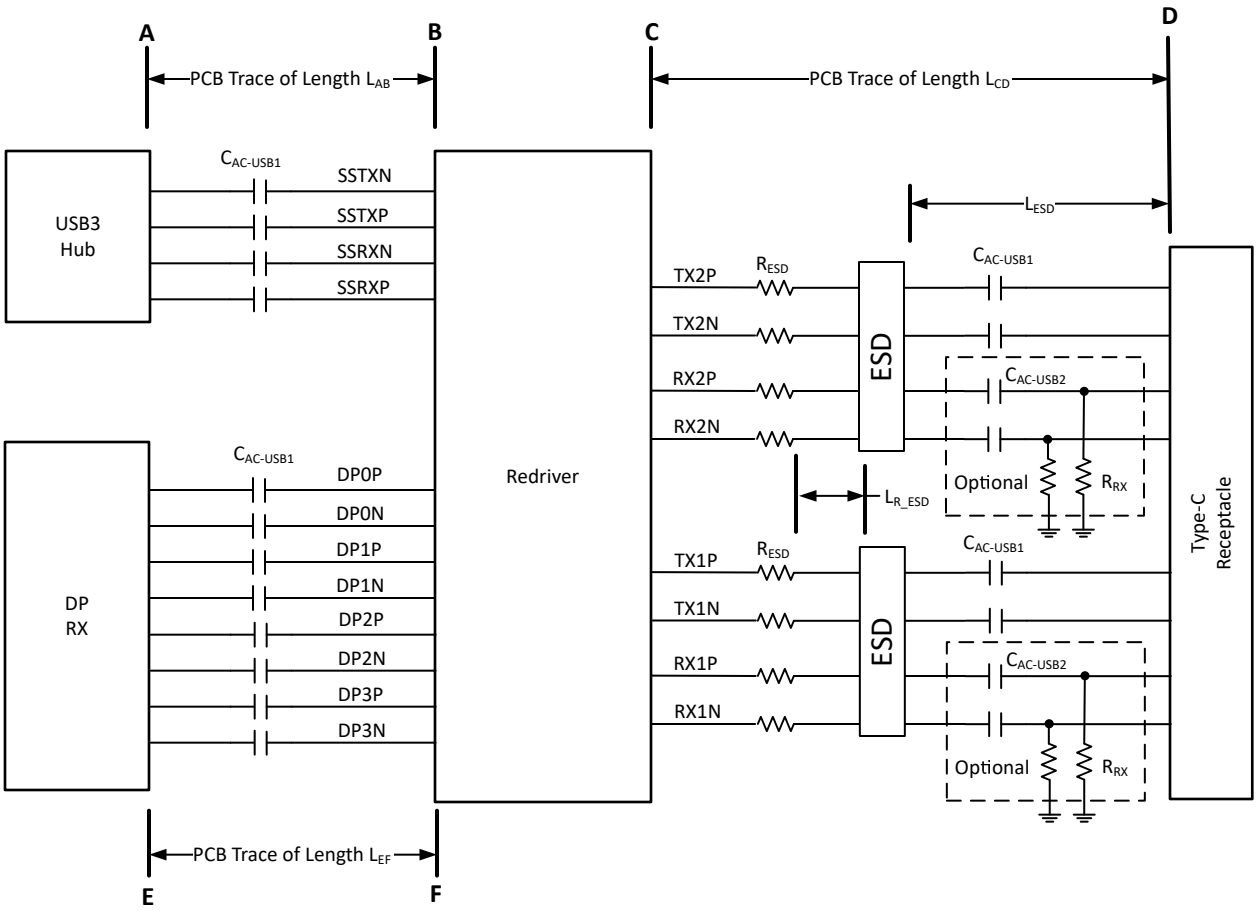


Figure 8-1. TUSB564-Q1 in a DP Alt Sink Application

8.2.1 Design Requirements

For this design example, use the parameters provided in Table 8-1.

Table 8-1. Design Parameters

PARAMETER(1)	VALUE
Redriver to USB3 Hub maximum PCB trace length, X_{AB}	8 inches
Redriver to DP RX maximum PCB trace length, X_{EF}	6 inches
Redriver to Type-C connector maximum PCB trace length, X_{CD}	2 inches
Maximum distance of ESD component from the USB receptacle, L_{ESD}	1.0 inches
Maximum distance of series resistor (R_{ESD}) from ESD component, L_{R_ESD}.	0.25 inches
$C_{AC\text{-}USB1}$ AC-coupling capacitor (75nF to 265nF)	100nF or 220nF
$C_{AC\text{-}USB2}$ AC-coupling capacitor (297nF to 363nF)	Options: • RX1 and RX2 are DC-coupled to USB receptacle • 330nF AC-couple with R_{RX} resistor
Optional R_{RX} resistor (220kΩ ± 5%)	220kΩ ± 5%
Optional R_{ESD} (0Ω to 2.2Ω)	1Ω
VCC supply (3V to 3.6V)	3.3V
I2C Mode or GPIO Mode	I2C Mode. (I2C_EN pin != "0")
1.8V or 3.3V I2C Interface	3.3V I2C. Pullup the I2C_EN pin to 3.3V with a 1K ohm resistor. CTL1, EQ[1:0], SSEQ[1:0], and DPEQ[1:0] pin unconnected.
EQ setting for DisplayPort Lanes	EQ Setting # 5 (Register 0x0A[4] = 1'b1, 0x10 = 0x55; 0x11 = 0x55)
EQ setting for Downstream USB Data Path	EQ Setting # 6 (Register 0x0A[4] = 1'b1, 0x20 = 0x66)
EQ setting for Upstream USB Data Path	EQ Setting # 6 (Register 0x0A[4] = 1'b1, 0x21 = 0x08)

(1) Maximum trace length assumes an insertion loss of 0.2dB/inch/GHz. If insertion loss is more than 0.2dB/inch/GHz, then maximum trace length must be reduced accordingly.

8.2.2 Detailed Design Procedure

A typical usage of the TUSB564-Q1 device is shown in Figure 8-2. The device can be controlled either through its GPIO pins or through its I^2C interface. In the example shown below, a Type-C PD controller is used to configure the device through the I^2C interface. In I^2C mode, the equalization settings for each receiver can be independently controlled through I^2C registers. For this reason, the configuration pin CTL1 and all of the equalization pins (EQ[1:0], SSEQ[1:0], and DPEQ[1:0]) can be left unconnected. If these pins are left unconnected, the TUSB564-Q1 7-bit I^2C target address is 0x12 because both DPEQ/A1 and SSEQ0/A0 are at pin level "F". If a different I^2C target address is desired, set the DPEQ/A1 and SSEQ0/A0 pins to a level which produces the desired I^2C target address.

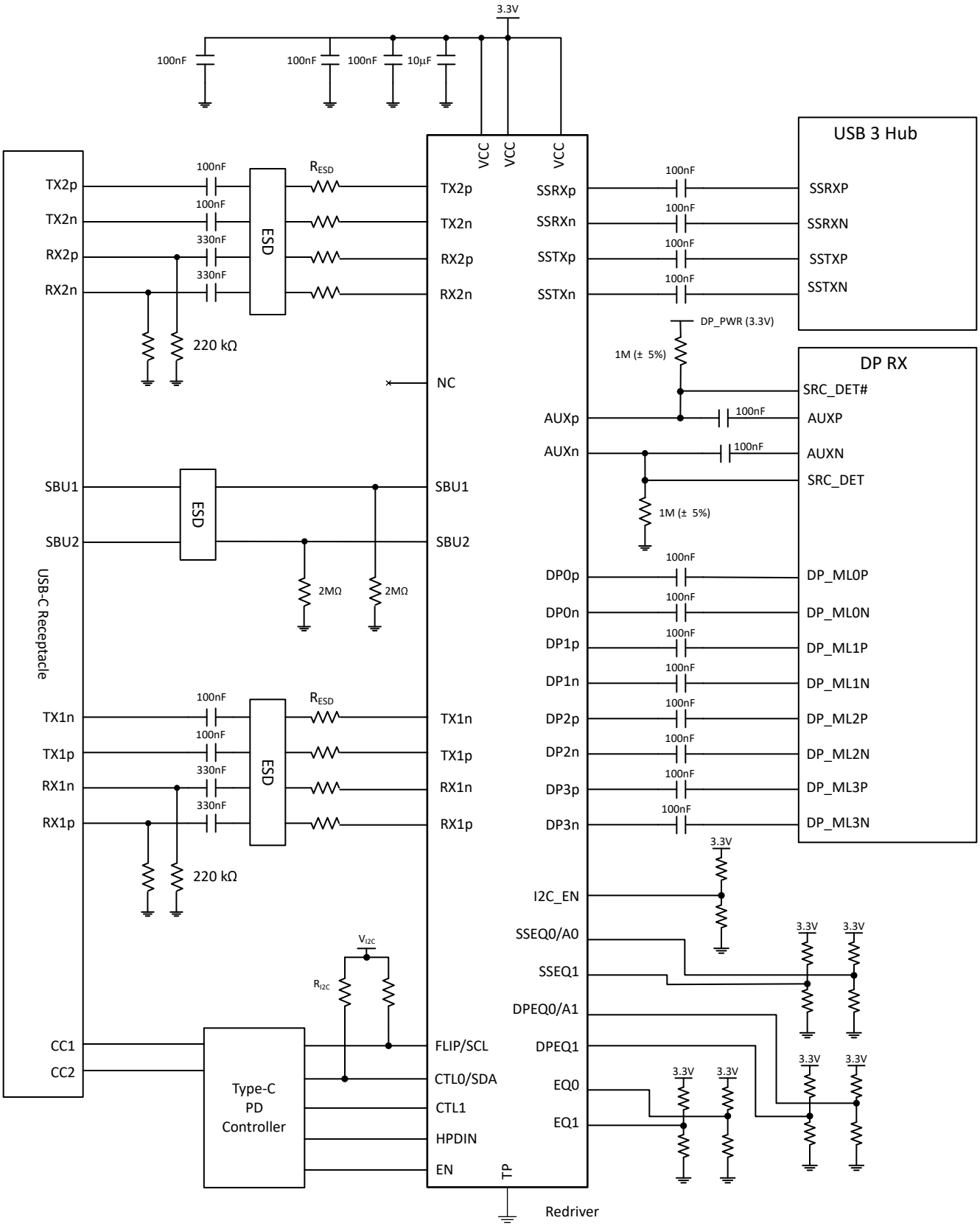


Figure 8-2. Application Circuit

8.2.2.1 ESD Protection

It may be necessary to incorporate an ESD component to protect the TUSB564-Q1 from electrostatic discharge (ESD). TI recommends following the ESD protection recommendations listed in Table 8-2. A clamp voltage greater than value specified in Table 8-2 may require a R_{ESD} on each differential pin. Place the ESD component near the USB connector.

Table 8-2. ESD Diodes Recommended Characteristics

PARAMETER	RECOMMENDATION
Breakdown voltage	≥ 3.5V
I/O line capacitance	Data rates ≤ 5Gbps: ≤ 0.50pF
	Data rates > 5Gbps: ≤ 0.35pF
Delta capacitance between any P and N I/O pins	≤ 0.07pF
Clamping voltage at 8A I_{PP} IO to GND (1)	≤ 4.5V
Typical dynamic resistance	≤ 30mΩ

(1) According to IEC 61000-4-5 (8/20µs current waveform)

Table 8-3. Recommended ESD Protection Component

MANUFACTURER	PART NUMBER	R_{ESD} TO SUPPORT IEC 61000-4-2 CONTACT ±8kV
Nexperia	PUSB3FR4	1Ω
Nexperia	PESD2V8Y1BSF	1Ω
Texas Instruments	TPD1E04U04DPLR	2Ω
Texas Instruments	TPD4E02B04DQAR	2Ω

8.2.2.2 Support for DisplayPort UFP_D Pin Assignment E

The TUSB564-Q1 device can be used in a system that handles DisplayPort UFP_D Pin Assignment E use-case if special measures are taken as described below. With UFP_D Pin Assignment E, the polarity of both the main link and AUX signals are inverted on the Type-C receptacle pins relative to Pin Assignment C. Moreover, on the Type-C receptacle, the location of Lane 0 is swapped with Lane 1 and that of Lane 2 is swapped with Lane 3 relative to Pin Assignment C. For correct reception of the DisplayPort video signal, the system must comprehend the above-described signaling variation.

The use of the TUSB564-Q1 device in a system that handles Pin Assignment E depends on whether AUX-to-SBU switching of the DisplayPort AUX signal is performed internally by the TUSB564-Q1 or by external devices such as a PD controller. It also depends on the configuration mode used: I^2C Mode or GPIO Mode. In all those scenarios, the TUSB564-Q1 passes the polarity of the Main Link signals as received. The DisplayPort sink must handle the polarity inversion of those signals. Moreover, the DisplayPort sink must handle the lane swapping with the following lane-to-pin mapping as received by the TUSB564-Q1 device: Lane 0 → DP1, Lane 1 → DP0, Lane 2 → DP3, and Lane 3 → DP2.

The use-case with the AUX-to-SBU switching performed internally by the TUSB564-Q1 device is shown in Figure 8-3. If the TUSB564-Q1 device configuration is through the I^2C Mode, AUX snooping must be disabled by setting AUX_SNOOP_DISABLE register 0x13[7] = 1'b1, and manual AUX-to-SBU switching must be performed through the AUX_SBU_OVR register 0x13[5:4]: AUX_SBU_OVR = 2'b01 for normal USB Type-C plug orientation, or AUX_SBU_OVR = 2'b10 for flipped USB Type-C plug orientation when Pin Assignment E signals are received. If the TUSB564-Q1 device configuration is through the GPIO Mode, all four DisplayPort lanes are automatically activated. The DisplayPort sink device must handle the polarity inversion of both the AUX and Main Link signals as well as main link lane swapping.

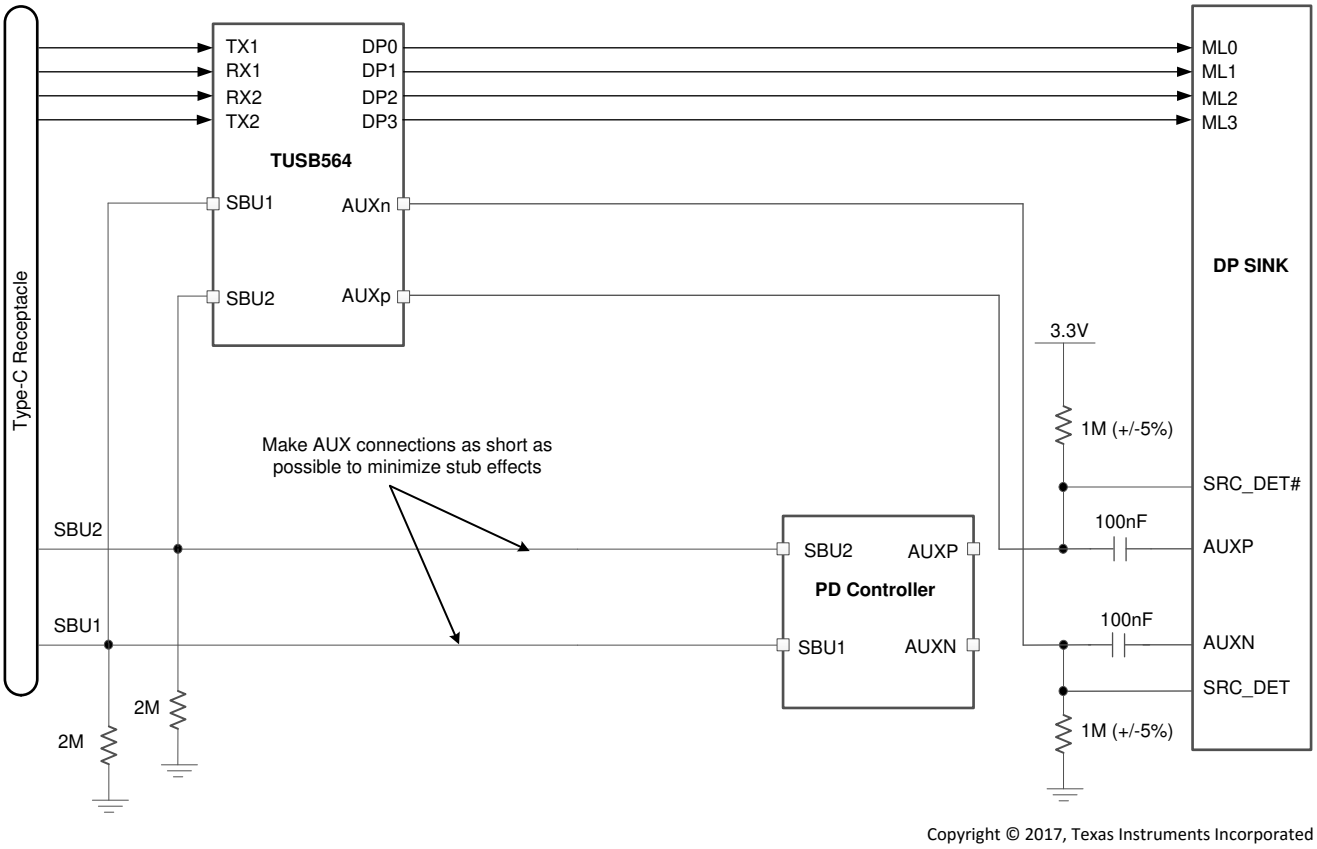


Figure 8-3. DisplayPort AUX Connections for UFP_D Pin Assignment E with Internal AUX Switching

The use-case with the AUX-to-SBU switching performed by an external device is shown in Figure 8-4. In this case, it is assumed that the PD controller is capable of correcting the polarity inversion of the AUX signal and the TUSB564-Q1 is provided with the corrected polarity of the AUX signal through its AUXp/AUXn pins. If the TUSB564-Q1 device configuration is through the I^2C Mode, disable AUX snooping by setting AUX_SNOOP_DISABLE register 0x13[7] = 1'b1. The DisplayPort sink device must handle the polarity inversion of the Main Link signals as well as the Main Link lane swapping.

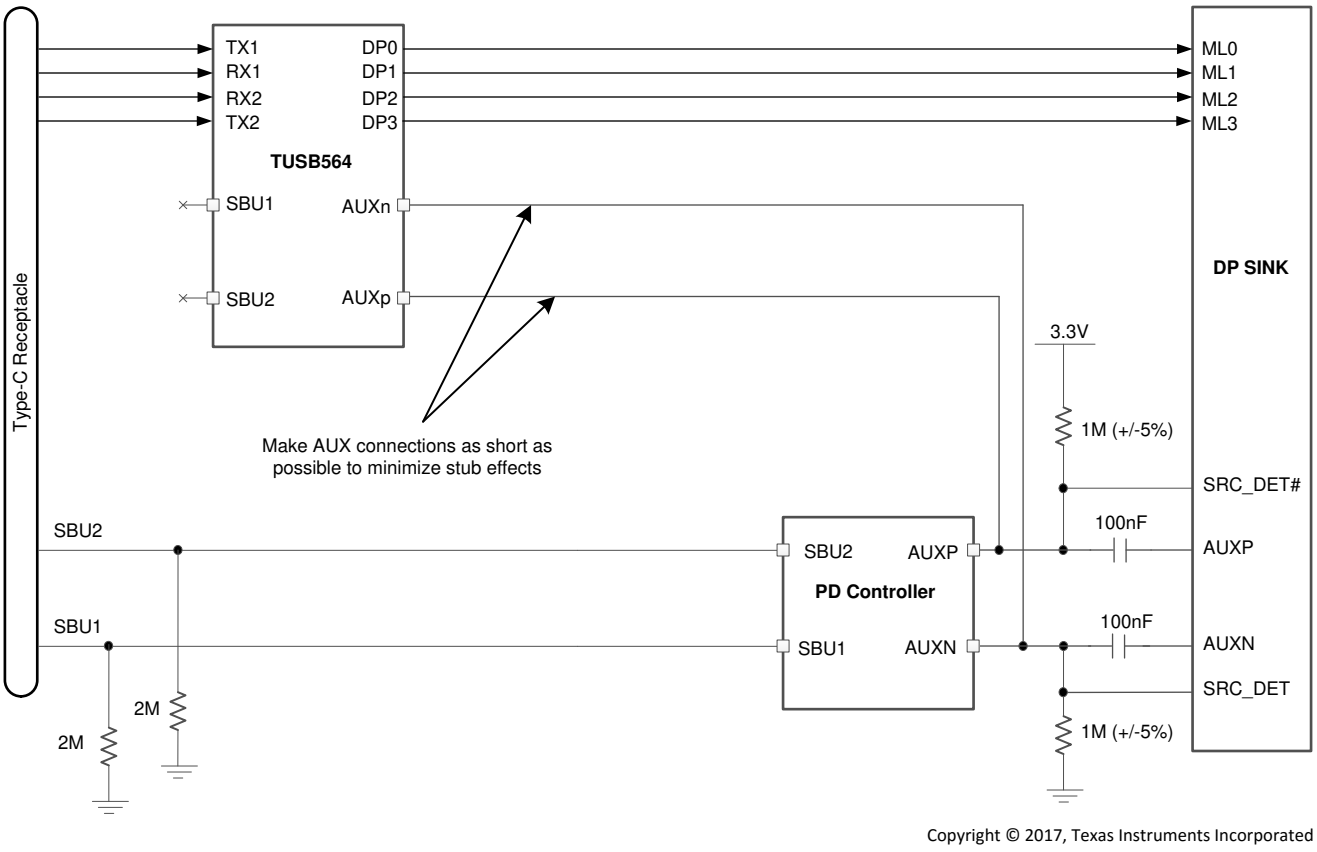


Figure 8-4. DisplayPort AUX Connections for UFP_D Pin Assignment E with External AUX Switching

8.2.3 Application Curve

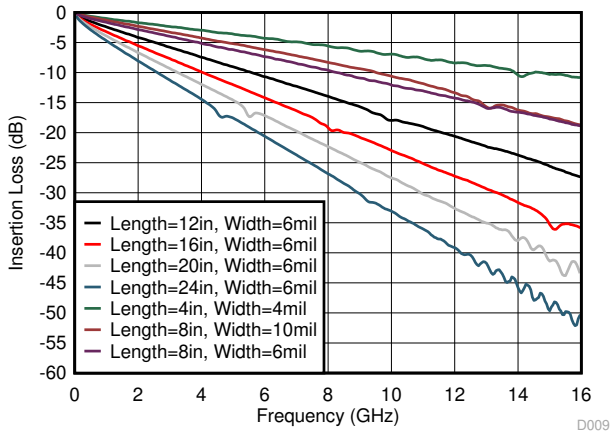


Figure 8-5. Insertion Loss of FR4 PCB Traces

8.3 System Examples

8.3.1 USB 3.1 Only

The TUSB564-Q1 is in USB3.1 only when the CTL1 pin is low and CTL0 pin is high.

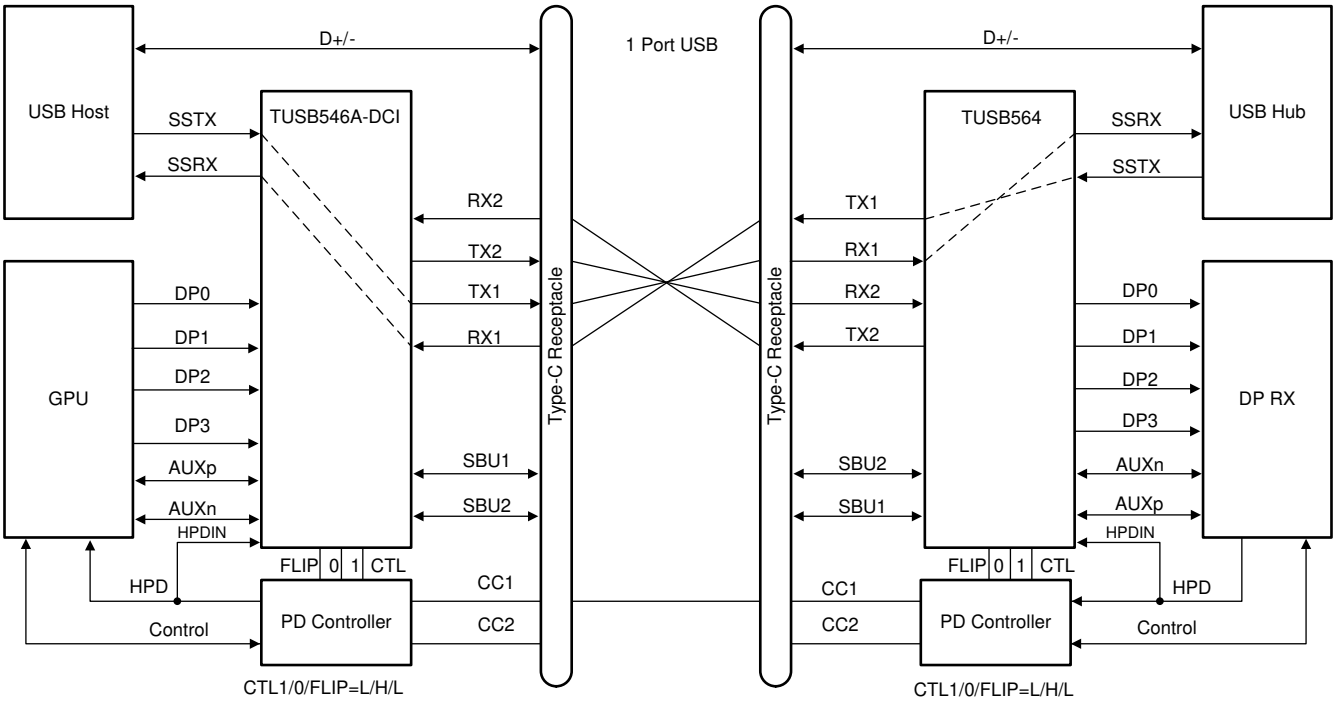


Figure 8-6. USB3.1 Only – No Flip (CTL1 = L, CTL0 = H, FLIP = L)

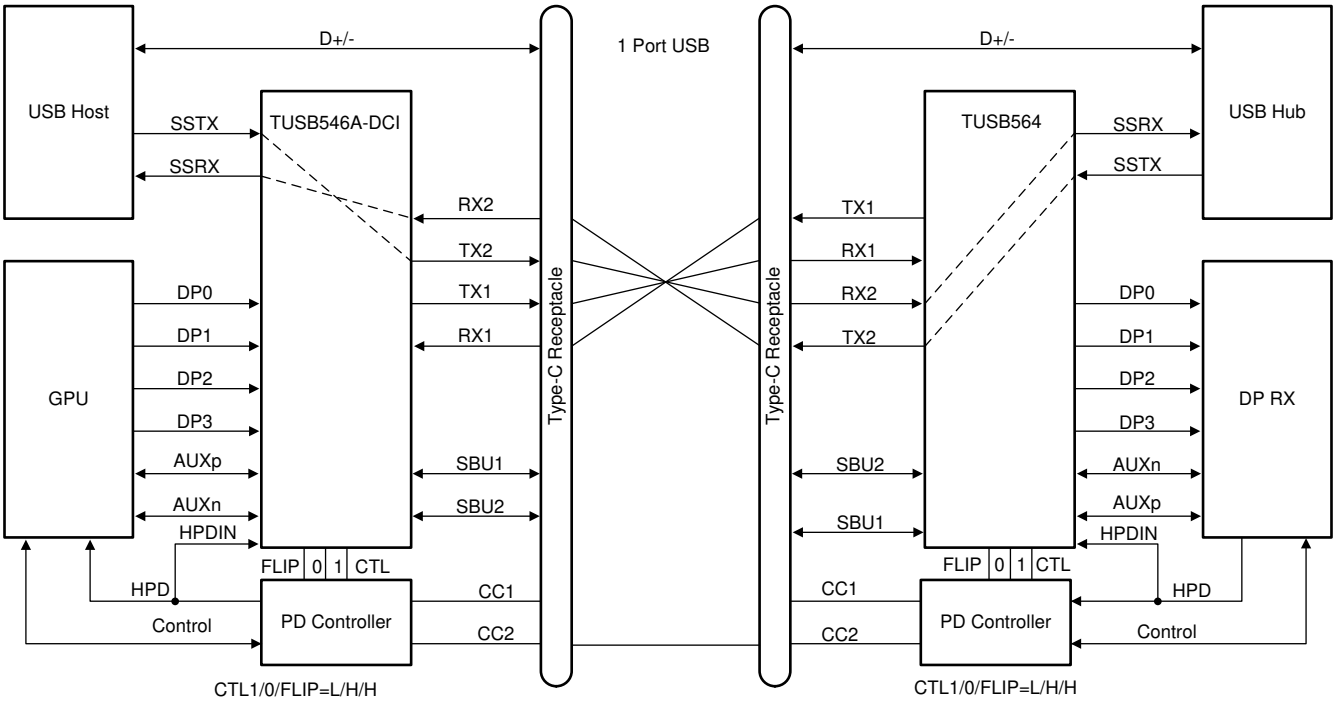


Figure 8-7. USB3.1 Only – With Flip (CTL1 = L, CTL0 = H, FLIP = H)

8.3.2 USB 3.1 and 2 Lanes of DisplayPort

The TUSB564-Q1 operates in USB3.1 and 2 Lanes of DisplayPort mode when the CTL1 pin is high and CTL0 pin is high.

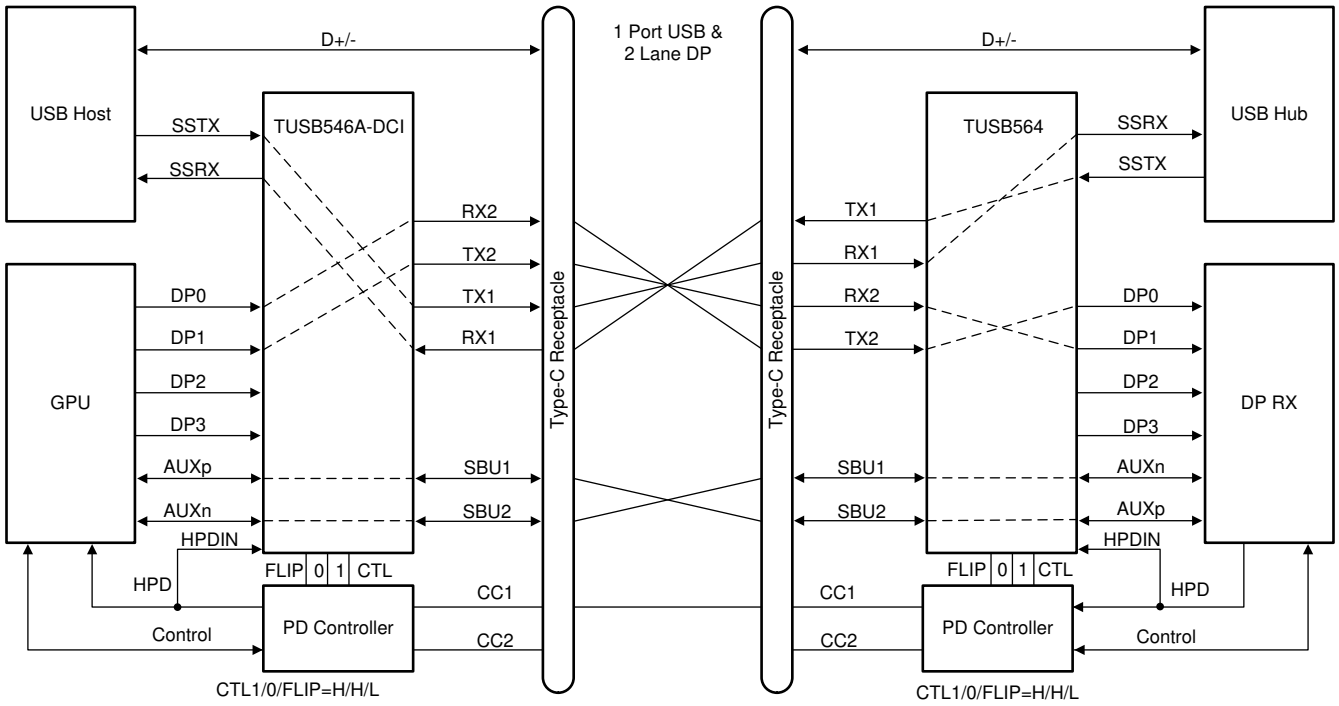


Figure 8-8. USB3.1 + 2 Lane DP – No Flip (CTL1 = H, CTL0 = H, FLIP = L)

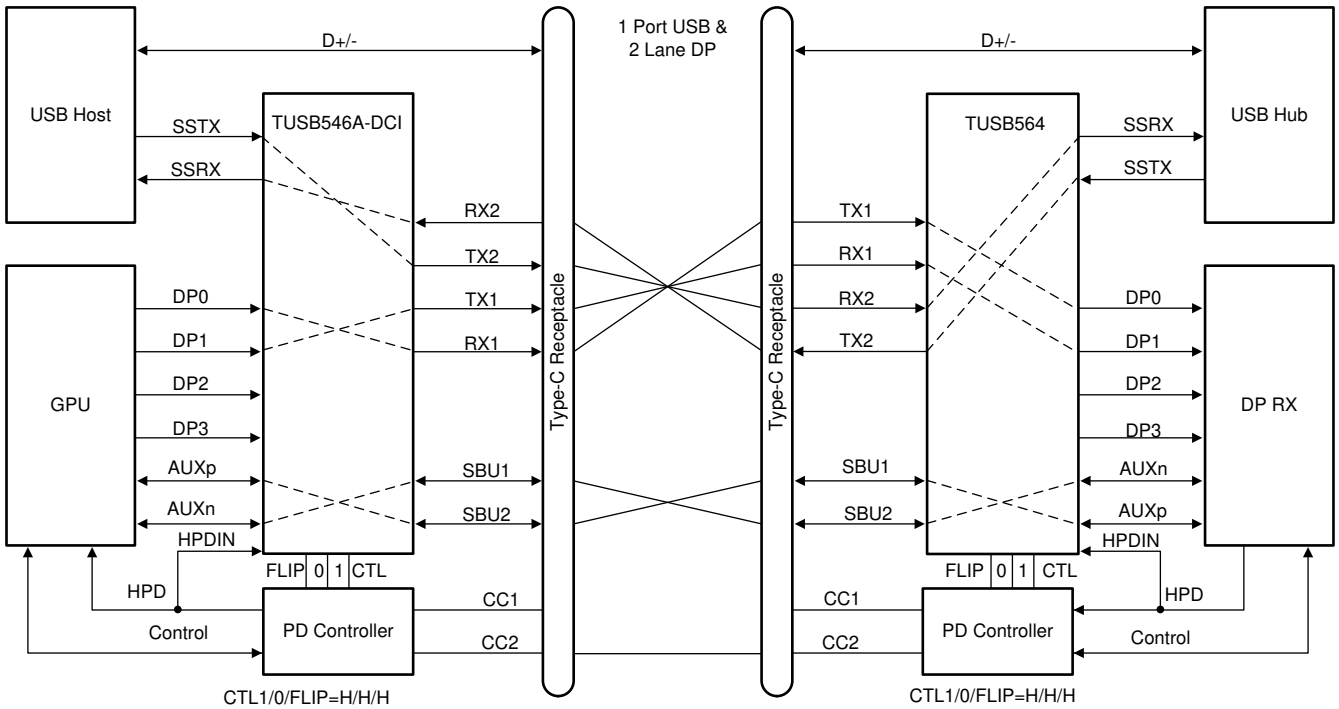


Figure 8-9. USB 3.1 + 2 Lane DP – Flip (CTL1 = H, CTL0 = H, FLIP = H)

8.3.3 DisplayPort Only

The TUSB564-Q1 operates in four lanes of DisplayPort-only mode when the CTL1 pin is high and CTL0 pin is low.

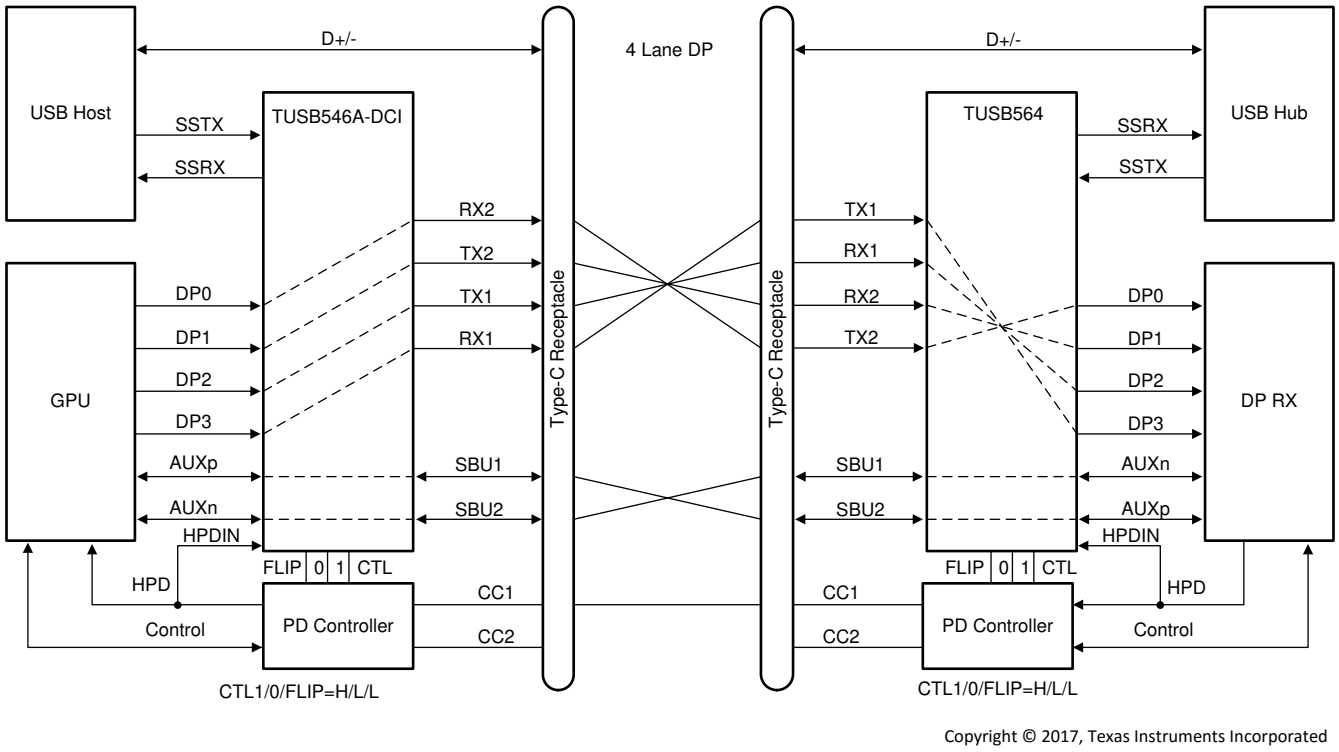


Figure 8-10. 4-Lane DP – No Flip (CTL1 = H, CTL0 = L, FLIP = L)

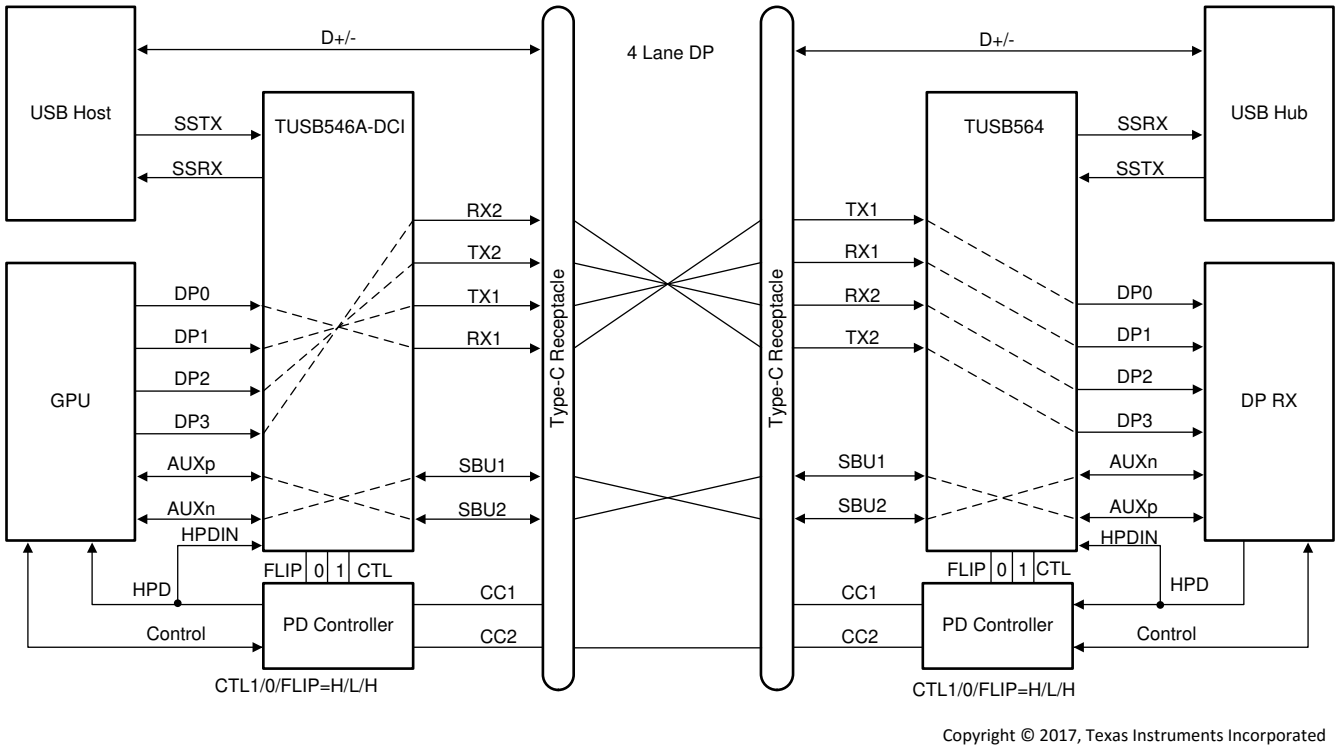


Figure 8-11. 4-Lane DP – With Flip (CTL1 = H, CTL0 = L, FLIP = H)

8.4 Power Supply Recommendations

The TUSB564-Q1 is designed to operate with a 3.3V power supply. Do not use levels above those listed in *Recommended Operating Conditions*. If using a higher voltage system power supply, a voltage regulator can be used to step down to 3.3V. Use decoupling capacitors to reduce noise and improve power supply integrity. Connect a 0.1µF capacitor between each power pin and ground.

8.5 Layout

8.5.1 Layout Guidelines

1. Route RXP/N and TXP/N pairs with controlled 90Ω differential impedance (±15%).
2. Keep away from other high speed signals.
3. Keep intra-pair routing to within 2 mils.
4. Place length matching near the location of mismatch.
5. Separate each pair by at least 3 times the signal trace width.
6. Keep the use of bends in differential traces to a minimum. When bends are used, make sure to keep the number of left and right bends as equal as possible and the angle of the bend ≥ 135 degrees. This minimizes any length mismatch causes by the bends and therefore minimizes the impact bends have on EMI.
7. Route all differential pairs on the same of layer.
8. Keep the number of vias to a minimum. TI recommends to keep the via count to 2 or less.
9. Keep traces on layers adjacent to ground plane.
10. Do NOT route differential pairs over any plane split.
11. Note that adding test points can cause impedance discontinuity, and therefore negatively impact signal performance. If test points are used, place the points in series and symmetrically. The points must not be placed in a manner that causes a stub on the differential pair.

8.5.2 Layout Example

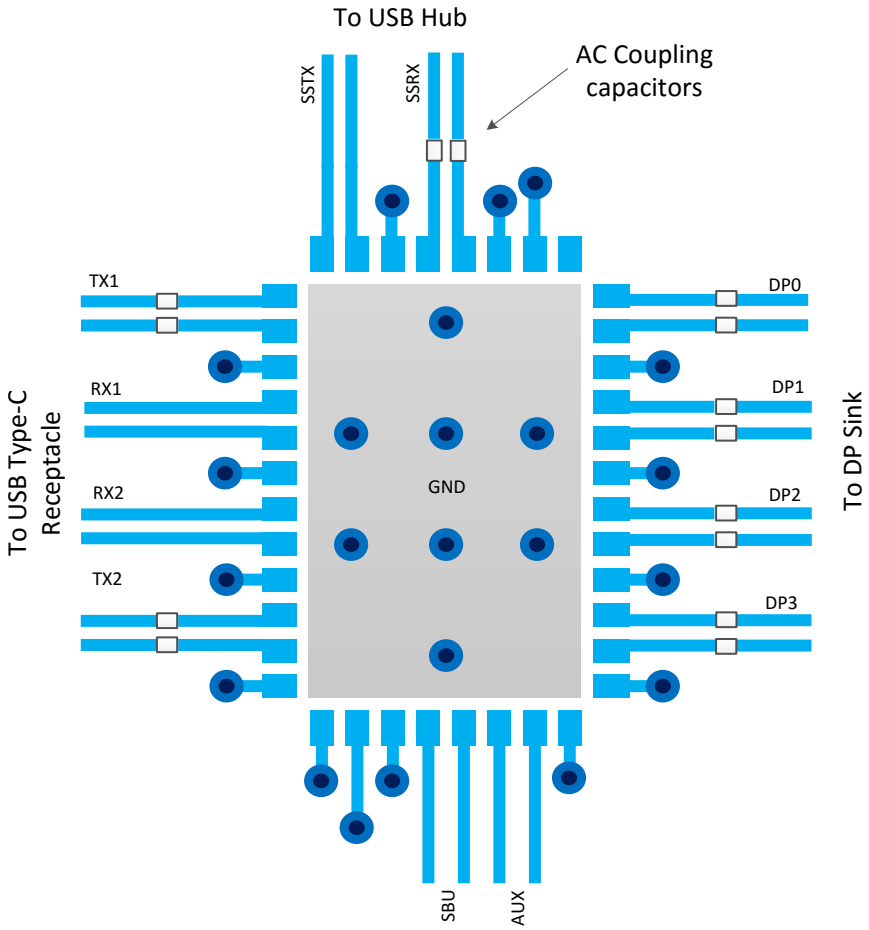


Figure 8-12. Layout Example

9 Register Maps

Table 9-1. Register Legend

ACCESS TAG	NAME	MEANING
R	Read	The field can be read by software
W	Write	The field can be written by software
S	Set	The field can be set by a write of one. Writes of zeros to the field have no effect.
C	Clear	The field can be cleared by a write of one. Write of zero to the field have no effect.
U	Update	Hardware can autonomously update this field.
NA	No Access	Not accessible or not applicable

9.1 General Register (address = 0x0A) [reset = 00000001]

Figure 9-1. General Registers

7	6	5	4	3	2	1	0
Reserved		Reserved	EQ_OVERRIDE	HPDIN_OVRRIDE	FLIPSEL	CTLSEL[1:0].	
R		R	R/W	R/W	R/W	R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-2. General Registers

Bit	Field	Type	Reset	Description
7:5	Reserved.	R	00	Reserved.
4	EQ_OVERRIDE	R/W	0	Setting this field allows software to use EQ settings from registers instead of value sample from pins. 0: EQ settings based on sampled state of the EQ pins (SSEQ[1:0], EQ[1:0], and DPEQ[1:0]). 1: EQ settings based on programmed value of each of the EQ registers
3	DP_EN_CTRL	R/W	0	Controls whether DisplayPort functionality is controlled by CTLSEL1 register or CTL1 pin. 0: DisplayPort enable/disable is based on CTLSEL1 register. 1: DisplayPort enable/disable is based on state of CTL1 pin.
2	FLIPSEL	R/W	0	FLIPSEL. Refer to Table 7-5 and Table 7-6 for this field functionality.
1:0	CTLSEL[1:0].	R/W	01	00: Disabled. All RX and TX for USB3 and DisplayPort are disabled. 01: USB3.1 only enabled. (Default) 10: Four DisplayPort lanes enabled. 11: Two DisplayPort lanes and one USB3.1

9.2 DisplayPort Control/Status Registers (address = 0x10) [reset = 00000000]

Figure 9-2. DisplayPort Control/Status Registers (0x10)

7	6	5	4	3	2	1	0
DP1EQ_SEL				DP3EQ_SEL			
R/W/U				R/W/U			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-3. DisplayPort Control/Status Registers (0x10)

Bit	Field	Type	Reset	Description
7:4	DP1EQ_SEL	R/W/U	0000	Field selects EQ level for DP lane 1. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for DP lane 1 based on value written to this field.

Table 9-3. DisplayPort Control/Status Registers (0x10) (continued)

Bit	Field	Type	Reset	Description
3:0	DP3EQ_SEL	R/W/U	0000	Field selects EQ level for DP lane 3. When EQ_OVERRIDE = 1’b0, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1’b1, software can change the EQ setting for DP lane 3 based on value written to this field.

9.3 DisplayPort Control/Status Registers (address = 0x11) [reset = 00000000]

Figure 9-3. DisplayPort Control/Status Registers (0x11)

7	6	5	4	3	2	1	0
DP0EQ_SEL				DP2EQ_SEL			
R/W/U				R/W/U			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-4. DisplayPort Control/Status Registers (0x11)

Bit	Field	Type	Reset	Description
7:4	DP0EQ_SEL	R/W/U	0000	Field selects EQ level for DP lane 0. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for DP lane 0 based on value written to this field.
3:0	DP2EQ_SEL	R/W/U	0000	Field selects EQ level for DP lane 2. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for DP lane 2 based on value written to this field.

9.4 DisplayPort Control/Status Registers (address = 0x12) [reset = 00000000]

Figure 9-4. DisplayPort Control/Status Registers (0x12)

7	6	5	4	3	2	1	0
Reserved	SET_POWER_STATE		LANE_COUNT_SET				
R	RU		RU				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-5. DisplayPort Control/Status Registers (0x12)

Bit	Field	Type	Reset	Description
7	Reserved	R	0	Reserved
6:5	SET_POWER_STATE	R/U	00	This field represents the snooped value of the AUX write to DPCD address 0x00600. When AUX_SNOOP_DISABLE = 1'b0, the TUSB564-Q1 enables or disables the DP lanes based on the snooped value. When AUX_SNOOP_DISABLE = 1'b1, then DP lane enable/disable are determined by state of DPx_DISABLE registers, where x = 0, 1, 2, or 3. This field is reset to 2'b00 by hardware when CTLSEL1 changes from a 1'b1 to a 1'b0.
4:0	LANE_COUNT_SET	R/U	00000	This field represents the snooped value of AUX write to DPCD address 0x00101 register. When AUX_SNOOP_DISABLE = 1'b0, the TUSB564-Q1 enables DP lanes specified by the snoop value. Unused DP lanes are disabled to save power. When AUX_SNOOP_DISABLE = 1'b1, then DP lanes enable/disable are determined by DPx_DISABLE registers, where x = 0, 1, 2, or 3. This field is reset to 0x0 by hardware when CTLSEL1 changes from a 1'b1 to a 1'b0.

9.5 DisplayPort Control/Status Registers (address = 0x13) [reset = 00000000]

Figure 9-5. DisplayPort Control/Status Registers (0x13)

7	6	5	4	3	2	1	0
AUX_SNOOP_DISABLE	Reserved	AUX_SBU_OVR		DP3_DISABLE	DP2_DISABLE	DP1_DISABLE	DP0_DISABLE
R/W	R	R/W		R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-6. DisplayPort Control/Status Registers (0x13)

Bit	Field	Type	Reset	Description
7	AUX_SNOOP_DISABLE	R/W	0	0: AUX snoop enabled. (Default) 1: AUX snoop disabled.
6	Reserved	R	0	Reserved
5:4	AUX_SBU_OVR	R/W	00	This field overrides the AUXp or AUXn to SBU1 or SBU2 connect and disconnect based on CTL1 and FLIP. Changing this field to 2'b01 or 2'b10 allows traffic to pass through AUX to SBU regardless of the state of CTLSEL1 and FLIPSEL register 00: AUX to SBU connect/disconnect determined by CTLSEL1 and FLIPSEL (Default) 01: AUXn -> SBU1 and AUXp -> SBU2 connection always enabled. 10: AUXn -> SBU2 and AUXp -> SBU1 connection always enabled. 11: AUX to SBU open.
3	DP3_DISABLE	R/W	0	When AUX_SNOOP_DISABLE = 1'b1, this field can be used to enable or disable DP lane 3. When AUX_SNOOP_DISABLE = 1'b0, changes to this field have no effect on lane 3 functionality. 0: DP Lane 3 Enabled (default) 1: DP Lane 3 Disabled.
2	DP2_DISABLE	R/W	0	When AUX_SNOOP_DISABLE = 1'b1, this field can be used to enable or disable DP lane 2. When AUX_SNOOP_DISABLE = 1'b0, changes to this field have no effect on lane 2 functionality. 0: DP Lane 2 Enabled (default) 1: DP Lane 2 Disabled.
1	DP1_DISABLE	R/W	0	When AUX_SNOOP_DISABLE = 1'b1, this field can be used to enable or disable DP lane 1. When AUX_SNOOP_DISABLE = 1'b0, changes to this field have no effect on lane 1 functionality. 0: DP Lane 1 Enabled (default) 1: DP Lane 1 Disabled.
0	DP0_DISABLE	R/W	0	DISABLE. When AUX_SNOOP_DISABLE = 1'b1, this field can be used to enable or disable DP lane 0. When AUX_SNOOP_DISABLE = 1'b0, changes to this field have no effect on lane 0 functionality. 0: DP Lane 0 Enabled (default) 1: DP Lane 0 Disabled.

9.6 USB3.1 Control/Status Registers (address = 0x20) [reset = 00000000]

Figure 9-6. USB3.1 Control/Status Registers (0x20)

7	6	5	4	3	2	1	0
EQ2_SEL				EQ1_SEL			
R/W/U				R/W/U			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-7. USB3.1 Control/Status Registers (0x20)

Bit	Field	Type	Reset	Description
7:4	EQ2_SEL	R/W/U	0000	Field selects EQ level for USB3.1 RX2 receiver. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of EQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for USB3.1 RX2 receiver based on value written to this field.
3:0	EQ1_SEL	R/W/U	0000	Field selects EQ level for USB3.1 RX1 receiver. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of EQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for USB3.1 RX1 receiver based on value written to this field.

9.7 USB3.1 Control/Status Registers (address = 0x21) [reset = 00000000]

Figure 9-7. USB3.1 Control/Status Registers (0x21)

7	6	5	4	3	2	1	0
Reserved				SSEQ_SEL			
R				R/W/U			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-8. USB3.1 Control/Status Registers (0x21)

Bit	Field	Type	Reset	Description
7:4	Reserved	R	0000	Reserved
3:0	SSEQ_SEL	R/W/U	0000	Field selects between 0dB to 11dB of EQ for USB3.1 SSTXP/N receiver. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of SSEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for USB3.1 SSTXP/N receiver based on value written to this field.

9.8 USB3.1 Control/Status Registers (address = 0x22) [reset = 00000000]

Figure 9-8. USB3.1 Control/Status Registers (0x22)

7	6	5	4	3	2	1	0
CM_ACTIVE	LFPS_EQ	U2U3_LFPS_DEBOUNCE	DISABLE_U2U3_RXDET	DFP_RXDET_INTERVAL		USB3_COMPLIANCE_CTRL	
R/U	R/W	R/W	R/W	R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-9. USB3.1 Control/Status Registers (0x22)

Bit	Field	Type	Reset	Description
7	CM_ACTIVE	R/U	0	0: Device not in USB 3.1 compliance mode. (Default) 1: Device in USB 3.1 compliance mode
6	LFPS_EQ	R/W	0	Controls whether settings of EQ based on EQ1_SEL, EQ2_SEL and SSEQ_SEL applies to received LFPS signal. 0 – EQ set to zero when receiving LFPS (default) 1 – EQ set to EQ1_SEL, EQ2_SEL, and SSEQ_SEL when receiving LFPS.
5	U2U3_LFPS_DEBOUNCE	R/W	0	0: No debounce of LFPS before U2/U3 exit. (Default) 1: 200µs debounce of LFPS before U2/U3 exit.
4	DISABLE_U2U3_RXDET	R/W	0	0: Rx.Detect in U2/U3 enabled. (Default) 1: Rx.Detect in U2/U3 disabled.
3:2	DFP_RXDET_INTERVAL	R/W	00	This field controls the Rx.Detect interval for the Downstream facing port (TX1P/N and TX2P/N). 00: 8ms 01: 12ms (default) 10: Reserved 11: Reserved
1:0	USB3_COMPLIANCE_CTRL	R/W	00	00: FSM determined compliance mode. (Default) 01: Compliance Mode enabled in DFP direction (SSTX -> TX1/TX2) 10: Compliance Mode enabled in UFP direction (RX1/RX2 -> SSRX) 11: Compliance Mode Disabled.

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

DisplayPort™ is a trademark of Video Electronics Standards Association.
TI E2E™ is a trademark of Texas Instruments.
USB Type-C® and USB-C® are registered trademarks of USB Implementers Forum.
VESA® is a registered trademark of Video Electronics Standards Association.
All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

Changes from Revision * (May 2024) to Revision A (September 2024)	Page
• Changed data sheet status from: Advanced Information to: Production Data	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TUSB564RGFRQ1	Active	Production	VQFN (RGF) | 40	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	TSB6421
TUSB564RGFRQ1.B	Active	Production	VQFN (RGF) | 40	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	TSB6421
TUSB564RGFTQ1	Active	Production	VQFN (RGF) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	TSB6421
TUSB564RGFTQ1.B	Active	Production	VQFN (RGF) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	TSB6421

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TUSB564-Q1 :

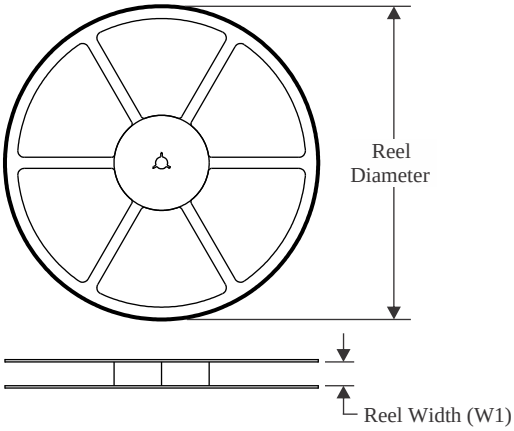
- Catalog : TUSB564

NOTE: Qualified Version Definitions:

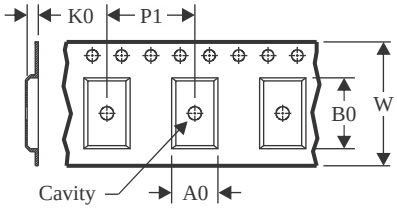
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

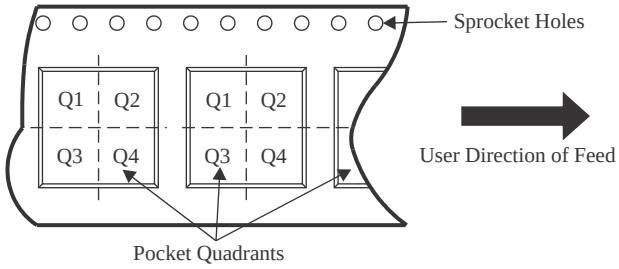


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

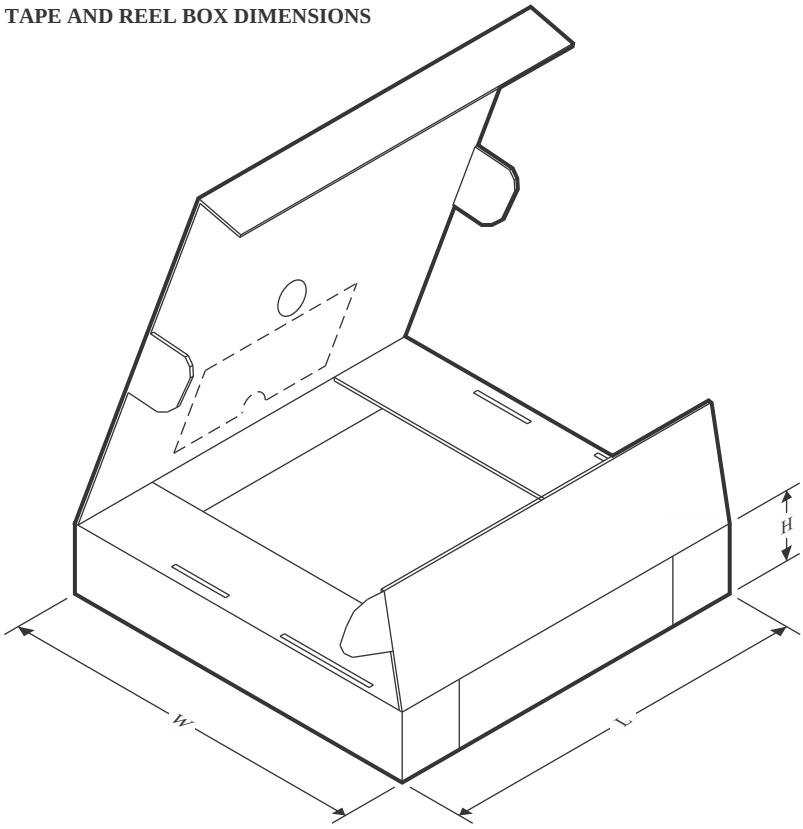
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB564RGFRQ1	VQFN	RGF	40	3000	330.0	16.4	5.25	7.25	1.45	8.0	16.0	Q1
TUSB564RGFTQ1	VQFN	RGF	40	250	180.0	16.4	5.25	7.25	1.45	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB564RGFRQ1	VQFN	RGF	40	3000	367.0	367.0	35.0
TUSB564RGFTQ1	VQFN	RGF	40	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

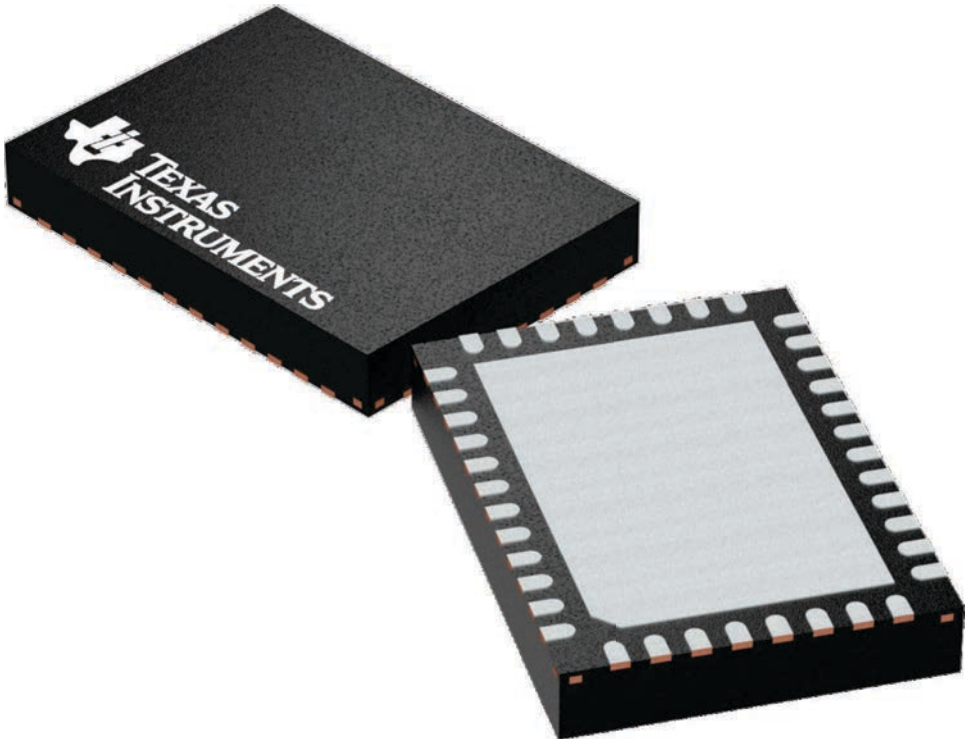
RGF 40

VQFN - 1 mm max height

5 x 7, 0.5 mm pitch

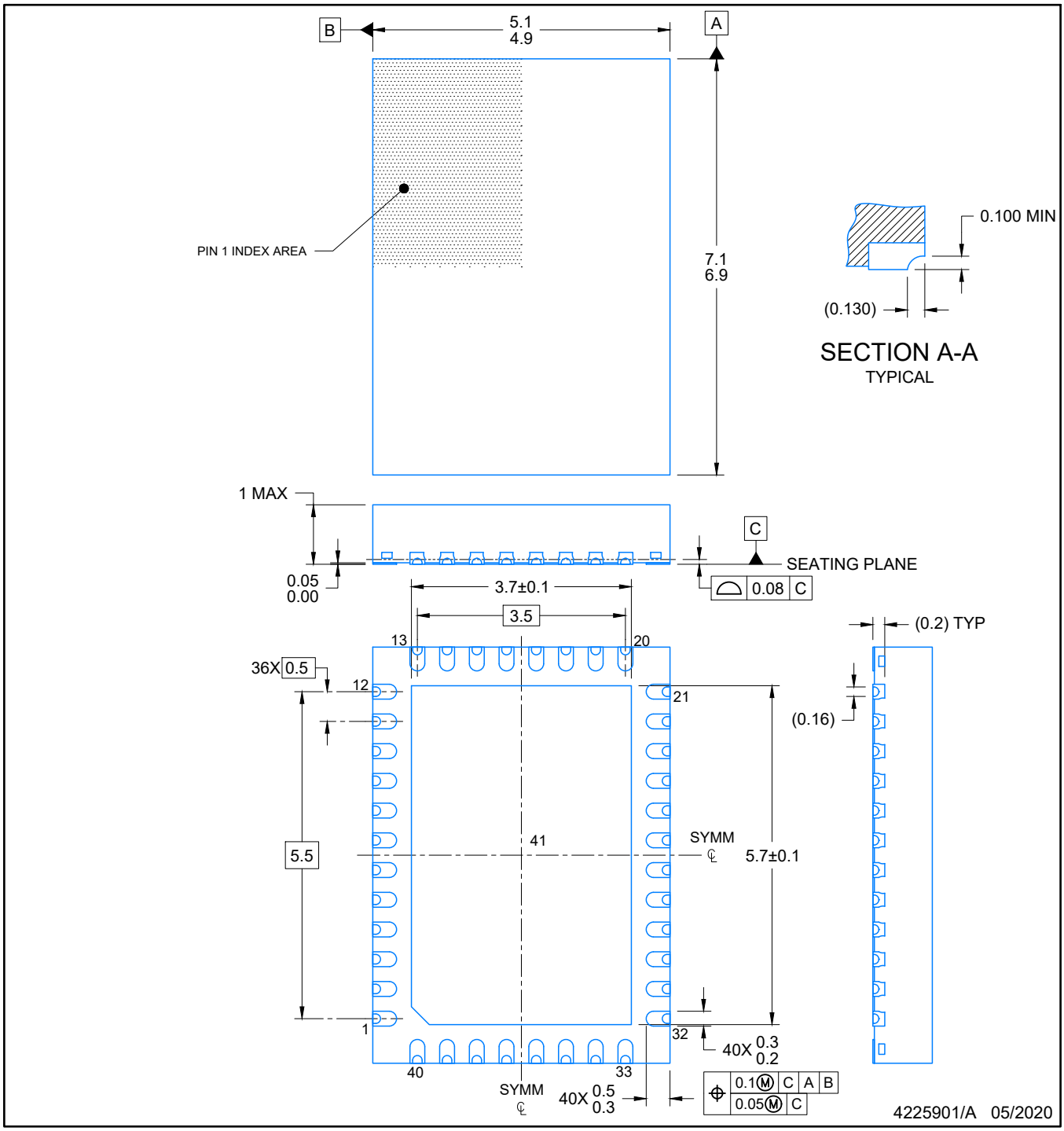
PLASTIC QUAD FLAT PACK- NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



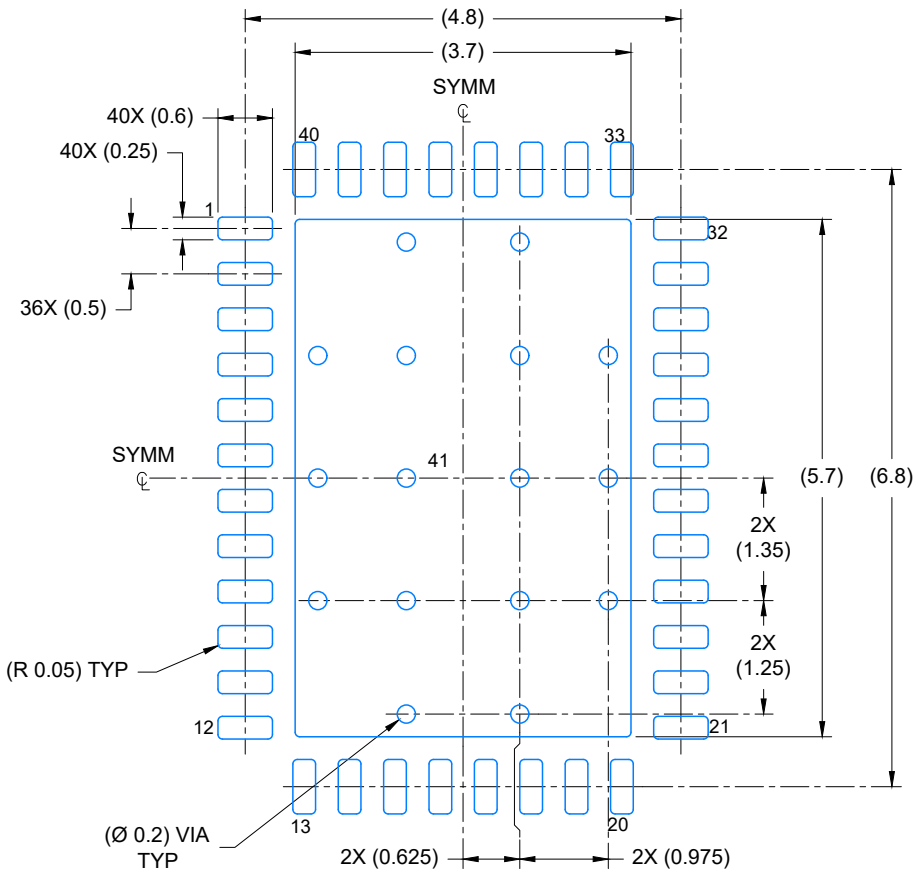
4225115/A

PLASTIC QUAD FLATPACK- NO LEAD

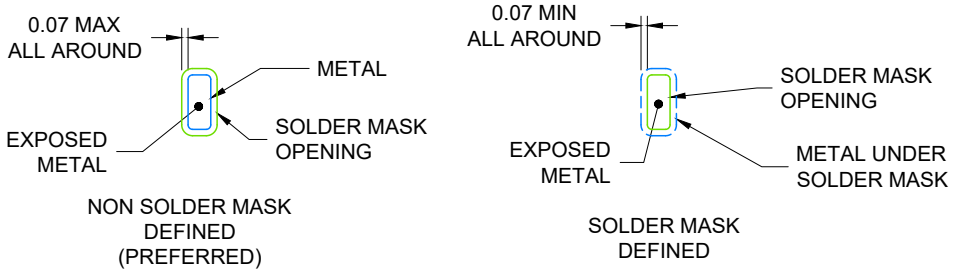


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

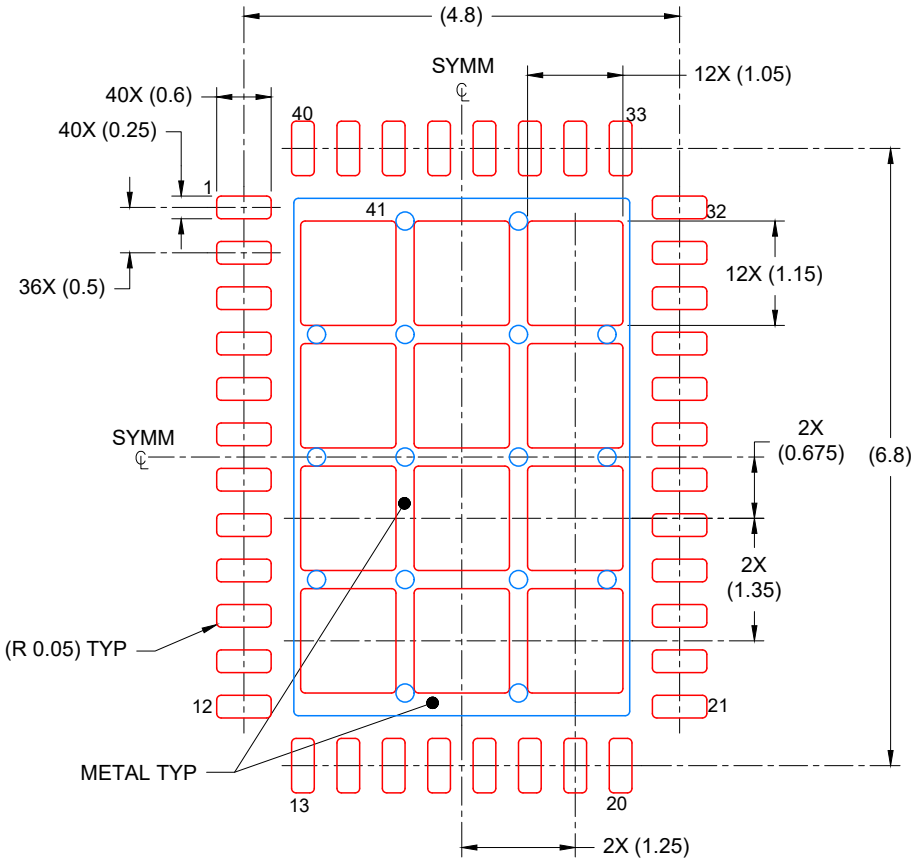


SOLDER MASK DETAILS

4225901/A 05/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
69% PRINTED COVERAGE BY AREA
SCALE: 12X

4225901/A 05/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265