TEXAS INSTRUMENTS

TUSB501-Q1

SLLSET3 – MAY 2016

TUSB501-Q1 USB 3.0 Single-Channel Redriver with Equalization

1 Features

- Q100 Automotive Qualified
- Aggressive Low-Power Architecture (Typical):
  - 126 mW Active Power
  - 20 mW in U2/U3
  - 4 mW with No Connection
- Automatic LFPS DE Control
- Excellent Jitter and Loss Compensation
  - 32 inches of FR4 4 mil Stripline
  - 3 m of 30 AWG cable
- Integrated Termination
- Small 2 x 2 mm QFN Package
- Selectable Receiver Equalization, Transmitter De-Emphasis and Output Swing
- Hot-Plug Capable
- ESD Protection ±5 kV HBM and 1500 V CDM

2 Applications

- Cell Phones
- Computers
- Docking Stations
- TVs
- Active Cables
- Backplanes

3 Description

The TUSB501-Q1 is a 3rd generation 3.3-V USB 3.0 single-channel redriver. When 5 Gbps SuperSpeed USB signals travel across a PCB or cable, signal integrity degrades due to loss and inter-symbol interference. The TUSB501-Q1 recovers incoming data by applying equalization that compensates channel loss, and drives out signals with a high differential voltage. This extends the possible channel length, and enables systems to pass USB 3.0 compliance. The TUSB501-Q1 advanced state machine makes it transparent to hosts and devices.

After power up, the TUSB501-Q1 periodically performs receiver detection on the TX pair. If it detects a SuperSpeed USB receiver, RX termination becomes enabled, and the TUSB501-Q1 is ready to redrive.

The receiver equalizer has three gain settings that are controlled by pin EQ: 3 dB, 6 dB, and 9 dB. This should be set based on amount of loss before the TUSB501-Q1. Likewise, the output driver supports configuration of De-Emphasis and Output Swing (pins DE and OS). These settings allow the TUSB501-Q1 to be flexibly placed in the SuperSpeed USB path, with optimal performance.

Over previous generations, the TUSB501-Q1 features reduced power in all link states, a stronger OS option, improved receiver equalization settings, and an intelligent LFPS Controller. This controller senses the low frequency signals and automatically disables driver de-emphasis, for full USB 3.0 compliance.
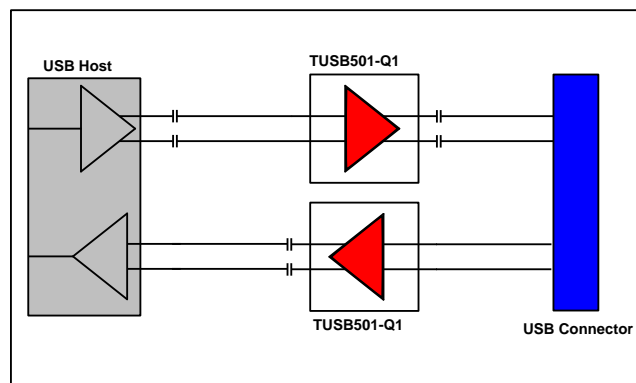
The TUSB501-Q1 is packaged in a small 2 x 2 mm QFN, and operates through an industrial temperature range of –40°C to 105°C.

Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSB501-Q1	WSON	2.00 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simple Application

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Table of Contents

4 Revision History

DATE	REVISION	NOTES
April 2016	*	Initial release.

Product Folder Links: *TUSB501-Q1*

5 Device Comparison Table

USB3.0 Re-drivers (5 Gbps)				
FEATURE	TUSB501-Q1	TUSB551	SN65LVPE502A	SN65LVPE512
Package	8 Pin WSON	12 Pin X2QFN	24 Pin VQFN	24 Pin WQFN
Package Size	2 mm x 2 mm	1.6 mm x 1.6 mm	3 mm x 3 mm, 4 mm x 4 mm	3 mm x 3 mm
Package Pitch	0.5 mm	0.4 mm	0.4 mm, 0.5 mm	0.4 mm
Channels	1	1	2	2
Active Power (Typical)	126 mW	< 130 mW	315 mW	315 mW
U2/U3	20 mW	< 22 mW	70 mW	70 mW
Low Power	4 mW (NC)	< 8 mW (NC)	3.6 µW (Sleep)	3.6 µW (Sleep)
EQ Settings (dB)	3, 6, 9	3, 6, 9	0, 7, 15	0, 7, 15
ESD Protection	5 kV HBM	2 kV HBM	5 kV HBM	5 kV HBM
Power Supply	3.3 VDC	1.8 VDC	3.3 VDC	3.3 VDC

6 Pin Configuration and Functions

DRF Package
8-Pin (WSON)
(Top View)
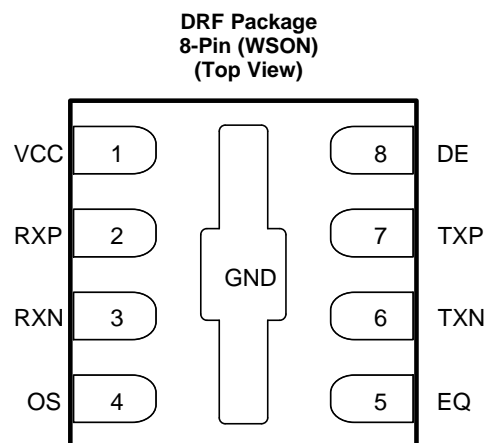
Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
RXP	2	Differential I/O	Differential input pair for 5 Gbps SuperSpeed USB signals.
RXN	3		
TXN	6		Differential output pair for 5 Gbps SuperSpeed USB signals.
TXP	7		
EQ	5	CMOS Input	Sets the receiver equalizer gain. 3-state input with integrated pull-up and pull-down resistors.
DE	8		Sets the output de-emphasis gain. 3-state input with integrated pull-up and pull-down resistors.
OS	4		Sets the output swing (differential voltage amplitude). 2-state input with an integrated pull-down resistor.
VCC	1	Power	3.3-V power supply
GND	Thermal Pad		Reference ground

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

		MIN	MAX	UNIT
Supply voltage range [2]	V_{CC}	−0.5	4	V
Voltage range at any input or output terminal	Differential I/O	−0.5	4	V
	CMOS inputs	−0.5	V_{CC} + 0.5	V
Storage temperature, T_{STG}		−65	150	°C
Maximum junction temperature, T_J		-40	125	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND terminals.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±5000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Main power supply	3	3.3	3.6	V
T_A	Operating free-air temperature	−40		105	°C
C_{AC}	AC coupling capacitor	75	100	200	nF

7.4 Thermal Information

THERMAL METRIC[1]		TUSB501-Q1	UNITS
		DRF (WSON)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	47.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	70.9	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	51.8	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

7.5 Power Supply Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX[2]	UNIT
$I_{CC\text{-}ACTIVE}$	Average active current	Link in U0 with SuperSpeed USB data transmission, OS = Low		38.1		mA
		Link in U0 with SuperSpeed USB data transmission, OS = High		43.8	65	
$I_{CC\text{-}IDLE}$	Average current in idle state	Link has some activity, not in U0, OS = Low		29.8		mA
$I_{CC\text{-}U2U3}$	Average current in U2/U3	Link in U2 or U3		6.1		mA
$I_{CC\text{-}NC}$	Average current with no connection	No SuperSpeed USB device is connected to TXP, TXN		1.3		mA
P_D	Power Dissipation in U0	OS = Low		126		mW
		OS = High		145	234	

(1)   TYP values use V_{CC} = 3.3 V, T_A = 25°C.
(2)   MAX values use V_{CC} = 3.6 V, T_A = –40°C.

7.6 DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
3-State CMOS Inputs (EQ, DE)						
V_{IH}	High-level input voltage		2.8			V
V_{IM}	Mid-level input voltage			V_{CC} / 2		V
V_{IL}	Low-level input voltage				0.6	V
V_F	Floating voltage	V_{IN} = High impedance		V_{CC} / 2		V
R_{PU}	Internal pull-up resistance			190		kΩ
R_{PD}	Internal pull-down resistance			190		kΩ
I_{IH}	High-level input current	V_{IN} = 3.6 V			36	µA
I_{IL}	Low-level input current	V_{IN} = GND, V_{CC} = 3.6 V	-36			µA
2-State CMOS Input (OS)						
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.5	V
V_F	Floating voltage	V_{IN} = High impedance		GND		V
R_{PD}	Internal pull-down resistance			270		kΩ
I_{IH}	High-level input current	V_{IN} = 3.6 V			26	µA
I_{IL}	Low-level input current	V_{IN} = GND	-1			µA

7.7 AC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Differential Receiver (RXP, RXN)						
$V_{DIFF-pp}$	Input differential voltage swing	AC-coupled differential peak-to-peak signal	100		1200	mV_{pp}
V_{CM-RX}	Common-mode voltage bias in the receiver (DC)			3.3		V
$Z_{RX-DIFF}$	Differential input impedance (DC)	Present after a SuperSpeed USB device is detected on TXP/TXN	72	91	120	Ω
Z_{RX-CM}	Common-mode input impedance (DC)	Present after a SuperSpeed USB device is detected on TXP, TXN	18	22.8	30	Ω
$Z_{RX-HIGH-IMP-DC-POS}$	Common-mode input impedance with termination disabled (DC)	Present when no SuperSpeed USB device is detected on TXP, TXN. Measured over the range of 0-500 mV with respect to GND.	25	35		kΩ
$V_{RX-LFPS-DET-DIFF-pp}$	Low Frequency Periodic Signaling (LFPS) Detect Threshold	Below the minimum is squelched	100		300	mV_{pp}
Differential Transmitter (TXP, TXN)						
$V_{TX-DIFF-PP}$	Transmitter differential voltage swing (transition-bit)	OS = Low, No load		930		mV_{pp}
		OS = High, No load		1300		
$V_{TX-DE-RATIO}$	Transmitter de-emphasis	DE = Floating, OS = Low		-3.5		dB
C_{TX}	TX input capacitance to GND	At 2.5 GHz		1.25		pF
$Z_{TX-DIFF}$	Differential impedance of the driver		75	93	125	Ω
Z_{TX-CM}	Common-mode impedance of the driver	Measured with respect to AC ground over 0-500 mV	18.75		31.25	Ω
I_{TX-SC}	TX short circuit current	TX ± shorted to GND			60	mA
V_{CM-TX}	Common-mode voltage bias in the transmitter (DC)		1.2		2.5	V
$V_{CM-TX-AC}$	AC common-mode voltage swing in active mode	Within U0 and within LFPS			100	mV_{pp}
$V_{TX-IDLE-DIFF-AC-pp}$	Differential voltage swing during electrical idle	Tested with a high-pass filter	0		10	mV_{pp}
$V_{TX-CM-DeltaU1-U0}$	Absolute delta of DC CM voltage during active and idle states	Restrict the test condition to meet 100 mV			100	mV
$V_{TX-idle-diff-DC}$	DC electrical idle differential output voltage	Voltage must be low pass filtered to remove any AC component	0		12	mV
Differential Transmitter (TXP, TXN)						
t_R, t_F	Output rise, fall time see Figure 6	20%-80% of differential voltage measured 1 inch from the output pin		80		ps
t_{RF-MM}	Output Rise, Fall time mismatch	20%-80% of differential voltage measured 1 inch from the output pin			20	ps
$t_{diff-LH}, t_{diff-HL}$	Differential propagation delay see Figure 4	De-emphasis = -3.5 dB propagation delay between 50% level at input and output		290		ps
$t_{idleEntry}, t_{idleExit}$	Idle entry and exit times see Figure 5			3.6		ns

Product Folder Links: *TUSB501-Q1*

AC Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Timing						
t_{READY}	Time from power applied until RX termination	Apply 0 V to VCC, connect SuperSpeed USB termination to TX±, apply 3.3 V to VCC, and measure when $Z_{RX-DIFF}$ is enabled.		9		ms
Jitter						
$T_{JTX-EYE}$	Total jitter [1] [2]	EQ = Floating, OS = High, DE = High See Figure 3.		0.213		UI [3]
D_{JTX}	Deterministic jitter [2]			0.197		UI [3]
R_{JTX}	Random jitter [2] [4]			0.016		UI [3]

(1)   Includes R_J at 10^{-12}.
(2)   Measured at the ends of reference channel in Figure 3 with K28.5 pattern, V_{ID} = 1000 mV_{pp}, 5 Gbps, -3.5 dB de-emphasis from source.
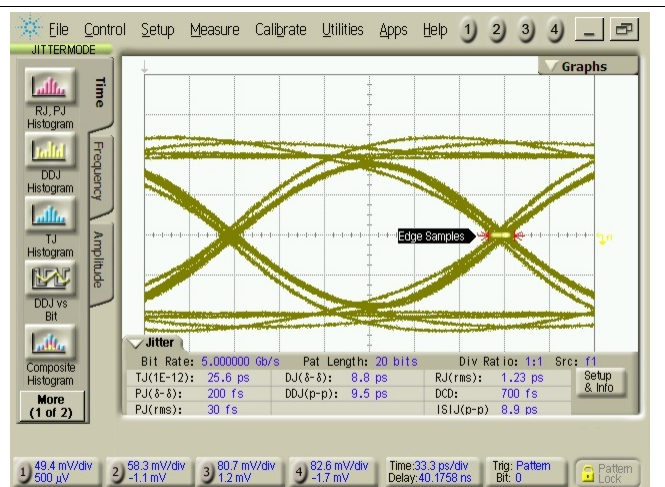(3)   UI = 200 ps.
(4) R_j calculated as 14.069 times the RMS random jitter for 10^{-12} BER.

7.8   Typical Characteristics
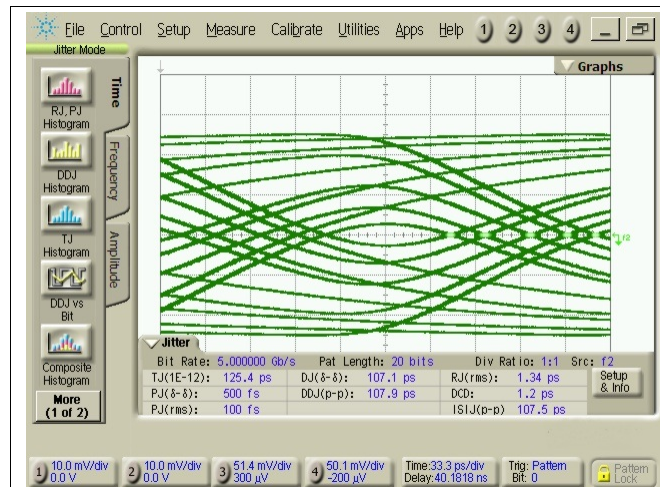
T_A = 25°C

Figure 1. Input for Typical Output Measurement at TUSB501-Q1

T_A = 25°C   DE = HIGH   OS = HIGH
EQ = NC

Figure 2. Typical Output Eye for Jitter Measurement Setup in Figure 3

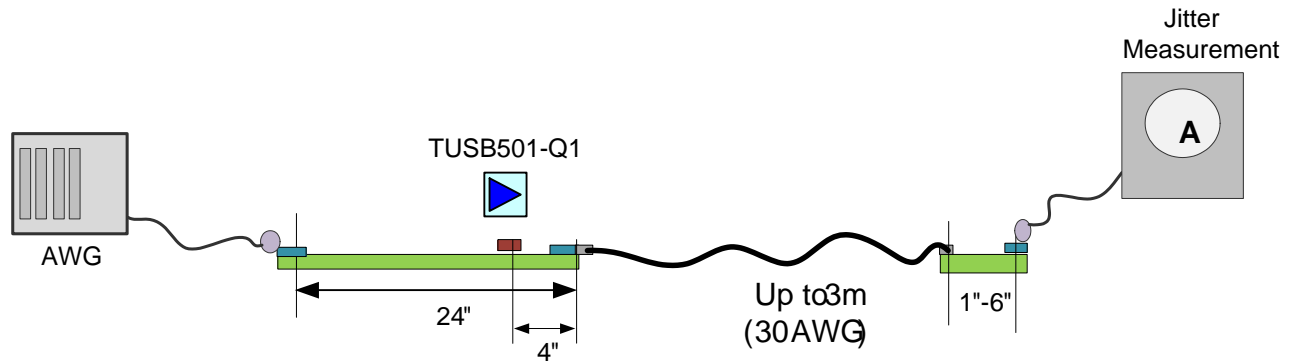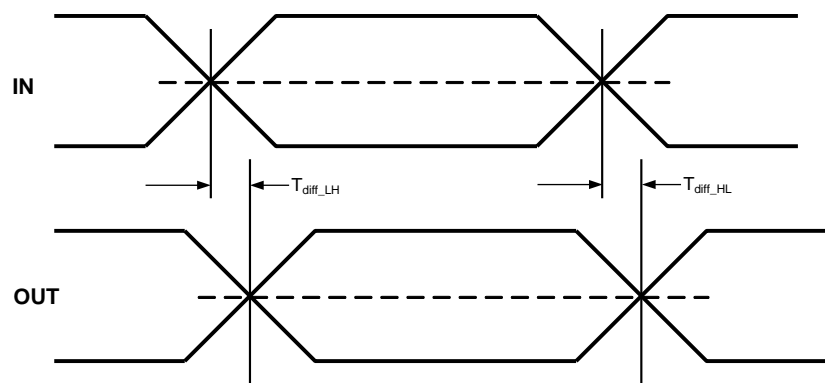# 8 Parameter Measurement Information

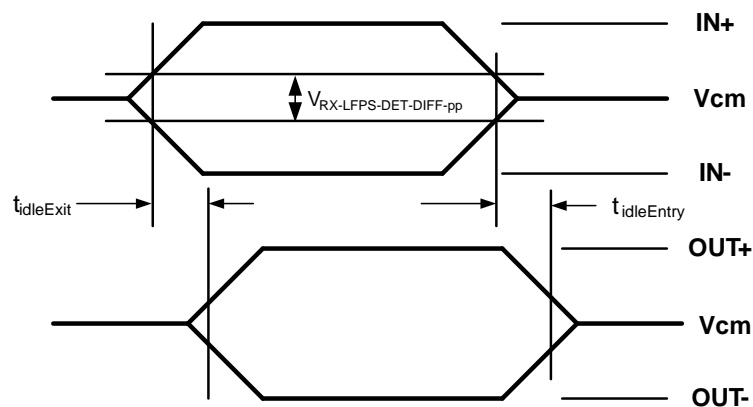**Figure 3. Jitter Measurement Setup**

Figure 4. Propagation Delay

Figure 5. Electrical Idle Mode Exit and Entry Delay

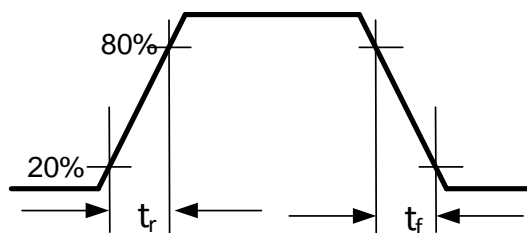## Parameter Measurement Information (continued)

Figure 6. Output Rise and Fall Times

Product Folder Links: *TUSB501-Q1*

9 Detailed Description

9.1 Overview

When 5 Gbps SuperSpeed USB signals travel across a PCB or cable, signal integrity degrades due to loss and inter-symbol interference. The TUSB501-Q1 recovers incoming data by applying equalization that compensates for channel loss, and drives out signals with a high differential voltage. This extends the possible channel length, and enables systems to pass USB 3.0 compliance.

The TUSB501-Q1 advanced state machine makes it transparent to hosts and devices. After power up, the TUSB501-Q1 periodically performs receiver detection on the TX pair. If it detects a SuperSpeed USB receiver, the RX termination is enabled, and the TUSB501-Q1 is ready to re-drive.

The device aggressive Low-Power Architecture operates at a 3.3-V power supply and achieves enhanced performance, as lower as 3 mW with no connection and 126 mW in active state. The receiver equalizer has three gain settings that are controlled by terminal EQ: 3 dB, 6 dB, and 9 dB. The equalization should be set based on amount of insertion loss in the channel before the TUSB501-Q1. Likewise, the output driver supports configuration of De-Emphasis and Output Swing (terminals DE and OS). The automatic LFPS De-Emphasis control further enables the system to be USB3.0 compliant. The TUSB501-Q1 operates over the industrial temperature range of -40ºC to 85ºC in a small 2 x 2 mm WSON package.

**Table 1. Control Pin Effects (Typical Values)**

PIN	DESCRIPTION	LOGIC STATE	GAIN
EQ	Equalization Amount	Low	3 dB
		Floating	6 dB
		High	9 dB

PIN	DESCRIPTION	LOGIC STATE	OUTPUT DIFFERENTIAL VOLTAGE FOR THE TRANSITION BIT
OS	Output Swing Amplitude	Low	930 mV$_{pp}$
		High	1300 mV$_{pp}$

PIN	DESCRIPTION	LOGIC STATE	DE-EMPHASIS RATIO [1]	
			FOR OS = LOW	FOR OS = HIGH
DE	De-Emphasis Amount	Low	0 dB	−2.6 dB
		Floating	−3.5 dB	−5.9 dB
		High	−6.2 dB	−8.3 dB

(1)   Typical values

9.2 Functional Block Diagram
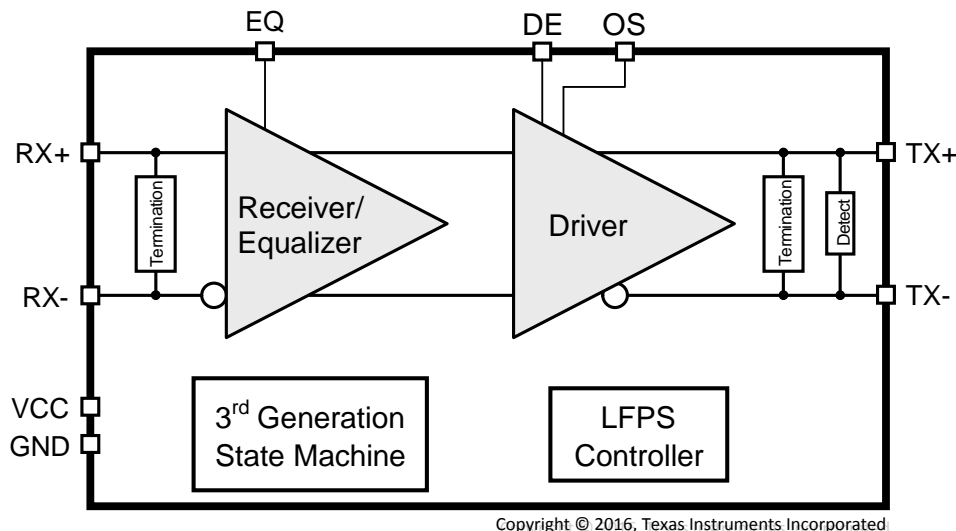
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9.3 Feature Description

9.3.1 Receiver Equalization

The purpose of receiver equalization is to compensate for channel insertion loss and inter-symbol interference in the system before the input of the TUSB501-Q1. The receiver overcomes these losses by attenuating the low frequency components of the signals with respect to the high frequency components. The proper gain setting should be selected to match the channel insertion loss before the input of the TUSB501-Q1.

9.3.2 De-Emphasis Control and Output Swing

The differential driver output provides selectable de-emphasis and output swing control in order to achieve USB3.0 compliance. The TUSB501-Q1 offers a unique way to adjust output de-emphasis and transmitter swing based on the OS and DE terminals. The level of de-emphasis required in the system depends on the channel length after the output of the re-driver.
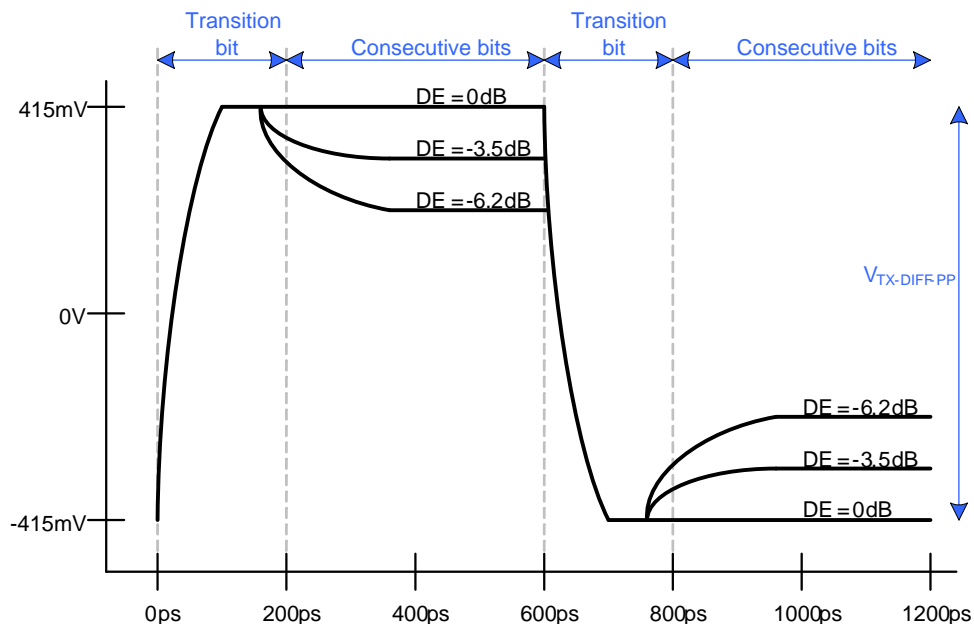

Figure 7. Transmitter Differential Voltage, OS = L

Feature Description (continued)

9.3.3 Automatic LFPS Detection

The TUSB501-Q1 features an intelligent low frequency periodic signaling (LFPS) controller. The controller senses the low frequency signals and automatically disables the driver de-emphasis, for full USB3.0 compliance.

9.3.4 Automatic Power Management

The TUSB501-Q1 deploys RX detect, LFPS signal detection and signal monitoring to implement an automatic power management scheme to provide active, U2/U3 and disconnect modes. The automatic power management is driven by an advanced state machine, which is implemented to manage the device such that the re-driver operates smoothly in the links.

9.4 Device Functional Modes

9.4.1 Disconnect Mode

The Disconnect mode is the lowest power state of the TUSB501-Q1. In this state, the TUSB501-Q1 periodically checks for far-end receiver termination on both TX. Upon detection of the far-end receiver's termination on both ports, the TUSB501-Q1 will transition to U0 mode.

9.4.2 U Modes

9.4.2.1 U0 Mode

The U0 mode is the highest power state of the TUSB501-Q1. Anytime super-speed traffic is being received, theTUSB501-Q1 remains in this mode.

9.4.2.2 U2/U3 Mode

Next to the disconnect mode, the U2/U3 mode is next lowest power state. While in this mode, the TUSB501-Q1 periodically performs far-end receiver detection.

Product Folder Links: *TUSB501-Q1*

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

One example of the TUSB501-Q1 used in a Host application on transmit and receive channels is shown in Figure 8. The re-driver is needed on the transmit path to pass transmitter compliance due to loss between the Host and connector. The re-driver uses the equalization to recover the insertion loss and re-drive the signal with boosted swing down the remaining channel, through the USB3.0 cable, and into the device PCB. Additionally, the TUSB501-Q1 is needed on the receive channel for the Host to pass receiver jitter tolerance. The re-driver recovers the loss from the Device PCB, connector, and USB 3.0 cable and re-drives the signal going into the Host receiver. The equalization, output swing, and de-emphasis settings are dependent upon the type of USB3.0 signal path and end application.

10.2 Typical Application

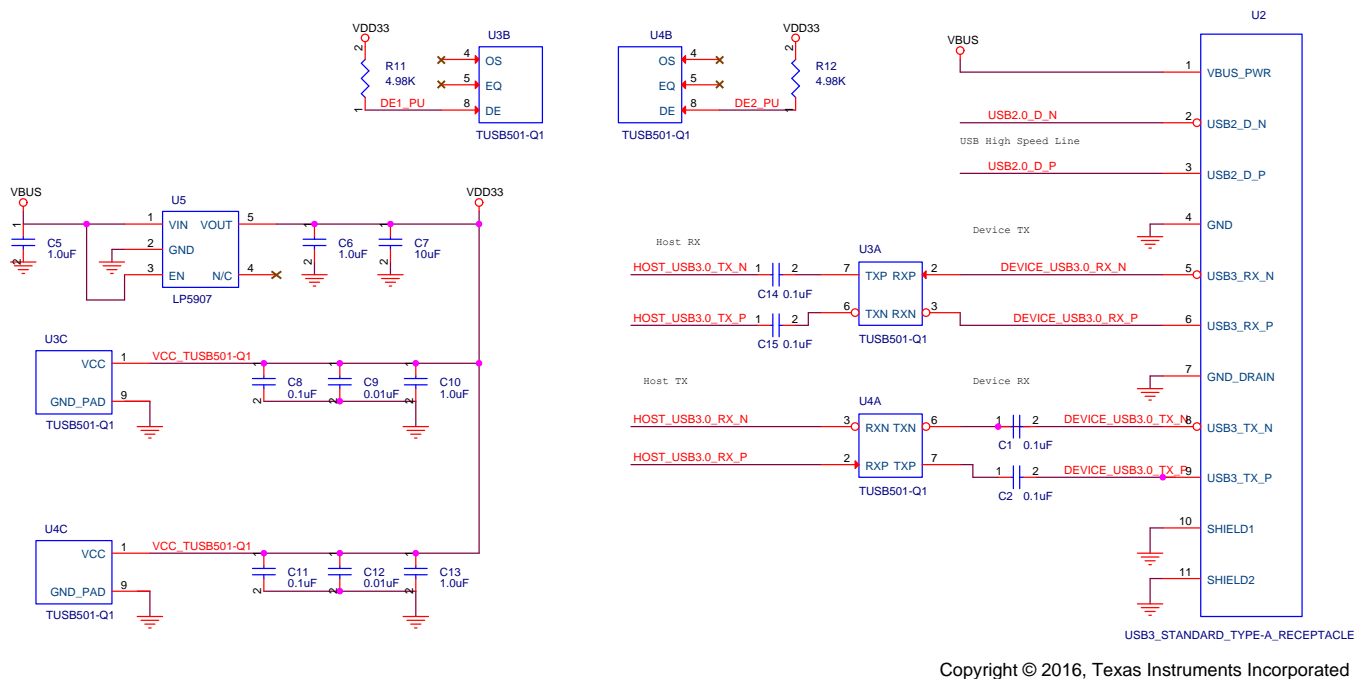Copyright © 2016, Texas Instruments Incorporated

Figure 8. Application Schematic

10.2.1 Design Requirements

For this design example, use the parameter shown in Table 2.

Table 2. Design Parameters

PARAMETER	VALUE
VCC	3.3 V
Supply nominal current	250 mA
Operating free-air temperature	T_A = 25°C
CAC AC coupling capacitor	100 nF
Pull-up resistors	4.98 kΩ

10.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Equalization (EQ) setting
- De-Emphasis (DE) setting
- Output Swing Amplitude (OS) setting

The equalization should be set based on the insertion loss in the pre-channel (channel before the TUSB501-Q1 device). The input voltage to the device is able to have a large range because of the receiver sensitivity and the available EQ settings. The EQ terminal can be pulled high through a resistor to VCC, low through a resistor to ground, or left floating. The application schematic above shows the implementation.

The De-Emphasis setting should be set based on the length and characteristics of the post channel (channel after the TUSB501-Q1 device). Output de-emphasis can be tailored using the DE terminal. This terminal should be pulled high through a resistor to VCC, low through a resistor to ground, or left floating. Figure 8 shows the implementation. The output swing setting can also be configured based on the amplitude needed to pass the compliance test. This setting will also be based on the length of interconnect or cable the TUSB501-Q1 is driving. This terminal should be pulled low through a resistor to ground or left floating. Figure 8 shows the implementation.
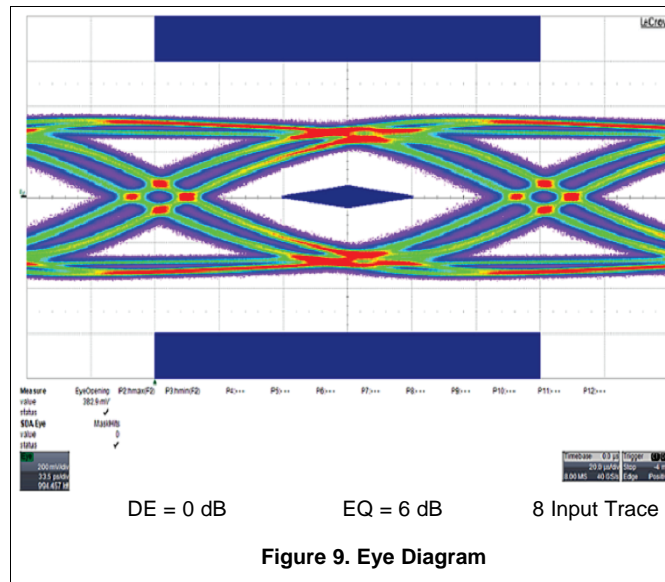
10.2.3 Application Curves

DE = 0 dB	EQ = 6 dB	8 Input Trace

Figure 9. Eye Diagram

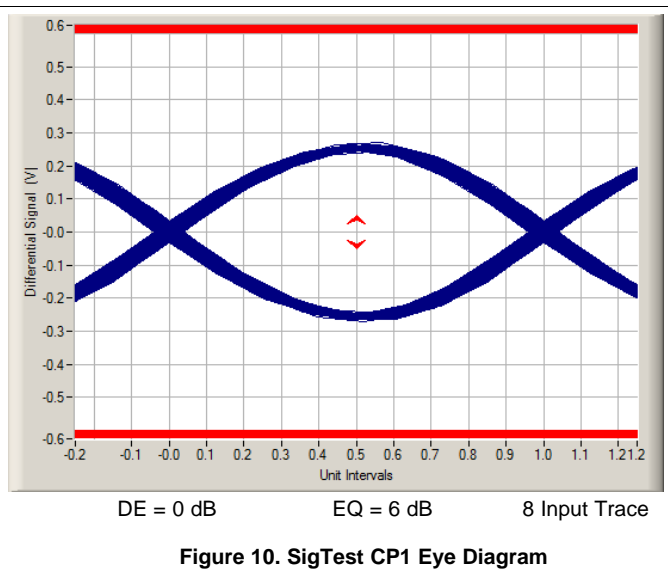| DE = 0 dB	EQ = 6 dB	8 Input Trace

Figure 10. SigTest CP1 Eye Diagram

11 Power Supply Recommendations

This device is designed to operate with a 3.3-V supply. If using a higher voltage system power supply such as VBUS, a voltage regulator can be used to step down to 3.3 V. Decoupling capacitors may be used to reduce noise and improve power supply integrity.

Product Folder Links: *TUSB501-Q1*

12 Layout

12.1 Layout Guidelines

- The 100-nF capacitors on the TXP and SSTXN nets should be placed close to the USB connector (Type A, Type B, and so forth).
- The ESD and EMI protection devices (if used) should also be placed as close as possible to the USB connector.
- Place voltage regulators as far away as possible from the differential pairs.
- In general, the large bulk capacitors associated with each power rail should be placed as close as possible to the voltage regulators.
- It is recommended that small decoupling capacitors for the 1.8-V power rail be placed close to the TUSB501-Q1 as shown in Figure 11.
- The SuperSpeed differential pair traces for RXP/N and TXP/N must be designed with a characteristic impedance of 90 Ω ±10%. The PCB stack-up and materials determines the width and spacing needed for a characteristic impedance of 90 Ω.
- The SuperSpeed differential pair traces should be routed parallel to each other as much as possible. It is recommended the traces be symmetrical.
- In order to minimize cross talk, it is recommended to keep high speed signals away from each other. Each pair should be separated by at least 5 times the signal trace width. Separating with ground also helps minimize cross talk.
- Route all differential pairs on the same layer adjacent to a solid ground plane.
- Do not route differential pairs over any plane split.
- Adding test points will cause impedance discontinuity and will therefore negatively impact signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes stub on the differential pair.
- Avoid 90 degree turns in traces. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135 degrees. This will minimize any length mismatch caused by the bends and therefore minimize the impact bends have on EMI.
- Match the etch lengths of the differential pair traces. There should be less than 5 mils difference between a SS differential pair signal and its complement. The USB 2.0 differential pairs should not exceed 50 mils relative trace length difference.
- The etch lengths of the differential pair groups do not need to match (that is, the length of the RXP/N pair to that of the TXP/N pair), but all trace lengths should be minimized.
- Minimize the use of vias in the differential pair paths as much as possible. If this is not practical, make sure that the same via type and placement are used for both signals in a pair. Any vias used should be placed as close as possible to the TUSB501-Q1 device.
- To ease routing, the polarity of the SS differential pairs can be swapped. This means that TXP can be routed to TXN or RXN can be routed to RXP.
- Do not place power fuses across the differential pair traces.

12.2 Layout Example

Figure 11. Example Layout

13 Device and Documentation Support

13.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TUSB501TDRFRQ1	Active	Production	WSON (DRF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	501Q
TUSB501TDRFRQ1.B	Active	Production	WSON (DRF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	501Q

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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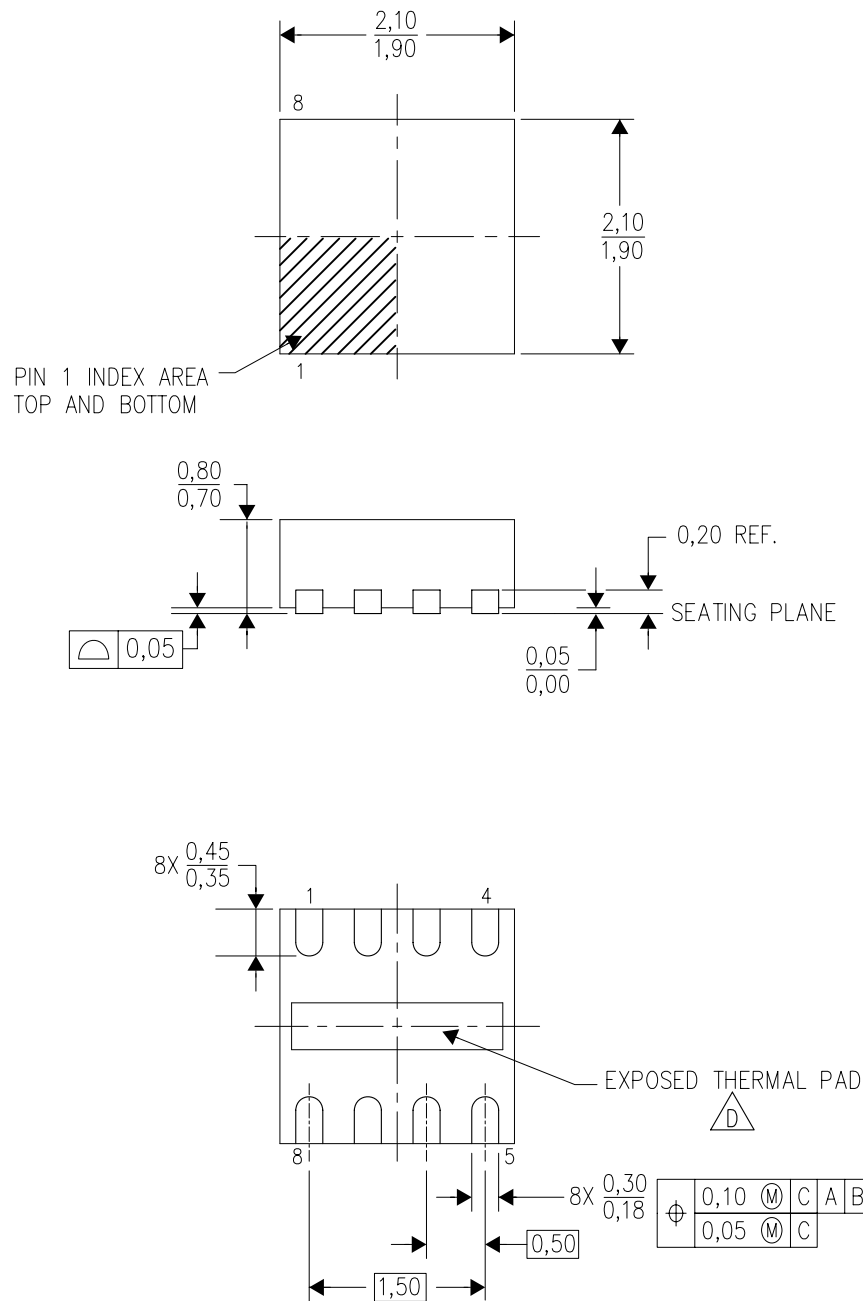
OTHER QUALIFIED VERSIONS OF TUSB501-Q1 :

● Catalog : TUSB501

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

DRF (S−PWSON−N8)   PLASTIC SMALL OUTLINE NO−LEAD

$\frac{2,10}{1,90}$

8

$\frac{2,10}{1,90}$

1

PIN 1 INDEX AREA
TOP AND BOTTOM

$\frac{0,80}{0,70}$

0,20 REF.

SEATING PLANE

$\boxed{\frown} \boxed{0,05}$

$\frac{0,05}{0,00}$

$8X \frac{0,45}{0,35}$

1   4

EXPOSED THERMAL PAD
⚠D

8   5

$8X \frac{0,30}{0,18}$

$\boxed{0,50}$

$\boxed{1,50}$

⊕	0,10 Ⓜ	C	A	B
	0,05 Ⓜ	C		

4205287/E 10/10

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
       B. This drawing is subject to change without notice.
       C. Quad Flatpack, No−Leads (QFN) package configuration.
    ⚠D. The Package thermal pad must be soldered to the board for thermal and mechanical performance.
       See product data sheet for details regarding the exposed thermal pad dimensions.
       E. Falls within JEDEC MO−229.

TEXAS INSTRUMENTS
www.ti.com

DRF (S−PWSON−N8)   PLASTIC SMALL OUTLINE NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.
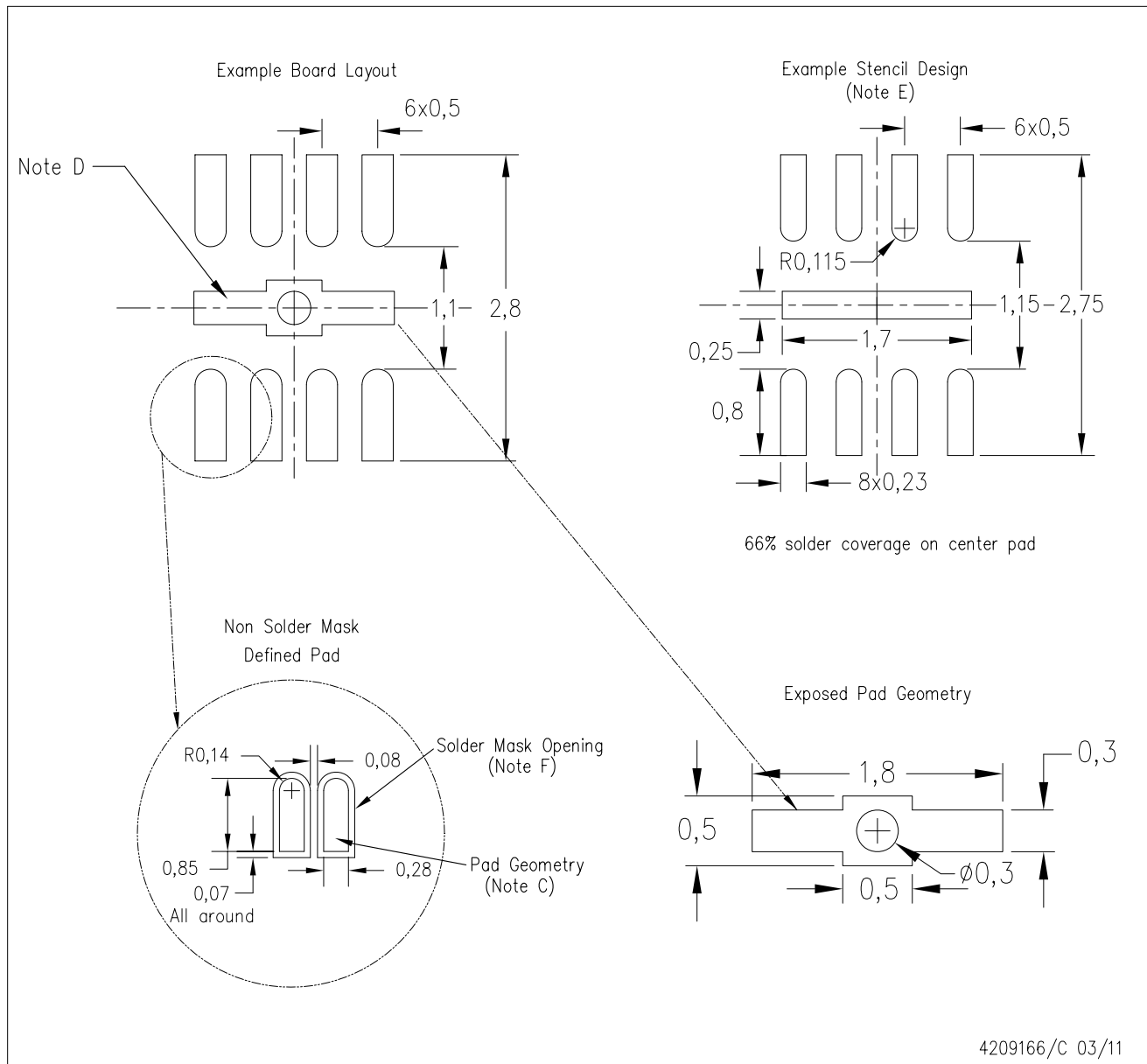

Bottom View

Exposed Thermal Pad Dimensions
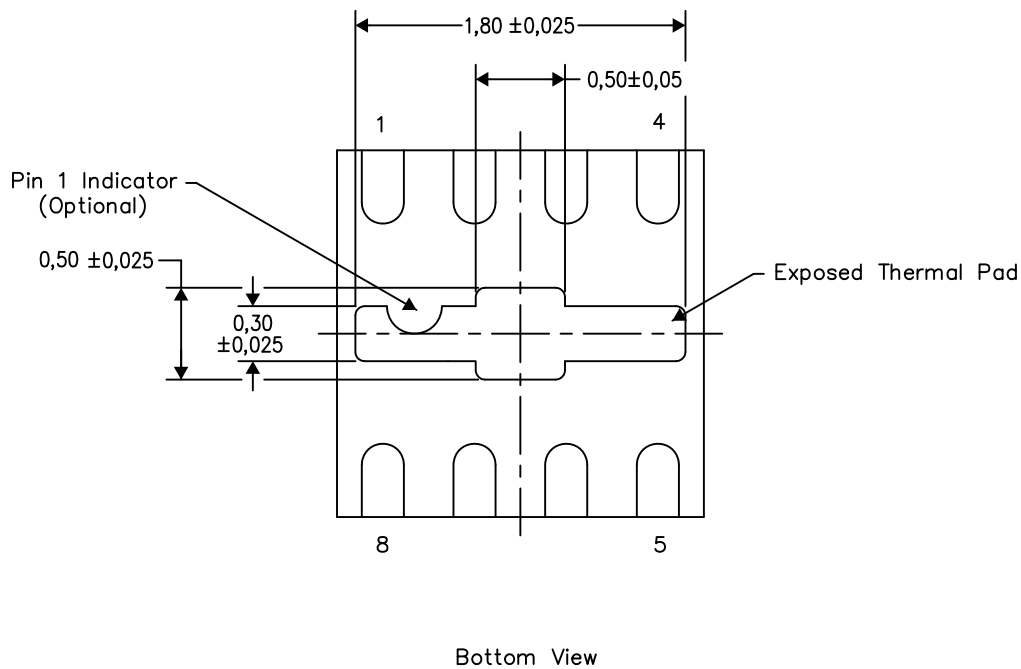
4206840/H 12/14

NOTE: A.   All linear dimensions are in millimeters

DRF (S−PWSON−N8)   PLASTIC SMALL OUTLINE NO−LEAD

Example Board Layout

6x0,5

Note D

1,1−   2,8

Non Solder Mask
Defined Pad

R0,14   0,08   Solder Mask Opening
                              (Note F)

0,85
0,07   0,28   Pad Geometry
All around   (Note C)

Example Stencil Design
(Note E)

6x0,5

R0,115

0,25   1,7   1,15−2,75

0,8

8x0,23

66% solder coverage on center pad

Exposed Pad Geometry

1,8   0,3

0,5   ⊕

0,5   Ø0,3

4209166/C 03/11

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat−Pack
            Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
            for specific thermal information, via requirements, and recommended board layout. These documents are available at
            www.ti.com <http://www.ti.com>.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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