











TS5A3159-Q1

SCDS336C - NOVEMBER 2012-REVISED OCTOBER 2016

TS5A3159-Q1 1- Ω SPDT Analog Switch

Features

- **Qualified for Automotive Applications**
- AEC-Q100 Qualified with the Following Results:
 - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
 - Device HBM ESD Classification Level 2
 - Device CDM ESD Classification Level C4B
- Specified Break-Before-Make Switching
- Low ON-State Resistance (1 Ω)
- Control Inputs are 5-V Tolerant
- Low Charge Injection
- **Excellent ON-Resistance Matching**
- Low Total Harmonic Distortion
- 1.65-V to 5.5-V Single-Supply Operation

Applications

- Automotive Infotainment and Cluster
- Body Electronics and Lighting

3 Description

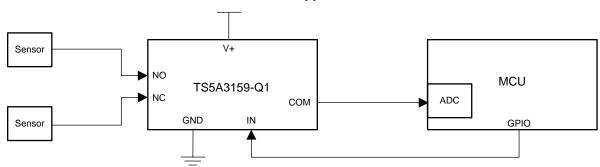
The TS5A3159-Q1 is a single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ONstate resistance and an excellent ON-resistance, matching with the break-before-make feature to prevent signal distortion during the transferring of a signal from one channel to another. The device has an excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)		
TS5A3159-Q1	SOT-23 (6)	2.90 mm × 4.00 mm		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Selector Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

CI	nanges from Revision B (October 2015) to Revision C	age
•	Changed I/O for V ₊ from I to —	4
•	Added V _{NC} to Analog voltage, Analog port diode current, and ON-state switch current	4
•	Added Junction temperature, T _J to <i>Absolute Maximum Ratings</i>	4
•	Changed MIN value for V+ from 1.8 to 1.65 and MAX value from 5 to 5.5	5
•	Changed MAX value for IN from 5 to 5.5	5
•	Changed MAX value for NO, NC, COM from 5 to V+	5
•	Added V _{IL} MAX value 0.6 and deleted TYP value 0.6	7
•	Added Receiving Notification of Documentation Updates section	. 20

Changes from Revision A (December 2012) to Revision B

Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section

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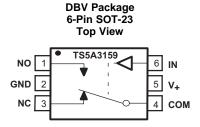
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•	Changed max values for r _{peak} from 2.1 to 2.2	. 6
	Changed max values for r _{on} from 1.5 to 1.8.	
•	Added 25°C to T _A column and added 0.5 max value to I ₊	7
•	Changed r _{peak} max values from 2.7 to 2.9.	. 8
•	Changed r _{on} max values from 2 to 2.3.	. 8
•	Added 25°C to T _A column and added 0.5 max value to I ₊ .	8
•	Changed r _{peak} max values from 4.9 to 5.2.	. 9
•	Changed r _{on} max values from 3.2 to 3.5.	. 9
•	Added 25°C to T _A column and added 0.5 max value to I ₊ .	
•	Changed ON-state resistance from 1.1 to 1.3 Ω .	17
•	Changd leakage current from ±20 nA to ±6 nA.	17

Product Folder Links: TS5A3159-Q1



5 Pin Configuration and Functions



Pin Functions

	PIN	1/0	DESCRIPTION
NO.	NAME	I/O	DESCRIPTION
1	NO	I/O	Normally-open terminal
2	GND	_	Digital ground
3	NC	I/O	Normally-closed terminal
4	COM	I/O	Common terminal
5	V ₊	_	Power supply
6	IN	I	Digital control pin to connect COM terminal to NO or NC terminals

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V ₊	Supply voltage (2)		-0.5	6.5	V
V_{NO}, V_{NC}, V_{COM}	Analog voltage (2)(3)(4)		-0.5	$V_{+} + 0.5$	٧
I _{I/OK}	Analog port diode current	V_{NO} , V_{NC} , $V_{COM} < 0$ or V_{NO} , V_{NC} , $V_{COM} > V_{+}$		±50	mA
I_{NO} , I_{NC} , I_{COM}	ON-state switch current	V_{NO} , V_{NC} , $V_{COM} = 0$ to V_{+}		±200	mA
	ON-state peak switch current (5)			±400	mA
V_{IN}	Digital input voltage range (2)(3)		-0.5	6.5	٧
I _{IK}	Digital input clamp current	V _{IN} < 0		-50	mA
	Continuous current through V ₊ or GND			±100	mA
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) This value is limited to 5.5 V maximum.
- (5) Pulse at 1 ms duration < 10% duty cycle.

6.2 ESD Ratings

				VALUE	UNIT
V _(ESD) Elec		Human body model (HBM), per AEC Q100	±2000		
	Electrostatic discharge	Charged device model (CDM), per AEC	Corner pins (NO, NC, IN, and COM)	±750	V
		Q100-011	Other pins	±500	

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(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V+	1.65	5.5	V
IN	0	5.5	V
NO, NC, COM	0	V+	V

6.4 Thermal Information

		TS5A3159-Q1	
	THERMAL METRIC ⁽¹⁾	DBV (SOT-23)	UNIT
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	192.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	133.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.6	°C/W
ΨЈТ	Junction-to-top characterization parameter	38.9	°C/W
ΨЈВ	Junction-to-board characterization parameter	37.1	°C/W
R _θ JC(bot)	Junction-to-case (bottom) thermal resistance	N/A	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics for 5-V Supply

 $V_{+} = 4.5 \text{ V}$ to 5.5 V and $T_{A} = -40 ^{\circ}\text{C}$ to +125 $^{\circ}\text{C}$ (unless otherwise noted)

	PARAMETER	TEST CONDI	TIONS	TA	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
ANALOG	SWITCH								
V _{COM} , V _{NO} ,V _{NC}	Analog signal range					0		V ₊	٧
	Peak ON resistance	$0 \le V_{NO} \text{ or } V_{NC} \le V_+,$	Switch ON,	25°C	4.5 V		1	1.5	Ω
r _{peak}	reak ON resistance	$I_{COM} = -30 \text{ mA}$	See Figure 11	Full	4.5 V			1.5	12
_	ON-state resistance	V_{NO} or $V_{NC} = 2.5 \text{ V}$,	Switch ON,	25°C	4.5 V		0.75	1.3	Ω
r _{on}	ON-state resistance	$I_{COM} = -30 \text{ mA}$	See Figure 10	Full	4.5 V			1.3	12
Δr_{on}	ON-state resistance match between channels	V_{NO} or $V_{NC} = 2.5 \text{ V}$, $I_{COM} = -30 \text{ mA}$	Switch ON, See Figure 10	25°C	4.5 V		0.1		Ω
	011	$0 \le V_{NO} \text{ or } V_{NC} \le V_+,$ $I_{COM} = -30 \text{ mA}$	Switch ON,	25°C	- 4.5 V		0.233		Ω
r _{on(flat)}	ON-state resistance flatness	V_{NO} or V_{NC} = 1 V, 1.5 V, 2.5 V, I_{COM} = -30 mA		25°C			0.15		
I _{NC(OFF)} ,	NC, NO	V_{NC} or $V_{NO} = 4.5 \text{ V}$,	Switch OFF,	25°C	E E V	-6	0.2	6	nA
I _{NO(OFF)}	OFF leakage current	$V_{COM} = 0$	See Figure 12	Full	5.5 V	-150		150	ΠA
I _{NC(ON)} ,	NC, NO	V_{NC} or $V_{NO} = 4.5 \text{ V}$,	Switch ON,	25°C	5 5 V	-6	2.8	6	Λ
I _{NO(ON)}	ON leakage current	VCOM = Open	See Figure 13	Full	5.5 V	-150		150	nA
	COM	V_{NC} or $V_{NO} = 4.5 \text{ V or Open}$,	Switch ON.	25°C	5.5.7	-8	0.47	8	
I _{COM(ON)}	ON leakage current	V _{COM} = 4.5 V	See Figure 13	Full	5.5 V	-150		150	nA
DIGITAL I	NPUTS (IN)	-	•	*	•	•			
V _{IH}	Input logic high			Full		2.4		5.5	V
V _{IL}	Input logic low			Full		0		0.8	V
I _{IH} , I _{IL}	Input leakage current	V _{IN} = 5.5 V or 0		Full	5.5 V	-1		1	μΑ

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(1) $T_A = 25^{\circ}C$



Electrical Characteristics for 5-V Supply (continued)

 $V_{+} = 4.5 \text{ V to } 5.5 \text{ V and } T_{A} = -40^{\circ}\text{C to } +125^{\circ}\text{C} \text{ (unless otherwise noted)}$

	PARAMETER	TEST CON	IDITIONS	TA	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
DYNAMIC		1		•					
	Turn on time	$V_{COM} = V_+,$	C _L = 35 pF,	25°C	4.5 V to		20	35	
t _{ON}	Turn-on time	$R_L = 50 \Omega$,	See Figure 15	Full	5.5 V			40	ns
•	Turn-off time	$V_{COM} = V_+,$	$C_L = 35 \text{ pF},$	25°C	4.5 V to		15	20	ns
t _{OFF}	rum-on ume	$R_L = 50 \Omega$,	See Figure 15	Full	5.5 V			35	115
+	Break-before-make time	$V_{NC} = V_{NO} = V_{+} / 2,$	$C_L = 35 \text{ pF},$	25°C	4.5 V to	1	12	14.5	ns
t _{BBM}	break-before-make time	$R_L = 50 \Omega$,	See Figure 16	Full	5.5 V	1			115
Q_{C}	Charge injection	$C_L = 1 \text{ nF}, V_{GEN} = 0 \text{ V},$	See Figure 19	25°C	5 V		36		рC
$\begin{array}{l} C_{NC(OFF)}, \\ C_{NO(OFF)} \end{array}$	NC, NO OFF capacitance	V_{NC} or $V_{NO} = V_{+}$ or GND, Switch OFF,	See Figure 13	25°C	5 V		23		pF
C _{NC(ON)} , C _{NO(ON)}	NC, NO ON capacitance	V_{NC} or $V_{NO} = V_{+}$ or GND, Switch ON,	See Figure 13	25°C	5 V		84		pF
C _{COM(ON)}	COM ON capacitance	V _{COM} = V ₊ or GND, Switch ON,	See Figure 13	25°C	5 V		84		pF
C _{IN}	Digital input capacitance	$V_{IN} = V_{+} \text{ or GND},$	See Figure 13	25°C	5 V		2.1		pF
BW	Bandwidth	$R_L = 50 \Omega$, Switch ON,	See Figure 16	25°C	5 V		100		MHz
O _{ISO}	OFF isolation	$R_L = 50 \Omega$, $f = 1 MHz$,	Switch OFF, See Figure 17	25°C	5 V		-65		dB
X _{TALK}	Crosstalk	$R_L = 50 \Omega$, $f = 1 MHz$,	Switch ON, See Figure 18	25°C	5 V		-65		dB
THD	Total harmonic distortion	$R_L = 600 \Omega,$ $C_L = 50 \text{ pF},$	f = 600 Hz to 20 kHz, See Figure 19	25°C	5 V		0.01%		
SUPPLY									
	Docitive eventy everent	V V or CND	Switch ON or OFF	25°C	5.5 V			0.1	
I ₊	Positive supply current	$V_{IN} = V_+ \text{ or GND},$	Switch ON or OFF	Full	5.5 V			0.5	μA

6.6 Electrical Characteristics for 3.3-V Supply

 $V_{+} = 3 \text{ V}$ to 3.6 V and $T_{A} = -40^{\circ}\text{C}$ to +125°C (unless otherwise noted)

	PARAMETER	TEST CON	DITIONS	T _A	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
ANALOG	SWITCH								
V_{COM} , V_{NO} , V_{NC}	Analog signal range					0		V ₊	V
	Peak ON-state resistance	$0 \le V_{NO} \text{ or } V_{NC} \le V+,$	Switch ON,	25°C	3 V		1.35	2.2	Ω
r _{peak}	Feak ON-State resistance	$I_{COM} = -24 \text{ mA},$	See Figure 10	Full	3 V			2.2	12
_	ON-state resistance V_{NO} or $V_{NC} = 2 \text{ V}$, Switch ON,	25°C	3 V		1.15	1.8	Ω		
r _{on}	ON-State resistance	$I_{COM} = -24 \text{ mA},$	See Figure 10	Full	3 V			1.8	12
Δr_{on}	ON-state resistance match between channels	V_{NO} or $V_{NC} = 2 \text{ V}$, 0.8 V, $I_{COM} = -24 \text{ mA}$,	Switch ON, See Figure 10	25°C	3 V		0.11		Ω
		$0 \le V_{NO} \text{ or } V_{NC} \le V+,$ $I_{COM} = -24 \text{ mA},$	Switch ON.	25°C			0.225		Ω
r _{on(flat)}	ON-state resistance flatness	V_{NO} or $V_{NC} = 2 \text{ V}$, 0.8 V, $I_{COM} = -24 \text{ mA}$,	See Figure 10	25°C	3 V		0.25		
I _{NC(OFF)} , I _{NO(OFF)}	NC, NO OFF leakage current	V_{NC} or $V_{NO} = 3 V$, $V_{COM} = 0$,	Switch OFF, See Figure 11	25°C	3.6 V		0.2		nA
I _{NC(ON)} , I _{NO(ON)}	NC, NO ON leakage current	V_{NC} or $V_{NO} = 3 V$, $V_{COM} = Open$,	Switch ON, See Figure 12	25°C	3.6 V		2.8		nA
I _{COM(ON)}	COM ON leakage current	V_{NC} or $V_{NO} = 3 \text{ V}$ or Open, $V_{COM} = 3 \text{ V}$,	Switch ON, See Figure 12	25°C	3.6 V		0.47		nA

(1) $T_A = 25^{\circ}C$

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Electrical Characteristics for 3.3-V Supply (continued)

 $V_{+} = 3 \text{ V to } 3.6 \text{ V and } T_{A} = -40^{\circ}\text{C to } +125^{\circ}\text{C (unless otherwise noted)}$

	PARAMETER	TEST CONDITIONS			V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
DIGITAL I	NPUTS (IN)			•					
V _{IH}	Input logic high			Full		2		5.5	V
V _{IL}	Input logic low			Full		0		0.6	V
I _{IH} , I _{IL}	Input leakage current	V _{IN} = 5.5 V or 0		Full	3.6 V	-1		1	μA
DYNAMIC	;								
t _{ON}	Turn-on time	$V_{COM} = V_+,$ $R_L = 50 \Omega$	C _L = 35 pF, See Figure 15	25°C Full	3 V to 3.6 V		30	40 55	ns
t _{OFF}	Turn-off time	$V_{COM} = V_+,$	C _L = 35 pF,	25°C	3 V to		20	25	ns
OFF	Turn on time	$R_L = 50 \Omega$	See Figure 15	Full	3.6 V			40	113
t _{BBM}	Break-before-make time	$V_{NC} = V_{NO} = V_{+} / 2,$	$C_L = 35 \text{ pF},$	25°C	3 V to	1	21	29	ns
чви	break before make time	$R_L = 50 \Omega$	See Figure 16	Full	3.6 V	1			113
Q_C	Charge injection	$C_L = 1 \text{ nF}, V_{GEN} = 0 \text{ V}$	See Figure 19	25°C	3.3 V		20		рC
$\begin{matrix} C_{NC(OFF)}, \\ C_{NO(OFF)} \end{matrix}$	NC, NO OFF capacitance	V_{NC} or $V_{NO} = V_{+}$ or GND, Switch OFF	See Figure 13	25°C	3.3 V		23		pF
C _{NC(ON)} , C _{NO(ON)}	NC, NO ON capacitance	V_{NC} or $V_{NO} = V_{+}$ or GND, Switch ON	See Figure 13	25°C	3.3 V		84		pF
C _{COM(ON)}	COM ON capacitance	V _{COM} = V ₊ or GND, Switch ON	See Figure 13	25°C	3.3 V		84		pF
C _{IN}	Digital input capacitance	V _{IN} = V ₊ or GND	See Figure 13	25°C	3.3 V		2.1		pF
BW	Bandwidth	$R_L = 50 \Omega$, Switch ON	See Figure 16	25°C	3.3 V		100		MHz
O _{ISO}	OFF isolation	$R_L = 50 \Omega$, $f = 1 MHz$	Switch OFF, See Figure 17	25°C	3.3 V		- 65		dB
X _{TALK}	Crosstalk	$R_L = 50 \Omega$, $f = 1 MHz$	Switch ON, See Figure 18	25°C	3.3 V		-65		dB
THD	Total harmonic distortion	$R_L = 600 \Omega,$ $C_L = 50 \text{ pF}$	f = 600 Hz to 20 kHz, See Figure 19	25°C	3.3 V		0.015%		
SUPPLY									
I ₊	Positive supply current	V _{IN} = V ₊ or GND	Switch ON or OFF	25°C Full	3.6 V			0.1 0.5	μА

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6.7 Electrical Characteristics For 2.5-V Supply

 $V_{+} = 2.3 \text{ V to } 2.7 \text{ V and } T_{A} = -40^{\circ}\text{C to } +125^{\circ}\text{C} \text{ (unless otherwise noted)}$

	PARAMETER	TEST COND	ITIONS	TA	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
ANALOG	SWITCH				1				
V_{COM} , V_{NO} , V_{NC}	Analog signal range					0		V ₊	V
r _{peak}	Peak ON-state resistance	$0 \le V_{NO}$ or $V_{NC} \le V_+$, $I_{COM} = -8 \text{ mA}$	Switch ON, See Figure 10	25°C Full	2.5 V		1.7	2.9 2.9	Ω
r _{on}	ON-state resistance	V_{NO} or $V_{NC} = 1.8 \text{ V}$, $I_{COM} = -8 \text{ mA}$	Switch ON, See Figure 10	25°C Full	2.5 V		1.45	2.3	Ω
$\Delta r_{\sf on}$	ON-state resistance match between channels	V_{NO} or $V_{NC} = 0.8 \text{ V}$, 1.8 V, $I_{COM} = -8 \text{ mA}$	Switch ON, See Figure 10	25°C	2.5 V		0.7	2.0	Ω
_	ON-state resistance flatness	$0 \le V_{NO} \text{ or } V_{NC} \le V_+,$ $I_{COM} = -8 \text{ mA}$	Switch ON,	25°C	251/		0.5		Ω
r _{on(flat)}	ON-state resistance natness	V_{NO} or V_{NC} = 0.8 V, 1.8 V, I_{COM} = -8 mA	See Figure 10	25°C	2.5 V		0.45		12
$I_{\text{NC(OFF)}},\\I_{\text{NO(OFF)}}$	NC, NO Off leakage current	V_{NC} or $V_{NO} = 2.3 \text{ V}$, $V_{COM} = 0$	Switch OFF, See Figure 11	25°C	2.7 V		0.2		nA
I _{NC(ON)} , I _{NO(ON)}	NC, NO On leakage current	V_{NC} or $V_{NO} = 2.3 \text{ V}$, $V_{COM} = \text{Open}$	Switch ON, See Figure 12	25°C	2.7 V		2.8		nA
I _{COM(ON)}	COM On leakage current	V_{NC} or V_{NO} = 2.3 V or Open, V_{COM} = 2.3 V	Switch ON, See Figure 12	25°C	2.7 V		0.47		nA
DIGITAL II	NPUTS (IN)			Т					
V _{IH}	Input logic high			Full		1.8		5.5	V
V _{IL}	Input logic low			Full		0	0.6		V
I _{IH} , I _{IL}	Input leakage current	$V_{IN} = 5.5 \text{ V or } 0$		Full	2.7 V	-1		1	μA
DYNAMIC				1					ı
t _{ON}	Turn-on time	$V_{COM} = V_+,$ $R_L = 50 \Omega,$	C _L = 35 pF, See Figure 15	25°C Full	2.3 V to 2.7 V		40	55 70	ns
t _{OFF}	Turn-off time	$V_{COM} = V_+,$ $R_L = 50 \Omega,$	C _L = 35 pF, See Figure 15	25°C Full	2.0 7 10		30	40 55	ns
t _{BBM}	Break-before-make time	$V_{NC} = V_{NO} = V_{+} / 2,$ $R_{1} = 50 \Omega,$	C _L = 35 pF, See Figure 16	25°C Full	2.5 V to		33	39	ns
Q _C	Charge injection	$C_L = 1 \text{ nF}, V_{GEN} = 0 \text{ V},$	See Figure 19	25°C	2.5 V	1	13		рС
C _{NC(OFF)} , C _{NO(OFF)}	NC, NO OFF capacitance	V_{NC} or $V_{NO} = V_{+}$ or GND, Switch OFF,	See Figure 14	25°C	2.5 V		23		pF
C _{NC(ON)} , C _{NO(ON)}	NC, NO ON capacitance	V_{NC} or $V_{NO} = V_{+}$ or GND, Switch ON,	See Figure 14	25°C	2.5 V		84		pF
C _{COM(ON)}	COM ON capacitance	V _{COM} = V ₊ or GND, Switch ON,	See Figure 14	25°C	2.5 V		84		pF
C _{IN}	Digital input capacitance	V _{IN} = V ₊ or GND,	See Figure 14	25°C	2.5 V		2.1		pF
BW	Bandwidth	$R_L = 50 \Omega$, Switch ON,	See Figure 16	25°C	2.5 V		100		MHz
O _{ISO}	OFF isolation	$R_L = 50 \Omega$, $f = 1 MHz$,	Switch OFF, See Figure 17	25°C	2.5 V —6-		-64		dB
X _{TALK}	Crosstalk	$ \begin{array}{ll} {\rm R_L = 50~\Omega,} & {\rm Switch~ON,} \\ {\rm f = 1~MHz,} & {\rm See~Figure~18} \end{array} $		25°C	2.5 V		-64		dB
THD	Total harmonic distortion	$R_L = 600 \Omega,$ $C_L = 50 pF,$	f = 600 Hz to 20 kHz, See Figure 19	25°C	2.5 V		0.025%		
SUPPLY									
I ₊	Positive supply current	$V_{IN} = V_{+}$ or GND,	Switch ON or OFF	25°C Full	2.7 V			0.1 0.5	μА

(1) $T_A = 25^{\circ}C$

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6.8 Electrical Characteristics For 1.8-V Supply

 V_{+} = 1.65 V to 1.95 V and T_{A} = -40°C to +125°C (unless otherwise noted

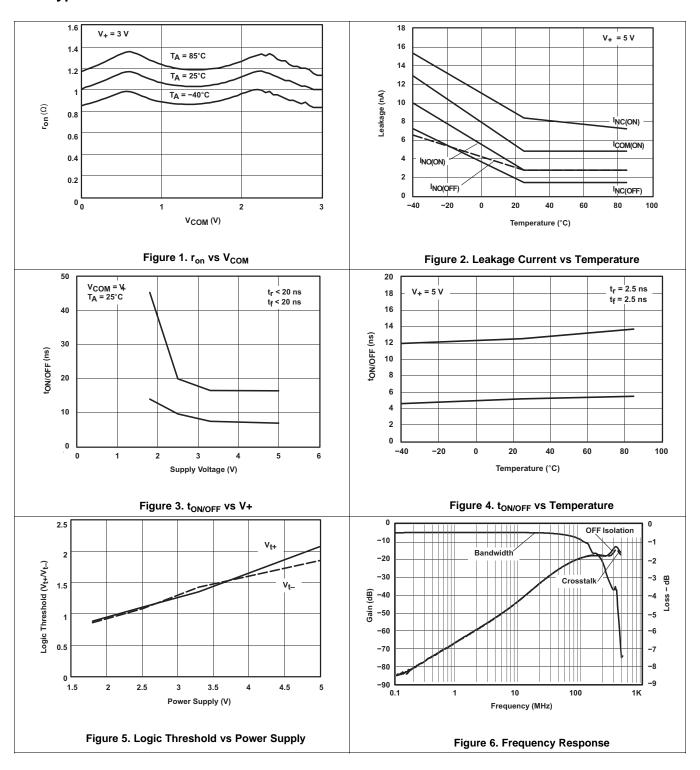
	PARAMETER	TEST COND	TIONS	TA	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
ANALOG S	SWITCH								
V _{COM} , V _{NO} ,V _{NC}	Analog signal range					0		V ₊	V
r _{peak}	Peak ON-state resistance	$0 \le V_{NO}$ or $V_{NC} \le V_+$, $I_{COM} = -2 \text{ mA}$	Switch ON, See Figure 10	25°C Full	1.8 V		4 5.2 5.2		Ω
r _{on}	ON-state resistance	V_{NO} or $V_{NC} = 1.5 \text{ V}$, $I_{COM} = -2 \text{ mA}$	Switch ON, See Figure 10	25°C Full	1.8 V		1.7	3.5 3.5	Ω
Δr_{on}	ON-state resistance match between channels	V_{NO} or $V_{NC} = 0.6 \text{ V}$, 1.5 V, $I_{COM} = -2 \text{ mA}$	Switch ON, See Figure 10	25°C Full	1.8 V		0.7		Ω
		$0 \le V_{NO} \text{ or } V_{NC} \le V_{+},$ $I_{COM} = -2 \text{ mA}$		25°C			1.85		
r _{on(flat)}	ON-state resistance flatness	V_{NO} or $V_{NC} = 0.6 \text{ V}$, 1.5 V, $I_{COM} = -2 \text{ mA}$	Switch ON, See Figure 11	Full 25°C	1.8 V		0.9		Ω
I _{NC(OFF)} , I _{NO(OFF)}	NC, NO Off leakage current	$V_{NC} \text{ or } V_{NO} = 1.65 \text{ V},$ $V_{COM} = 0$	Switch OFF, See Figure 11	Full 25°C	1.95 V		0.9		nA
I _{NC(ON)} , I _{NO(ON)}	NC, NO On leakage current	V_{NC} or $V_{NO} = 1.65 \text{ V}$, $V_{COM} = \text{Open}$	Switch ON, See Figure 12	25°C	1.95 V		2.8		nA
I _{COM(ON)}	COM On leakage current	V_{NC} or V_{NO} = 1.65 V or Open, V_{COM} = 1.65 V	Switch ON, See Figure 12	25°C	1.95 V	0.47		nA	
DIGITAL IN	NPUTS (IN)								
V_{IH}	Input logic high			Full		1.5		5.5	V
V_{IL}	Input logic low			Full		0		0.6	V
$I_{IH},\ I_{IL}$	Input leakage current	V _{IN} = 5.5 V or 0		Full	1.95 V	-1		1	μΑ
DYNAMIC									
t _{ON}	Turn-on time	$V_{COM} = V_+,$ $R_L = 50 \Omega,$	C _L = 35 pF, See Figure 15	25°C Full	1.65 V to 1.95 V		65	70 95	ns
t _{OFF}	Turn-off time	$V_{COM} = V_+,$ $R_L = 50 \Omega,$	C _L = 35 pF, See Figure 15	25°C Full	1.65 V to 1.95 V		40	55 70	ns
t _{BBM}	Break-before-make time	$V_{NC} = V_{NO} = V_{+} / 2,$ $R_{L} = 50 \Omega,$	C _L = 35 pF, See Figure 15	25°C Full	1.65 V to 1.95 V	1 0.5	60	72	ns
Q _C	Charge injection	C _L = 1 nF, V _{GEN} = 0 V,	See Figure 19	25°C	1.8 V	0.0	13		рC
C _{NC(OFF)} , C _{NO(OFF)}	NC, NO OFF capacitance	V _{NC} or V _{NO} = V ₊ or GND, Switch OFF,	See Figure 14	25°C	1.8 V		23		pF
C _{NC(ON)} , C _{NO(ON)}	NC, NO ON capacitance	V _{NC} or V _{NO} = V ₊ or GND, Switch ON,	See Figure 14	25°C	1.8 V		84		pF
C _{COM(ON)}	COM ON capacitance	V _{COM} = V ₊ or GND, Switch ON,	See Figure 14	25°C	1.8 V		84		pF
C _{IN}	Digital input capacitance	$V_{IN} = V_{+} \text{ or GND},$	See Figure 14	25°C	1.8 V		2.1		pF
BW	Bandwidth	$R_L = 50 \Omega$, Switch ON,	See Figure 16	25°C	1.8 V		100		MHz
O _{ISO}	OFF isolation	$R_L = 50 \Omega$, f = 1 MHz,	Switch OFF, See Figure 17	25°C	C 1.8 V –63			dB	
X _{TALK}	Crosstalk	$R_L = 50 \Omega,$ f = 1 MHz,	Switch ON, See Figure 18	25°C	1.8 V		-63		dB
SUPPLY									
l ₊	Positive supply current	$V_{IN} = V_{+} \text{ or GND},$	Switch ON or OFF	25°C Full	1.95 V			0.1	μА

Product Folder Links: TS5A3159-Q1

⁽¹⁾ $T_A = 25^{\circ}C$

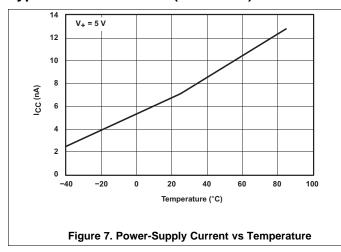


6.9 Typical Characteristics





Typical Characteristics (continued)



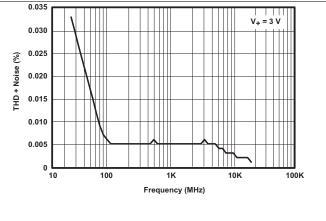


Figure 8. Total Harmonic Distortion (THD) vs Frequency



7 Parameter Measurement Information

Table 1. Parameter Description

SYMBOL	DESCRIPTION
V _{COM}	Voltage at COM
V _{NC}	Voltage at NC
V _{NO}	Voltage at NO
r _{on}	Resistance between COM and NC or COM and NO ports, when the channel is ON
r _{peak}	Peak ON-state resistance over a specified voltage range
Δr_{on}	Difference of r _{on} between channels
ron(flat)	Difference between the maximum and minimum value of ron in a channel over the specified range of conditions
I _{NC(OFF)}	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions
I _{NO(OFF)}	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions
I _{NC(ON)}	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) being open
I _{NO(ON)}	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) being open
I _{COM(ON)}	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) being open
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Minimum input voltage for logic low for the control input (IN)
V_{IN}	Voltage at IN
$I_{\text{IH}},\ I_{\text{IL}}$	Leakage current measured at IN
t _{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM, NC, or NO) signal, when the switch is turning ON.
t _{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM, NC, or NO) signal, when the switch is turning OFF.
t _{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO), when the control signal changes state.
$Q_{\mathbb{C}}$	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_O$, C_L is the load capacitance, and ΔV_O is the change in analog output voltage.
C _{NC(OFF)}	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
C _{NO(OFF)}	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
C _{NC(ON)}	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
C _{NO(ON)}	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
C _{COM(ON)}	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
C _{IN}	Capacitance of IN
O _{ISO}	OFF isolation of the switch is a measurement OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
X _{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is −3 dB below the DC gain.
I ₊	Static power-supply current with the control (IN) pin at V ₊ or GND
ΔI_{+}	This is the increase in I ₊ for each control (IN) input that is at the specified voltage, rather than at V ₊ or GND.

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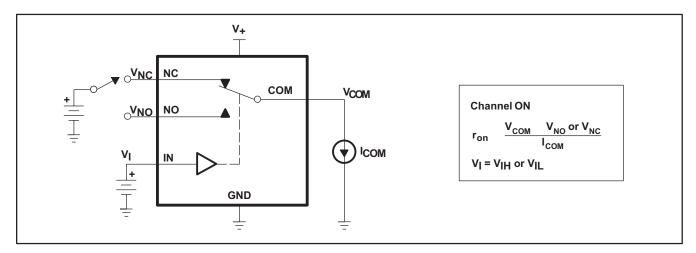


Figure 9. On-State Resistance (ron)

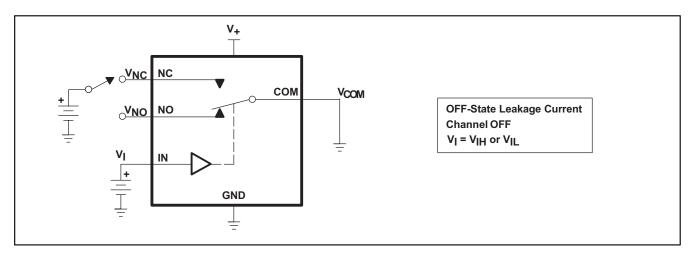


Figure 10. Off-State Leakage Current (I_{NC(OFF)}, I_{NO(OFF)})

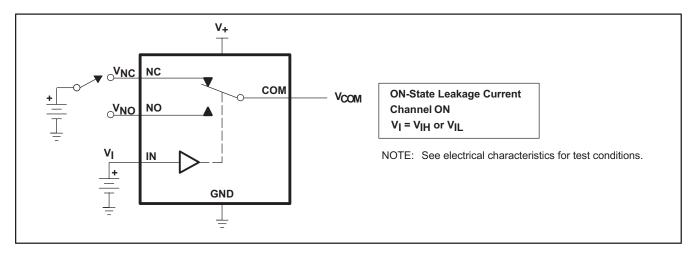


Figure 11. On-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)



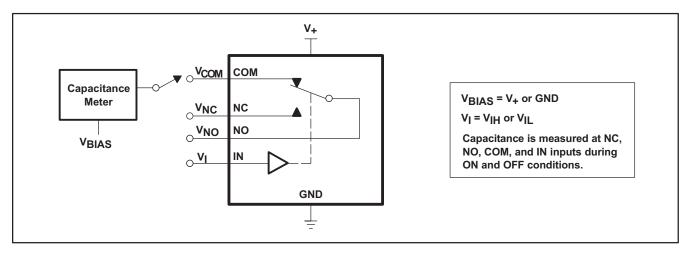
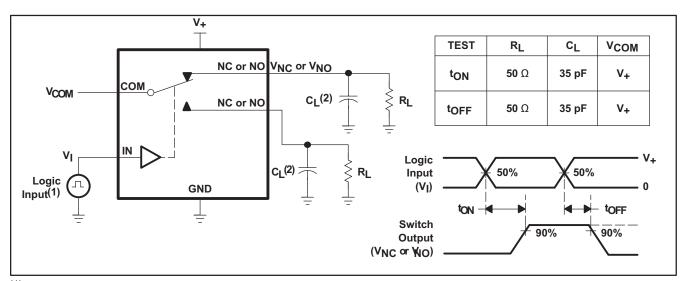


Figure 12. Capacitance (C_I, C_{COM(ON)}, C_{NC(OFF)}, C_{NO(OFF)}, C_{NC(ON)}, C_{NO(ON)})



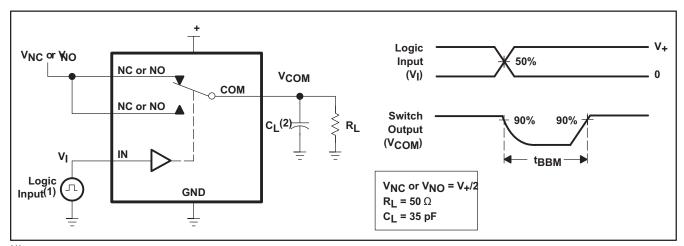
(1) All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f < 5 ns. t_f < 5 ns.

Figure 13. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

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⁽²⁾ C_L includes probe and jig capacitance.





- (1) All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_f < 5 ns, t_f < 5 ns.
- (2) C_L includes probe and jig capacitance.

Figure 14. Break-Before-Make Time (t_{BBM})

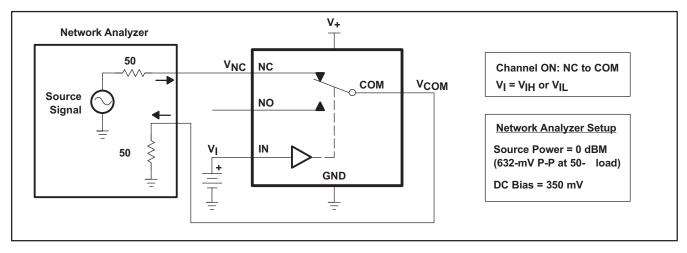


Figure 15. Bandwidth (BW)

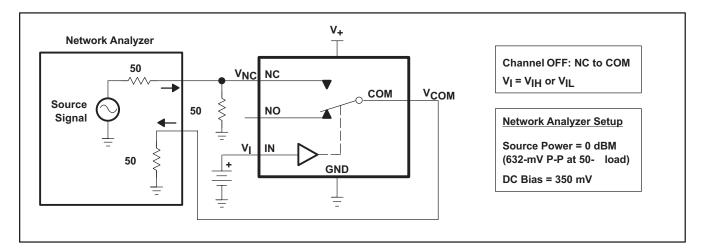


Figure 16. OFF Isolation (O_{ISO})

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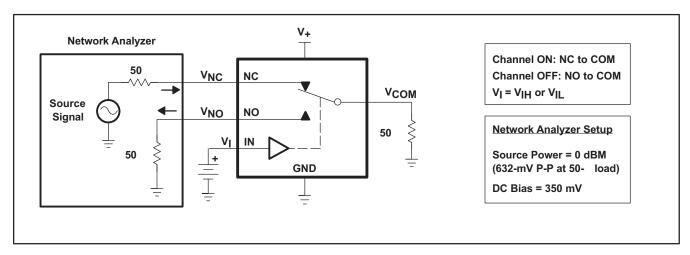
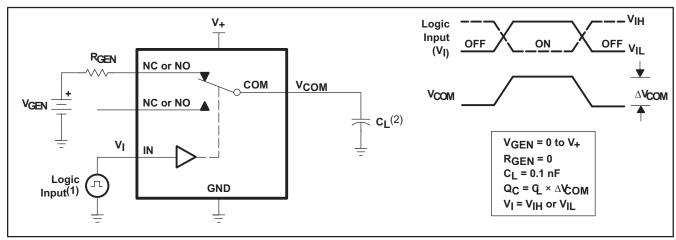
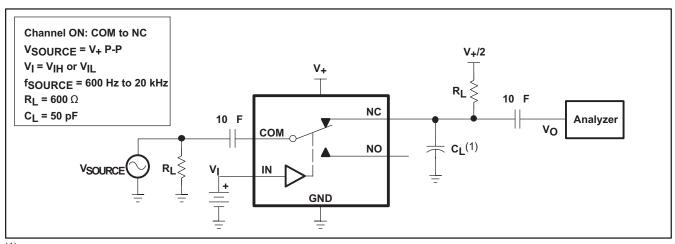


Figure 17. Crosstalk (X_{TALK})



- (1) All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_f < 5 ns, t_f < 5 ns.
- (2) C_L includes probe and jig capacitance.

Figure 18. Charge Injection (Q_C)



(1) C_L includes probe and jig capacitance.

Figure 19. Total Harmonic Distortion (THD)

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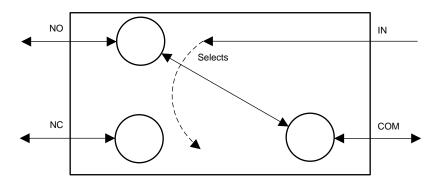


8 Detailed Description

8.1 Overview

The TS5A3159-Q1 is a single-pole double-throw (SPDT) analog switch designed to operate from 1.65 V to 5.5 V. Either the NO or the NC pin is shorted to the COM pin, depending on the logic level input to the IN pin.

8.2 Functional Block Diagram



8.3 Feature Description

The main feature of this device is the excellent total harmonic distortion performance and low power consumption. Additionally, the NO, NC, and COM pins can be used as either inputs or outputs.

Table 2. Summary Of Characteristics⁽¹⁾

CONFIGURATION	2:1 MULTIPLEXER / DEMULTIPLEXER (1 × SPDT)
Number of channels	1
ON-state resistance (r _{on})	1.3 Ω
ON-state resistance match (Δr _{on})	0.1 Ω
ON-state resistance flatness (r _{on(flat)})	0.15 Ω
Turn on/turn off time (t _{ON} / t _{OFF})	20 ns / 15 ns
Break-before-make time (t _{BBM})	12 ns
Charge injection (Q _C)	36 pC
Bandwidth (BW)	100 MHz
OFF isolation (O _{ISO})	-65 dB at 1 MHz
Crosstalk (X _{TALK})	-65 dB at 1 MHz
Total harmonic distortion (THD)	0.01%
Leakage current (I _{NO(OFF)} / I _{NC(OFF)})	±6 nA
Package option	6-pin DBV

⁽¹⁾ $V_{+} = 5 \text{ V} \text{ and } T_{A} = 25^{\circ}\text{C}$

8.4 Device Functional Modes

Table 3 lists the functions for the TS5A3159-Q1 device.

Table 3. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
Н	OFF	ON

Product Folder Links: TS5A3159-Q1



9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Analog switches are commonly used in battery powered applications to route audio signals. A typical use case is highlighted in Figure 20. The analog switch is supplied with 5 V and the control input is from a 5-V processor GPIO. In this case, there are no concerns related to excess power consumption.

9.2 Typical Application

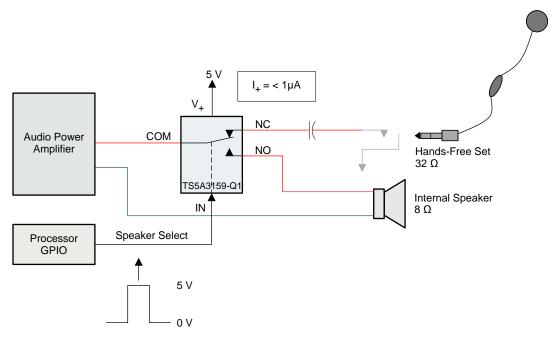


Figure 20. Typical Application Schematic

9.2.1 Design Requirements

In this application example, the device receives the control signal from a 5-V GPIO and common input from an Audio Power amplifier. The input is routed to either the Hands free set or the internal speaker depending upon the control signal.

9.2.2 Detailed Design Procedure

Since the control signal varies from 0 to 5 V (Vdd), there's no excess current consumption. However, if the control signal comes from lower voltage GPIOs while the V+ of TS5A3159 is connected to the battery whose voltage varies, it can lead to an excess current draw from the V+ suppl pin. Such a scenario requires the use of an external voltage level translator such as the SN74LVC1T45. For more information see *Preventing Excess Current Consumption on Analog Switches*, SCDA011.

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Typical Application (continued)

9.2.3 Application Curve

The ON state resistance of the switch is a critical parameter to measure since it helps select the right switch for the application. The on state resistance versus the common voltage can be seen in Figure 21.

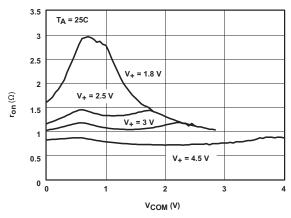


Figure 21. r_{on} vs V_{COM}

10 Power Supply Recommendations

Most systems have a common 3.3 V or 5 V rail that can supply the V+ pin of this device. If this is not available, a Switch-Mode-Power-Supply (SMPS) or a Linear Dropout Regulator (LDO) can supply this device from a higher voltage rail. Proper decouping of the supply rail is a must to avoid any spikes that may exceed the absolute ratings of the V+ pin of the device.

11 Layout

11.1 Layout Guidelines

TI recommends to keep signal lines as short as possible. Incorporation of microstrip or stripline techniques is also recommended when signal lines are greater than 1 inch in length. These traces must be designed with a characteristic impedance of either 50 Ω or 75 Ω , as required by the application. Do not place this device too close to high voltage switching components, as they may cause interference.

11.2 Layout Example

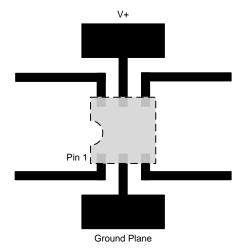


Figure 22. Layout Example

Product Folder Links: TS5A3159-Q1

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Preventing Excess Current Consumption on Analog Switches, SCDA011

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: TS5A3159-Q1

www.ti.com 7-Oct-2025

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
TS5A3159QDBVRQ1	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UAAQ
TS5A3159QDBVRQ1.B	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UAAQ

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TS5A3159-Q1:

Catalog: TS5A3159

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

www.ti.com 7-Oct-2025

● Enhanced Product : TS5A3159-EP

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Enhanced Product Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

www.ti.com 24-Apr-2020

TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3159QDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

PACKAGE MATERIALS INFORMATION

www.ti.com 24-Apr-2020



*All dimensions are nominal

Device	Device Package Type		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
TS5A3159QDBVRQ1	SOT-23	DBV	6	3000	202.0	201.0	28.0	





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

 4. Falls within JEDEC MO-203 variation AB.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

- 4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- 5. Refernce JEDEC MO-178.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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