











TS5A3159

NO

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TS5A3159 1-Ω SPDT Analog Switch

Features

- Specified Break-Before-Make Switching
- Low ON-State Resistance (1 Ω)
- Control Inputs are 5-V Tolerant
- Low Charge Injection
- **Excellent ON-Resistance Matching**
- Low Total Harmonic Distortion
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)

2 Applications

- Mobile Phones
- Consumer and Computing
- Portable Instrumentation

3 Description

The TS5A3159 device is a single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ONstate resistance and an excellent ON-state resistance matching, with the break-before-make feature to prevent signal distortion during the transferring of a signal from one channel to another. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TCE 424E0	SOT-23 (6)	2.90 mm × 1.60 mm
TS5A3159	SC70 (6)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram IN COM NC



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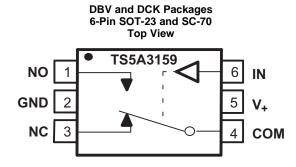
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2015) to Revision D	Page
Changed NO Pin description	3
Deleted Added Junction temperature to the Absolute Maximum Ratings table	3
Changes from Revision B (September 2004) to Revision C	Page
 Added Applications, Device Information table, Pin Functions table, ESD Ratings table, Therr Typical Characteristics, Feature Description section, Device Functional Modes, Application a section, Power Supply Recommendations section, Layout section, Device and Documentation Mechanical, Packaging, and Orderable Information section. 	and Implementation on Support section, and
Changes from Revision A (September 2004) to Revision B	Page
Removed Ordering Information table.	1
Changes from Original (August 2004) to Revision A	Page
Corrected Figure 11 graphic	



5 Pin Configuration and Functions



Pin Functions

	PIN	1/0	DESCRIPTION
NO.	NAME	1/0	DESCRIPTION
1	NO	I/O	Normally open switch port
2	GND	_	Ground
3	NC	I/O	Normally closed switch port
4	COM	I/O	Common switch port
5	V+	_	Power supply
6	IN	I	Switch select. High = COM connected to NO; Low = COM connected to NC.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V ₊	Supply voltage (2)		-0.5	6.5	V
$V_{NO} \ V_{COM}$	Analog voltage ⁽²⁾⁽³⁾⁽⁴⁾		-0.5	V ₊ + 0.5	V
I _{I/OK}	Analog port diode current	V_{NO} , $V_{COM} < 0$ or V_{NO} , $V_{COM} > V_{+}$		±50	mA
I _{NO} I _{COM}	ON-state switch current	V_{NO} , $V_{COM} = 0$ to V_{+}		±200	mA
	ON-state peak switch current (5)			±400	mA
V_{IN}	Digital input voltage (2)(3)		-0.5	6.5	V
I_{IK}	Digital input clamp current	V _{IN} < 0		-50	mA
	Continuous current through V+ or GN	ID		±100	mA
Tj	Junction temperature			150	°C
T _{stg}	Storage temperature		-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

⁽²⁾ All voltages are with respect to ground, unless otherwise specified.

⁽³⁾ The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

⁽⁴⁾ This value is limited to 5.5 V maximum.

⁽⁵⁾ Pulse at 1-ms duration < 10% duty cycle.



6.2 ESD Ratings

				VALUE	UNIT
			Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	
\	$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{I/O}	Switch input/output voltage	0	V ₊	V
V+	Supply voltage	1.65	5.5	V
VI	Control input voltage	0	5.5	V
T _A	Operating temperature	-40	85	°C

6.4 Thermal Information

		TS5A3	159	
	THERMAL METRIC ⁽¹⁾	DBV (SOT-23)	DCK (SC-70)	UNIT
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165	165	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics for 5-V Supply

 $V_{+} = 4.5 \text{ V to } 5.5 \text{ V and } T_{A} = -40^{\circ}\text{C} \text{ to } 85^{\circ}\text{C} \text{ (unless otherwise noted)}$

P	PARAMETER	TEST CONDITIO	NS	TA	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
Analog Sw	ritch								
V_{COM} , V_{NO} , V_{NC}	Analog signal range					0		V ₊	V
	Peak ON-state	$0 \le V_{NO}$ or $V_{NC} \le V_+$,	Switch ON,	25°C	4.5 V		1	1.5	Ω
r _{peak}	resistance	$I_{COM} = -30 \text{ mA},$	see Figure 10	Full	4.5 V			1.5	32
r	ON-state resistance	V_{NO} or $V_{NC} = 2.5 \text{ V}$,	Switch ON,	25°C	4.5 V		0.75	1.1	Ω
r _{on}	ON-State resistance	$I_{COM} = -30 \text{ mA},$	see Figure 10	Full	4.5 V			1.1	32
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 2.5 V, I_{COM} = -30 mA,	Switch ON, see Figure 10	25°C	4.5 V		0.1		Ω
	ON-state resistance	$0 \le V_{NO} \text{ or } V_{NC} \le V_+,$ $I_{COM} = -30 \text{ mA}$	Switch ON,	25°C	4.5 V		0.233		Ω
r _{on(flat)}	flatness	V_{NO} or V_{NC} = 1 V, 1.5 V, 2.5 V, I_{COM} = -30 mA	see Figure 10	25°C	4.5 V		0.15		22
I _{NC(OFF)} ,	NC, NO	V_{NC} or $V_{NO} = 4.5 \text{ V}$,	Switch OFF,	25°C	5.5 V	-2	0.2	2	nA
I _{NO(OFF)}	Off leakage current	$V_{COM} = 0 V,$	see Figure 11	Full	5.5 V	-20		20	ΠA
I _{NC(ON)} ,	NC, NO	V_{NC} or $V_{NO} = 4.5 \text{ V}$,	Switch ON,	25°C	5.5 V	-4	2.8	4	nA
I _{NO(ON)}	On leakage current	V _{COM} = Open,	see Figure 12	Full	5.5 V	-40		40	ΠA
	COM	V_{NC} or $V_{NO} = 4.5 \text{ V or Open}$,	Switch ON,	25°C	<i>E E \/</i>	-4	0.47	4	~ ^
I _{COM(ON)}	On leakage current	$V_{COM} = 4.5 V$	see Figure 12	Full	5.5 V	-40		40	nA
Digital Inpu	ut (IN)								
V _{IH}	Input logic high			Full		2.4		5.5	V
V_{IL}	Input logic low			Full		0		8.0	V
I _{IH} , I _{IL}	Input leakage current	V _{IN} = 5.5 V or 0		Full	5.5 V	-1		1	μΑ

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(1) $T_A = 25^{\circ}C$.

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Electrical Characteristics for 5-V Supply (continued)

 $V_{+} = 4.5 \text{ V to } 5.5 \text{ V and } T_{A} = -40 ^{\circ}\text{C} \text{ to } 85 ^{\circ}\text{C} \text{ (unless otherwise noted)}$

F	PARAMETER	TEST CONDI	TIONS	T _A	V ₊	MIN TYP(1)	MAX	UNIT
Dynamic							'	
		$V_{COM} = V_+$	$C_1 = 35 pF$,	25°C	4.5 V	20	35	
t _{ON}	Turnon time	$R_L = 50 \Omega$	see Figure 14	Full	to 5.5 V		40	ns
		$V_{COM} = V_+,$	$C_1 = 35 pF$,	25°C	4.5 V	15	20	
t _{OFF}	Turnoff time	$R_L = 50 \Omega$	see Figure 14	Full	to 5.5 V		35	ns
	Break-before-make	$V_{NC} = V_{NO} = V_{+} / 2$	$C_1 = 35 pF$,	25°C	4.5 V	1 12	14.5	-
t _{BBM}	time	$R_{L} = 50 \Omega,$	see Figure 15	Full	to 5.5 V	1		ns
$Q_{\mathbb{C}}$	Charge injection	$C_L = 1 \text{ nF},$ $V_{GEN} = 0 \text{ V},$	See Figure 19	25°C	5 V	36		рС
C _{NC(OFF)} , C _{NO(OFF)}	NC, NO OFF capacitance	V_{NC} or $V_{NO} = V_{+}$ or GND,	Switch OFF, see Figure 13	25°C	5 V	23		pF
C _{NC(ON)} , C _{NO(ON)}	NC, NO ON capacitance	V_{NC} or $V_{NO} = V_{+}$ or GND,	Switch ON, see Figure 13	25°C	5 V	84		pF
C _{COM(ON)}	COM ON capacitance	V _{COM} = V ₊ or GND,	Switch ON, see Figure 13	25°C	5 V	84		pF
C _{IN}	Digital input capacitance	$V_{IN} = V_{+} \text{ or GND},$	See Figure 13	25°C	5 V	2.1		pF
BW	Bandwidth	$R_L = 50 \Omega$,	Switch ON, see Figure 16	25°C	5 V	100		MHz
O _{ISO}	OFF isolation	$R_L = 50 \Omega$, f = 1 MHz,	Switch OFF, see Figure 17	25°C	5 V	-65		dB
X _{TALK}	Crosstalk	$R_L = 50 \Omega$, f = 1 MHz,	Switch ON, see Figure 18	25°C	5 V	-65		dB
THD	Total harmonic distortion	$R_L = 600 \Omega,$ $C_L = 50 pF,$	f = 600 Hz to 20 kHz, see Figure 20	25°C	5 V	0.01%		
Supply								
I ₊	Positive supply current	$V_{IN} = V_{+}$ or GND,	Switch ON or OFF	Full	5.5 V		0.1	μΑ

6.6 Electrical Characteristics for 3.3-V Supply

 $V_{+} = 3 \text{ V to } 3.6 \text{ V and } T_{A} = -40 ^{\circ}\text{C to } 85 ^{\circ}\text{C} \text{ (unless otherwise noted)}$

Р	ARAMETER	TEST CON	IDITIONS	T _A	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
Analog Swi	tch								
V_{COM} , V_{NO} , V_{NC}	Analog signal range					0		V ₊	V
-	Peak ON-state	$0 \le V_{NO}$ or $V_{NC} \le V_+$,	Switch ON,	25°C	3 V		1.35	2.1	Ω
r _{peak}	resistance	$I_{COM} = -24 \text{ mA},$	see Figure 10	Full	3 V			2.1	12
_	ON state resistance	V_{NO} or $V_{NC} = 2 V$,	Switch ON,	25°C	2.1/		1.15	1.5	0
ron	r ()NI-etata racictanca (NO NO /	see Figure 10	Full	3 V			1.5	Ω	
Δr _{on}	ON-state resistance match between channels	V_{NO} or $V_{NC} = 2 \text{ V}$, 0.8 V, $I_{COM} = -24 \text{ mA}$,	Switch ON, see Figure 10	25°C	3 V		0.11		Ω
	ON-state resistance	$0 \le V_{NO} \text{ or } V_{NC} \le V_+,$ $I_{COM} = -24 \text{ mA},$	Switch ON	25°C			0.225		
r _{on(flat)}	flatness V_{NO} or V_{N}	V_{NO} or $V_{NC} = 2 \text{ V}$, 0.8 V, $I_{COM} = -24 \text{ mA}$,	Switch ON, see Figure 10	25°C	3 V		0.25		Ω

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(1) $T_A = 25^{\circ}C$.



Electrical Characteristics for 3.3-V Supply (continued)

 $V_{+} = 3 \text{ V to } 3.6 \text{ V and } T_{A} = -40^{\circ}\text{C to } 85^{\circ}\text{C (unless otherwise noted)}$

F	ARAMETER	TEST CO	NDITIONS	TA	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
I _{NC(OFF)} , I _{NO(OFF)}	NC, NO Off leakage current	V_{NC} or $V_{NO} = 3 V$, $V_{COM} = 0$,	Switch OFF, see Figure 11	25°C	3.6 V		0.2		nA
I _{NC(ON)} , I _{NO(ON)}	NC, NO On leakage current	V_{NC} or $V_{NO} = 3 V$, $V_{COM} = Open$,	Switch ON, see Figure 12	25°C	3.6 V		2.8		nA
I _{COM(ON)}	COM On leakage current	V_{NC} or $V_{NO} = 3 \text{ V}$ or Open, $V_{COM} = 3 \text{ V}$,	Switch ON, see Figure 12	25°C	3.6 V		0.47		nA
Digital Inpu	ts (IN)	·							
V _{IH}	Input logic high			Full		2		5.5	V
V _{IL}	Input logic low			Full		0		0.6	V
I _{IH} , I _{IL}	Input leakage current	V _{IN} = 5.5 V or 0		Full	3.6 V	-1		1	μΑ
Dynamic									
	T C	$V_{COM} = V_+,$	$C_{L} = 35 \text{ pF},$	25°C	3 V		30	40	
t _{ON}	Turnon time	$R_L = 50 \Omega$	see Figure 14	Full	to 3.6 V			55	ns
		$V_{COM} = V_+,$	$C_1 = 35 \text{ pF},$	25°C	3 V		20	25	
t _{OFF}	Turnoff time	$R_L = 50 \Omega$,	see Figure 14	Full	to 3.6 V			40	ns
	Break-before-make	V -V -V /2	C _L = 35 pF,	25°C	3 V	1	21	29	
t _{BBM}	time	$V_{NC} = V_{NO} = V_{+} / 2,$ $R_{L} = 50 \Omega,$	see Figure 15	Full	to 3.6 V	1			ns
Q _C	Charge injection	$C_L = 1 \text{ nF},$ $V_{GEN} = 0 \text{ V},$	see Figure 19	25°C	3.3 V		20		рС
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or $V_{NO} = V+$ or GND,	Switch OFF, see Figure 13	25°C	3.3 V		23		pF
C _{NC(ON)} , C _{NO(ON)}	NC, NO ON capacitance	V_{NC} or $V_{NO} = V_{+}$ or GND,	Switch ON, see Figure 13	25°C	3.3 V		84		pF
C _{COM(ON)}	COM ON capacitance	$V_{COM} = V_{+} \text{ or GND},$	Switch ON, see Figure 13	25°C	3.3 V		84		pF
C _{IN}	Digital input capacitance	$V_{IN} = V_{+}$ or GND,	See Figure 13	25°C	3.3 V		2.1		pF
BW	Bandwidth	$R_L = 50 \Omega$,	Switch ON, see Figure 16	25°C	3.3 V		100		MHz
O _{ISO}	OFF isolation	$R_L = 50 \Omega$, f = 1 MHz,	Switch OFF, see Figure 17	25°C	3.3 V		-65		dB
X _{TALK}	Crosstalk	$R_L = 50 \Omega$, f = 1 MHz,	Switch ON, see Figure 18	25°C	3.3 V		-65		dB
THD	Total harmonic distortion	$R_L = 600 \Omega,$ $C_L = 50 pF,$	f = 600 Hz to 20 kHz, see Figure 20	25°C	3.3 V		0.015%		
Supply									
l ₊	Positive supply current	$V_{IN} = V_{+}$ or GND,	Switch ON or OFF	Full	3.6 V			0.1	μΑ

6.7 Electrical Characteristics for 2.5-V Supply

 $V_{+} = 2.3 \text{ V to } 2.7 \text{ V and } T_{A} = -40^{\circ}\text{C} \text{ to } 85^{\circ}\text{C} \text{ (unless otherwise noted)}$

PAI	RAMETER	TEST CONDITIONS	V ₊	MIN	TYP ⁽¹⁾ MAX	UNIT		
Analog Switch								
V_{COM} , V_{NO} , V_{NC}	Analog signal range				0	V ₊	V	

(1) $T_A = 25^{\circ}C$.

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Electrical Characteristics for 2.5-V Supply (continued)

 $V_{+} = 2.3 \text{ V to } 2.7 \text{ V}$ and $T_{A} = -40 ^{\circ}\text{C}$ to 85 $^{\circ}\text{C}$ (unless otherwise noted)

P/	ARAMETER	TEST CONI	DITIONS	T _A	V ₊	MIN TYP ⁽¹⁾	MAX	UNIT
	Peak ON-state	$0 \le V_{NO}$ or $V_{NC} \le V_+$,	Switch ON,	25°C	0.5.1	1.7	2.7	
r _{peak}	resistance	$I_{COM} = -8 \text{ mA},$	see Figure 10	Full	2.5 V		2.7	Ω
r _{on}	ON-state resistance	V_{NO} or $V_{NC} = 1.8 \text{ V}$, $I_{COM} = -8 \text{ mA}$,	Switch ON, see Figure 10	25°C Full	2.5 V	1.45	2	Ω
Δr _{on}	ON-state resistance match between channels	V_{NO} or $V_{NC} = 0.8 \text{ V}$, 1.8 V, $I_{COM} = -8 \text{ mA}$,	Switch ON, see Figure 10	25°C	2.5 V	0.7		Ω
_	ON-state	$0 \le V_{NO} \text{ or } V_{NC} \le V_+,$ $I_{COM} = -8 \text{ mA},$	Switch ON,	25°C	2.5 V	0.5		0
r _{on(flat)}	resistance flatness	V_{NO} or V_{NC} = 0.8 V, 1.8 V I_{COM} = -8 mA,	see Figure 10	25°C	2.5 V	0.45		Ω
I _{NC(OFF)} , I _{NO(OFF)}	NC, NO Off leakage current	V_{NC} or $V_{NO} = 2.3 \text{ V}$, $V_{COM} = 0$,	Switch OFF, see Figure 11	25°C	2.7 V	0.2		nA
I _{NC(ON)} , I _{NO(ON)}	NC, NO On leakage current	V_{NC} or $V_{NO} = 2.3 \text{ V}$, $V_{COM} = \text{Open}$,	Switch ON, see Figure 12	25°C	2.7 V	2.8		nA
I _{COM(ON)}	COM On leakage current	V_{NC} or V_{NO} = 2.3 V or Open, V_{COM} = 2.3 V,	Switch ON, see Figure 12	25°C	2.7 V	0.47		nA
Digital Inpu	t (IN)			•				
V_{IH}	Input logic high			Full		1.8	5.5	V
V_{IL}	Input logic low			Full		0	0.6	V
I _{IH} , I _{IL}	Input leakage current	V _{IN} = 5.5 V or 0		Full	2.7 V	-1	1	μA
Dynamic								•
	_		$C_1 = 35 \text{ pF},$	25°C	2.3 V	40	55	
t _{ON}	Turnon time	$V_{COM} = V_+, R_L = 50 \Omega,$	see Figure 14	Full	to 2.7 V		70	ns
	T # C	V D 50.0	$C_1 = 35 pF$,	25°C	2.3 V	30	40	
t _{OFF}	Turnoff time	$V_{COM} = V_+, R_L = 50 \Omega,$	see Figure 14	Full	to 2.7 V		55	ns
t	Break-before-make	$V_{NC} = V_{NO} = V_{+} / 2,$	$C_L = 35 \text{ pF},$	25°C	2.3 V to	1 33	39	ns
t _{BBM}	time	$R_L = 50 \Omega$,	see Figure 15	Full	2.7 V	1		113
$Q_{\mathbb{C}}$	Charge injection	C _L = 1 nF, V _{GEN} = 0 V,	See Figure 19	25°C	2.5 V	13		рС
$\begin{array}{l} C_{NC(OFF)}, \\ C_{NO(OFF)} \end{array}$	NC, NO OFF capacitance	V_{NC} or $V_{NO} = V_{+}$ or GND,	Switch OFF, see Figure 13	25°C	2.5 V	23		pF
C _{NC(ON)} , C _{NO(ON)}	NC, NO ON capacitance	V_{NC} or $V_{NO} = V_{+}$ or GND,	Switch ON, see Figure 13	25°C	2.5 V	84		pF
C _{COM(ON)}	COM ON capacitance	$V_{COM} = V_{+} \text{ or GND},$	Switch ON, see Figure 13	25°C	2.5 V	84		pF
C _{IN}	Digital input capacitance	$V_{IN} = V+ \text{ or GND},$	See Figure 13	25°C	2.5 V	2.1		pF
BW	Bandwidth	$R_L = 50 \Omega$,	Switch ON, see Figure 16	25°C	2.5 V	100		MHz
O _{ISO}	OFF isolation	$R_L = 50 \Omega$, f = 1 MHz,	Switch OFF, see Figure 17	25°C	2.5 V	-64		dB
X _{TALK}	Crosstalk	$R_L = 50 \Omega$, $f = 1 MHz$,	Switch ON, see Figure 18	25°C	2.5 V	-64		dB
THD	Total harmonic distortion	$R_L = 600 \Omega$, f = 600 Hz to 20 kHz,	C _L = 50 pF, see Figure 20	25°C	2.5 V	0.025%		
Supply								
I ₊	Positive supply current	$V_{IN} = V_{+} \text{ or GND},$	Switch ON or OFF	Full	2.7 V		0.1	μΑ



6.8 Electrical Characteristics for 1.8-V Supply

 $V_{+} = 1.65 \text{ V}$ to 1.95 V and $T_{\Delta} = -40^{\circ}\text{C}$ to 85°C (unless otherwise noted)

P	ARAMETER	TEST CONDI	TIONS	T _A	V ₊	MIN TYP(1)	MAX	UNIT
Analog Sw	vitch							
V _{COM} , V _{NO} , V _{NC}	Analog signal					0	V ₊	V
r _{peak}	Peak ON- resistance	$0 \le V_{NO} \text{ or } V_{NC} \le V_+,$ $I_{COM} = -2 \text{ mA},$	Switch ON, see Figure 10	25°C Full	1.8 V	4	4.9 4.9	Ω
r _{on}	ON-state resistance	V_{NO} or $V_{NC} = 1.5 \text{ V}$, $I_{COM} = -2 \text{ mA}$,	Switch ON, see Figure 10	25°C Full	1.8 V	1.7 3.2 3.2		Ω
Δr _{on}	ON-state resistance match	V_{NO} or $V_{NC} = 0.6 \text{ V}$, 1.5 V,	Switch ON,	25°C	1.8 V	0.7	5.2	Ω
	between channels	$I_{COM} = -2 \text{ mA},$ $0 \le V_{NO} \text{ or } V_{NC} \le V_{+},$	see Figure 10	Full 25°C		1.85		
r _{on(flat)}	ON-state resistance flatness	$I_{COM} = -2 \text{ mA},$ $V_{NO} \text{ or } V_{NC} = 0.6 \text{ V}, 1.5 \text{ V},$	Switch ON, see Figure 10	Full 25°C	1.8 V	1.85 0.9		Ω
	NO NO	$I_{COM} = -2 \text{ mA},$		Full		0.9		
I _{NC(OFF)} , I _{NO(OFF)}	NC, NO OFF leakage current	V_{NC} or $V_{NO} = 1.65 V$, $V_{COM} = 0$,	Switch OFF, see Figure 11	25°C	1.95 V	0.2		nA
I _{NC(ON)} , I _{NO(ON)}	NC, NO ON leakage current	V_{NC} or V_{NO} = 1.65 V, V_{COM} = Open,	Switch ON, see Figure 12	25°C	1.95 V	2.8		nA
I _{COM(ON)}	COM ON leakage current	V_{NC} or V_{NO} = 1.65 V or open, V_{COM} = 1.65 V,	Switch ON, see Figure 12	25°C	1.95 V	0.47		nA
Digital Inpu	ut (IN)							
V _{IH}	Input logic high			Full		1.5	5.5	V
V _{IL}	Input logic low			Full		0	0.6	V
I _{IH} , I _{IL}	Input leakage current	V _{IN} = 5.5 V or 0		Full	1.95 V	-1	1	μΑ
Dynamic								
t _{ON}	Turnon time	$V_{COM} = V_+,$ $R_L = 50 \Omega,$	$C_L = 35 \text{ pF},$ see Figure 14	25°C Full	1.65 V to	65	70 95	ns
	- ##	$V_{COM} = V_+,$	C _L = 35 pF,	25°C	1.95 V 1.65 V	40	55	
toff	Turnoff time	$R_L = 50 \Omega$	see Figure 14	Full	to 1.95 V		70	ns
t _{BBM}	Break-before-make time	$V_{NC} = V_{NO} = V_{+} / 2,$ $R_{L} = 50 \Omega,$	$C_L = 35 pF$, see Figure 15	25°C Full	1.65 V to 1.95 V	0.5	72	ns
Q _C	Charge injection	C _L = 1 nF, V _{GEN} = 0 V,	See Figure 19	25°C	1.8 V	13		рС
C _{NC(OFF)} , C _{NO(OFF)}	NC, NO OFF capacitance	V_{NC} or $V_{NO} = V + \text{ or GND}$,	Switch OFF, see Figure 13	25°C	1.8 V	23		pF
C _{NC(ON)} , C _{NO(ON)}	NC, NO ON capacitance	V_{NC} or $V_{NO} = V_{+}$ or GND,	Switch ON, see Figure 13	25°C	1.8 V	84		pF
C _{COM(ON)}	COM ON capacitance	$V_{COM} = V_{+}$ or GND,	Switch ON, see Figure 13	25°C	1.8 V	84		pF
C _{IN}	Digital input capacitance	$V_{IN} = V_{+} \text{ or GND},$	See Figure 13	25°C	1.8 V	2.1		pF
BW	Bandwidth	$R_L = 50 \Omega$,	Switch ON, see Figure 16	25°C	5.5 V	100		MHz
O _{ISO}	OFF isolation	$R_L = 50 \Omega,$ f = 1 MHz,	Switch OFF, see Figure 17	25°C	1.8 V	-63		dB
X _{TALK}	Crosstalk	$R_L = 50 \Omega$, f = 1 MHz,	Switch ON, see Figure 18	25°C	1.8 V	-63		dB

⁽¹⁾ $T_A = 25^{\circ}C$.

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Electrical Characteristics for 1.8-V Supply (continued)

 $V_{+} = 1.65 \text{ V}$ to 1.95 V and $T_{A} = -40 ^{\circ}\text{C}$ to 85 $^{\circ}\text{C}$ (unless otherwise noted)

	PARAMETER	TEST CONDITIONS			V ₊	MIN TYP ⁽¹⁾	MAX	UNIT
Supply								
I ₊	Positive supply current	$V_{IN} = V_{+}$ or GND,	Switch ON or OFF	Full	1.8 V		0.1	μΑ

6.9 Switching Characteristics for 5-V Supply

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS			V ₊	MIN	TYP	MAX	UNIT		
	Turnon time	$V_{COM} = V_+,$	$C_L = 35 pF$,	25°C	4.5 V to		20	35			
t _{ON}	Turnon time	$R_L = 50 \Omega$	see Figure 14	Full	5.5 V			40	ns		
t _{OFF}	Turn off time o	$V_{COM} = V_+,$	C _L = 35 pF,		4.5 V to		15	20			
	Turnoff time	$R_L = 50 \Omega$	see Figure 14	Full	5.5 V			35	ns		
	Break-before-	$V_{NC} = V_{NO} = V_{+}/2,$	$C_L = 35 pF,$	25°C	4.5 V to	1	12	14.5	20		
t _{BBM}	make time	$R_L = 50 \Omega$,	see Figure 15	Full	5.5 V	1			ns		

6.10 Switching Characteristics for 3.3-V Supply

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS			V ₊	MIN	TYP	MAX	UNIT
	Turnon time	$V_{COM} = V_+,$	$C_{L} = 35 pF,$		3 V to		30	40	
t _{ON}	rumon time	$R_L = 50 \Omega$	see Figure 14	Full	3.6 V			55	ns
	Turnoff time	$V_{COM} = V_+,$ $R_1 = 50 \Omega,$	$C_{L} = 35 \text{ pF},$	25°C	3 V to		20	25	no
t _{OFF}	rumon time	$R_L = 50 \Omega$,	see Figure 14	Full	3.6 V			40	ns
	Break-before-	$V_{NC} = V_{NO} = V_{+}/2,$	$C_L = 35 pF$,	25°C	3 V to	1	21	29	no
t _{BBM}	make time	$R_L = 50 \Omega$,	see Figure 15	Full	3.6 V	1			ns

6.11 Switching Characteristics for 2.5-V Supply

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS			V ₊	MIN	TYP	MAX	UNIT
	Turnon time	$V_{COM} = V_+,$	$C_{L} = 35 \text{ pF},$	25°C	2.3 V to		40	55	
t _{ON}	rumon time	$R_L = 50 \Omega$,	see Figure 14	Full	2.7 V			70	ns
	Turnoff time	$V_{COM} = V_+,$	$C_L = 35 pF$,	25°C	2.3 V to		30	40	no
t _{OFF}	rumon ume	$R_L = 50 \Omega$,	see Figure 14	Full	2.7 V			55	ns
+	Break-before-	$V_{NC} = V_{NO} = V_{+}/2,$ $R_{L} = 50 \Omega,$	$C_{L} = 35 \text{ pF},$	25°C	2.3 V to	1	33	39	ns
t _{BBM}	make time	$R_L = 50 \Omega$,	see Figure 15	Full	2.7 V	1			115

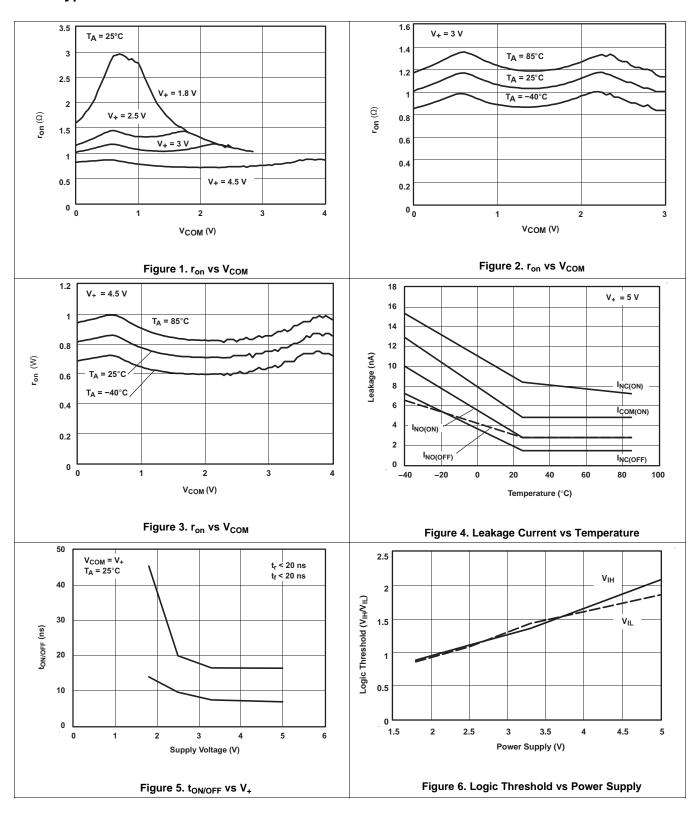
6.12 Switching Characteristics for 1.8-V Supply

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS			V ₊	MIN	TYP	MAX	UNIT
		Voor - V	C _L = 35 pF,	25°C	1.65 V		65	70	
t _{ON}	Turnon time	$V_{COM} = V_+,$ $R_L = 50 \Omega,$	see Figure 14	Full	to 1.95 V			95	ns
		Voor = V	$C_L = 35 pF$,	25°C	1.65 V		40	55	
t _{OFF}	Turnoff time	$V_{COM} = V_+,$ $R_L = 50 \Omega,$	see Figure 14	Full	to 1.95 V			70	ns
	Break-before-	$V_{NC} = V_{NO} = V_{+}/2,$	$C_L = 35 pF$,	25°C	1.65 V	1	60	72	
t _{BBM}	make time	$R_L = 50 \Omega$,	see Figure 15	Full	to 1.95 V	1			ns



6.13 Typical Characteristics



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Typical Characteristics (continued)

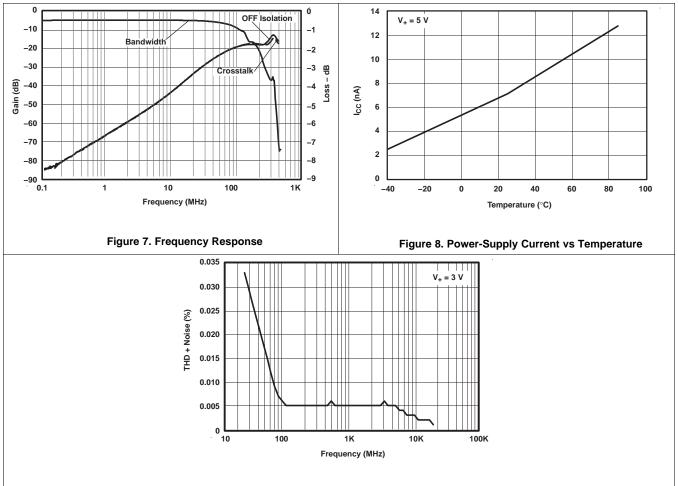


Figure 9. Total Harmonic Distortion (THD) vs Frequency



7 Parameter Measurement Information

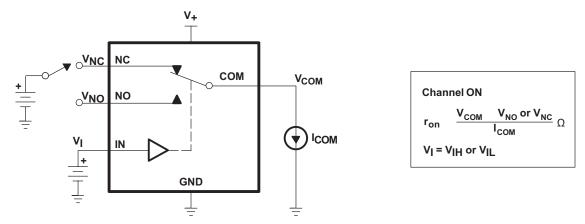


Figure 10. ON-State Resistance (ron)

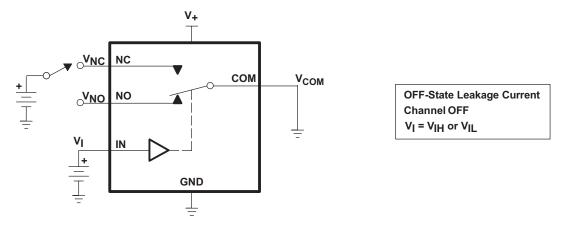


Figure 11. OFF-State Leakage Current (I_{NC(OFF)}, I_{NO(OFF)})

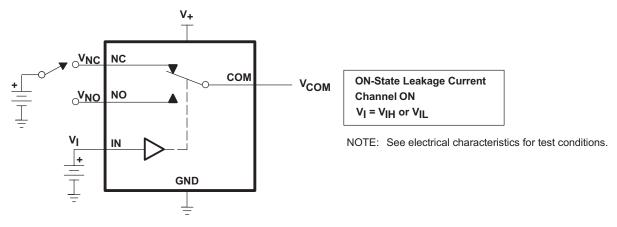


Figure 12. ON-State Leakage Current (I_{COM(ON)}, I_{NC(ON)}, I_{NO(ON)})



Parameter Measurement Information (continued)

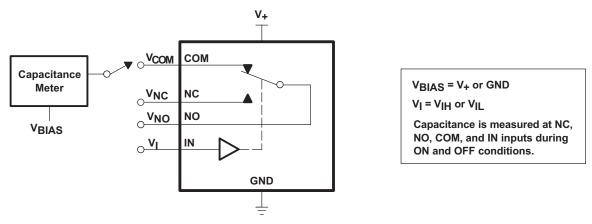
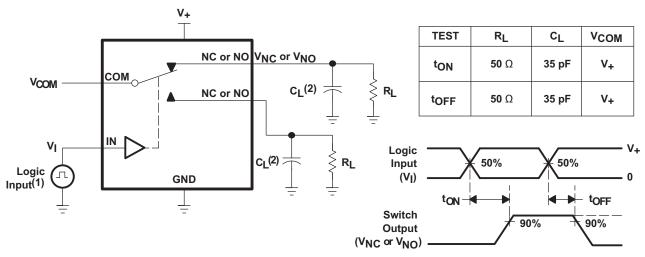


Figure 13. Capacitance (C_I, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)

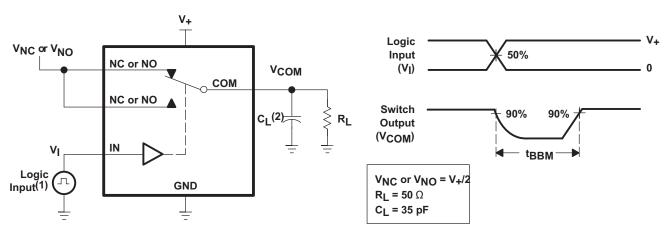


- (1) All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r < 5 \text{ ns}$, $t_f < 5 \text{ ns}$.
- (2) C_L includes probe and jig capacitance.

Figure 14. Turnon (t_{ON}) and Turnoff Time (t_{OFF})



Parameter Measurement Information (continued)



- (1) All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r < 5 ns$, $t_f < 5 \text{ ns.}$
- (2) C_L includes probe and jig capacitance.

Figure 15. Break-Before-Make Time (t_{BBM})

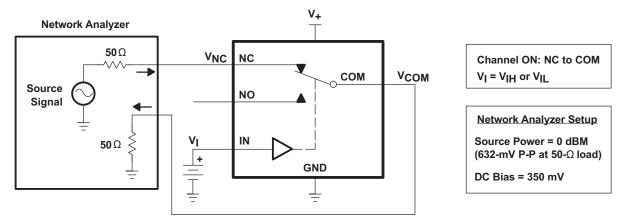


Figure 16. Bandwidth (BW)

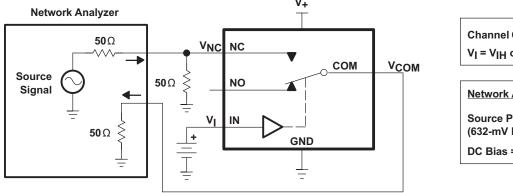


Figure 17. OFF Isolation (O_{ISO})

Channel OFF: NC to COM $V_I = V_{IH}$ or V_{IL}

Network Analyzer Setup

Source Power = 0 dBM (632-mV P-P at 50- Ω load)

DC Bias = 350 mV



Parameter Measurement Information (continued)

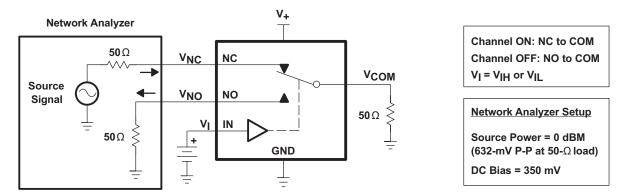
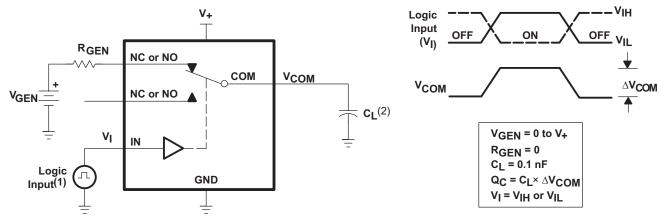
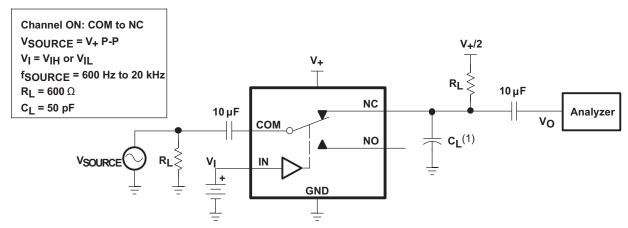


Figure 18. Crosstalk (X_{TALK})



- (1) All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r < 5 \text{ ns}$, $t_f < 5 \text{ ns}$.
- (2) C₁ includes probe and jig capacitance.

Figure 19. Charge Injection (Q_C)



(1) C_L includes probe and jig capacitance.

Figure 20. Total Harmonic Distortion (THD)



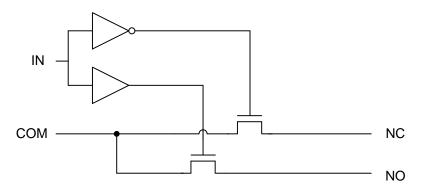
8 Detailed Description

8.1 Overview

The TS5A3159 is a single-pole-double-throw (SPDT) solid-state analog switch. The TS5A3159, like all analog switches, is bidirectional. When powered on, each COM pin is connected to the NC pin. For this device, NC stands for *normally closed* and NO stands for *normally open*. If IN is low, COM is connected to NC. If IN is high, COM is connected to NO.

The TS5A3159 is a break-before-make switch. This means that during switching, a connection is broken before a new connection is established. The NC and NO pins are never connected to each other.

8.2 Functional Block Diagram



8.3 Feature Description

The low ON-state resistance, ON-state resistance matching, and charge injection in the TS5A3159 make this switch an excellent choice for analog signals that require minimal distortion. In addition, the low THD allows audio signals to be preserved more clearly as they pass through the device.

The 1.65-V to 5.5-V operation allows compatibility with more logic levels, and the bidirectional I/Os can pass analog signals from 0 V to V_+ with low distortion.

8.4 Device Functional Modes

Table 1. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
Н	OFF	ON



9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS5A3159 can be used in a variety of customer systems. The TS5A3159 can be used anywhere multiple analog or digital signals must be selected to pass across a single line.

9.2 Typical Application

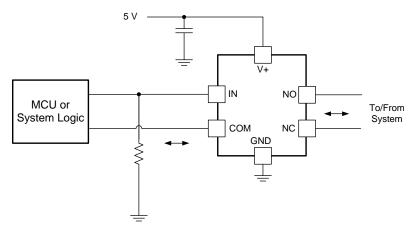


Figure 21. System Schematic for TS5A3159

9.2.1 Design Requirements

In this particular application, V_+ was 1.8 V, although V_+ is allowed to be any voltage specified in *Recommended Operating Conditions*. A decoupling capacitor is recommended on the V+ pin. See *Power Supply Recommendations* for more details.

9.2.2 Detailed Design Procedure

In this application, IN is, by default, pulled low to GND. Choose the resistor size based on the current driving strength of the GPIO, the desired power consumption, and the switching frequency (if applicable). If the GPIO is open-drain, use pullup resistors instead.

9.2.3 Application Curve

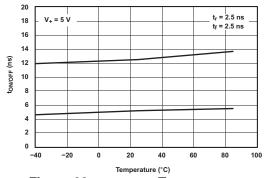


Figure 22. t_{ON/OFF} vs Temperature



10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μ F bypass capacitor is recommended. If there are multiple pins labeled V_{CC} , then a 0.01- μ F or 0.022- μ F capacitor is recommended for each V_{CC} because the VCC pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD} , a 0.1- μ F bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Below figure shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

Unused switch I/Os, such as NO, NC, and COM, can be left floating or tied to GND. However, the IN pin must be driven high or low. Due to partial transistor turnon when control inputs are at threshold levels, floating control inputs can cause increased I_{CC} or unknown switch selection states.

11.2 Layout Example

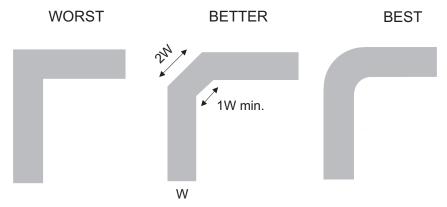


Figure 23. Trace Example



12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

Table 2. Parameter Description

SYMBOL	DESCRIPTION
V _{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
r _{on}	Resistance between COM and NC or COM and NO ports when the channel is ON
r _{peak}	Peak ON-state resistance over a specified voltage range
Δr_{on}	Difference of ron between channels
r _{on(flat)}	Difference between the maximum and minimum value of ron in a channel over the specified range of conditions
I _{NC(OFF)}	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions
I _{NO(OFF)}	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions
I _{NC(ON)}	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) being open
I _{NO(ON)}	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) being open
I _{COM(ON)}	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) being open
V _{IH}	Minimum input voltage for logic high for the control input (IN)
V _{IL}	Minimum input voltage for logic low for the control input (IN)
V _{IN}	Voltage at IN
I _{IH} , I _{IL}	Leakage current measured at IN
t _{ON}	Turnon time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal, and analog outputs (COM, NC, or NO) signal when the switch is turning ON.
t _{OFF}	Turnoff time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal, and analog outputs (COM, NC, or NO) signal when the switch is turning OFF.
t _{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO), when the control signal changes state.
Q _C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_O$, C_L is the load capacitance, and ΔV_O is the change in analog output voltage.



Table 2. Parameter Description (continued)

SYMBOL	DESCRIPTION
C _{NC(OFF)}	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
C _{NO(OFF)}	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
C _{NC(ON)}	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
C _{NO(ON)}	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
C _{COM(ON)}	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
C _{IN}	Capacitance of IN
O _{ISO}	OFF isolation of the switch is a measurement OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
X _{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is -3 dB below the DC gain.
I ₊	Static power-supply current with the control (IN) terminal at V ₊ or GND
ΔI_{+}	This is the increase in I+ for each control (IN) input that is at the specified voltage, rather than at V+ or GND.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10-Nov-2025

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
TS5A3159DBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JA8R
TS5A3159DBVR.B	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JA8R
TS5A3159DBVT	Obsolete	Production	SOT-23 (DBV) 6	-	-	Call TI	Call TI	-40 to 85	(JA8K, JA8R)
TS5A3159DCKR	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JAR, JAZ)
TS5A3159DCKR.B	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JAR, JAZ)
TS5A3159DCKT	Obsolete	Production	SC70 (DCK) 6	-	-	Call TI	Call TI	-40 to 85	(JAR, JAZ)

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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OTHER QUALIFIED VERSIONS OF TS5A3159:

Automotive: TS5A3159-Q1

● Enhanced Product : TS5A3159-EP

NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3159DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TS5A3159DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3159DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TS5A3159DCKR	SC70	DCK	6	3000	202.0	201.0	28.0





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

 4. Falls within JEDEC MO-203 variation AB.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

- 4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- 5. Refernce JEDEC MO-178.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
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