











TS5A23159

SCDS201H-AUGUST 2005-REVISED FEBRUARY 2015

TS5A23159 1-Ω 2-Channel SPDT Analog Switch 5-V / 3.3-V 2-Channel 2:1 Multiplexer / Demultiplexer

Features

- Isolation in Power-Down Mode, $V_{CC} = 0$
- Specified Break-Before-Make Switching
- Low ON-State Resistance (1 Ω)
- Control Inputs are 5.5-V Tolerant
- Low Charge Injection
- **Excellent ON-State Resistance Matching**
- Low Total Harmonic Distortion (THD)
- Supports Analog and Digital Signals
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)

Applications

- Cell Phones
- **PDAs**
- Portable Instrumentation
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communication Circuits
- Modems
- **Hard Drives**
- Computer Peripherals
- Wireless Terminals and Peripherals

3 Description

The TS5A23159 is a bidirectional 2-channel singlepole double-throw (SPDT) switch that is designed to operate from 1.65 V to 5.5 V. The device offers low ON-state resistance and excellent **ON-state** resistance matching with the break-before-make feature which prevents signal distortion during the transferring of a signal from one channel to another. The device has an excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for a wide variety of portable applications including cell phones, audio devices, and instrumentation.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
T05 100150	VSSOP (10)	3.00 mm × 3.00 mm
TS5A23159	UQFN (10)	1.50 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

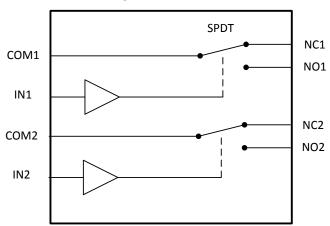




Table of Contents

	Factoria		8.1 Overview	24
1	Features 1			
2	Applications 1		8.2 Functional Block Diagram	
3	Description 1		8.3 Feature Description	21
4	Revision History2		8.4 Device Functional Modes	21
5	Pin Configuration and Functions	9	Application and Implementation	22
6	Specifications		9.1 Application Information	22
U	•		9.2 Typical Application	22
	6.1 Absolute Maximum Ratings	10	Power Supply Recommendations	
	6.2 ESD Ratings	11	Layout	
	6.4 Thermal Information		11.1 Layout Guidelines	
			11.2 Layout Example	
	6.5 Electrical Characteristics for 5-V Supply	12	Device and Documentation Support	
	6.6 Electrical Characteristics for 3.3-V Supply	12	12.1 Trademarks	
	6.7 Electrical Characteristics for 2.5-V Supply9			
	6.8 Electrical Characteristics for 1.8-V Supply 11		12.2 Electrostatic Discharge Caution	
	6.9 Typical Characteristics		12.3 Glossary	25
7	Parameter Measurement Information 16	13	Mechanical, Packaging, and Orderable	25
8	Detailed Description 21		Information	25

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (August 2013) to Revision H

Page

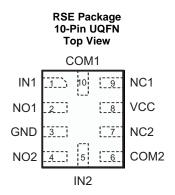
Added ESD Ratings table, Recommended Operating Conditions table, Thermal Information table, Feature
Description section, Device Functional Modes, Application and Implementation section, Power Supply
Recommendations section, Layout section, Device and Documentation Support section, and Mechanical,
Packaging, and Orderable Information section

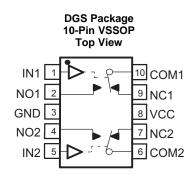
Changes from Revision F (September 2010) to Revision G

Page



5 Pin Configuration and Functions





Pin Functions

Р	IN	I/O	DESCRIPTION
NO.	NAME	1/0	DESCRIPTION
1	IN1	I	Digital control to connect COM to NO or NC
2	NO1	I/O	Normally open
3	GND	_	Ground
4	NO2	I/O	Normally open
5	IN2	1	Digital control to connect COM to NO or NC
6	COM2	I/O	Common
7	NC2	I/O	Normally closed
8	VCC	_	Power supply
9	NC1	I/O	Normally closed
10	COM1	I/O	Common

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

			MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽³⁾		-0.5	6.5	V
$V_{NC} V_{NO} V_{COM}$	Analog voltage ⁽³⁾ (4) (5)		-0.5	V _{CC} + 0.5	V
I _K	Analog port diode current	V_{NC} , V_{NO} , $V_{COM} < 0$	-50		mA
I _{NC}	On-state switch current		-200	200	
I _{NO} I _{COM}	On-state peak switch current ⁽⁶⁾	V_{NC} , V_{NO} , $V_{COM} = 0$ to V_{CC}	-400	400	mA
V _{IN}	Digital input voltage (3) (4)		-0.5	6.5	V
I _{IK}	Digital input clamp current	V _I < 0	-50		mA
Icc	Continuous current through V _{CC}	•		100	mA
I _{GND}	Continuous current through GND		-100	100	mA
T _{stg}	Storage temperature		-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

3) All voltages are with respect to ground, unless otherwise specified.

- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.
- 6) Pulse at 1-ms duration < 10% duty cycle

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6.2 ESD Ratings

			VALUE	UNIT
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply LC Voltage	0	5.5	
$V_{NC} \ V_{NO} \ V_{COM}$	Analog voltage	0	V _{CC}	V
V_{IN}	Digital input voltage range	0	V_{CC}	

6.4 Thermal Information

		TS5A23159				
	THERMAL METRIC ⁽¹⁾	DGS (VSSOP)	RSE (UQFN)	UNIT		
		10 PINS	10 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	203.9	180.8			
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.3	117.8			
$R_{\theta JB}$	Junction-to-board thermal resistance	123.9	98.6	°C/W		
ΨЈТ	Junction-to-top characterization parameter	2.1	6.8	C/VV		
ΨЈВ	Junction-to-board characterization parameter	122.5	98.4			
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	_	_			

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.



6.5 Electrical Characteristics for 5-V Supply

 $V_{cc} = 4.5 \text{ V}$ to 5.5 V. $T_{b} = -40^{\circ}\text{C}$ to 85°C (unless otherwise noted)⁽¹⁾

	PARAMETER	TEST CONDI	TIONS	TA	V _{cc}	MIN	TYP	MAX	UNIT
ANALOG SW	ITCH								
V _{COM} V _{NO}	Analog signal range					0		V _{CC}	٧
V _{NC}	Peak ON	$0 \le (V_{NO} \text{ or } V_{NC}) \le V_{CC},$	Switch ON	25°C			0.8	1.1	
R _{peak}	resistance	$I_{\text{COM}} = -100 \text{ mA},$	See Figure 14	Full	4.5 V		0.0	1.5	Ω
D	ON-state	V_{NO} or $V_{NC} = 2.5 \text{ V}$,	Switch ON,	25°C	4.5 V		0.7	0.9	Ω
R _{on}	resistance	$I_{COM} = -100 \text{ mA},$	See Figure 14	Full	4.5 V			1.1	12
ΔR_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 2.5 V, I_{COM} = -100 mA,	Switch ON, See Figure 14	25°C Full	4.5 V		0.05	0.1	Ω
	ON state	$0 \le (V_{NO} \text{ or } V_{NC}) \le V_{CC},$ $I_{COM} = -100 \text{ mA},$	Switch ON, See Figure 14	25°C			0.15		
R _{on(flat)}	ON-state resistance	V_{NO} or $V_{NC} = 1 \text{ V}, 1.5$	0 11 011	25°C	4.5 V		0.1	0.25	Ω
(22)	flatness	V, 2.5 V, I _{COM} = -100 mA,	Switch ON, See Figure 14	Full				0.25	
		V_{NC} or $V_{NO} = 1 V$,		25°C		-20	2	20	
	NC, NO OFF leakage current	$V_{COM} = 1 \text{ V to } 4.5 \text{ V},$ or V_{NC} or $V_{NO} = 4.5 \text{ V},$ $V_{COM} = 1 \text{ V to } 4.5 \text{ V},$	Switch OFF, See Figure 15	Full	5.5 V	-100		100	nA
	OFF leakage culterit	V_{NC} or $V_{NO} = 0$ to 5.5	Switch OFF,	25°C		-1	0.2	1	
I _{NC(PWROFF)} , I _{NO(PWROFF)}		$V_{COM} = 5.5 \text{ V to } 0,$	See Figure 15	Full	0 V	-20		20	μΑ
I _{NO(ON)} ,	NC, NO ON leakage current	V_{NC} or $V_{NO} = 1 V$, $V_{COM} = Open$, or	Switch ON, See Figure 16	25°C	5.5 V	-20	2	20	nA
I _{NC(ON)}		V_{NC} or $V_{NO} = 4.5 \text{ V}$, $V_{COM} = \text{Open}$,	IO = 4.5 V,	Full		-100		100	
l	COM OFF leakage	V_{NC} or $V_{NO} = 0$ to 5.5 V ,	Switch OFF,	25°C	0 V	-1	0.1	1	μA
COM(PWROFF)	current	$V_{COM} = 5.5 \text{ V to } 0,$	See Figure 15	Full	O V	-20		20	μΛ
	COM	V_{NC} or V_{NO} = Open,		25°C		-20	2	20	
I _{COM(ON)}	COM ON leakage current	$V_{COM} = 1 \text{ V},$ or $V_{NC} \text{ or } V_{NO} = \text{Open},$ $V_{COM} = 4.5 \text{ V},$	Switch ON, See Figure 16	Full	5.5 V	-100		100	nA
DIGITAL CON	ITROL INPUTS (IN1, IN2)(2)								
V _{IH}	Input logic high			Full		2.4		5.5	V
V _{IL}	Input logic low			Full		0		8.0	V
I _{IH} , I _{IL}	Input leakage current	V _{IN} = 5.5 V or 0		25°C Full	5.5 V	-2 -100		100	nA
DYNAMIC				1	I				
				25°C	5 V	1	8	13	
t _{ON}	Turnon time	$V_{COM} = V_{CC},$ $R_L = 50 \Omega,$	C _L = 35 pF, See Figure 18	Full	4.5 V to 5.5 V	1		16.5	ns
				25°C	5 V	1	5	8	
t _{OFF}	Turnoff time	$V_{COM} = V_{CC},$ $R_L = 50 \Omega,$	C _L = 35 pF, See Figure 18	Full	4.5 V to 5.5 V	1		8	ns

 ⁽¹⁾ The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
 (2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, SCBA004.



Electrical Characteristics for 5-V Supply (continued)

 V_{CC} = 4.5 V to 5.5 V, T_A = -40°C to 85°C (unless otherwise noted)⁽¹⁾

	PARAMETER	TEST COND	OITIONS	T _A	V _{CC}	MIN	TYP	MAX	UNIT
				25°C	5 V	1	5.5	13	
t _{BBM}	Break-before-make time	$V_{NC} = V_{NO} = V_{CC},$ $R_L = 50 \Omega,$	$C_L = 35 \text{ pF},$ See Figure 19	Full	4.5 V to 5.5 V	1		14	ns
Q _C	Charge injection	V _{GEN} = 0, R _{GEN} = 0,	C _L = 1 nF, See Figure 23	25°C	5 V		-7		рС
C _{NC(OFF)} , C _{NO(OFF)}	NC, NO OFF capacitance	V_{NC} or $V_{NO} = V_{CC}$ or GND, Switch OFF,	See Figure 17	25°C	5 V		18		pF
C _{NC(ON)} , C _{NO(ON)}	NC, NO ON capacitance	V_{NC} or $V_{NO} = V_{CC}$ or GND, Switch ON,	See Figure 17	25°C	5 V		55		pF
C _{COM(ON)}	COM ON capacitance	V _{COM} = V _{CC} or GND, Switch ON,	See Figure 17	25°C	5 V		54.5		pF
C _I	Digital input capacitance	$V_{IN} = V_{CC}$ or GND,	See Figure 17	25°C	5 V		2		pF
BW	Bandwidth	$R_L = 50 \Omega$, Switch ON,	See Figure 20	25°C	5 V		100		MHz
O _{ISO}	OFF isolation	$R_L = 50 \Omega$, $f = 1 MHz$,	Switch OFF, See Figure 21	25°C	5 V		-64		dB
X _{TALK}	Crosstalk	$R_L = 50 \Omega$, f = 1 MHz,	Switch ON, See Figure 22	25°C	5 V		-64		dB
THD	Total harmonic distortion	$R_L = 600 \Omega,$ $C_L = 50 \text{ pF},$	f = 20 Hz to 20 kHz, See Figure 24	25°C	5 V	0.0	04%		
SUPPLY									
1	Positive	$V_{IN} = V_{CC}$ or GND,	Switch (INLOR		10	50	nA		
Icc	supply current	VIN = VCC OF GIAD,	OFF	Full	5.5 V			750	ПА

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6.6 Electrical Characteristics for 3.3-V Supply

	AMETER	to 85°C (unless otherwis		т	V	MIN	TYP	MAX	UNIT
		TEST CONL	DITIONS	T _A	V _{cc}	IVIIN	ITP	WAX	UNII
ANALOG SWI									
V _{COM} , V _{NO} , V _{NC}	Analog signal range					0		V _{CC}	V
R _{peak}	Peak ON resistance	$0 \le (V_{NO} \text{ or } V_{NC}) \le V_{CC},$ $I_{COM} = -100 \text{ mA},$	Switch ON, See Figure 14	25°C	3 V		1.3	1.6	Ω
				Full 25°C			1.2	2	
R _{on}	ON-state resistance	V_{NO} or $V_{NC} = 2 V$, $I_{COM} = -100 \text{ mA}$,	Switch ON, See Figure 14	Full	3 V		1.2	1.5	Ω
	ON-state			25°C			0.1	0.15	
ΔR_{on}	resistance match between channels	V_{NO} or $V_{NC} = 2 \text{ V}$, 0.8 V, $I_{COM} = -100 \text{ mA}$,	Switch ON, See Figure 14	Full	3 V		0.2		Ω
	ON-state	$0 \le (V_{NO} \text{ or } V_{NC}) \le V_{CC},$ $I_{COM} = -100 \text{ mA},$	Switch ON, See Figure 14	25°C			0.15		
$R_{on(flat)}$	resistance flatness	V_{NO} or $V_{NC} = 2 \text{ V}, 0.8 \text{ V},$	Switch ON,	25°C	3 V				Ω
	nati icos	$I_{COM} = -100 \text{ mA},$	See Figure 14	Full					
		V_{NC} or $V_{NO} = 1 V$,		25°C		-20	2	20	
I _{NO(OFF)} , I _{NC(OFF)}	NC, NO OFF leakage current	$\begin{split} &V_{COM} = 1 \text{ V to 3 V,}\\ &\text{or}\\ &V_{NC} \text{ or } V_{NO} = 3 \text{ V,}\\ &V_{COM} = 1 \text{ V to 3 V,} \end{split}$	Switch OFF, See Figure 15	Full	3.6 V	-50		50	nA
I _{NC(PWROFF)} ,	Garrone	V_{NC} or $V_{NO} = 0$ to 3.6 V,	Switch OFF,	25°C	0 V	-1	0.2	1	
I _{NO(PWROFF)}		$V_{COM} = 3.6 \text{ V to 0},$	See Figure 15	Full	0 0	-15		15	μA
		V_{NC} or $V_{NO} = 1 V$,		25°C		-10	2	10	
I _{NO(ON)} , I _{NC(ON)}	NC, NO ON leakage current	$V_{COM} = Open,$ or V_{NC} or $V_{NO} = 3 V,$ $V_{COM} = Open,$	Switch ON, See Figure 16	Full	3.6 V	-20		20	nA
	COM		Switch OFF,	25°C		-1	0.2	-	
I _{COM(PWROFF)}	OFF leakage current	V_{NC} or $V_{NO} = 3.6 \text{ V to } 0$, $V_{COM} = 0 \text{ to } 3.6 \text{ V}$,	See Figure 15	Full	0 V	-15		15	μA
		V _{NC} or V _{NO} = Open,		25°C		-10	2	10	
I _{COM(ON)}	COM ON leakage current	$\begin{split} &V_{COM} = 1 \ V, \\ ∨ \\ &V_{NC} \ or \ V_{NO} = Open, \\ &V_{COM} = 3 \ V, \end{split}$	Switch ON, See Figure 16	Full	3.6 V	-20		20	nA
DIGITAL CON	TROL INPUTS (IN	1, IN2) ⁽²⁾							
V _{IH}	Input logic high			Full		2		5.5	V
V _{IL}	Input logic low			Full		0		8.0	V
I _{IH} , I _{IL}	Input leakage	V _{IN} = 5.5 V or 0		25°C	3.6 V	-2		2	nA
'IH' 'IL	current	VIN = 5.5 V 61 6		Full	3.0 V	-20		20	ш
DYNAMIC									
	_	$V_{COM} = V_{CC}$	$C_L = 35 \text{ pF},$	25°C	3.3 V	5	11	19	
t _{ON}	Turnon time	$R_L = 50 \Omega$,	See Figure 18	Full	3 V to 3.6 V	3		22	ns
			25°C	3.3 V	1	5	9		
		$V_{COM} = V_{CC}$	$C_{L} = 35 \text{ pF},$		3 V to				ns
t _{OFF}	Turnoff time	$R_L = 50 \Omega$,	See Figure 18	Full	3.6 V	1		9	
t _{OFF}	Turnoff time Break-before-	$R_L = 50 \Omega$, $V_{NC} = V_{NO} = V_{CC}$,	See Figure 18 C _L = 35 pF,	Full 25°C		1	7	9 17	

 ⁽¹⁾ The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
 (2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, SCBA004.



Electrical Characteristics for 3.3-V Supply (continued)

 V_{CC} = 3 V to 3.6 V, T_A = -40°C to 85°C (unless otherwise noted)⁽¹⁾

PA	RAMETER	TEST COND	TIONS	TA	V _{CC}	MIN TYP M	AX UNIT
Q _C	Charge injection	$V_{GEN} = 0,$ $R_{GEN} = 0,$	C _L = 1 nF, See Figure 23	25°C	3.3 V	-4	рС
C _{NC(OFF)} , C _{NO(OFF)}	NC, NO OFF capacitance	V_{NC} or $V_{NO} = V_{CC}$ or GND, Switch OFF,	See Figure 17	25°C	3.3 V	18	pF
C _{NC(ON)} , C _{NO(ON)}	NC, NO ON capacitance	V_{NC} or $V_{NO} = V_{CC}$ or GND, Switch ON,	See Figure 17	25°C	3.3 V	56	pF
C _{COM(ON)}	COM ON capacitance	V _{COM} = V _{CC} or GND, Switch ON,	See Figure 17	25°C	3.3 V	56	pF
C _I	Digital input capacitance	$V_{IN} = V_{CC}$ or GND,	See Figure 17	25°C	3.3 V	2	pF
BW	Bandwidth	$R_L = 50 \Omega$, Switch ON,	See Figure 20	25°C	3.3 V	100	MHz
O _{ISO}	OFF isolation	$R_L = 50 \Omega$, f = 1 MHz,	Switch OFF, See Figure 21	25°C	3.3 V	-64	dB
X _{TALK}	Crosstalk	$R_L = 50 \Omega$, f = 1 MHz,	Switch ON, See Figure 22	25°C	3.3 V	-64	dB
THD	Total harmonic distortion	$R_L = 600 \ \Omega,$ $C_L = 50 \ pF,$	f = 20 Hz to 20 kHz, See Figure 24	25°C	3.3 V	0.01%	
SUPPLY				•			*
loo	Positive supply	$V_{IN} = V_{CC}$ or GND,	Switch ON or OFF	25°C	3.6 V		25 nA
I _{CC}	current	VIN - VCC OI OIND,	GWILCH CIV OF OFF	Full	5.0 V	1	150

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6.7 Electrical Characteristics for 2.5-V Supply⁽¹⁾

	AMETER	C to 85°C (unless otherwi		TA	V _{cc}	MIN	TYP	MAX	UNIT
ANALOG SWI		1201 00110	1110110	'A	• 66	10.1114		ШАХ	Oitii
V _{COM} , V _{NO} ,	Analog signal								
V _{NC}	range					0		V_{CC}	V
D	Peak ON	$0 \le (V_{NO} \text{ or } V_{NC}) \le V_{CC}$	Switch ON,	25°C	221/		1.8	2.5	Ω
R _{peak}	resistance	$I_{COM} = -8 \text{ mA},$	See Figure 14	Full	2.3 V			2.7	12
D	ON-state	V_{NO} or $V_{NC} = 1.8 \text{ V}$,	Switch ON,	25°C	2.3 V		1.5	2	Ω
R _{on}	resistance	$I_{COM} = -8 \text{ mA},$	See Figure 14	Full	2.5 V			2.4	32
	ON-state			25°C			0.15	0.2	
ΔR_{on}	resistance match between channels	V_{NO} or V_{NC} = 1.8 V, 0.8 V, I_{COM} = -8 mA,	Switch ON, See Figure 14	Full	2.3 V			0.2	Ω
5	ON-state	$0 \le (V_{NO} \text{ or } V_{NC}) \le V_{CC},$ $I_{COM} = -8 \text{ mA},$	Switch ON, See Figure 14	25°C	- 001/		0.6		0
$R_{on(flat)}$	resistance flatness	V_{NO} or $V_{NC} = 0.8 \text{ V}$, 1.8 V,		25°C	2.3 V		0.6	1	Ω
	ı	$I_{COM} = -8 \text{ mA},$	See Figure 14	Full				1	
		V_{NC} or $V_{NO} = 0.5 \text{ V}$,		25°C		-20	2	20	
I _{NO(OFF)} , I _{NC(OFF)}	NC, NO OFF leakage current	$V_{COM} = 0.5 \text{ V to } 2.3 \text{ V,}$ or V_{NC} or $V_{NO} = 2.2 \text{ V,}$ $V_{COM} = 0.5 \text{ V to } 2.3 \text{ V,}$	Switch OFF, See Figure 15	Full	2.3 V	-50		50	nA
I _{NC(PWROFF)} ,	Garrone	V_{NC} or $V_{NO} = 0$ to 2.7 V,	Switch OFF,	25°C	0 V	-1	0.1	1.0	μA
I _{NO(PWROFF)}		$V_{COM} = 2.7 \text{ V to } 0,$	See Figure 15	Full	U V	-10		10	h., ,
	NO NO	V_{NC} or $V_{NO} = 0.5 \text{ V}$,		25°C		-10	2	10	nA
I _{NO(ON)} , I _{NC(ON)}	NC, NO ON leakage current	$V_{COM} = Open,$ or V_{NC} or $V_{NO} = 2.2 V,$ $V_{COM} = Open,$	Switch ON, See Figure 16	Full	2.7 V	-20		20	
	COM	V_{NC} or $V_{NO} = 2.7 \text{ V to } 0$,	Switch OFF,	25°C		-1	0.1	1	
I _{COM(PWROFF)}	OFF leakage current	$V_{COM} = 0 \text{ to } 2.7 \text{ V},$	See Figure 15	Full	0 V	-10		10	μA
		V _{NC} or V _{NO} = Open,		25°C		-10	2	10	
I _{COM(ON)}	COM ON leakage current	$\begin{split} &V_{COM} = 0.5 \text{ V},\\ &\text{or}\\ &V_{NC} \text{ or } V_{NO} = \text{Open},\\ &V_{COM} = 2.2 \text{ V}, \end{split}$	Switch ON, See Figure 16	Full	2.7 V	-20		20	nA
DIGITAL CON	TROL INPUTS (IN	1, IN2) ⁽²⁾							
V_{IH}	Input logic high			Full		1.8		5.5	V
V _{IL}	Input logic low			Full		0		0.6	V
I _{IH} , I _{IL}	Input leakage	V _{IN} = 5.5 V or 0		25°C	2.7 V	-2		2	nA
	current	· IIV		Full		-20		20	
DYNAMIC									
tau	Turnon time	$V_{COM} = V_{CC}$	$C_L = 35 \text{ pF},$	25°C	2.5 V	5	15	28	ns
t _{ON}	rumon time	$R_L = 50 \Omega$,	See Figure 18	Full	2.3 V to 2.7 V	5		32	115
				25°C	2.5 V	2	6	9	
t _{OFF}	Turnoff time	$V_{COM} = V_{CC},$ $R_L = 50 \Omega,$	C _L = 35 pF, See Figure 18	Full	2.3 V to 2.7 V	2		10	ns
	Drook bafara	V V	0 25 -5	25°C	2.5 V	1	10	27	
t _{BBM}	Break-before- make time	$\begin{aligned} &V_{NC} = V_{NO} = V_{CC}, \\ &R_L = 50 \ \Omega, \end{aligned}$	C _L = 35 pF, See Figure 19	Full	2.3 V to 2.7 V	1		30	ns
		i .		1	1				

 ⁽¹⁾ The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
 (2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, SCBA004.



Electrical Characteristics for 2.5-V Supply⁽¹⁾ (continued)

 V_{CC} = 2.3 V to 2.7 V, T_A = -40°C to 85°C (unless otherwise noted)

PARAMETER		TEST COND	ITIONS	TA	V _{CC}	MIN TYP	MAX	UNIT
$Q_{\mathbb{C}}$	Charge injection	$V_{GEN} = 0,$ $R_{GEN} = 0,$	C _L = 1 nF, See Figure 23	25°C	2.5 V	-3		рС
$\begin{matrix} C_{NC(OFF)}, \\ C_{NO(OFF)} \end{matrix}$	NC, NO OFF capacitance	V_{NC} or $V_{NO} = V_{CC}$ or GND, Switch OFF,	See Figure 17	25°C	2.5 V	18.5		pF
C _{NC(ON)} , C _{NO(ON)}	NC, NO ON capacitance	V_{NC} or $V_{NO} = V_{CC}$ or GND, Switch ON,	See Figure 17	25°C	2.5 V	56.5		pF
C _{COM(ON)}	COM ON capacitance	V _{COM} = V _{CC} or GND, Switch ON,	See Figure 17	25°C	2.5 V	56.5		pF
C _I	Digital input capacitance	$V_{IN} = V_{CC}$ or GND,	See Figure 17	25°C	2.5 V	2		pF
BW	Bandwidth	$R_L = 50 \Omega$, Switch ON,	See Figure 20	25°C	2.5 V	100		MHz
O _{ISO}	OFF isolation	$R_L = 50 \Omega$, f = 1 MHz,	Switch OFF, See Figure 21	25°C	2.5 V	-64		dB
X _{TALK}	Crosstalk	$R_L = 50 \Omega$, f = 1 MHz,	Switch ON, See Figure 22	25°C	2.5 V	-64		dB
THD	Total harmonic distortion	$R_L = 600 \Omega,$ $C_L = 50 pF,$	f = 20 Hz to 20 kHz, See Figure 24	25°C	2.5 V	0.02%		
SUPPLY								
la a	Positive supply	$V_{IN} = V_{CC}$ or GND,	Switch ON or OFF	25°C	2.7 V	10	25	nA
I _{CC}	current	AIM - ACC OL CLAD	GWILLII ON OI OIT	Full	Z.1 V		100	ш

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6.8 Electrical Characteristics for 1.8-V Supply

 V_{CC} = 1.65 V to 1.95 V, T_A = -40°C to 85°C (unless otherwise noted)⁽¹⁾

PAR	AMETER	TEST COND	TIONS	T _A	V _{CC}	MIN	TYP	MAX	UNIT
ANALOG SWI	тсн	•							
V _{COM} , V _{NO} , V _{NC}	Analog signal range					0		V _{CC}	V
R _{peak}	Peak ON resistance	$0 \le (V_{NO} \text{ or } V_{NC}) \le V_{CC},$ $I_{COM} = -2 \text{ mA},$	Switch ON, See Figure 14	25°C Full	1.65 V		5	15	Ω
R _{on}	ON-state resistance	V_{NO} or $V_{NC} = 1.5 \text{ V}$, $I_{COM} = -2 \text{ mA}$,	Switch ON, See Figure 14	25°C Full	1.65 V		2	2.5	Ω
	ON-state			25°C			0.15	0.4	
ΔR_{on}	resistance match between channels	V_{NO} or $V_{NC} = 0.6 \text{ V}$, 1.5 V, $I_{COM} = -2 \text{ mA}$,	Switch ON, See Figure 14	Full	1.65 V		0.10	0.4	Ω
	ON-state	$0 \le (V_{NO} \text{ or } V_{NC}) \le V_{CC},$ $I_{COM} = -2 \text{ mA},$	Switch ON, See Figure 14	25°C	4.05.1/		5		•
$R_{on(flat)}$	resistance flatness	V_{NO} or $V_{NC} = 0.6 \text{ V}$, 1.5 V,		25°C	1.65 V		4.5		Ω
		$I_{COM} = -2 \text{ mA},$	See Figure 14	Full					
		V_{NC} or $V_{NO} = 0.3 \text{ V}$,		25°C		-20	2	20	
I _{NO(OFF)} , I _{NC(OFF)}	NC, NO OFF leakage	$V_{COM} = 0.3 \text{ V to } 1.65 \text{ V},$ or V_{NC} or $V_{NO} = 1.65 \text{ V},$ $V_{COM} = 0.3 \text{ V to } 1.65 \text{ V}$	Switch OFF, See Figure 15	Full	1.65 V	-50		50	nA
hio(purposs)	current	V_{NC} or $V_{NO} = 0$ to	Switch OFF,	25°C	0 V	-1	0.1	1	
I _{NC(PWROFF)} , I _{NO(PWROFF)}		1.95 V, $V_{COM} = 1.95 V \text{ to } 0$,	See Figure 15	Full		- 5		5	μΑ
		V_{NC} or $V_{NO} = 0.3 \text{ V}$,		25°C		-5	2	5	
I _{NO(ON)} , I _{NC(ON)}	NC, NO ON leakage current	V_{COM} = Open, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = Open,	Switch ON, See Figure 16	Full	1.95 V	-20		20	nA
	COM	V_{NC} or $V_{NO} = 1.95 \text{ V to } 0$	Switch OFF, See Figure 15	25°C		-1	0.1	1	
I _{COM(PWROFF)}	OFF leakage current	$V_{\text{COM}} = 0 \text{ to } 1.95 \text{ V},$		Full	0 V	-5		5	μA
		V _{NC} or V _{NO} = Open,		25°C		-10	2	10	
I _{COM(ON)}	COM ON leakage current	$V_{COM} = 0.3 \text{ V},$ or $V_{NC} \text{ or } V_{NO} = \text{Open},$ $V_{COM} = 1.65 \text{ V},$	Switch ON, See Figure 16	Full	1.95 V	-20		20	nA
DIGITAL CON	TROL INPUTS (IN	1, IN2)							
V_{IH}	Input logic high			Full		1.5		5.5	V
V_{IL}	Input logic low			Full		0		0.6	V
L. L.	Input leakage	V _{IN} = 5.5 V or 0		25°C	1.95 V	-2		2	nA
I _{IH} , I _{IL}	current	VIN = 5.5 V 01 0		Full	1.95 V	-20		20	IIA
DYNAMIC					T T			-	
		.,		25°C	1.8 V	10	27.5	48.5	
t _{ON}	Turnon time	$V_{COM} = V_{CC},$ $R_L = 50 \Omega,$	C _L = 35 pF, See Figure 18	Full	1.65 V to 1.95 V	10		55	ns
				25°C	1.8 V	2	6.5	11	
t _{OFF}	Turnoff time	$\begin{aligned} &V_{COM} = V_{CC}, \\ &R_L = 50~\Omega, \end{aligned}$	C _L = 35 pF, See Figure 18	Full	1.65 V to 1.95 V	2		12	ns

⁽¹⁾ The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum



Electrical Characteristics for 1.8-V Supply (continued)

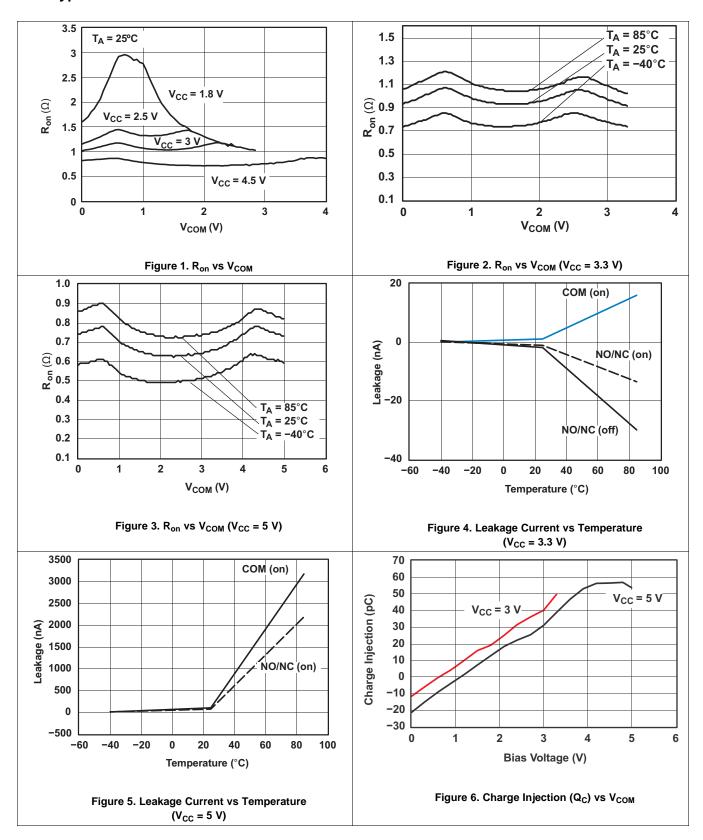
 V_{CC} = 1.65 V to 1.95 V, T_A = -40°C to 85°C (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CON	TA	V _{cc}	MIN	TYP	MAX	UNIT	
				25°C	1.8 V	1	18	50	
t _{BBM}	Break-before- make time	$\begin{aligned} V_{NC} &= V_{NO} = V_{CC}, \\ R_L &= 50 \ \Omega, \end{aligned}$	C _L = 35 pF, See Figure 19	Full	1.65 V to 1.95 V	1		55	ns
$Q_{\mathbb{C}}$	Charge injection	V _{GEN} = 0, R _{GEN} = 0,	$C_L = 1 \text{ nF},$ See Figure 23	25°C	1.8 V		2		рС
C _{NC(OFF)} , C _{NO(OFF)}	NC, NO OFF capacitance	V _{NC} or V _{NO} = V _{CC} or GND, Switch OFF,	See Figure 17	25°C	1.8 V		18.5		pF
C _{NC(ON)} , C _{NO(ON)}	NC, NO ON capacitance	V_{NC} or $V_{NO} = V_{CC}$ or GND, Switch ON,	See Figure 17	25°C	1.8 V		56.5		pF
C _{COM(ON)}	COM ON capacitance	V _{COM} = V _{CC} or GND, Switch ON,	See Figure 17	25°C	1.8 V		56.5		pF
C _I	Digital input capacitance	$V_{IN} = V_{CC}$ or GND,	See Figure 17	25°C	1.8 V		2		pF
BW	Bandwidth	$R_L = 50 \Omega$, Switch ON,	See Figure 20	25°C	1.8 V		105		MHz
O _{ISO}	OFF isolation	$R_L = 50 \Omega$, f = 1 MHz,	Switch OFF, See Figure 21	25°C	1.8 V		-64		dB
X _{TALK}	Crosstalk	$R_L = 50 \Omega$, f = 1 MHz,	Switch ON, See Figure 22	25°C	1.8 V		-64		dB
THD	Total harmonic distortion	$R_L = 600 \Omega,$ $C_L = 50 pF,$	f = 20 Hz to 20 kHz, See Figure 24	25°C	1.8 V		0.06%		
SUPPLY					'			'	
1	Positive supply	$V_{IN} = V_{CC}$ or GND,	Switch ON or OFF	25°C	1.95 V		10	25	nA
I _{CC}	current	VIN - VCC OI GIVD,	SWILCH ON OF OFF	Full	1.95 V			50	IIA

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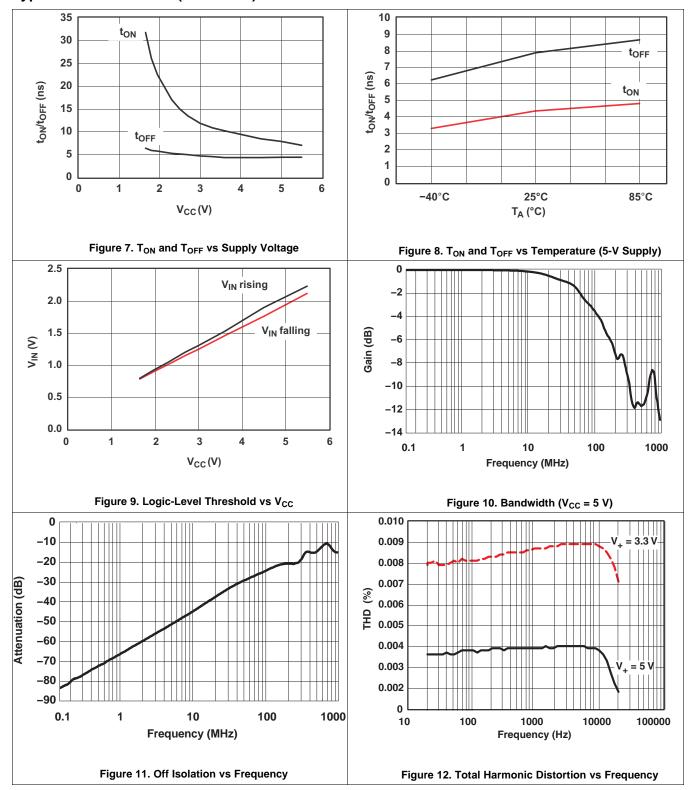


6.9 Typical Characteristics



TEXAS INSTRUMENTS

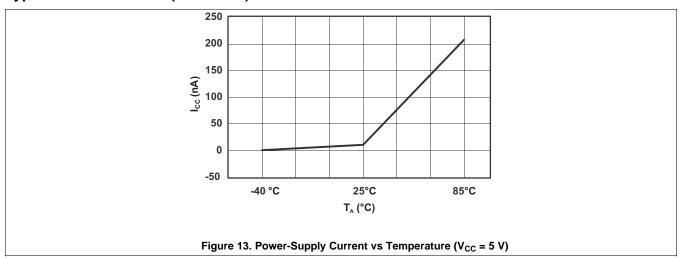
Typical Characteristics (continued)



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Typical Characteristics (continued)





7 Parameter Measurement Information

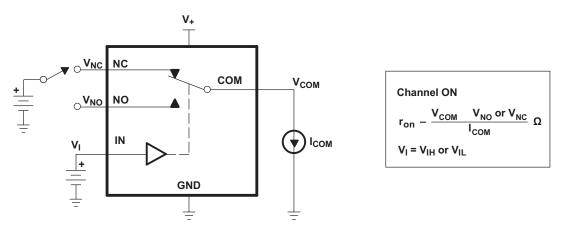


Figure 14. ON-State Resistance (Ron)

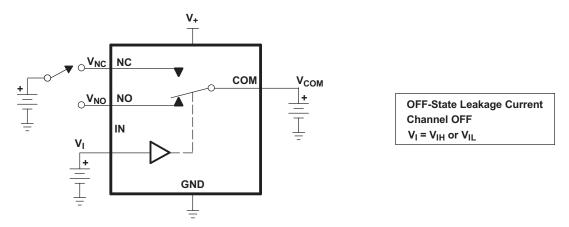


Figure 15. OFF-State Leakage Current (I_{NC(OFF)}, I_{NC(PWROFF)}, I_{NO(OFF)}, I_{NO(PWROFF)}, I_{COM(PWROFF)})

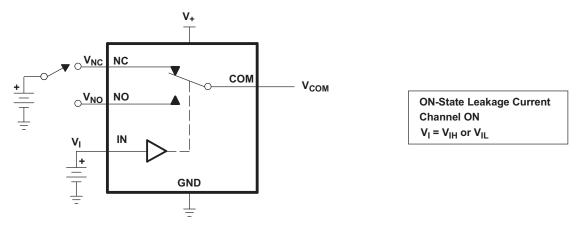


Figure 16. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

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Parameter Measurement Information (continued)

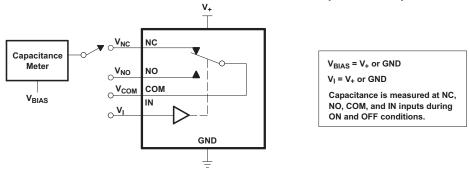
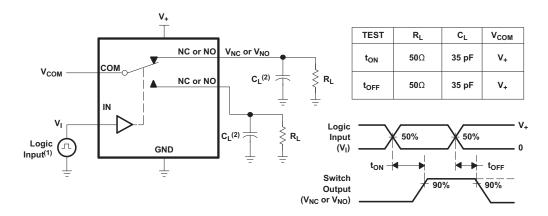
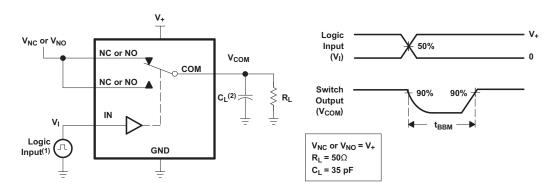


Figure 17. Capacitance (C_I, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)



- 1. All input pulses are supplied by generators having the following characteristics:
- PRR 3 10 MHz, Z_O = 50 Ω , t_r < 5 ns, t_f < 5 ns.
- 2. C_L includes probe and jig capacitance.

Figure 18. Turnon (T_{ON}) and Turnoff Time (T_{OFF})

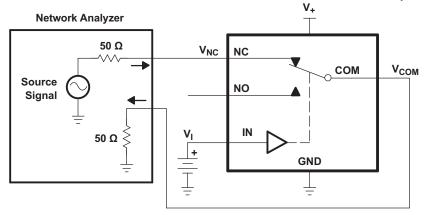


- 1. All input pulses are supplied by generators having the following characteristics:
- PRR 3 10 MHz, Z_O = 50 Ω , t_r < 5 ns, t_f < 5 ns.
- 2. C_L includes probe and jig capacitance.

Figure 19. Break-Before-Make Time (T_{BBM})



Parameter Measurement Information (continued)



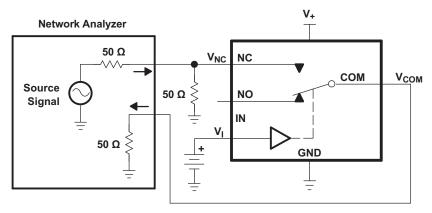
Channel ON: NC to COM $V_1 = V_+$ or GND

Network Analyzer Setup

Source Power = 0 dBm(632-mV P-P at $50-\Omega \text{ load}$)

DC Bias = 350 mV

Figure 20. Bandwidth (Bw)



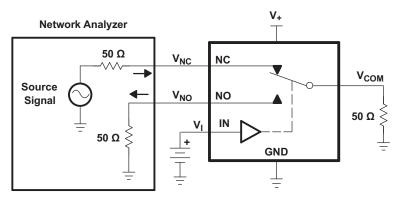
Channel OFF: NC to COM V_I = V₊ or GND

Network Analyzer Setup

Source Power = 0 dBm(632-mV P-P at $50-\Omega \text{ load}$)

DC Bias = 350 mV

Figure 21. Off Isolation (O_{ISO})



Channel ON: NC to COM Channel OFF: NO to COM $V_1 = V_+$ or GND

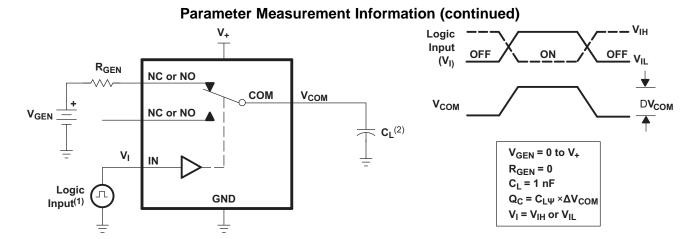
Network Analyzer Setup

Source Power = 0 dBm (632-mV P-P at $50-\Omega$ load)

DC Bias = 350 mV

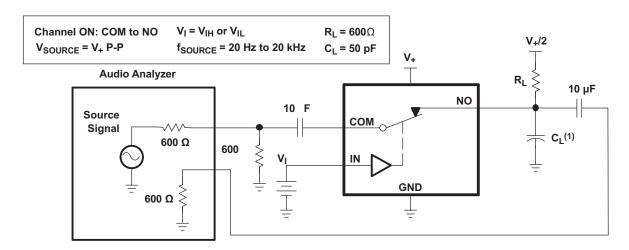
Figure 22. Crosstalk (X_{TALK})





- 1. All input pulses are supplied by generators having the following characteristics: PRR 3 10 MHz, Z_O = 50 Ω , t_r < 5 ns, t_f < 5 ns.
- 2. C_L includes probe and jig capacitance.

Figure 23. Charge Injection (Q_C)



1. C_L includes probe and jig capacitance.

Figure 24. Total Harmonic Distortion (THD)



Parameter Measurement Information (continued) Table 1. Parameter Description

SYMBOL	DESCRIPTION
V _{COM}	Voltage at COM
V _{NC}	Voltage at NC
V _{NO}	Voltage at NO
R _{on}	Resistance between COM and NC or COM and NO ports when the channel is ON
R _{peak}	Peak on-state resistance over a specified voltage range
ΔR _{on}	Difference of R _{on} between channels in a specific device
R _{on(flat)}	Difference between the maximum and minimum value of R _{on} in a channel over the specified range of conditions
I _{NC(OFF)}	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions
I _{NC(PWROFF)}	Leakage current measured at the NC port during the power-down condition, V _{CC} = 0
I _{NO(OFF)}	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions
I _{NO(PWROFF)}	Leakage current measured at the NO port during the power-down condition, V _{CC} = 0
I _{NC(ON)}	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
I _{NO(ON)}	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
I _{COM(ON)}	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open
I _{COM(PWROFF)}	Leakage current measured at the COM port during the power-down condition, $V_{CC} = 0$
V _{IH}	Minimum input voltage for logic high for the control input (IN)
V _{IL}	Maximum input voltage for logic low for the control input (IN)
V _{IN}	Voltage at the control input (IN)
I _{IH} , I _{IL}	Leakage current measured at the control input (IN)
t _{ON}	Turnon time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning ON.
t _{OFF}	Turnoff time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning OFF.
t _{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
Q _C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$. C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.
C _{NC(OFF)}	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
C _{NO(OFF)}	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
C _{NC(ON)}	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
C _{NO(ON)}	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
C _{COM(ON)}	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
Cı	Capacitance of control input (IN)
O _{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
X _{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is -3 dB below the DC gain.
THD	Total harmonic distortion is defined as the ratio of the root mean square (RMS) value of the second, third, and higher harmonics to the magnitude of fundamental harmonic.
I _{CC}	Static power-supply current with the control (IN) pin at V _{CC} or GND

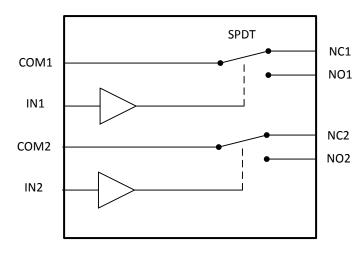


8 Detailed Description

8.1 Overview

The TS5A23159 is a bidirectional 2-channel single-pole double-throw (SPDT) switch that is designed to operate from 1.65 V to 5.5 V. The device offers low ON-state resistance and excellent ON-state resistance matching with the break-before-make feature which prevents signal distortion during the transferring of a signal from one channel to another. The device has an excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for a wide variety of portable applications including cell phones, audio devices, and instrumentation.

8.2 Functional Block Diagram



8.3 Feature Description

The TS5A23159 is a bidirectional device that has two single-pole, double-throw switches. The two channels of the switch are contorled independently by two digital signals; one digital control for each single-pole, double-throw switch.

8.4 Device Functional Modes

Table 2. Function Table

IN	NC to COM, COM to NC	NO to COM, COM to NO
L	ON	OFF
Н	OFF	ON



9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The switches are bidirectional, so the NO, NC, and COM pins can be used as either inputs or outputs.

9.2 Typical Application

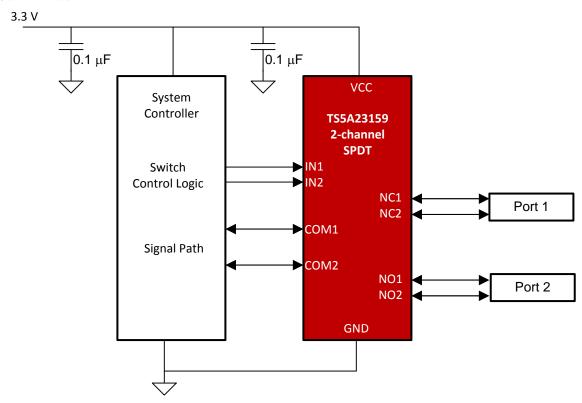


Figure 25. Typical Application Diagram

9.2.1 Design Requirements

Ensure that all of the signals passing through the switch are within the specified ranges in the recommended operating conditions to ensure proper performance.

9.2.2 Detailed Design Procedure

The TS5A23159 can be properly operated without any external components. However, TI recommends connecting unused pins to ground through a $50-\Omega$ resistor to prevent signal reflections back into the device. TI also recommends that the digital control pins (INX) be pulled up to VCC or down to GND to avoid undesired switch positions that could result from the floating pin.



Typical Application (continued)

9.2.3 Application Curve

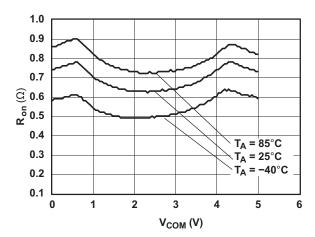


Figure 26. R_{on} vs V_{COM} ($V_{CC} = 5$ V)

10 Power Supply Recommendations

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence VCC on first, followed by NO, NC, or COM. Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the VCC supply to other components. A 0.1-µF capacitor, connected from VCC to GND, is adequate for most applications.



11 Layout

11.1 Layout Guidelines

High-speed switches require proper layout and design procedures for optimum performance. Reduce stray inductance and capacitance by keeping traces short and wide. Ensure that bypass capacitors are as close to the device as possible. Use large ground planes where possible.

11.2 Layout Example



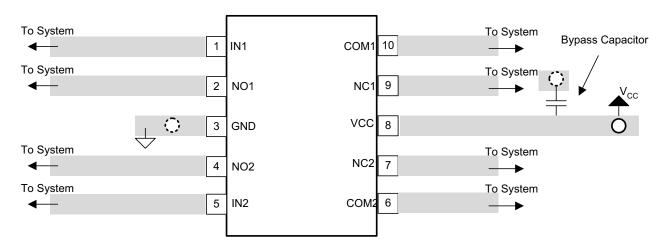


Figure 27. Layout Recommendation

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12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com 10-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
TS5A23159DGSR	Active	Production	VSSOP (DGS) 10	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(JEQ, JER)
TS5A23159DGSR.B	Active	Production	VSSOP (DGS) 10	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(JEQ, JER)
TS5A23159RSER	Active	Production	UQFN (RSE) 10	3000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(JE7, JEO, JER, JE V)
TS5A23159RSER.B	Active	Production	UQFN (RSE) 10	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(JE7, JEO, JER, JE V)

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE MATERIALS INFORMATION

www.ti.com 7-Oct-2025

TAPE AND REEL INFORMATION





	-
A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A23159DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TS5A23159RSER	UQFN	RSE	10	3000	180.0	9.5	1.7	2.2	0.75	4.0	8.0	Q1
TS5A23159RSER	UQFN	RSE	10	3000	180.0	9.5	1.7	2.3	0.75	4.0	8.0	Q1

www.ti.com 7-Oct-2025



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A23159DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TS5A23159RSER	UQFN	RSE	10	3000	189.0	185.0	36.0
TS5A23159RSER	UQFN	RSE	10	3000	184.0	184.0	19.0



SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-187, variation BA.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



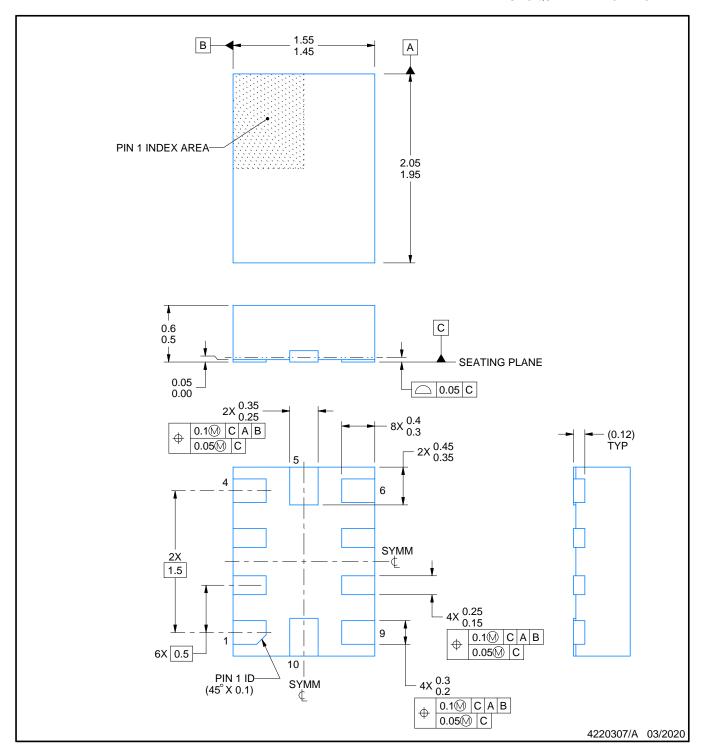
NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





PLASTIC QUAD FLATPACK - NO LEAD

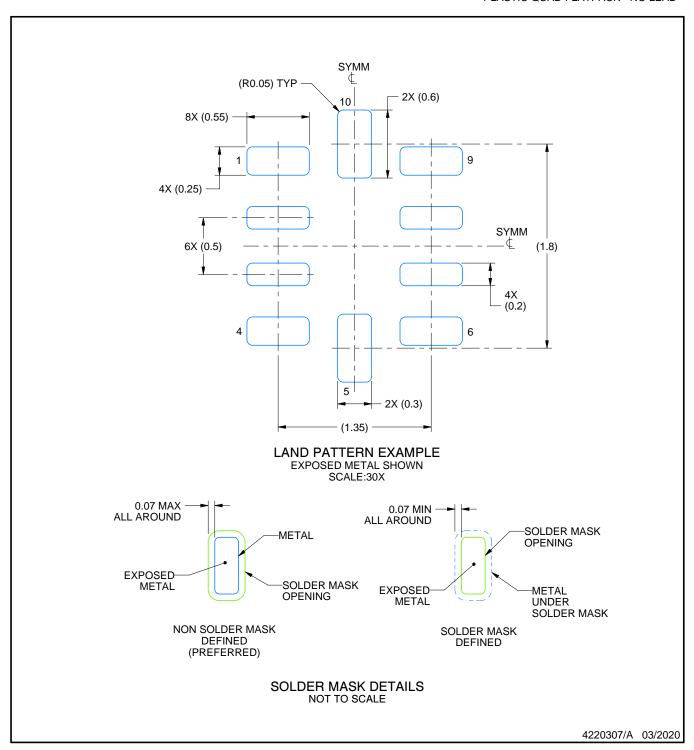


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



PLASTIC QUAD FLATPACK - NO LEAD

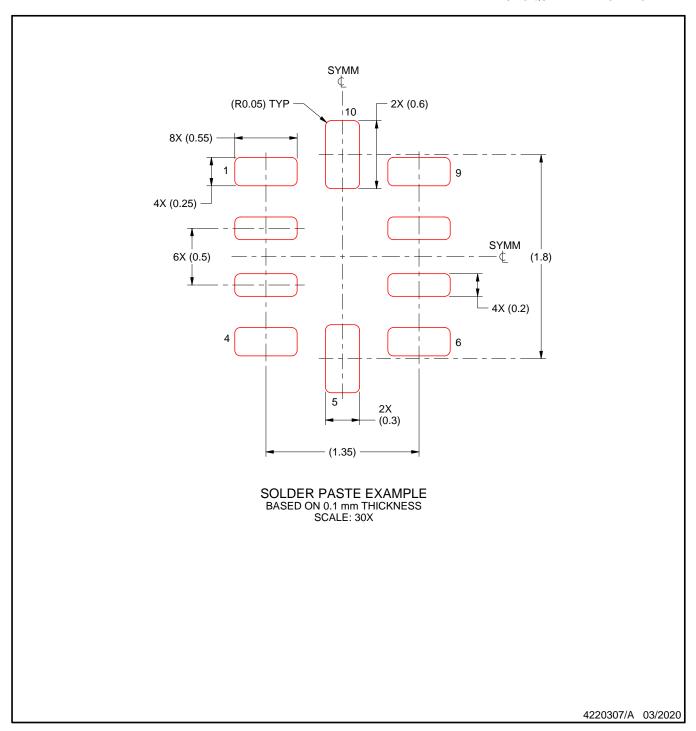


NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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