

















TS5A23157

SCDS165F - MAY 2004 - REVISED JANUARY 2019

TS5A23157 Dual 10-Ω SPDT Analog Switch

Features

- Low ON-State Resistance (15 Ω at 125°C)
- 125°C Operation
- Control Inputs are 5-V Tolerant
- Specified Break-Before-Make Switching
- Low Charge Injection
- **Excellent ON-Resistance Matching**
- Low Total Harmonic Distortion
- 1.8-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)

Applications

- Sample-and-Hold Circuits
- **Battery-Powered Equipment**
- Audio and Video Signal Routing
- Communication Circuits

Description

The TS5A23157 device is a dual single-pole doublethrow (SPDT) analog switch designed to operate from 1.65 V to 5.5 V. This device can handle both digital and analog signals. Signals up to 5.5 V (peak) can be transmitted in either direction.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A23157DGS	VSSOP (10)	3.00 mm × 3.00 mm
TS5A23157RSE	UQFN (10)	2.00 mm × 1.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram

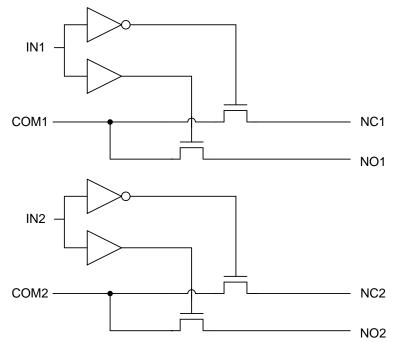




Table of Contents

1	Features 1	8.2 Functional Block Diagram 1
2	Applications 1	8.3 Feature Description 1
3	Description 1	8.4 Device Functional Modes 1
4	Revision History2	9 Application and Implementation 1
5	Pin Configuration and Functions	9.1 Application Information 1
6	Specifications	9.2 Typical Application1
U	6.1 Absolute Maximum Ratings	10 Power Supply Recommendations 1
	6.2 ESD Ratings	11 Layout1
	6.3 Recommended Operating Conditions	11.1 Layout Guidelines 1
	6.4 Thermal Information	11.2 Layout Example 1
	6.5 Electrical Characteristics for 5-V Supply	12 Device and Documentation Support 2
	6.6 Electrical Characteristics for 3.3-V Supply	12.1 Device Support
	6.7 Electrical Characteristics for 2.5-V Supply	12.2 Documentation Support
	6.8 Electrical Characteristics for 1.8-V Supply	12.3 Community Resources 2
	6.9 Typical Characteristics	12.4 Trademarks 2
7	Parameter Measurement Information	12.5 Electrostatic Discharge Caution 2
8	Detailed Description	12.6 Glossary 2
	8.1 Overview	13 Mechanical, Packaging, and Orderable Information

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

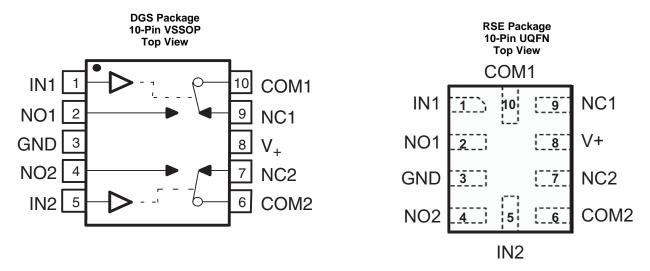
CI	hanges from Revision E (June 2015) to Revision F	Page
•	Changed Feature From: Low ON-State Resistance (10 Ω) To: Low ON-State Resistance (15 Ω at 125°C)	1
•	Added Feature: 125°C Operation	1
•	Added Junction Temperature To the Absolute Maximum Ratings table	4
•	Changed the Operating temperature MAX value From: 85°C To: 125°C in the Recommended Operating Conditions table	
•	Changed the Thermal Information table	4
•	Changed r _{on} in the Electrical Characteristics for 5-V Supply table	5
•	Changed V _{IH} in the <i>Electrical Characteristics for 5-V Supply</i> table	5
•	Changed t _{ON} and t _{OFF} in the <i>Electrical Characteristics for 5-V Supply</i> table	5
•	Changed r _{on} in the <i>Electrical Characteristics for 3.3-V Supply</i> table	<mark>7</mark>
•	Changed t _{ON} and t _{OFF} in the <i>Electrical Characteristics for 3.3-V Supply</i> table	<mark>7</mark>
•	Changed r _{on} in the <i>Electrical Characteristics for 2.5-V Supply</i> table	8
•	Changed t _{ON} and t _{OFF} in the <i>Electrical Characteristics for 2.5-V Supply</i> table	8
•	Changed r _{on} in the <i>Electrical Characteristics for 1.8-V Supply</i> table	9
•	Changed t _{ON} and t _{OFF} in the <i>Electrical Characteristics for 1.8-V Supply</i> table	

Changes from Revision D (October 2013) to Revision E

Page



5 Pin Configuration and Functions



Pin Functions

PIN		1/0	DESCRIPTION				
NO.	NAME	1/0	DESCRIPTION				
1	IN1	I	Select pin for switch 1				
2	NO1	I/O	Normally open I/O for switch 1				
3	GND	_	Ground				
4	NO2	I/O	Normally open I/O for switch 2				
5	IN2	I	Select pin for switch 2				
6	COM2	I/O	Common I/O for switch 2				
7	NC2	I/O	Normally closed I/O for switch 2				
8	V+	_	Power supply pin				
9	NC1	I/O	Normally closed I/O for switch 1				
10	COM1	I/O	Common I/O for switch 1				



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V ₊	Supply voltage ⁽²⁾		-0.5	6.5	V
$V_{NC} \ V_{NO} \ V_{COM}$	Analog voltage (2)(3)(4)		-0.5	V ₊ + 0.5	٧
I _{I/OK}	Analog port diode current	V_{NC} , V_{NO} , $V_{COM} < 0$ or V_{NC} , V_{NO} , $V_{COM} > V_{+}$		±50	mA
I _{NC} I _{NO} I _{COM}	On-state switch current	V_{NC} , V_{NO} , $V_{COM} = 0$ to V_{+}		±50	mA
V_{IN}	Digital input voltage (2)(3)		-0.5	6.5	V
I_{IK}	Digital input clamp current	V _{IN} < 0		-50	mA
	Continuous current through V+ or GND			±100	mA
TJ	Junction Temperature			150	°C
T _{stg}	Storage temperature		- 65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V	Electrostatic	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
V _(ESD)	discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{I/O}	Switch input/output voltage	0	V_{+}	V
V+	Supply voltage	1.65	5.5	V
VI	Control input voltage	0	5.5	V
T _A	Operating temperature	-40	125	°C

6.4 Thermal Information

		TS5A2	TS5A23157				
	THERMAL METRIC ⁽¹⁾	DGS (VSSOP)	RSE (UQFN)	UNIT			
		10 PINS	10 PINS				
$R_{\theta JA}$	Junction-to-ambient thermal resistance	210.5	215.4	°C/W			
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	99.1	140.2	°C/W			
$R_{\theta JB}$	Junction-to-board thermal resistance	132.4	137.9	°C/W			
ΨЈТ	Junction-to-top characterization parameter	29.1	13.7	°C/W			
ΨЈВ	Junction-to-board characterization parameter	130.5	137.6	°C/W			

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

⁽²⁾ All voltages are with respect to ground, unless otherwise specified.

⁽³⁾ The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

⁴⁾ This value is limited to 5.5 V maximum.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



6.5 Electrical Characteristics for 5-V Supply

 $V_{+} = 4.5 \text{ V}$ to 5.5 V, $T_{A} = -40 ^{\circ}\text{C}$ to 85 $^{\circ}\text{C}$ (unless otherwise noted)

l l	PARAMETER	TEST CON	IDITIONS	T _A	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT	
ANALOG S	WITCH									
V _{COM} , V _{NO} , V _{NC}	Analog signal range					0		V ₊	٧	
		0 < \/ or \/ < \/	Switch ON,	Full				10		
r _{on}	ON-state resistance	$0 \le V_{NO} \text{ or } V_{NC} \le V_+,$ $I_{COM} = -30 \text{ mA},$	see Figure 9	-40 to 125°C	4.5 V			15	Ω	
Δr_{on}	ON-state resistance match between channels	V_{NO} or $V_{NC} = 3.15 \text{ V}$, $I_{COM} = -30 \text{ mA}$,	Switch ON, see Figure 9	25°C	4.5 V		0.15		Ω	
r _{on(flat)}	ON-state resistance flatness	$0 \le V_{NO} \text{ or } V_{NC} \le V_+,$ $I_{COM} = -30 \text{ mA},$	Switch ON, see Figure 9	25°C	4.5 V		4		Ω	
I _{NC(OFF)} , I _{NO(OFF)}	NC, NO OFF leakage current	V_{NC} or $V_{NO} = 0$ to V_+ , $V_{COM} = 0$ to V_+ ,	Switch OFF, see Figure 10	25°C Full	5.5 V	-1 -1	0.05	1	μΑ	
	NC, NO	V_{NC} or $V_{NO} = 0$ to V_+ ,	Switch ON,	25°C		-0.1		0.1		
I _{NC(ON)} , I _{NO(ON)}	ON leakage current	$V_{COM} = Open,$	see Figure 10	Full	5.5 V	-1		1	μΑ	
	COM	V _{NC} or V _{NO} = Open,	Switch ON,	25°C	5 5 \/	-0.1		0.1		
I _{COM(ON)}	ON leakage current	$V_{COM} = 0$ to V_+ ,	see Figure 10	Full	5.5 V	-1		1	μA	
DIGITAL IN	PUTS (IN12, IN2) ⁽²⁾									
				Full		$V_{+} \times 0.7$				
V _{IH}	Input logic high			-40 to 125°C	4.75 V to 5.25 V	3.1			V	
V _{IL}	Input logic low			Full				V ₊ × 0.3	V	
	land lanks are summed	V 55V0		25°C	5.5.1/	-1	0.05	1		
I _{IH} , I _{IL}	Input leakage current	$V_{IN} = 5.5 \text{ V or } 0$		Full 5.5 V —1	-1		1	μA		
DYNAMIC										
			V_{NC} = GND and V_{NO} = V_{+}	$R_L = 500 \Omega$,	Full	4.5 V to 5.5 V	1.7		5.7	ns
t _{ON}	Turnon time	or $V_{NC} = V_{+}$ and $V_{NO} = GND$,	C _L = 50 pF, see Figure 12	-40 to 125°C	4.75 V to 5.25 V	1.2		8.7	ns	
		V_{NC} = GND and V_{NO} = V_{+}	$R_{L} = 500 \Omega$	Full	4.5 V to 5.5 V	0.8		3.8	ns	
t _{OFF}	Turnoff time	or $V_{NC} = V_{+}$ and $V_{NO} = GND$,	C _L = 50 pF, see Figure 12	-40 to 125°C	4.75 V to 5.25 V	0.5		6.8	ns	
t _{BBM}	Break-before-make time	$V_{NC} = V_{NO} = V_{\downarrow}/2,$ $R_L = 50 \Omega,$	C _L = 35 pF, see Figure 13	Full	4.5 V to 5.5 V	0.5			ns	
Q_C	Charge injection	$V_{NC} = V_{NO} = V_{+}/2,$ $R_{L} = 50 \Omega,$	See Figure 17	25°C	5 V		7		рС	
$C_{NC(OFF)},$ $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or $V_{NO} = V_{+}$ or GND,	Switch OFF, see Figure 11	25°C	5 V		5.5		pF	
C _{NC(ON)} , C _{NO(ON)}	NC, NO ON capacitance	V_{NC} or $V_{NO} = V_{+}$ or GND,	Switch ON, see Figure 11	25°C	5 V		17.5		pF	
C _{COM(ON)}	COM ON capacitance	$V_{COM} = V_{+}$ or GND,	Switch ON, see Figure 11	25°C	5 V		17.5		pF	
C _{IN}	Digital input capacitance	$V_{IN} = V_{+}$ or GND,	See Figure 11	25°C	5 V		2.8		pF	
BW	Bandwidth	$R_1 = 50 \Omega$,	Switch ON, see Figure 14	25°C	4.5 V		220		MHz	

 ⁽¹⁾ T_A = 25°C.
 (2) All unused digital inputs of the device must be held at V₊ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.



Electrical Characteristics for 5-V Supply (continued)

 $V_{+} = 4.5 \ V$ to 5.5 V, $T_{A} = -40 ^{\circ} C$ to 85 $^{\circ} C$ (unless otherwise noted)

	PARAMETER	TEST CONDITIONS			V ₊	MIN TYP ⁽¹⁾	IAX	UNIT
O _{ISO}	OFF isolation	$R_L = 50 \Omega$, f = 10 MHz,	Switch OFF, see Figure 15	25°C	4.5 V	-65		dB
X _{TALK}	Crosstalk	$R_L = 50 \Omega$, f = 10 MHz,	Switch ON, see Figure 16	25°C	4.5 V	-66	dB	
THD	Total harmonic distortion	$R_L = 600 \Omega,$ $C_L = 50 pF,$	f = 600 Hz to 20 kHz, see Figure 18	25°C	4.5 V	0.01%		
SUPPLY								
	Positive supply	V V or CND	Switch ON or OFF	25°C	E E V		1	
1+	current	$V_{IN} = V_{+} \text{ or GND},$	SWILCTI ON OF OFF	Full	5.5 V		10	μA
Δl_{+}	Change in supply current	$V_{IN} = V_{+} - 0.6 \text{ V}$		Full	5.5 V		500	μΑ

Submit Documentation Feedback



6.6 Electrical Characteristics for 3.3-V Supply

 $V_{+} = 3 \text{ V to } 3.6 \text{ V}, T_{A} = -40^{\circ}\text{C} \text{ to } 85^{\circ}\text{C} \text{ (unless otherwise noted)}$

	PARAMETER	TEST CON	DITIONS	T _A	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
ANALOG	SWITCH								
V_{COM}, V_{NO}	' Analog signal range					0		V ₊	V
		$0 \le V_{NO} \text{ or } V_{NC} \le V_+,$	Switch ON,	Full				18	
r _{on}	ON-state resistance	$I_{\text{COM}} = -24 \text{ mA},$	see Figure 9	-40 to 125°C	3 V			23	Ω
Δr_{on}	ON-state resistance match between channels	V_{NO} or $V_{NC} = 2.1 \text{ V}$, $I_{COM} = -24 \text{ mA}$,	Switch ON, see Figure 9	25°C	3 V		0.2		Ω
r _{on(flat)}	ON-state resistance flatness	$0 \le V_{NO} \text{ or } V_{NC} \le V_+,$ $I_{COM} = -24 \text{ mA},$	Switch ON, see Figure 11	25°C	3 V		9		Ω
I _{NC(OFF)} ,	NC, NO	V_{NC} or $V_{NO} = 0$ to V_+ ,	Switch OFF,	25°C	3.6 V	-1	0.05	1	μA
I _{NO(OFF)}	OFF leakage current	$V_{COM} = 0 \text{ to } V_+,$	see Figure 10	Full	3.0 V	-1		1	μ/ι
I _{NC(ON)} ,	NC, NO	V_{NC} or $V_{NO} = 0$ to V_+ ,	Switch ON,	25°C	3.6 V	-0.1		0.1	μA
I _{NO(ON)}	ON leakage current	V _{COM} = Open,	see Figure 10	Full	3.0 V	-1		1	μΛ
I _{COM(ON)}	COM	V_{NC} or V_{NO} = Open,	Switch ON,	25°C	3.6 V	-0.1		0.1	μA
	ON leakage current	$V_{COM} = 0 \text{ to } V_+,$	see Figure 10	Full	3.3 v	-1		1	μ,,
	NPUTS (IN12, IN2) ⁽²⁾	I							
V _{IH}	Input logic high			Full		V ₊ × 0.7			V
V_{IL}	Input logic low			Full				V ₊ × 0.3	V
L. L.	Input lookage current	V _{IN} = 5.5 V or 0		25°C	3.6 V	-1	0.05	1	
I _{IH} , I _{IL}	Input leakage current	VIN = 3.3 V 01 0		Full	3.0 V	-1		1	μΑ
DYNAMIC								1	
		$V_{NC} = GND$ and $V_{NO} = V_{+}$	$R_L = 500 \Omega$	Full	3 V to	2.5		7.6	ns
t _{ON}	Turn-on time	or $V_{NC} = V_{+}$ and $V_{NO} = GND$,	C _L = 50 pF, see Figure 12	-40 to 125°C	3.6 V	2.0		10.6	ns
		$V_{NC} = GND$ and $V_{NO} = V_{+}$	$R_L = 500 \Omega$,	Full	3 V to	1.5		5.3	ns
t _{OFF}	Turnoff time	or $V_{NC} = V_{+}$ and $V_{NO} = GND$,	C _L = 50 pF, see Figure 12	-40 to 125°C	3.6 V	1.0		8.3	ns
t _{BBM}	Break-before-make time	$\begin{aligned} V_{NC} &= V_{NO} = V_{+}/2, \\ R_{L} &= 50 \ \Omega, \end{aligned}$	$C_L = 35 \text{ pF},$ see Figure 13	Full	3 V to 3.6 V	0.5			ns
$Q_{\mathbb{C}}$	Charge injection	$R_L = 50 \ \Omega,$ $C_L = 0.1 \ nF,$	see Figure 17	25°C	3.3 V		3		pC
BW	Bandwidth	$R_L = 50 \Omega$, Switch ON,	see Figure 14	25°C	3 V		220		MHz
O _{ISO}	OFF isolation	$R_L = 50 \Omega$, f = 10 MHz,	Switch OFF, see Figure 15	25°C	3 V		-65		dB
X _{TALK}	Crosstalk	$R_L = 50 \Omega$, f = 10 MHz,	Switch ON, see Figure 16	25°C	3 V		-66		dB
THD	Total harmonic distortion	$R_L = 600 \Omega,$ $C_L = 50 \text{ pF},$	f = 600 Hz to 20 kHz, see Figure 18	25°C	3 V		0.015%		
SUPPLY				1					
l ₊	Positive supply	$V_{IN} = V_{+}$ or GND,	Switch ON or OFF	25°C	3.6 V			1	μA
•+	current	VIN - V+ 01 014D,	Owner On or or I	Full	0.0 V			10	μΛ
Δl_{+}	Change in supply current	$V_{IN} = V_{+} - 0.6 V$		Full	3.6 V			500	μΑ

 ⁽¹⁾ T_A = 25°C.
 (2) All unused digital inputs of the device must be held at V₊ or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, SCBA004.



6.7 Electrical Characteristics for 2.5-V Supply

 $V_{+} = 2.3 \text{ V}$ to 2.7 V, $T_{A} = -40^{\circ}\text{C}$ to 85°C (unless otherwise noted)

	PARAMETER	TEST CON	DITIONS	T _A	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
ANALOG S	SWITCH								
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_{+}	V
		0 < \/ or \/ < \/	Switch ON,	Full				45	
r _{on}	ON-state resistance	$0 \le V_{NO} \text{ or } V_{NC} \le V_+,$ $I_{COM} = -8 \text{ mA},$	see Figure 9	-40 to 125°C	2.3 V			50	Ω
Δr_{on}	ON-state resistance match between channels	V_{NO} or $V_{NC} = 1.6 \text{ V}$, $I_{COM} = -8 \text{ mA}$,	Switch ON, see Figure 9	25°C	2.3 V		0.5		Ω
r _{on(flat)}	ON-state resistance flatness	$0 \le V_{NO} \text{ or } V_{NC} \le V_+,$ $I_{COM} = -8 \text{ mA},$	Switch ON, see Figure 9	25°C	2.3 V		27		Ω
I _{NC(OFF)} ,	NC, NO	V_{NC} or $V_{NO} = 0$ to V_{+} ,	Switch OFF,	25°C	2.7 V	-1	0.05	1	μA
I _{NO(OFF)}	OFF leakage current	$V_{COM} = 0 \text{ to } V_+,$	see Figure 10	Full	2.7 V	-1		1	μΛ
I _{NC(ON)} ,	NC, NO	V_{NC} or $V_{NO} = 0$ to V_{+} ,	Switch ON,	25°C	2.7 V	-0.1		0.1	μA
I _{NO(ON)}	ON leakage current	V _{COM} = Open,	see Figure 10	Full	2.7 0	-1		1	μ, ,
I _{COM(ON)}	COM	V_{NC} or V_{NO} = Open,	Switch ON,	25°C	2.7 V	-0.1		0.1	μA
	ON leakage current	$V_{COM} = 0 \text{ to } V_+,$	see Figure 10	Full		-1		1	P** '
	NPUTS (IN12, IN2) ⁽²⁾	I						ı	
V_{IH}	Input logic high			Full		$V_{+} \times 0.7$			V
V_{IL}	Input logic low			Full				V ₊ × 0.3	V
I _{IH} , I _{IL}	Input leakage current	V _{IN} = 5.5 V or 0		25°C	2.7 V	-1	0.05	1	μA
'IH, 'IL	input leakage current	VIIN = 0.0 V 01 0		Full	2.7 V	-1		1	μΛ
DYNAMIC									
		V_{NC} = GND and V_{NO} = V_{+}	$R_L = 500 \Omega$	Full	2.3 V	3.5		14	
t _{ON}	Turnon time	or $V_{NC} = V_{+}$ and $V_{NO} = GND$,	C _L = 50 pF, see Figure 12	-40 to 125°C	to 2.7 V	2.5		17	ns
		$V_{NC} = GND$ and $V_{NO} = V_{+}$	$R_L = 500 \Omega$,	Full	2.3 V	2		7.5	ns
t _{OFF}	Turnoff time	or $V_{NC} = V_{+}$ and $V_{NO} = GND$,	$C_L = 50 \text{ pF},$ see Figure 12	-40 to 125°C	to 2.7 V	1.5		10.5	ns
t _{BBM}	Break-before-make time	$V_{NC} = V_{NO} = V_{\downarrow}/2,$ $R_{L} = 50 \Omega,$	C _L = 35 pF, see Figure 13	Full	2.3 V to 2.7 V	0.5			ns
BW	Bandwidth	$R_L = 50 \Omega$,	Switch ON, see Figure 14	25°C	2.3 V		220		MHz
O _{ISO}	OFF isolation	$R_L = 50 \Omega$, f = 10 MHz,	Switch OFF, see Figure 15	25°C	2.3 V		-65		dB
X _{TALK}	Crosstalk	$R_L = 50 \Omega$, f = 10 MHz,	Switch ON, see Figure 16	25°C	2.3 V		-66		dB
THD	Total harmonic distortion	$R_L = 600 \Omega,$ $C_L = 50 \text{ pF},$	f = 600 Hz to 20 kHz, see Figure 18	25°C	2.3 V		0.025%		
SUPPLY								,	
I ₊	Positive supply	$V_{IN} = V_{+}$ or GND,	Switch ON or OFF	25°C	2.7 V			1	μA
'+	current	V	SWIGH ON GOT	Full	2.7 V			10	μ/ \
Δl_{+}	Change in supply current	$V_{IN} = V_{+} - 0.6 \text{ V}$		Full	2.7 V			500	μΑ

⁽¹⁾ $T_A = 25^{\circ}C$.

Submit Documentation Feedback

Copyright © 2004–2019, Texas Instruments Incorporated

 ^{(1) 1}A = 25 S.
 (2) All unused digital inputs of the device must be held at V₊ or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, SCBA004.



6.8 Electrical Characteristics for 1.8-V Supply

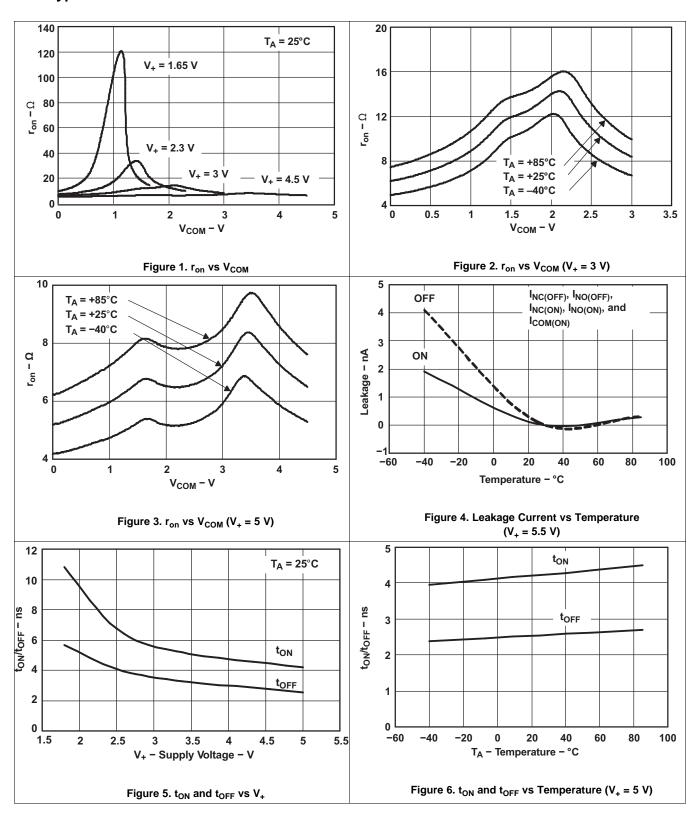
 $V_{+} = 1.65 \text{ V}$ to 1.95 V, $T_{A} = -40 ^{\circ}\text{C}$ to 85 $^{\circ}\text{C}$ (unless otherwise noted)

	PARAMETER	TEST CONI	DITIONS	TA	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
ANALOG	SWITCH								
$\begin{matrix} V_{COM}, \\ V_{NO}, V_{NC} \end{matrix}$	Analog signal range					0		V ₊	V
		$0 \le V_{NO} \text{ or } V_{NC} \le V_+,$	Switch ON,	Full				140	_
r _{on}	ON-state resistance	$I_{\text{COM}} = -4 \text{ mA},$	see Figure 9	-40 to 125°C	1.65 V			180	Ω
Δr_{on}	ON-state resistance match between channels	V_{NO} or $V_{NC} = 1.15 \text{ V}$, $I_{COM} = -4 \text{ mA}$,	Switch ON, see Figure 9	25°C	1.65 V		1		Ω
r _{on(flat)}	ON-state resistance flatness	$0 \le V_{NO} \text{ or } V_{NC} \le V_+,$ $I_{COM} = -4 \text{ mA},$	Switch ON, see Figure 9	25°C	1.65 V		110		Ω
I _{NC(OFF)} ,	NC, NO	V_{NC} or $V_{NO} = 0$ to V_{+} ,	Switch OFF,	25°C	1.95 V	-1	0.05	1	μA
I _{NO(OFF)}	OFF leakage current	$V_{COM} = 0 \text{ to } V_+,$	see Figure 10	Full	1.95 V	-1		1	μ
I _{NC(ON)} ,	NC, NO	V_{NC} or $V_{NO} = 0$ to V_+ ,	Switch ON,	25°C	1.95 V	-0.1		0.1	μA
I _{NO(ON)}	ON leakage current	V _{COM} = Open,	see Figure 10	Full	1.95 V	-1		1	μ.Α.
	COM	V_{NC} or V_{NO} = Open,	Switch ON,	25°C	1.95 V	-0.1		0.1	μA
I _{COM(ON)}	ON leakage current	$V_{COM} = 0 \text{ to } V_+,$	see Figure 10	Full	1.95 V	-1		1	μΑ
DIGITAL	INPUTS (IN12, IN2) ⁽²⁾								
V_{IH}	Input logic high			Full		$V_{+} \times 0.75$			V
V_{IL}	Input logic low			Full				V ₊ × 0.25	V
	1	V 55V 0		25°C	4.05.1/	_1	0.05	1	
I _{IH} , I _{IL}	Input leakage current	$V_{IN} = 5.5 \text{ V or } 0$		Full	1.95 V	-1		1	μA
DYNAMIC	C								
		V_{NC} = GND and V_{NO} = V_{+}	$R_L = 500 \Omega$,	Full	1.65 V	7		24	ns
t _{ON}	Turnon time	or $V_{NC} = V_{+}$ and $V_{NO} = GND$,	$C_L = 50 \text{ pF,}$ see Figure 12	-40 to 125°C	to 1.95 V	5.5		27	ns
		$V_{NC} = GND \text{ and } V_{NO} = V_{+}$	$R_L = 500 \Omega$,	Full	1.65 V	3		13	
t _{OFF}	Turnoff time	or $V_{NC} = V_{+}$ and $V_{NO} = GND$,	$C_L = 50 \text{ pF},$ see Figure 12	-40 to 125°C	to 1.95 V	2		16	ns
t _{BBM}	Break-before-make time	$\begin{aligned} V_{NC} &= V_{NO} = V_{+}/2, \\ R_{L} &= 50~\Omega, \end{aligned}$	C _L = 35 pF, see Figure 13	Full	1.65 V to 1.95 V	0.5			ns
BW	Bandwidth	$R_L = 50 \Omega$,	Switch ON, see Figure 14	25°C	1.8 V		220		MHz
O _{ISO}	OFF isolation	$R_L = 50 \Omega$, f = 10 MHz,	Switch OFF, see Figure 15	25°C	1.8 V		-60		dB
X _{TALK}	Crosstalk	$R_L = 50 \Omega$, f = 10 MHz,	Switch ON, see Figure 16	25°C	1.8 V		-66		dB
THD	Total harmonic distortion	$R_L = 600 \ \Omega,$ $C_L = 50 \ pF,$	f = 600 Hz to 20 kHz, see Figure 18	25°C	1.8 V		0.015%		
SUPPLY									,
I ₊	Positive supply	$V_{IN} = V_{+}$ or GND,	Switch ON or OFF	25°C	1.95 V			1	μA
'+	current	VIN - V+ OI GIVD,	Switch Old Old	Full	1.33 V			10	μΛ
Δl_{+}	Change in supply current	$V_{IN} = V_{+} - 0.6 \text{ V}$		Full	1.95 V			500	μA

 ⁽¹⁾ T_A = 25°C.
 (2) All unused digital inputs of the device must be held at V₊ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

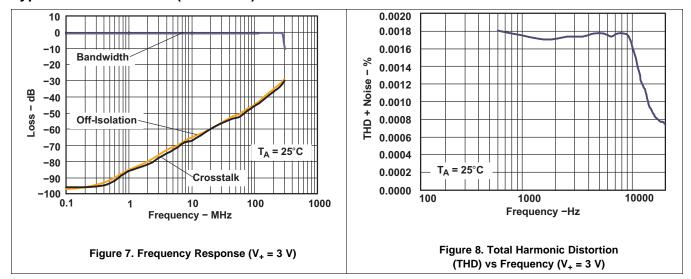
TEXAS INSTRUMENTS

6.9 Typical Characteristics



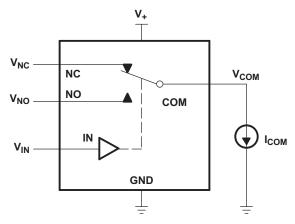


Typical Characteristics (continued)





7 Parameter Measurement Information



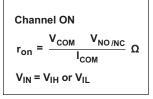
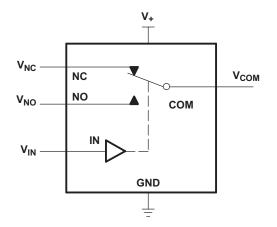
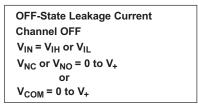


Figure 9. ON-State Resistance (ron)





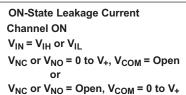
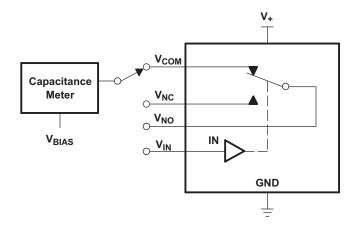


Figure 10. ON- and OFF-State Leakage Current ($I_{COM(ON)}$, $I_{NC(OFF)}$, $I_{NO(OFF)}$, $I_{NO(ON)}$)



V_{BIAS} = V₊ or GND
V_{IN} = V_{IH} or V_{IL}
Capacitance is measured at NC, NO, COM, and IN inputs during ON and OFF conditions.

Figure 11. Capacitance (C_{IN}, C_{COM(ON)}, C_{NC(OFF)}, C_{NO(OFF)}, C_{NC(ON)}, C_{NO(ON)})

Submit Documentation Feedback



Parameter Measurement Information (continued)

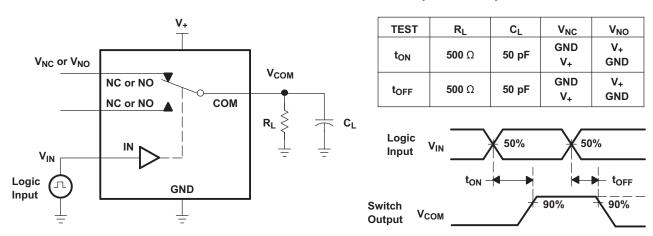


Figure 12. Turnon (t_{ON}) and Turnoff (t_{OFF}) Time

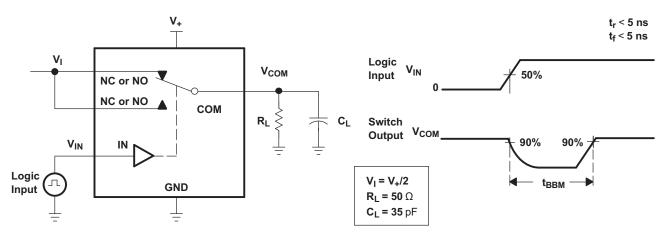


Figure 13. Break-Before-Make (t_{BBM}) Time

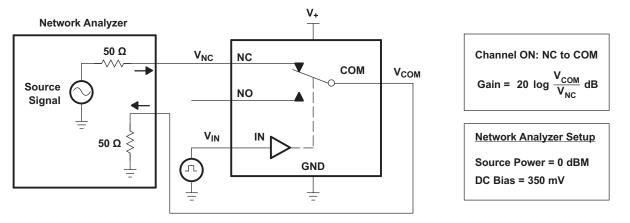


Figure 14. Frequency Response (BW)

Submit Documentation Feedback



Parameter Measurement Information (continued)

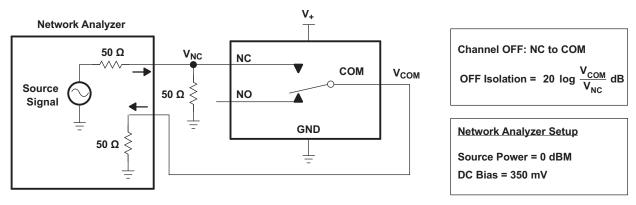


Figure 15. OFF Isolation (O_{ISO})

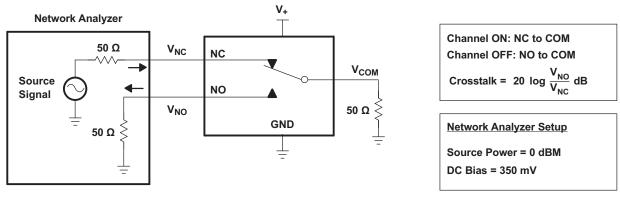


Figure 16. Crosstalk (X_{TALK})

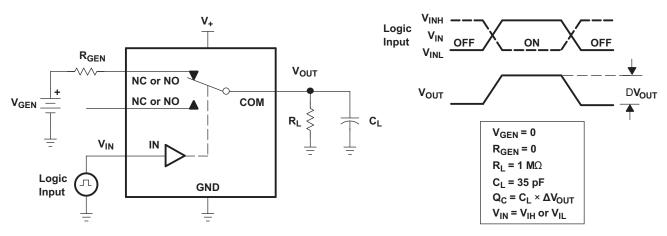


Figure 17. Charge Injection (Q_C)

Submit Documentation Feedback



Parameter Measurement Information (continued)

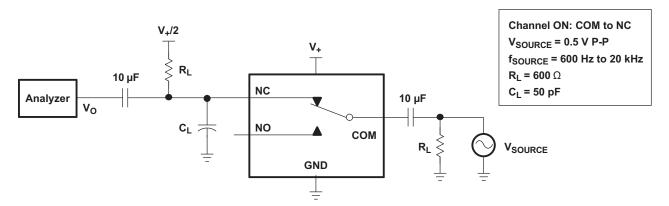


Figure 18. Total Harmonic Distortion (THD)



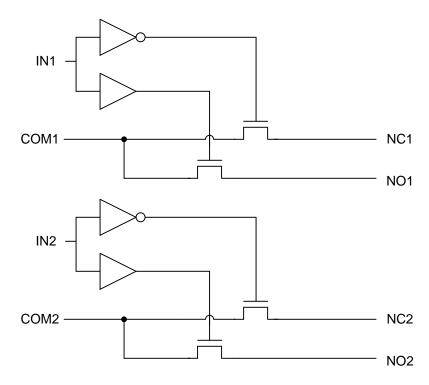
8 Detailed Description

8.1 Overview

The TS5A23157 is a dual single-pole-double-throw (SPDT) solid-state analog switch. The TS5A23157, like all analog switches, is bidirectional. When powered on, each COM pin is connected to its respective NC pin when the IN pin is low. For this device, NC stands for *normally closed* and NO stands for *normally open*. If IN is low, COM is connected to NC. If IN is high, COM is connected to NO.

The TS5A23157 is a break-before-make switch. This means that during switching, a connection is broken before a new connection is established. The NC and NO pins are never connected to each other.

8.2 Functional Block Diagram



8.3 Feature Description

The low ON-state resistance, ON-state resistance matching, and charge injection in the TS5A23157 make this switch an excellent choice for analog signals that require minimal distortion. In addition, the low THD allows audio signals to be preserved more clearly as they pass through the device.

The 1.65-V to 5.5-V operation allows compatibility with more logic levels, and the bidirectional I/Os can pass analog signals from 0 V to V_+ with low distortion. The control inputs are 5-V tolerant, allowing control signals to be present without V_{CC} .

8.4 Device Functional Modes

Table 1 lists the functional modes for TS5A23157.

Table 1. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO		
L	ON	OFF		
Н	OFF	ON		



9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS5A3157 can be used in a variety of customer systems. The TS5A3157 can be used anywhere multiple analog or digital signals must be selected to pass across a single line.

9.2 Typical Application

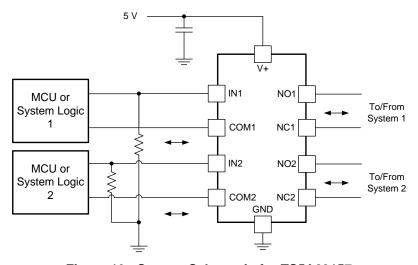


Figure 19. System Schematic for TS5A23157

9.2.1 Design Requirements

In this particular application, V_+ was 5 V, although V_+ is allowed to be any voltage specified in *Recommended Operating Conditions*. A decoupling capacitor is recommended on the V+ pin. See *Power Supply Recommendations* for more details.

9.2.2 Detailed Design Procedure

In this application, IN is, by default, pulled low to GND. Choose the resistor size based on the current driving strength of the GPIO, the desired power consumption, and the switching frequency (if applicable). If the GPIO is open-drain, use pullup resistors instead.



Typical Application (continued)

9.2.3 Application Curve

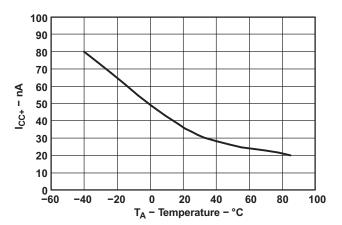


Figure 20. Power-Supply Current vs Temperature ($V_{+} = 5 \text{ V}$)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μF bypass capacitor is recommended. If there are multiple pins labeled V_{CC} , then a 0.01- μF or 0.022- μF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD} , a 0.1- μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

Submit Documentation Feedback



11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Below figure shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

Unused switch I/Os, such as NO, NC, and COM, can be left floating or tied to GND. However, the IN pin must be driven high or low. Due to partial transistor turnon when control inputs are at threshold levels, floating control inputs can cause increased I_{CC} or unknown switch selection states.

11.2 Layout Example

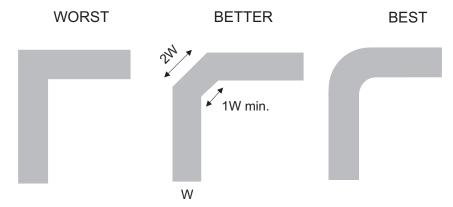


Figure 21. Trace Example



12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

Table 2. Parameter Description

SYMBOL	DESCRIPTION									
V _{COM}	Voltage at COM									
V _{NC}	Voltage at NC									
V _{NO}	Voltage at NO									
r _{on}	Resistance between COM and NC or COM and NO ports when the channel is ON									
$\Delta r_{\sf on}$	Difference of r _{on} between channels									
r _{on(flat)}	Difference between the maximum and minimum value of ron in a channel over the specified range of conditions									
I _{NC(OFF)}	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions									
I _{NO(OFF)}	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions									
I _{NC(ON)}	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) being open									
I _{NO(ON)}	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) being open									
I _{COM(ON)}	Leakage current measured at the COM port, with the corresponding channel (NO to COM or NC to COM) in the ON state and the output (NC or NO) being open									
V_{IH}	Minimum input voltage for logic high for the control input (IN)									
V_{IL}	Minimum input voltage for logic low for the control input (IN)									
V_{IN}	Voltage at IN									
$I_{IH},\ I_{IL}$	Leakage current measured at IN									
t _{ON}	Turnon time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM/NC/NO) signal when the switch is turning ON.									
t _{OFF}	Turnoff time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM/NC/NO) signal when the switch is turning OFF.									
t _{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.									
$Q_{\mathbb{C}}$	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulombs (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_O$, C_L is the load capacitance and ΔV_O is the change in analog output voltage.									
C _{NC(OFF)}	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF									
C _{NO(OFF)}	Capacitance at the NO port when the corresponding channel (NC to COM) is OFF									
C _{NC(ON)}	Capacitance at the NC port when the corresponding channel (NC to COM) is ON									
C _{NO(ON)}	Capacitance at the NO port when the corresponding channel (NC to COM) is ON									
C _{COM(ON)}	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON									
C_{IN}	Capacitance of IN									
O _{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state. OFF isolation, $O_{ISO} = 20 \text{ LOG}$ (V_{NC}/V_{COM}) dB, V_{COM} is the input and V_{NC} is the output.									
X _{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured at a specific frequency and in dB. Crosstalk, $X_{TALK} = 20 \log (V_{NC1}/V_{NO1})$, V_{NO1} is the input and V_{NC1} is the output.									
BW	Bandwidth of the switch. This is the frequency where the gain of an ON channel is -3 dB below the dc gain. Gain is measured from the equation, 20 log (V_{NC}/V_{COM}) dB, where V_{NC} is the output and V_{COM} is the input.									
I ₊	Static power-supply current with the control (IN) pin at V ₊ or GND									
ΔI_{+}	This is the increase in I_+ for each control (IN) input that is at the specified voltage, rather than at V_+ or GND.									



Table 3. Summary of Characteristics

CONFIGURATION	2:1 MULTIPLEXER/DEMULTIPLEXER (2 × SPDT)
Number of channels	2
ON-state resistance (r _{on})	10 Ω
ON-state resistance match between channels (Δr _{on})	0.15 Ω
ON-state resistance flatness (r _{on(flat)})	4 Ω
Turnon/turnoff time (t _{ON} /t _{OFF})	5.7 ns/3.8 ns
Break-before-make time (t _{BBM})	0.5 ns
Charge injection (Q _C)	7 pC
Bandwidth (BW)	220 MHz
OFF isolation (O _{SIO})	-65 dB at 10 MHz
Crosstalk 9XTALK)	-66 dB at 10 MHz
Total harmo nic distortion (THD)	0.01%
Leakage current (I _{COM(OFF)} /I _{NC(OFF)})	±1 μA
Package options	10-pin DGS and RSE

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com 7-Oct-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
TS5A23157DGSR	Active	Production	VSSOP (DGS) 10	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(3BR, JBR)
TS5A23157DGSR.B	Active	Production	VSSOP (DGS) 10	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(3BR, JBR)
TS5A23157DGSRG4	Active	Production	VSSOP (DGS) 10	2500 null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBR
TS5A23157DGSRG4.B	Active	Production	VSSOP (DGS) 10	2500 null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBR
TS5A23157RSER	Active	Production	UQFN (RSE) 10	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBO
TS5A23157RSER.B	Active	Production	UQFN (RSE) 10	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBO
TS5A23157RSERG4.B	Active	Production	UQFN (RSE) 10	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBO

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

www.ti.com 7-Oct-2025

OTHER QUALIFIED VERSIONS OF TS5A23157:

Automotive: TS5A23157-Q1

NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

www.ti.com 14-Dec-2024

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A23157DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TS5A23157RSER	UQFN	RSE	10	3000	180.0	9.5	1.7	2.2	0.75	4.0	8.0	Q1

www.ti.com 14-Dec-2024



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A23157DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TS5A23157RSER	UQFN	RSE	10	3000	189.0	185.0	36.0



SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-187, variation BA.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



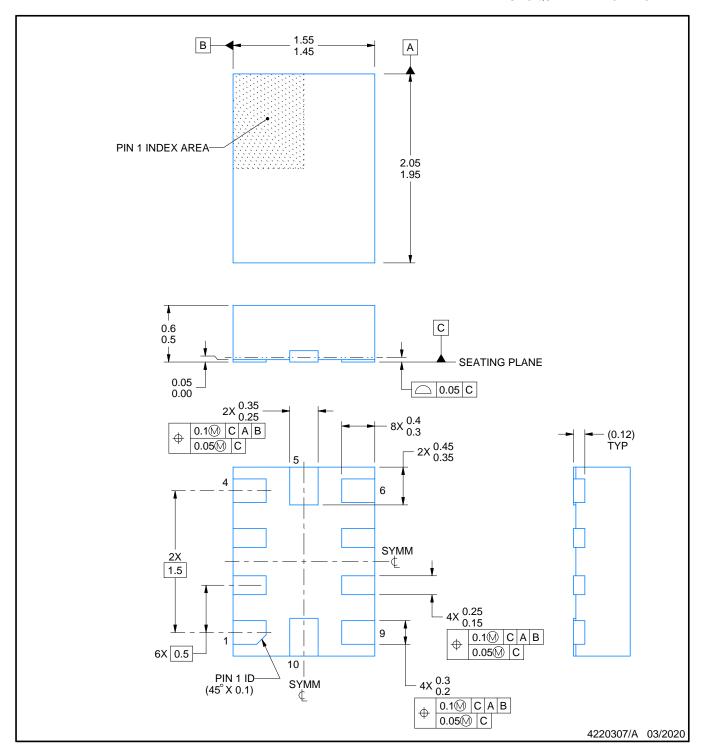
NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





PLASTIC QUAD FLATPACK - NO LEAD

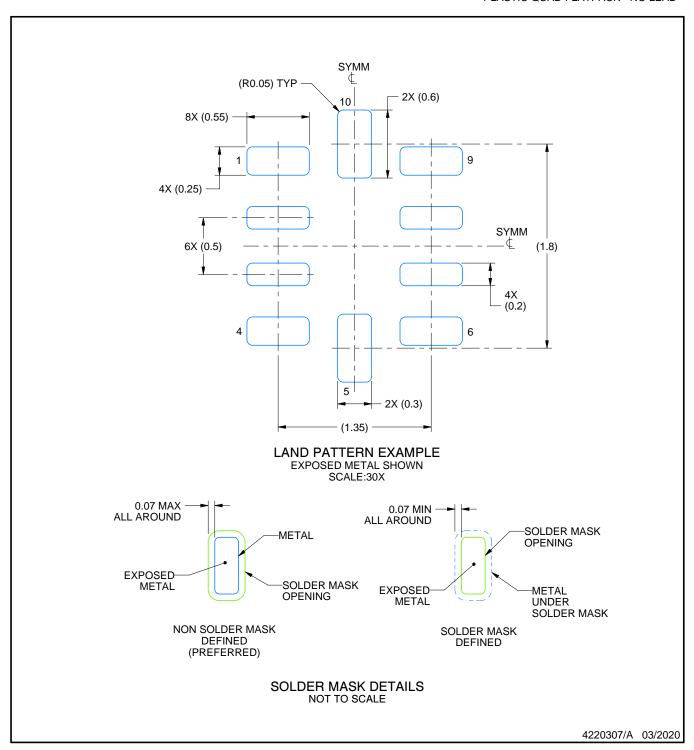


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



PLASTIC QUAD FLATPACK - NO LEAD

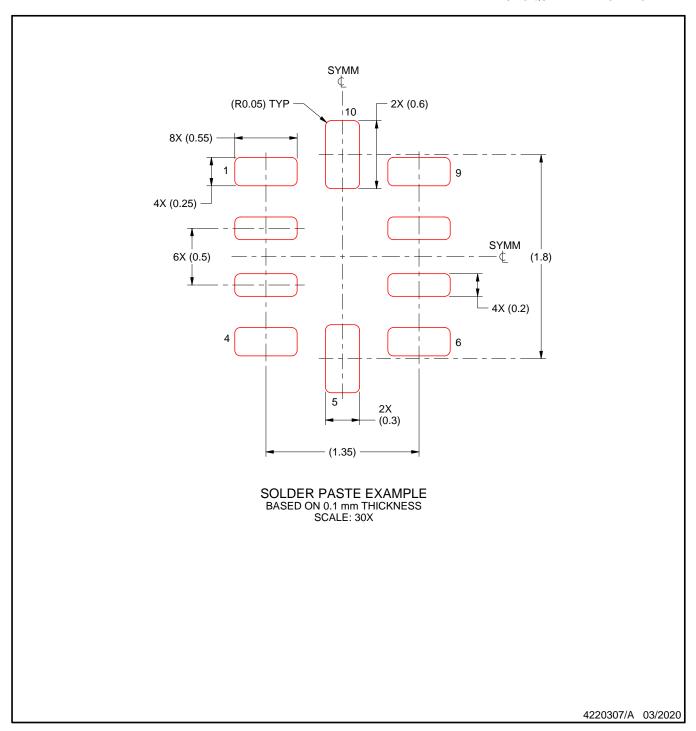


NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2025. Texas Instruments Incorporated