TEXAS INSTRUMENTS

TS3DDR4000

SCDS356C – NOVEMBER 2014 – REVISED MARCH 2019

TS3DDR4000 12-bits 1:2 high speed DDR2/DDR3/DDR4 switch/multiplexer

1 Features

- Wide V_{DD} Range: 2.375 V – 3.6 V
- High Bandwidth: 5.6 GHz Typical (single-ended); 6.0 GHz Typical (differential)
- Low Switch On-Resistance (R_{ON}): 8 Ω Typical
- Low Bit-to-Bit Skew: 3ps Typical; 6ps Max across All Channels
- Low Crosstalk: –34 dB Typical at 1067 MHz
- Low Operating Current: 40 µA Typical
- Low-Power Mode with Low Current Consumption: 2 µA Typical
- I_{OFF} Protection Prevents Current Leakage in Powered Down State (V_{DD} = 0 V)
- Supports POD_12, SSTL_12, SSTL_15 and SSTL_18 Signaling
- ESD Performance:
  - 3-kV Human Body Model (A114B, Class II)
  - 1-kV Charged Device Model (C101)
- 8 mm x 3 mm 48-balls 0.65-mm Pitch ZBA Package

2 Applications

- NVDIMM Modules
- Enterprise Data Systems and Servers
- Notebook/Desktop PCs
- General DDR3/DDR4 Signal Switching
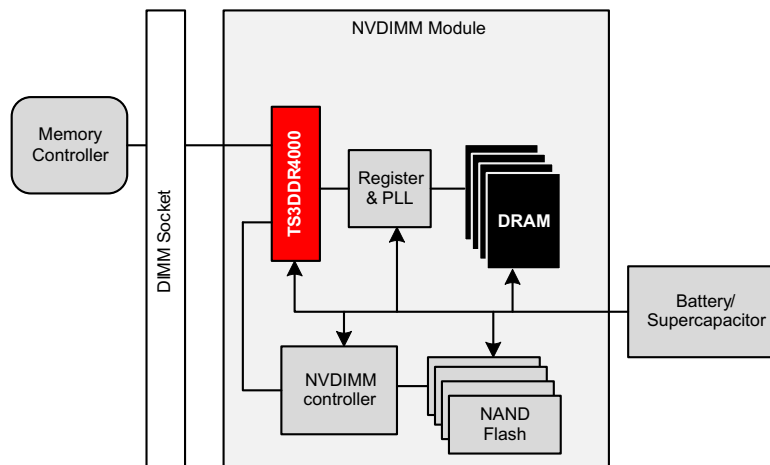- General High-Speed Signal Switching

3 Description

The TS3DDR4000 is 1:2 or 2:1 high speed DDR2/DDR3/DDR4 switch that offers 12-bit wide bus switching. The A port can be switched to the B or C port for all bits simultaneously. Designed for operation in DDR2, DDR3 and DDR4 memory bus systems, the TS3DDR4000 uses a proprietary architecture that delivers high bandwidth (single-ended –3dB bandwidth at 5.6 GHz), low insertion loss at low frequency, and very low propagation delay. The TS3DDR4000 is 1.8 V logic compatible, and all switches are bi-directional for added design flexibility. The TS3DDR4000 also offers a low-power mode, in which all channels become high-Z and the device consumes minimal power.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS3DDR4000	NFBGA (48)	8.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Application Diagram

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4 Revision History

Changes from Revision B (May 2017) to Revision C   **Page**

- Changed the *Pin Configuration* image 3
- Changed V_{IH} From: SEL1m and SEL2 To: SEL0 and SEL1 with a MIN value of 1 V in the *Recommended Operating Conditions* 4
- Changed SEL1 To: SEL0 and SLE2 To: SEL1 in Figure 18 11
- Changed text 'Standard layout technique for 0.5 mm pitch BGA package" To: "Standard layout technique for 0.65 mm pitch BGA package..." in the *Layout Guidelines* 15

Changes from Revision A (March 2015) to Revision B   **Page**

- Changed V_{DD} Max value From: 5.5 V toTo: 4.8 V in the *Absolute Maximum Ratings* 4
- Added the Note to the *Application and Implementation* section 13

Changes from Original (November 2014) to Revision A   **Page**

- Updated document to full version. 1

Product Folder Links: *TS3DDR4000*

5 Pin Configuration and Functions

**ZBA Package
48-Balls (NFBGA)
Top View**

Not to scale
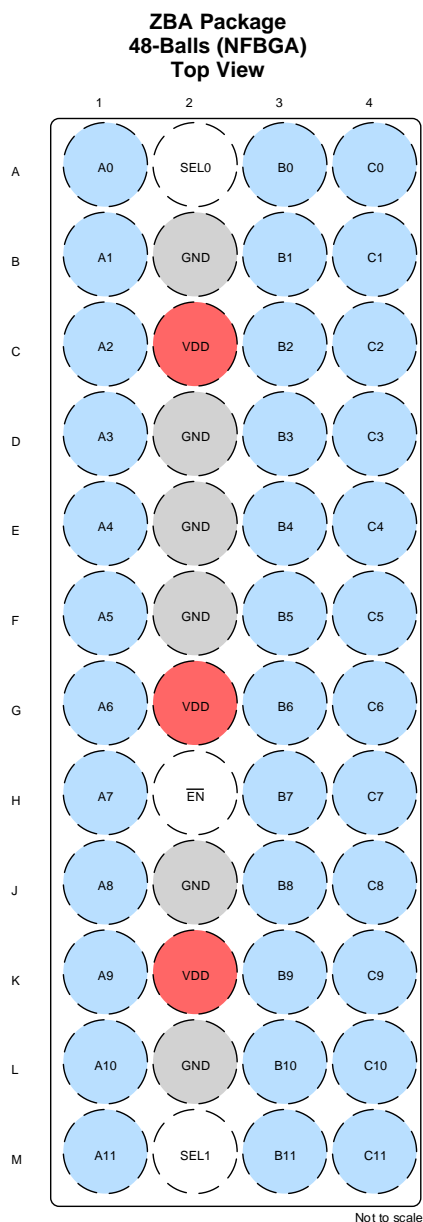
Pin Functions

PINS		TYPE	DESCRIPTION
NAME	**NO.**		
VDD	C2, G2, K2	Power	Power supply
GND	B2, D2, E2, F2, J2, L2	Ground	Ground
A0-A11	A1-M1	I/O	Port A, signal 0-11
B0-B11	A3-M3	I/O	Port B, signal 0-11
C0-C11	A4-M4	I/O	Port C, signal 0-11
SEL0	A2	I	Select control 0
SEL1	M2	I	Select control 1
$\overline{EN}$	H2	I	Enable

Product Folder Links: *TS3DDR4000*

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

		MIN	MAX	UNIT
V_{DD}	Voltage range on V_{DD}	-0.3	4.8	V
V_{IN}	Control input voltage range: SEL0, SEL1, and /EN	-0.3	5.5	V
$V_{I/O}$	Analog voltage range: A0-A11, B0-B11, and C0-C11	-0.3	3.6	V
T_A	Operating ambient temperature range	-40	85	°C
T_{stg}	Storage temperature range	-65	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Charge device model (CDM)[1]	±1000	V
		Human body model (HBM) on all pins[2]	±3000	V

(1) Tested in accordance with JEDEC Standard 22, Test Method C101
(2) Tested in accordance with JEDEC Standard 22, Test Method A114

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Voltage range on V_{DD}	2.375	3.6	V
$V_{I/O}$	Analog voltage range: A0-A11, B0-B11, and C0-C11	0	3.3	V
V_{IH}	High-level control input voltage threshold ($\overline{EN}$)	1.4	V_{DD}	V
	High-level control input voltage threshold (SEL0 and SEL1)	1	V_{DD}	V
V_{IL}	Low-level control input voltage threshold ($\overline{EN}$, SEL0 and SEL1)	0	0.5	V
T_A	Operating ambient temperature range	-40	85	°C

6.4 Thermal Information

THERMAL METRIC[1]		TS3DDR4000 BGA (48)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	56.2	
ψ_{JT}	Junction-to-top characterization parameter	1.3	
ψ_{JB}	Junction-to-board characterization parameter	54.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report .

6.5 Static Electrical Characteristics

Unless otherwise noted the specification applies over the V_{DD} range and operation junction temp of –40°C ≤ T_J ≤ 85°C.
Typical values are for V_{DD} = 3.3 V and T_J = 25°C.

PARAMETER			TEST CONDITION	MIN	TYP	MAX	UNIT
R_{ON}	On-state resistance	Port A to B	V_{DD} = 2.375 V, $V_{I/O}$ = 1.2 V, $I_{I/O}$ = 10 mA	–	8.3	11.2	Ω
		Port A to C		–	8.3	11.2	Ω
R_{ON} (FLAT)	On-state resistance flatness for all I/Os	Port A to B	V_{DD} = 2.375 V, $V_{I/O}$ = 1.2 V, $I_{I/O}$ = 10 mA	–	0.6	–	Ω
		Port A to C		–	0.6	–	Ω
ΔR_{ON}	On-state resistance match between channels	Port A to B	V_{DD} = 2.375 V, $V_{I/O}$ = 1.2 V, $I_{I/O}$ = 10 mA	–	0.2	1.0	Ω
		Port A to C		–	0.2	1.0	Ω
I_{IH}	Control input high leakage current	EN	V_{DD} = 3.6 V, $V_{/EN}$ = 1.4 V	–	–	±1	µA
			V_{DD} = 2.375 V, $V_{/EN}$ = 3.3 V	–	–	±1	µA
		SEL1	V_{DD} = 3.6 V, V_{SEL1} = 1.4 V	–	–	±1	µA
			V_{DD} = 2.375 V, V_{SEL1} = 3.3 V	–	–	±1	µA
		SEL2	V_{DD} = 3.6 V, V_{SEL2} = 1.4 V	–	–	±1	µA
			V_{DD} = 2.375 V, V_{SEL2} = 3.3 V	–	–	±1	µA
I_{IL}	Control input low leakage current	EN	V_{DD} = 3.6 V, $V_{/EN}$ = 0 V	–	–	±0.5	µA
		SEL1	V_{DD} = 3.6 V, V_{SEL1} = 0 V	–	–	±0.5	µA
		SEL2	V_{DD} = 3.6 V, V_{SEL2} = 0 V	–	–	±0.5	µA
I_{OFF}	Leakage under power off condition for all I/Os	EN	V_{DD} = 0 V, $V_{/EN}$ = 0 V, $V_{I/O}$ = 0 V to 3.3 V	–	–	±5	µA
			V_{DD} = 0 V, $V_{//EN}$ = 3.6 V, $V_{I/O}$ = 0 V to 3.3 V	–	–	±5	µA
		SEL1	V_{DD} = 0 V, V_{SEL1} = 0 V, $V_{I/O}$ = 0 V to 3.3 V	–	–	±5	µA
			V_{DD} = 0 V, V_{SEL1} = 3.6 V, $V_{I/O}$ = 0 V to 3.3 V	–	–	±5	µA
		SEL2	V_{DD} = 0 V, V_{SEL2} = 0 V, $V_{I/O}$ = 0 V to 3.3 V	–	–	±5	µA
			V_{DD} = 0 V, V_{SEL2} = 3.6 V, $V_{I/O}$ = 0 V to 3.3 V	–	–	±5	µA
I_{DD}	V_{DD} supply current		V_{DD} = 3.6 V, $I_{I/O}$ = 0 A, /EN = 0 V, V_{SEL1} = V_{SEL2}= 0 V	–	28	35	µA
			V_{DD} = 3.6 V, $I_{I/O}$ = 0 A, /EN = 0 V, V_{SEL1} = V_{SEL2}= 1.8 V	–	40	48	µA
			V_{DD} = 3.6 V, $I_{I/O}$ = 0 A, /EN = 0 V, V_{SEL1} = 0 V, V_{SEL2}= 1.8 V	–	40	44	µA
			V_{DD} = 3.6 V, $I_{I/O}$ = 0 A, /EN = 0 V, V_{SEL1} = 1.8 V, V_{SEL2}= 0 V	–	40	44	µA
$I_{DD, PD}$	V_{DD} supply current in power-down mode		V_{DD} = 3.6 V, $I_{I/O}$ = 0 A, /EN = 1.8 V	–	2	5	µA

6.6 Dynamic Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITION	MIN	TYP	MAX	UNIT
t_{ON}	Switch turn-on time	EN to B	V_{DD} = 2.375 V, R_L = 50 Ω, V_{An} = 3.3 V, $V_{/EN}$ = 1.8 V→ 0 V, V_{SEL1} = V_{SEL2} = 0 V (See Figure 12)	–	65	140	µs
		EN to C	V_{DD} = 2.375 V, R_L = 50 Ω, V_{An} = 3.3 V, $V_{/EN}$ = 1.8 V→ 0 V, V_{SEL1} = V_{SEL2} = 1.8 V (See Figure 12)	–	65	140	µs
t_{SWITCH}	Switching time between channels for all I/Os	SEL to B	V_{DD} = 2.375 V, $V_{/EN}$ = 0 V, R_L = 50 Ω, V_{An} = 3.3 V, (See Figure 13)	–	65	–	ns
		SEL to C	V_{DD} = 2.375 V, $V_{/EN}$ = 0 V, R_L = 50 Ω, V_{An} = 3.3 V, (See Figure 13)	–	50	–	ns
t_{PD}	Propagation delay	Port A to B	V_{DD} = 2.375 V, (See Figure 14)	–	85	–	ps
		Port A to C	V_{DD} = 2.375 V, (See Figure 14)	–	85	–	ps
t_{SKEW}[1]	Singe-ended skew between channels	B0 to B11	V_{DD} = 2.375 V, from any output to any other output	–	3	8	ps
		C0 to C11		–	3	6	ps
C_{IN}	Control input capacitance	EN	f = 1 MHz, V_{IN}= 0 V	–	6	–	pF
		SEL1	f = 1 MHz, V_{IN}= 0 V	–	6	–	pF
		SEL2	f = 1 MHz, V_{IN}= 0 V	–	6	–	pF
C_{OFF}	Switch off capacitance	Port A to B	f = 1067 MHz, $V_{I/O}$ = 0 V, V_{SEL1} = V_{SEL2} = 1.8V	–	0.5	–	pF
		Port A to C	f = 1067 MHz, $V_{I/O}$ = 0 V, V_{SEL1} = V_{SEL2} = 0 V	–	0.5	–	pF
C_{ON}	Switch on capacitance	Port A to B	f = 1067 MHz, $V_{I/O}$ = 1.2 V, V_{SEL1} = V_{SEL2}= 0V	–	1.0	–	pF
		Port A to C	f = 1067 MHz, $V_{I/O}$= 1.2 V, V_{SEL1} = V_{SEL2} = 1.8V	–	1.0	–	pF
X_{TALK}	Crosstalk between channels	B0 to B11	f = 1067 MHz, V_{SEL1} = V_{SEL2} = 0 V, R_L = 50 Ω	–	-34	–	dB
		C0 to C11	f = 1067 MHz, V_{SEL1} = V_{SEL2} = 1.8 V, R_L = 50 Ω	–	-31	–	dB
O_{ISO}	Off-isolation	Port A to B	f = 1067 MHz, V_{SEL1} = V_{SEL2} = 1.8 V, R_L = 50 Ω	–	-21	–	dB
		Port A to C	f = 1067 MHz, V_{SEL1} = V_{SEL2} = 0 V, R_L = 50 Ω	–	-21	–	dB
I_L	Insertion loss (channel on)	Port A to B	f = DC, R_L = 50 Ω	–	-0.75	-1	dB
		Port A to C	f = DC, R_L = 50 Ω	–	-0.75	-1	dB
BW_{SE}	-3 dB bandwidth (Single-ended)	Port A to B	R_L = 50 Ω	–	5.6	–	GHz
		Port A to C		–	5.6	–	
BW_{DIFF}	-3 dB bandwidth (Differential)	Port A to B	R_L = 100 Ω	–	6	–	GHz
		Port A to C		–	6	–	

(1)   Verified by design.

Product Folder Links: *TS3DDR4000*
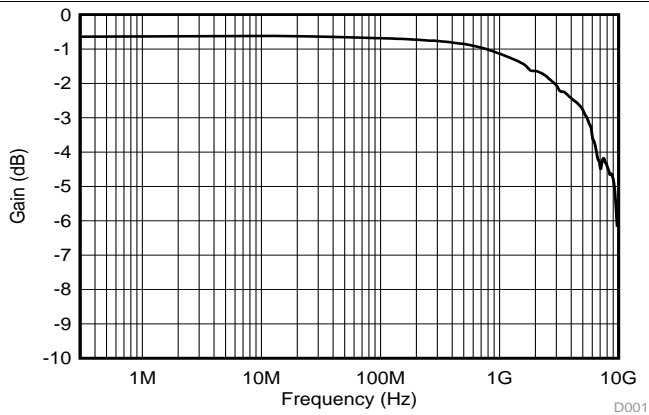
6.7 Typical Characteristics

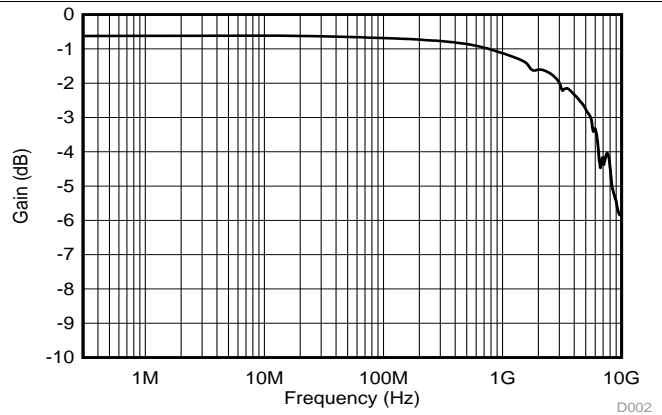Figure 1. Single-Ended S21 vs Frequency for Port B

Figure 2. Single-Ended S21 vs Frequency for Port C
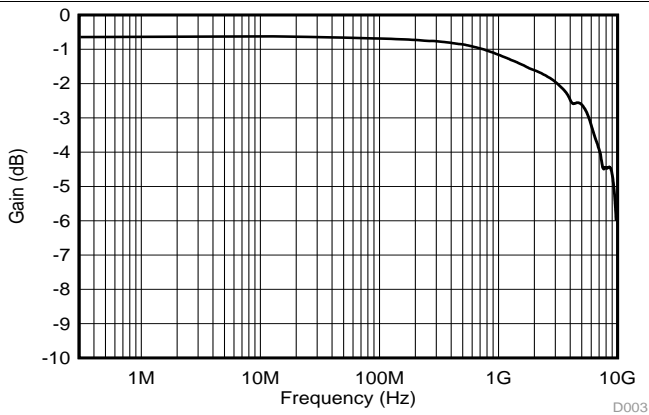

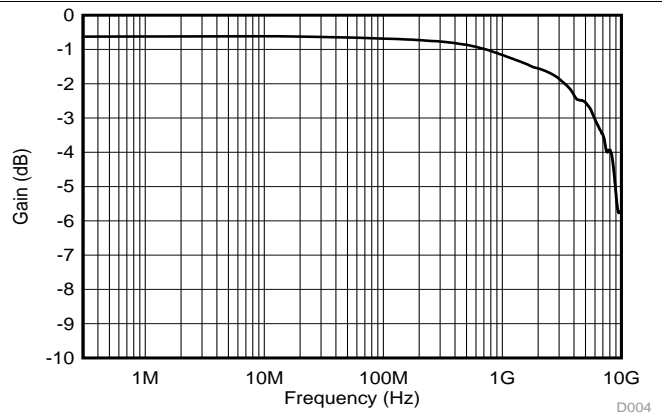Figure 3. Differential S21 vs Frequence for Port B

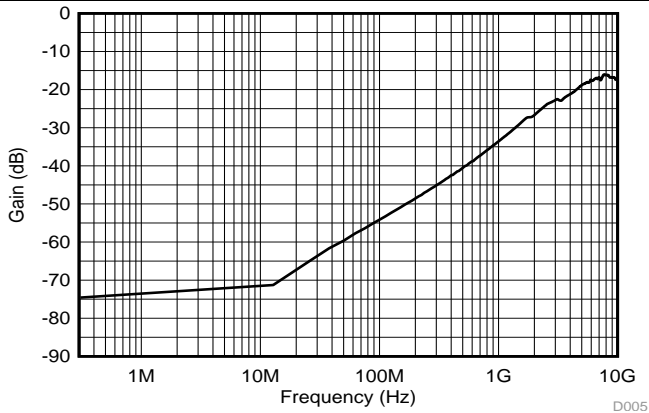Figure 4. Differential S21 vs Frequence for Port C

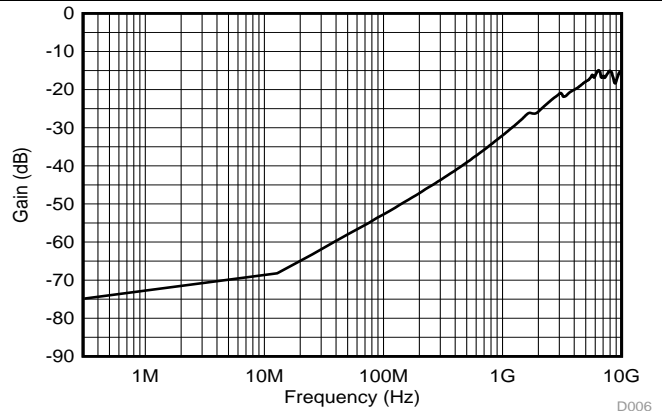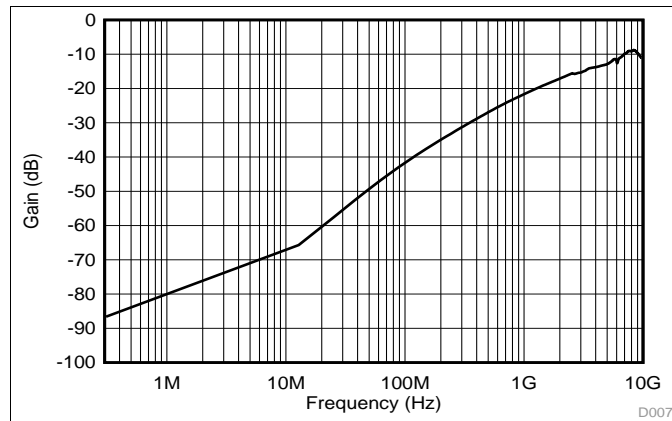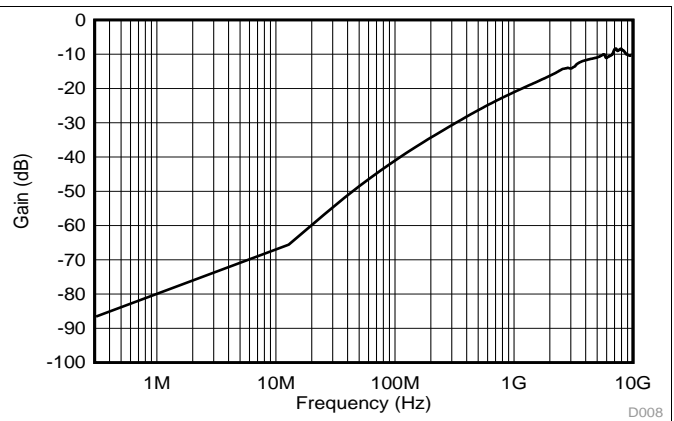Figure 5. Crosstalk vs Frequency for Port B

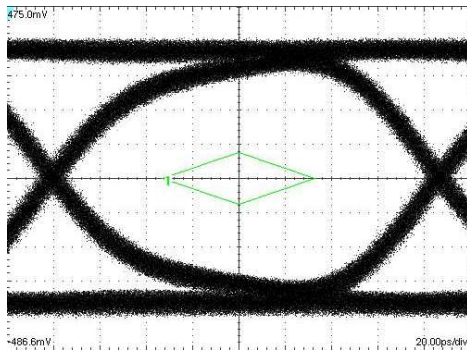Figure 6. Crosstalk vs Frequency for Port C
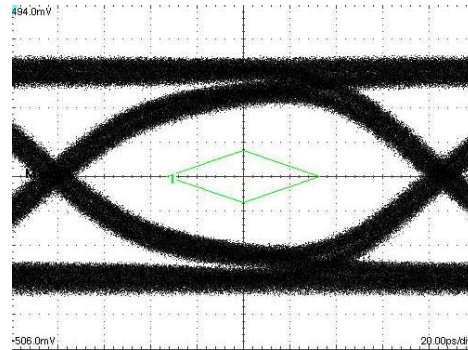
Typical Characteristics (continued)

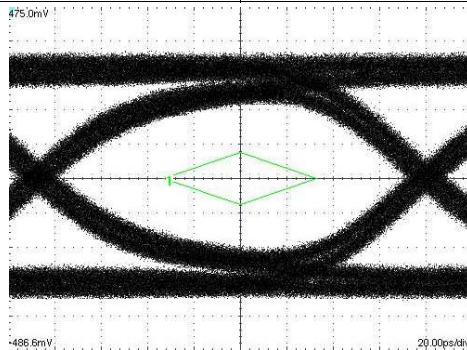**Figure 7. Off-Isolation vs Frequency for Port B**

Figure 8. Off-Isolation vs Frequency for Port C

Figure 9. Eye Diagram (6 Gbps Data Rate): Through Path Without Device

Figure 10. Eye Diagram (6 Gbps Data Rate): Port A to Port B Through TS3DDR4000

Figure 11. Eye Diagram (6 Gbps Data Rate): Port A to Port C Through TS3DDR4000

Product Folder Links: *TS3DDR4000*

7 Parameter Measurement Information
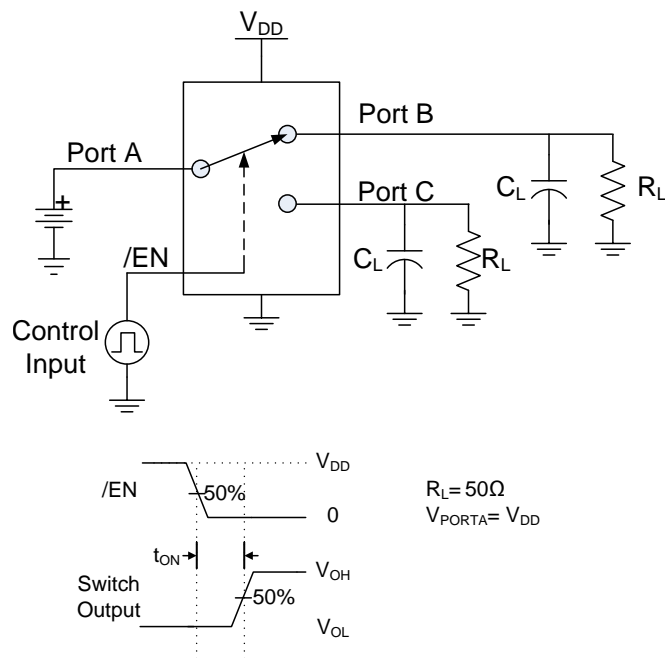
Figure 12. Switch Turn-on Time (t$_{ON}$) Measurement
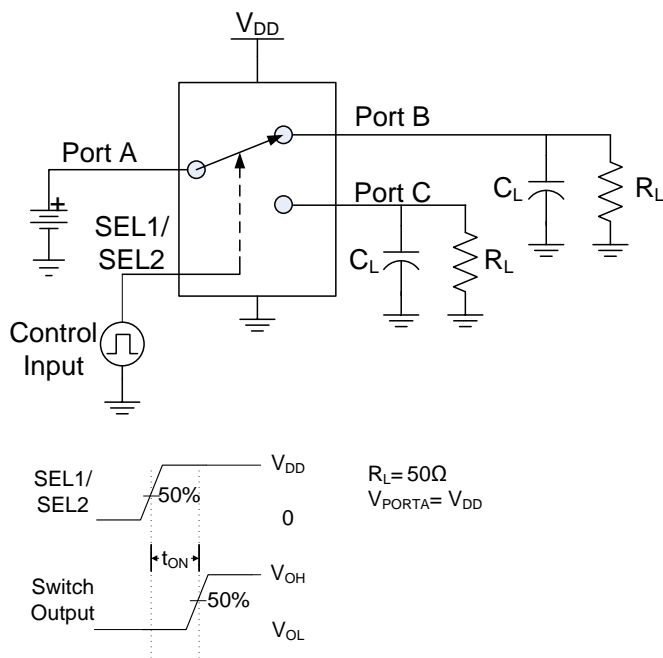
Figure 13. Switch Switching Time (t$_{SWITCH}$) Measurement

$$t_{PD}= (t_{PLH}+t_{PLH})/2$$
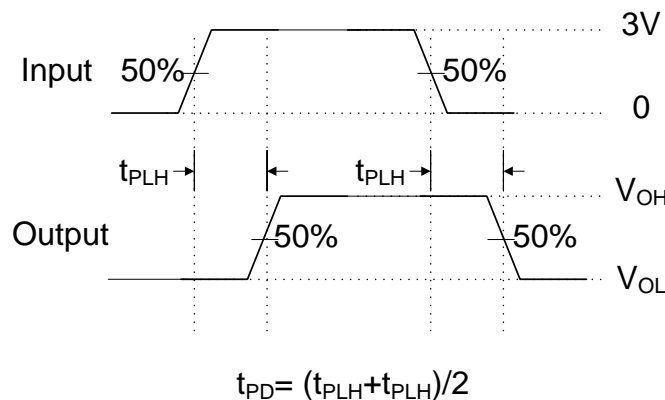
Figure 14. Propagation Delay (t$_{PD}$) Measurement

Channel ON
SEL = H or L
R$_S$=R$_T$=50Ω
V$_S$= -10dBm (200mV at 50Ω Load)
V$_{DC\_BIAS}$ = 0.6V
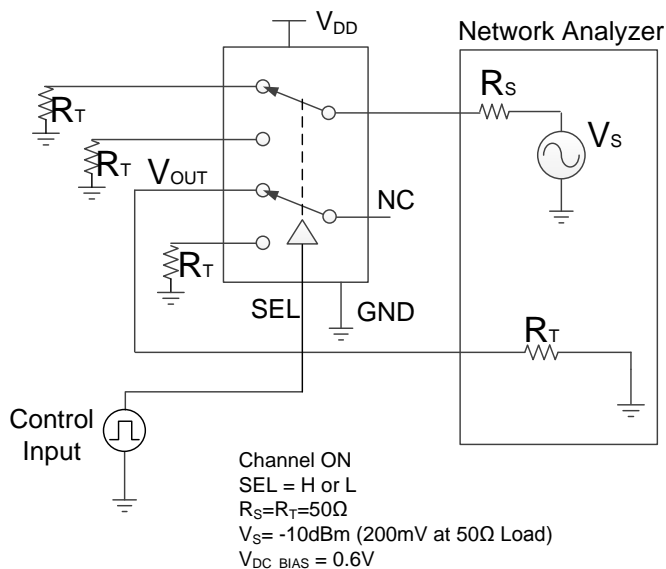
Figure 15. Crosstalk Measurement

Parameter Measurement Information (continued)

Channel OFF
SEL = H or L
$R_S = R_T = 50\Omega$
$V_S = -10$dBm (200mV at 50Ω Load)
$V_{DC\_BIAS} = 0.6$V
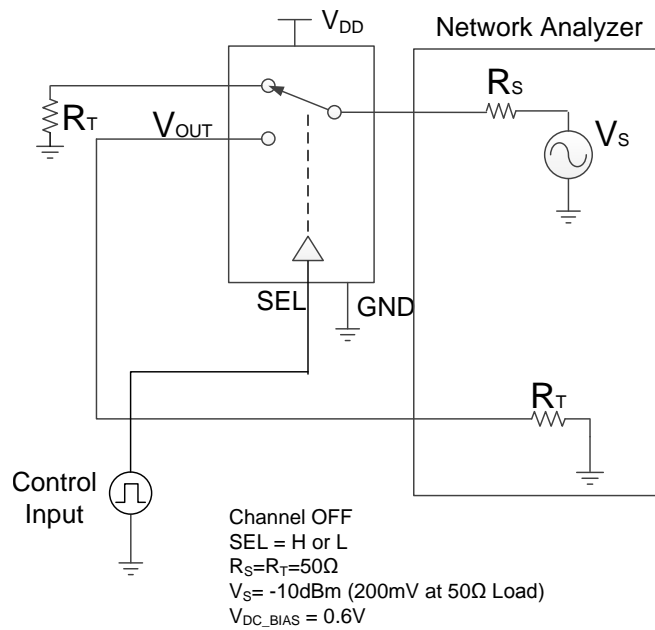
Figure 16. Off Isolation Measurement

Channel ON
SEL = H or L
$R_S = R_T = 50\Omega$
$V_S = -10$dBm (200mV at 50Ω Load)
$V_{DC\_BIAS} = 0.6$V
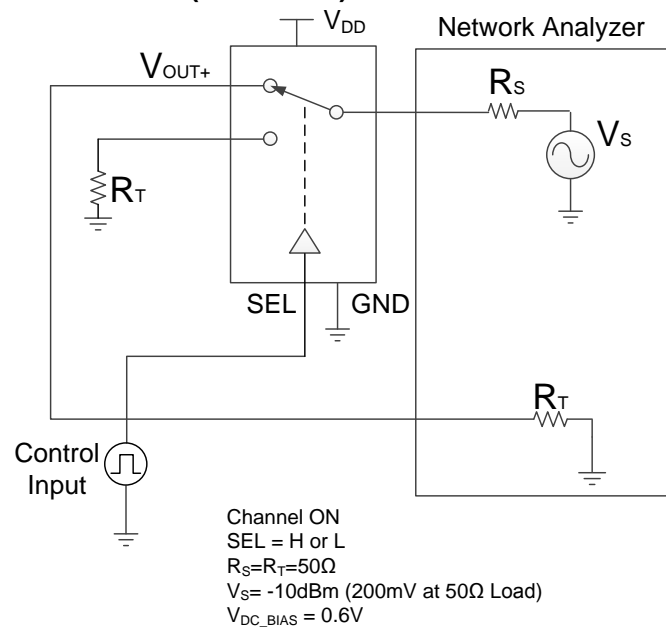
Figure 17. Bandwidth Measurement

Product Folder Links: *TS3DDR4000*

8 Detailed Description

8.1 Overview

The TS3DDR4000 is 1:2 or 2:1 high speed DDR2/DDR3/DDR4 switch that offers 12-bit wide bus switching. The A port can be routed to the B or C port for all bits simultaneously. Designed for operation in DDR2, DDR3 and DDR4 memory bus systems that support POD_12, SSTL_12, SSTL_135, SSTL_15, or SSTL_18 signaling, the TS3DDR4000 uses a proprietary architecture that delivers high bandwidth (differential -3dB bandwidth of up to 6 GHz), and very low propagation delay and skew across all channels. The TS3DDR4000 is 1.8 V logic compatible, and all switches are bi-directional for added design flexibility. The TS3DDR4000 also offers a low-power mode, in which all channels become high-Z and the device operates with minimal power.

8.2 Functional Block Diagram

The following diagram (Figure 18) represents the switch function block diagram of the TS3DDR4000. Port A (A0-A11) can be routed to either port B (B0-B11) or port C (C0-C11) by configuring the SEL0 and SEL1 pins. The EN pin can be toggled high to put the device into the low-power mode with minimal power consumption.
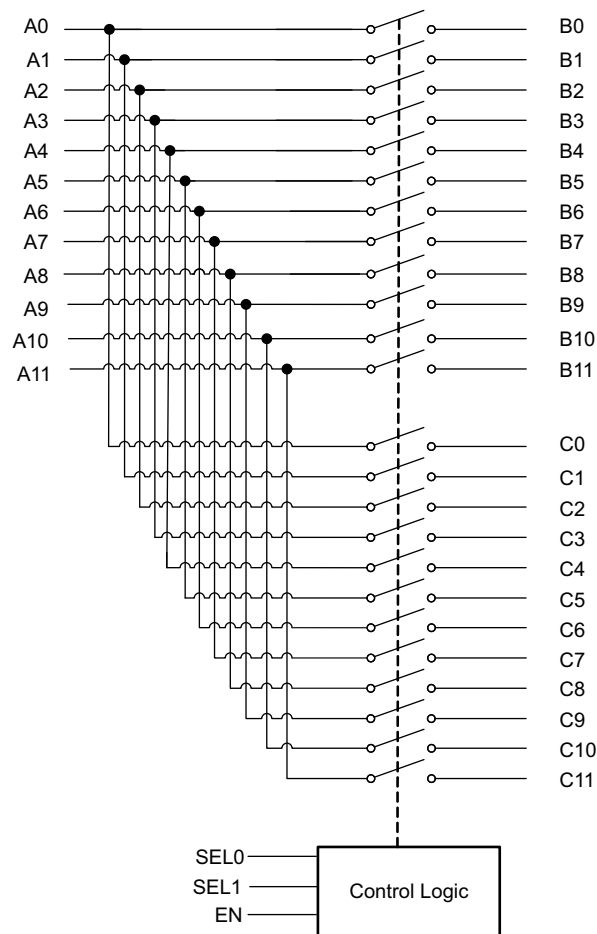
Figure 18. TS3DDR4000 Switch Function Block Diagram

8.3 Feature Description

- I_{OFF} Protection: When no power is provided to the device (V_{CC} = 0 V), the TS3DDR4000 prevents any I/O signals from back-powering the device. The leakage current is tightly controlled under such condition (refer to the I_{OFF} in the *Specifications* section) so it does not cause any system issues.

- Low-power mode: The $\overline{EN}$ pin can be driven high to make the TS3DDR4000 enter the low-power mode. When in low power mode, all channels are isolated and the device consumes less than 5 µA of current.

8.4 Device Functional Modes

When $\overline{EN}$ pin is driven high, the TS3DDR4000 enters into the power-down mode, in which all channels are isolated and the device consumes less than 5 µA of current. When $\overline{EN}$ pin is driven low, the A port is routed to either B port or C port depending on the configuration of SEL0 and SEL1 signals. The B and C port can also be partially turned on when SEL0 and SEL1 are not both high or both low. Refer to Table 1 for the control logic details.

Table 1. Logic Control Table

CONTROL PINS			FUNCTION
$\overline{EN}$	SEL0	SEL1	
H	X	X	Power –down mode. All channels off (isolated)
L	L	L	Port A to port B ON Port A to port C OFF (isolated)
L	L	H	A [0,1,4,5,8,9] ↔ B [0,1,4,5,8,9] A [2,3,6,7,10,11] ↔ C [2,3,6,7,10,11] All other channels OFF (isolated)
L	H	L	A [2,3,6,7,10,11] ↔ B [2,3,6,7,10,11] A [0,1,4,5,8,9] ↔ C [0,1,4,5,8,9] All other channels OFF (isolated)
L	H	H	Port A to port B OFF (isolated) Port A to port C ON

Product Folder Links: *TS3DDR4000*

9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS3DDR4000 is a high-speed switch targeted for DDR memory applications that require 1:2 or 2:1 switching. The following sections describe two application scenarios that are widely used. In addition to memory applications, the TS3DDR4000 can also be used for generic high-speed switching that requires high bandwidth and minimal signal degradation.

9.2 Typical Application

9.2.1 Non-Volatile Dual In-line Memory Module (NVDIMM) application
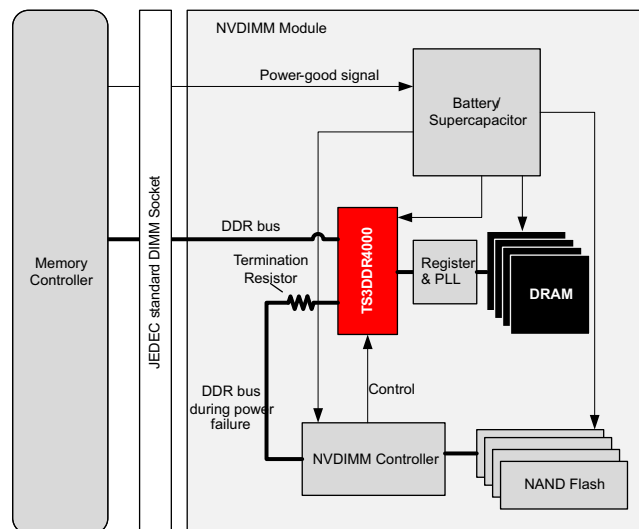
Figure 19. TS3DDR4000 Used In NVDIMM Application

9.2.1.1 Design Requirements

The TS3DDR4000 can be used in the NVDIMM application to provide server systems reliable data backups when the system encounters power-failure conditions. Figure 19 depicts a typical NVDIMM design utilizing the TS3DDR4000.

In normal system operation, the TS3DDR4000 routes the DDR signals between the system and the DRAM for normal data access. When the system encounters power failure, the charge stored in the battery or the super capacitor is used to power the NVDIMM controller, which configures the TS3DDR4000 to save the data from DRAM into the NAND Flash. The NAND Flash is non-volatile in nature, so the data stored internally stays intact even when the power goes away eventually. When the system power comes back on, the NVDIMM controller can re-route the data from the NAND Flash through the TS3DDR4000 back into the DRAM and can subsequently re-start the normal system operation.

Typical Application (continued)

9.2.1.2 *Detailed Design Procedure*

The battery or the super capacitor needs to be designed to have enough capacity to maintain the power long enough for the backup procedure to be completed. At a backup speed of 128 MB/sec, it takes about 10 seconds per 1 GB to either backup or restore the data. Typically a super capacitor is preferred for its longer life of operation. The super capacitor is usually a separate module and is connected to the NVDIMM via a cable.

NVDIMMs require support from the system motherboard. When plugged in, the BIOS must recognize the NVDIMMs. Manufacturers who control the BIOS and MRC (memory reference code) can make the necessary code changes to implement NVDIMMs into their servers.

9.2.2 Load Isolation Application
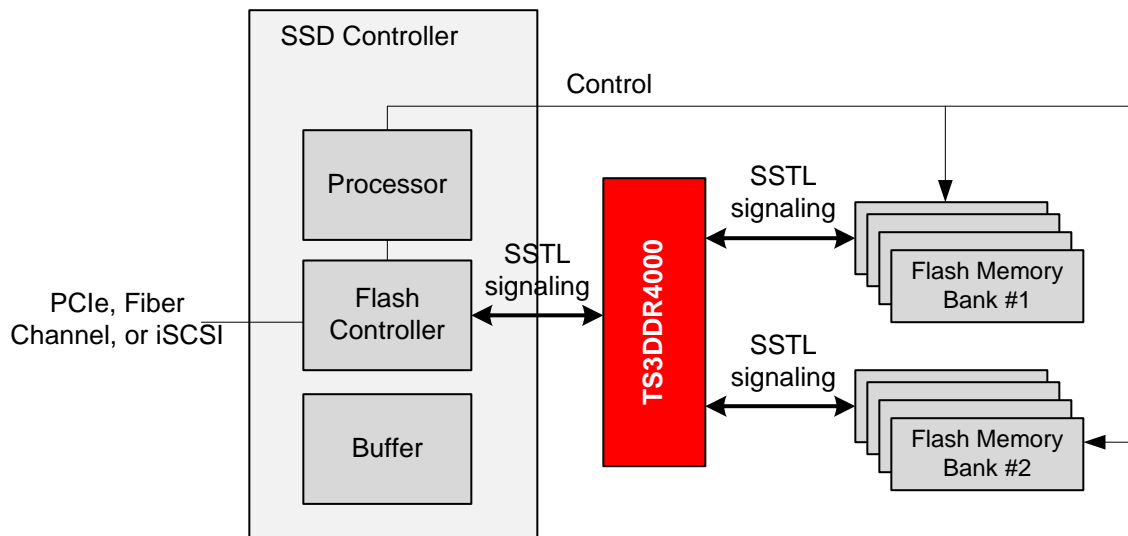
Figure 20. TS3DDR4000 Used In Load Isolation Application

9.2.2.1 *Design Requirements*

In recent years, the size of Solid-State-Drives (SSDs) has increased rapidly, making it necessary to increase the number of flash memory devices in each drive. The flash memory devices sometimes share the same control and data channel to communicate with the controller. This causes increased loading to each communication channel as the number of flash memory devices increases. To meet the performance requirement of an SSD, the ability to isolate the loading becomes necessary.

9.2.2.2 *Detailed Design Procedure*

As depicted in Figure 20, the TS3DDR4000 can be used for load isolation purpose. Flash memory bank #1 and #2 can share the same communication channel to the flash controller without increasing the loading to each other. While the TS3DDR4000 is enabled for one channel, the other channel is fully isolated. The off-isolation specification is about –21 dB at 1067 MHz, as described in the *Specifications* section.

10 Power Supply Recommendations

V_{DD} should be in the range of 2.375 V to 3.6 V. A 0.1 µF or higher decoupling capacitors placed as closed to the BGA pad as possible is recommended. There are no power sequence requirements for the TS3DDR4000.

11 Layout

11.1 Layout Guidelines

Standard layout technique for 0.65 mm pitch BGA package shall be employed. The following commonly-used printed-circuit-board (PCB) layout guidelines are recommended:

- Use Non-Solder-Mask-Defined (NSMD), rather than Solder-Mask-Defined (SMD) pads for the BGA solder balls to adhere if possible. For most applications, the NSMD pads provide more flexibility, fewer stress.

Solder mask   Copper pad   Solder mask

PCB   PCB

Solder Mask Defined   Non-Solder Mask Defined
(SMD) Pads   (NSMD) Pads
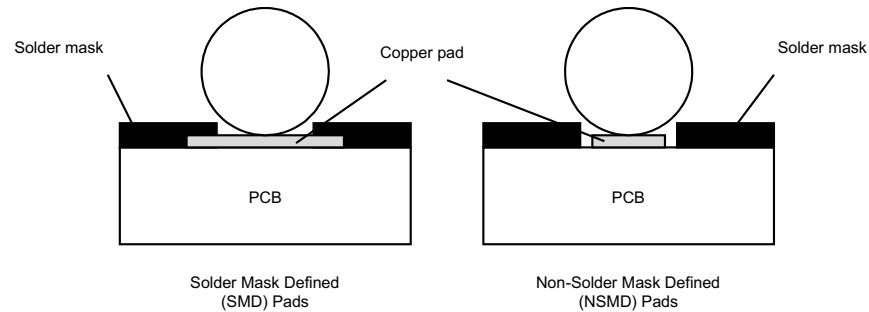
Figure 21. Solder-Mask-Defined (SMD) and Non-Solder-Mask-Defined (NSMD) Pads

- One trace can generally be routed between two solder pads of a 0.65 mm pitch BGA. This allows the outer two rows of solder pads to be routed on the same top/bottom layer. The TS3DDR4000 has 4 rows, and thus no VIAs is generally required to route all the inner balls out.
- Generally high-speed signal layout guidelines:
  - To minimize the effects of crosstalk on adjacent traces, keep the traces at least two times the trace width apart.
  - Separate high-speed signals from low-speed signals and digital from analog signals.
  - Avoid right-angle bends in a trace and try to route them at least with two 45° corners.
  - The high-speed differential signal traces should be routed parallel to each other as much as possible. The traces are recommended to be symmetrical.
  - A solid ground plane should be placed next to the high-speed signal layer. This also provides an excellent low-inductance path for the return current flow.

11.2 Layout Example
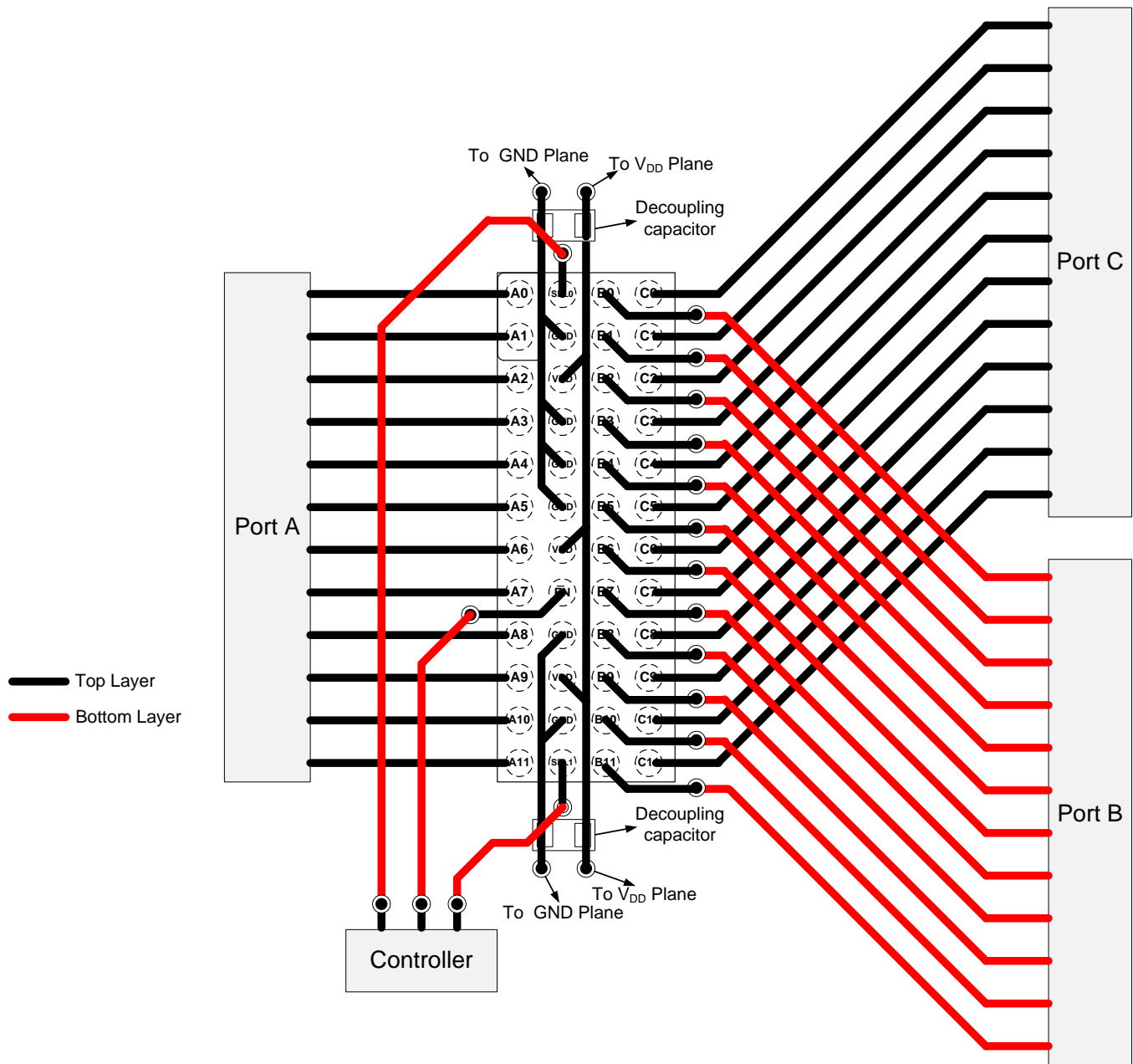
Figure 22. TS3DDR4000 Layout Example

Product Folder Links: *TS3DDR4000*

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

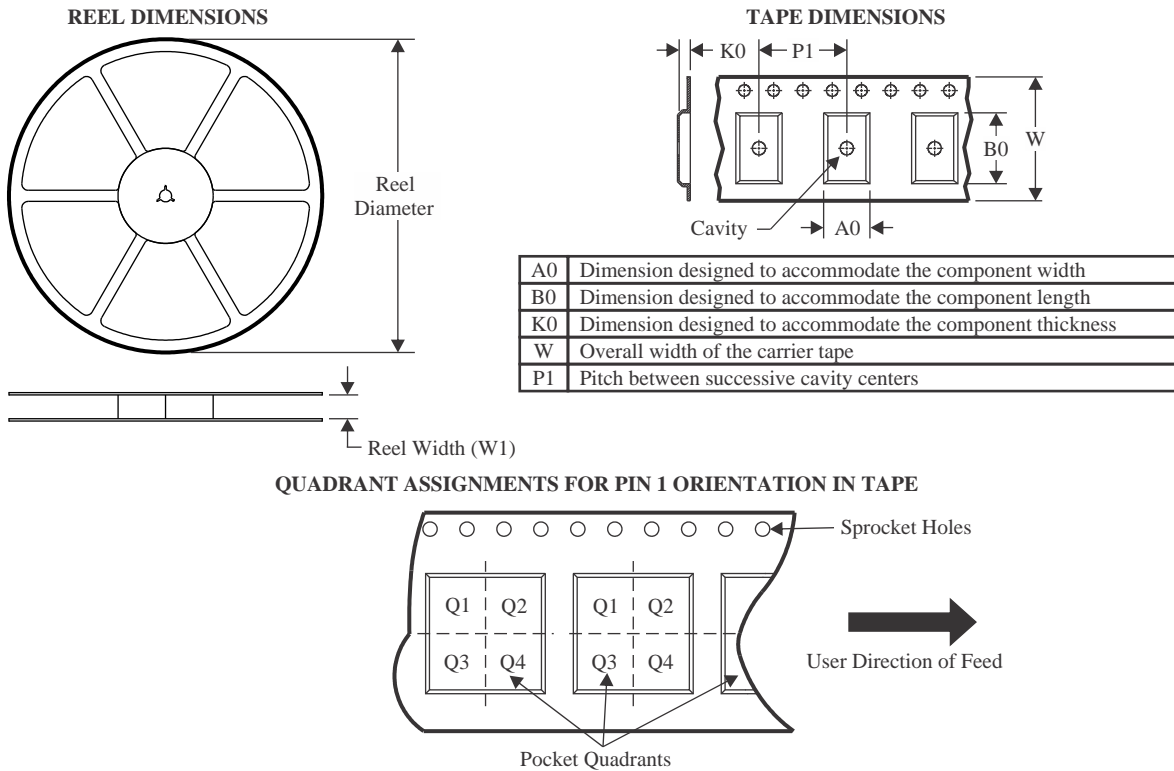| Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS3DDR4000ZBAR	Active	Production	NFBGA (ZBA) | 48	3000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DDR4000
TS3DDR4000ZBAR.A	Active	Production	NFBGA (ZBA) | 48	3000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DDR4000

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

K0 P1 W B0 Cavity A0

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

Q1 Q2 Q3 Q4

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3DDR4000ZBAR	NFBGA	ZBA	48	3000	330.0	16.4	3.4	8.4	1.3	8.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3DDR4000ZBAR	NFBGA	ZBA	48	3000	336.6	336.6	31.8

A | 3.1 / 2.9 | B

BALL A1 CORNER

8.1 / 7.9

1.95 TYP

0.65 TYP

0.65 TYP

4 3 2 1

A B C D E F G H J K L M

SYMM ₵

7.15 TYP

SYMM ₵

(0.43) TYP

(0.53) TYP

48X ⌀ 0.4 / 0.3

| ⌖ | ⌀ 0.15 Ⓜ | C | A Ⓢ | B Ⓢ |
| | ⌀ 0.08 Ⓜ | C | NOTE 3 | |

1.2 MAX

C | NOTE 4

SEATING PLANE

0.24 / 0.19 TYP

BALL TYP

⌒ | 0.1
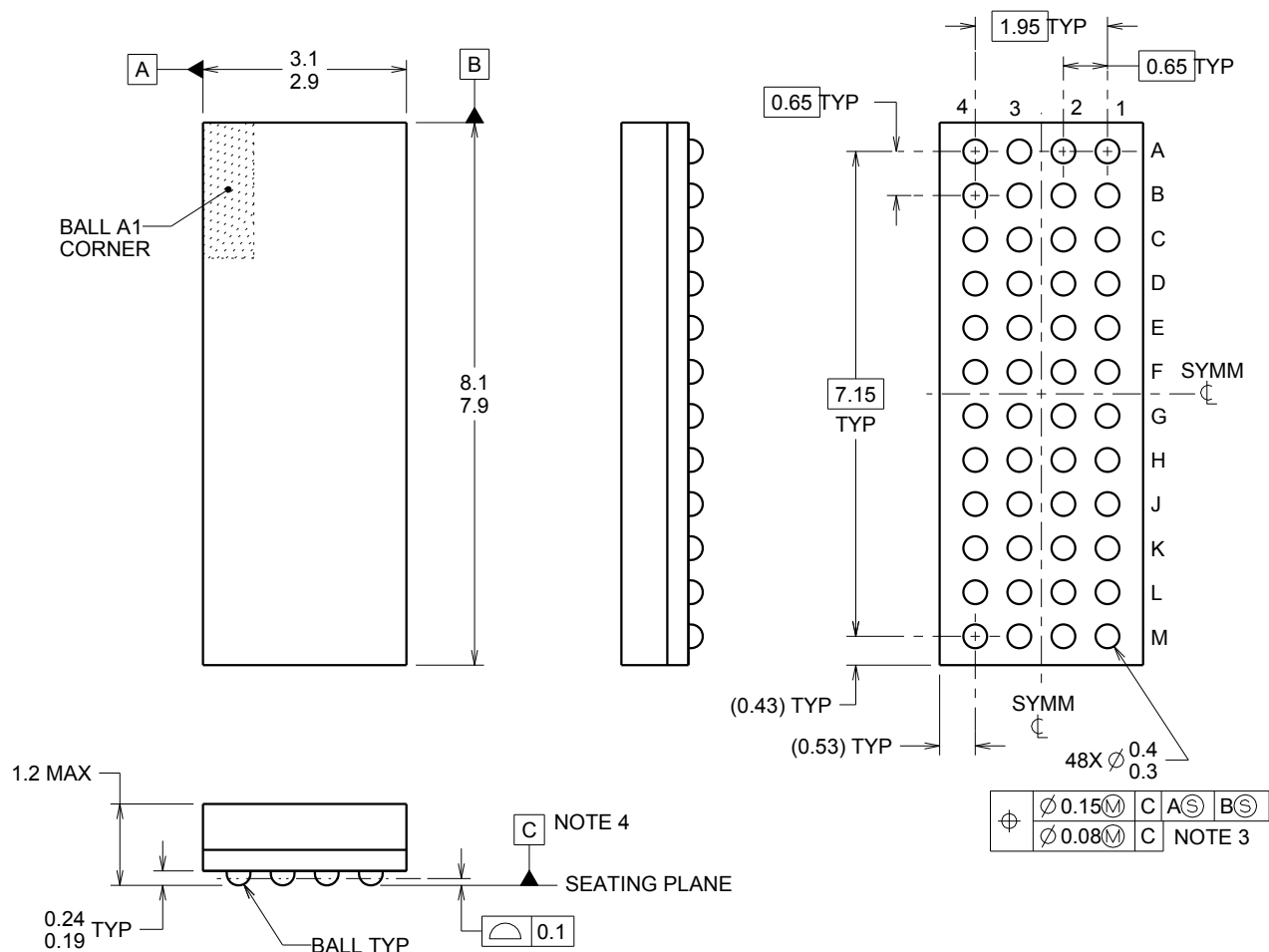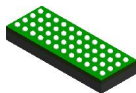
4221524/A 07/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.

48X ($\varnothing$ 0.35)

(0.65) TYP

(0.65) TYP

1 2 3 4

A B C D E F G H J K L M

SYMM ₡

SYMM ₡
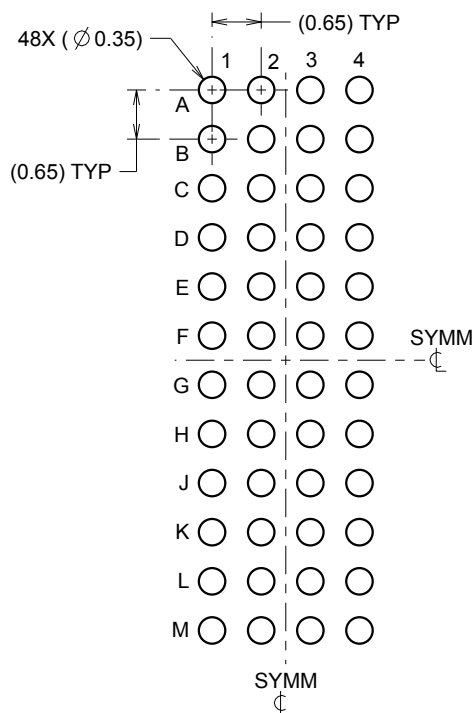
LAND PATTERN EXAMPLE
SCALE:10X

($\varnothing$ 0.35) METAL

0.05 MAX

SOLDER MASK OPENING

NON-SOLDER MASK DEFINED (PREFERRED)

0.05 MIN

METAL UNDER MASK

($\varnothing$ 0.35) SOLDER MASK OPENING

SOLDER MASK DEFINED
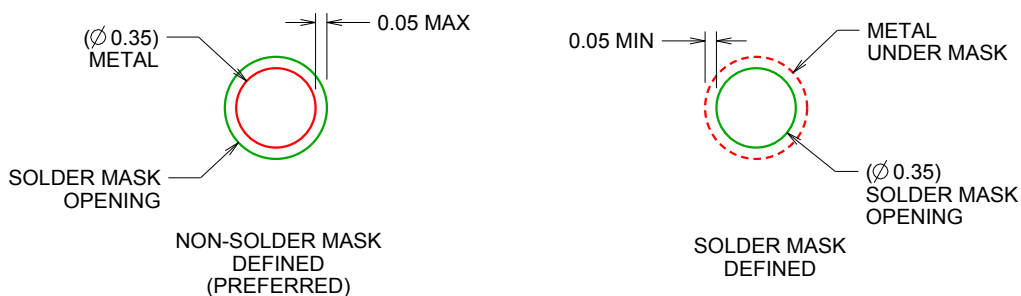
SOLDER MASK DETAILS
NOT TO SCALE

4221524/A   07/2014

NOTES: (continued)

5. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments Literature number SPRAA99 (www.ti.com/lit/spraa99).

(0.65) TYP

48X (⌀ 0.35)

(0.65) TYP

SYMM ℄

SYMM ℄
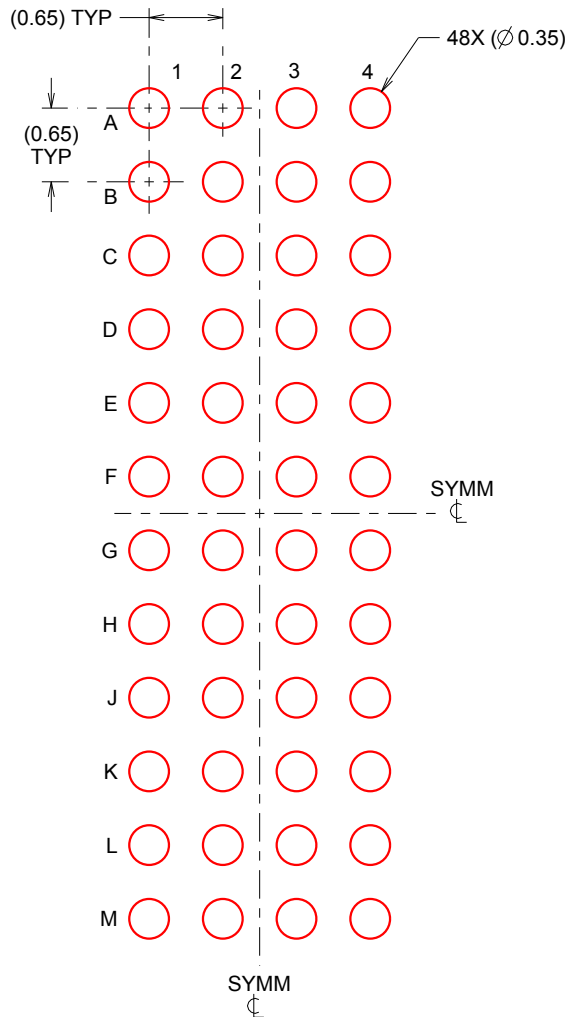
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4221524/A 07/2014

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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