











Instruments

TS3A4751

SCDS227F - JULY 2006-REVISED MARCH 2015

TS3A4751 0.9-Ω Low-voltage, single-supply, 4-channel spst analog switch

Features

- Low ON-State Resistance (R_{ON})
 - 0.9 Ω Max (3-V Supply)
 - 1.5 Ω Max (1.8-V Supply)
- R_{ON} Flatness: 0.4 Ω Max (3-V)
- R_{ON} Channel Matching
 - 0.05 Ω Max (3-V Supply)
 - 0.15 Ω Max (1.8-V Supply)
- 1.6-V to 3.6-V Single-Supply Operation
- 1.8-V CMOS Logic Compatible (3-V Supply)
- High Current-Handling Capacity (100 mA Continuous)
- Fast Switching: $t_{ON} = 5$ ns, $t_{OFF} = 4$ ns
- Supports Both Digital and Analog Applications
- ESD Protection Exceeds JESD-22
 - ±4000-V Human Body Model (A114-A)
 - 300-V Machine Model (A115-A)
 - ±1000-V Charged-Device Model (C101)

Applications

- **Power Routing**
- **Battery-Powered Systems**
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communications Circuits
- **PCMCIA Cards**
- Cellular Phones
- Modems
- Hard Drives

3 Description

The TS3A4751 device is a bidirectional, 4-channel, normally open (NO) single-pole single-throw (SPST) analog switch that operates from a single 1.6-V to 3.6-V supply. This device has fast switching speeds, handles rail-to-rail analog signals, and consumes very low quiescent power.

The digital input is 1.8-V CMOS compatible when using a 3-V supply.

The TS3A4751 device has four normally open (NO) switches. The TS3A4751 is available in a 14-pin thin shrink small-outline package (TSSOP) and in spacesaving 14-pin VQFN (RGY) and micro X2QFN (RUC) packages.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
	TSSOP (14)	5.00 mm × 4.40 mm
TS3A4751	VQFN (14)	3.50 mm × 3.50 mm
	X2QFN (14)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

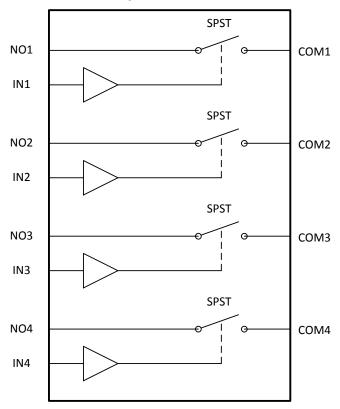




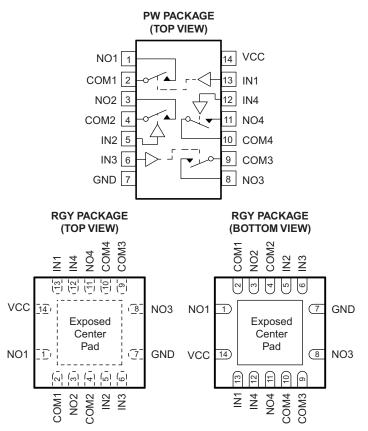
Table of Contents

1	Features 1	7.3	Feature Description	13
2	Applications 1	7.4	Device Functional Modes	13
3	Description 1	8 Appl	ication and Implementation	14
4	Revision History2	8.1	Application Information	14
5	Pin Configuration and Functions	8.2	Typical Application	14
6	Specifications4	9 Pow	er Supply Recommendations	16
٠	6.1 Absolute Maximum Ratings	10 Lay	out	16
	6.2 ESD Ratings	10.1	Layout Guidelines	16
	6.3 Recommended Operating Conditions	10.2	Layout Example	16
	6.4 Thermal Information	11 Devi	ice and Documentation Support	17
	6.5 Electrical Characteristics for 1.8-V Supply	11.1	Receiving Notification of Documentation Upda	tes 17
	6.6 Electrical Characteristics for 3-V Supply	11.2	Community Resources	17
	6.7 Typical Characteristics	11.3	Trademarks	17
7	Detailed Description	11.4	Electrostatic Discharge Caution	17
-	7.1 Overview	11.5	Glossary	17
	7.2 Functional Block Diagram		hanical, Packaging, and Orderable mation	17

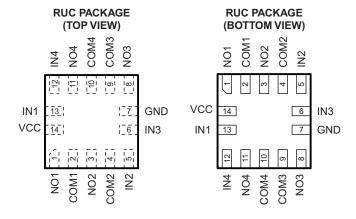
4	Revision History	
Cł	nanges from Revision E (January 2015) to Revision F	Page
•	Changed Supply Voltage from: 3.3 V to: 3.6 V in the Recommended Operating Conditions	5
Cł	nanges from Revision D (July 2008) to Revision E	Page
•	Added Pin Configuration and Functions section, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section	1



5 Pin Configuration and Functions



If the exposed center pad is used, it must be connected as a secondary ground or left electrically open.





Pin Functions

PIN		1/0	DESCRIPTION
NO.	NAME	I/O	DESCRIPTION
1	NO1	I/O	Normally open signal path
2	COM1	I/O	Common signal path
3	NO2	I/O	Normally open signal path
4	COM2	I/O	Common signal path
5	IN2	I	Logic control input
6	IN3	I	Logic control input
7	GND	_	Ground
8	NO3	I/O	Normally open signal path
9	COM3	I/O	Common signal path
10	COM4	I/O	Common signal path
11	NO4	I/O	Normally open signal path
12	IN4	I	Logic control input
13	IN1	I	Logic control input
14	V _{CC}	I	Positive supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage referenced to GND ⁽²⁾	-0.3	4	٧	
$\begin{array}{c} V_{NO} \\ V_{COM} \\ V_{IN} \end{array}$	Analog and digital voltage	-0.3	V _{CC} + 0.3	٧	
I _{NO} I _{COM}	On-state switch current	V_{NO} , $V_{COM} = 0$ to V_{CC}	-100	100	mA
I_{CC} I_{GND}	Continuous current through V _{CC} or GND			±100	mA
V	Peak current pulsed at 1 ms, 10% duty cycle	COM, V _{I/O}		±200	mA
T _A	Operating temperature		-40	85	°C
T_{J}	Junction temperature			150	°C
T _{stg}	Storage temperature	-65	150	°C	

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000		
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002 (2)	±1000	V
		Machine Model	±300	

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

⁽²⁾ Signals on COM or NO exceeding V_{CC} or GND are clamped by internal diodes. Limit forward diode current to maximum current rating.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply Voltage	1.65	3.6	V
$V_{NO} \ V_{COM} \ V_{IN}$	Analog and digital voltage range	0	V _{CC}	V

6.4 Thermal Information

			TS3A4751		
	THERMAL METRIC ⁽¹⁾	PW	RGY	RUC	UNIT
			14 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	132.3	68.5	196.4	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.6	83.1	73.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	74.2	44.6	130.7	°C/W
ΨЈТ	Junction-to-top characterization parameter	11.2	7.8	2.1	10/00
ΨЈВ	Junction-to-board characterization parameter	73.6	44.7	130.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	24.6	N/A	

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.



6.5 Electrical Characteristics for 1.8-V Supply

 $V_{cc} = 1.65 \text{ V}$ to 1.95 V. $T_{A} = -40 \text{ °C}$ to 85 °C. $V_{UJ} = 1 \text{ V}$. $V_{U} = 0.4 \text{ V}$ (unless otherwise noted) (1) (2)

	PARAMETER	TEST CONDITION	ONS	T _A	MIN	TYP ⁽³⁾	MAX	UNIT
ANALOG SV	WITCH							
V _{COM} , V _{NO}	Analog signal range				0		V_{CC}	V
D	ONI state resistance	V _{CC} = 1.8 V, I _{COM} = -10 m/	Vcc = 1.8 V. Icom = -10 mA.			1	1.5	
R _{on}	ON-state resistance	$V_{NO} = 0.9 \text{ V}$		Full			2	Ω
4.D	ON-state resistance match	V _{CC} = 1.8 V, I _{COM} = -10 m/	٩,	25°C		0.09	0.15	
ΔR_{on}	between channels (4)	$V_{NO} = 0.9 \text{ V}$		Full			0.25	Ω
D	ON-state resistance	$V_{CC} = 1.8 \text{ V}, I_{COM} = -10 \text{ m/s}$	۹,	25°C		0.7	0.9	0
R _{on(flat)}	flatness (5)	0 ≤ V _{NO} ≤ V _{CC}		Full			1.5	Ω
	NO	$V_{CC} = 1.95 \text{ V}, V_{COM} = 0.15$	V, 1.65 V,	25°C	-1	0.5	1	
I _{NO(OFF)}	OFF leakage current ⁽⁶⁾	$V_{NO} = 1.8 \text{ V}, 0.15 \text{ V}$,	Full	-10		10	nA
	COM	V _{CC} = 1.95 V, V _{COM} = 0.15	V, 1.65 V,	25°C	-1	0.5	1	- 0
COM(OFF)	OFF leakage current ⁽⁶⁾	$V_{NO} = 1.65 \text{ V}, 0.15 \text{ V}$,	Full	-10		10	nA
	COM	V _{CC} = 1.95 V, V _{COM} = 0.15	V. 1.65 V.	25°C	-1	0.01	1	
ICOM(ON)	ON leakage current ⁽⁶⁾	$V_{NO} = 0.15 \text{ V}, 1.65 \text{ V}, or flow$		Full	-3		3	nA
DYNAMIC							'	
	Town on Care	$V_{NO} = 1.5 \text{ V}, R_{L} = 50 \Omega,$		25°C		6	18	
t _{ON}	Turn-on time	C _L = 35 pF, See Figure 1		Full			20	ns
	- ""	$V_{NO} = 1.5 \text{ V}, R_L = 50 \Omega,$		25°C		5	10	
t _{OFF}	Turn-off time	$C_L = 35 \text{ pF}, \text{ See Figure 1}$		Full			12	ns
Q _C	Charge injection	V _{GEN} = 0, R _{GEN} = 0, C _L = 1 nF, See Figure 5		25°C		3.2		pC
C _{NO(OFF)}	NO OFF capacitance	f = 1 MHz, See Figure 2		25°C		23		pF
C _{COM(OFF)}	COM OFF capacitance	f = 1 MHz, See Figure 2		25°C		20		pF
C _{COM(ON)}	COM ON capacitance	f = 1 MHz, See Figure 2		25°C		43		pF
BW	Bandwidth	$R_L = 50 \Omega$, Switch ON		25°C		123		MHz
0	OFF inslation (7)	$R_L = 50 \Omega, C_L = 5 pF,$	f = 1 MHz	0500		-61		-10
O _{ISO}	OFF isolation ⁽⁷⁾	See Figure 3	f = 10 MHz	25°C		-36		dB
V	0	$R_L = 50 \Omega, C_L = 5 pF,$	f = 10 MHz	0500		-95		-ID
X _{TALK}	Crosstalk	See Figure 3	f = 100 MHz	25°C		-73		dB
TUD	Total bassassia distantas	f = 20 Hz to 20 kHz, V _{COM}	$R_L = 32 \Omega$	0500		0.14%		
THD	Total harmonic distortion	= 2 V _{P-P}	$R_L = 600 \Omega$	25°C		0.013%		
DIGITAL CO	NTROL INPUTS (IN1–IN4)							
V _{IH}	Input logic high			Full	1			V
V _{IL}	Input logic low			Full			0.4	V
	Innut lookogo	\/ 0 or \/		25°C		0.1	5	A
I _{IN}	Input leakage current	$V_I = 0 \text{ or } V_{CC}$		Full	-10		10	nA
SUPPLY							'	
V _{CC}	Power-supply range				1.6		3.6	V
_	Decitive construction	\/ O ==\/		25°C			0.05	
I _{CC}	Positive-supply current	$V_I = 0$ or V_{CC}		Full			0.5	μΑ

The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Submit Documentation Feedback

Copyright © 2006-2015, Texas Instruments Incorporated

⁽²⁾ Parts are tested at 85°C and specified by design and correlation over the full temperature range.

Typical values are at $T_A = 25$ °C. (3)

 $[\]Delta r_{on} = r_{on(max)} - r_{on(min)}$ Flatness is defined as the difference between the maximum and minimum value of r_{on} as measured over the specified analog signal (5)

Leakage parameters are 100% tested at the maximum-rated hot operating temperature and specified by correlation at $T_A = 25$ °C. OFF isolation = $20_{log}10$ (V_{COM}/V_{NO}), $V_{COM} = output$, $V_{NO} = input$ to OFF switch



6.6 Electrical Characteristics for 3-V Supply

 $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}, T_{A} = -40 ^{\circ}\text{C} \text{ to } 85 ^{\circ}\text{C}, V_{IH} = 1.4 \text{ V}, V_{II} = 0.5 \text{ V (unless otherwise noted)}.$ (1) (2)

	PARAMETER	TEST COND	ITIONS	TA	MIN	TYP ⁽³⁾	MAX	UNIT
ANALOG SW	/ITCH							
V _{COM} , V _{NO}	Analog signal range				0		V _{CC}	V
		$V_{CC} = 2.7 \text{ V}, I_{COM} = -1$	00 mA.	25°C		0.7	0.9	
R _{on}	ON-state resistance	$V_{NO} = 1.5 \text{ V}$,	Full			1.1	Ω
	ON-state resistance match	$V_{CC} = 2.7 \text{ V}, I_{COM} = -1$	00 mA.	25°C		0.03	0.05	
ΔR_{on}	between channels (4)	V _{NO} = 1.5 V	,	Full			0.15	Ω
_	ON-state resistance	Voc = 2.7 V. Icon = -1	00 mA.	25°C		0.23	0.4	
R _{on(flat)}	flatness ⁽⁵⁾	$V_{NO} = 1 \text{ V}, 1.5 \text{ V}, 2 \text{ V}$	$V_{CC} = 2.7 \text{ V}, I_{COM} = -100 \text{ mA},$ $V_{NO} = 1 \text{ V}, 1.5 \text{ V}, 2 \text{ V}$				0.5	Ω
	NO	$V_{CC} = 3.6 \text{ V}, V_{COM} = 0$.3 V. 3 V.	25°C	-2	1	2	
I _{NO(OFF)}	OFF leakage current (6)	$V_{NO} = 3 \text{ V}, 0.3 \text{ V}$, ,	Full	-18		18	nA
	COM	$V_{CC} = 3.6 \text{ V. } V_{COM} = 0$.3 V. 3 V.	25°C	-2	1	2	
I _{COM(OFF)}	OFF leakage current (6)	$V_{CC} = 3.6 \text{ V}, V_{COM} = 0.3 \text{ V}, 3 \text{ V}, V_{NO} = 3 \text{ V}, 0.3 \text{ V}$		Full	-18		18	nA
	COM	$V_{CC} = 3.6 \text{ V}, V_{COM} = 0$.3 V. 3 V.	25°C	-2.5	0.01	2.5	
I _{COM(ON)}	ON leakage current ⁽⁶⁾	$V_{NO} = 0.3 \text{ V}, 3 \text{ V}, or flow$		Full	-5		5	nA
DYNAMIC								
	Turn-on time $ \begin{array}{c} V_{NO} = 1.5 \text{ V, R}_L = 50 \ \Omega, \\ C_L = 35 \text{ pF, See Figure 1} \end{array} $		25°C		5	14		
t _{ON}			1	Full			15	ns
	-	V _{NO} = 1.5 V, R _L = 50 Ω	Σ.	25°C		4	9	ns
t _{OFF}	Turn-off time	$C_L = 35 \text{ pF}, \text{ See Figure}$		Full			10	
Q_C	Charge injection	V _{GEN} = 0, R _{GEN} = 0, C _L = 1 nF, See Figure 5		25°C		3		рС
C _{NO(OFF)}	NO OFF capacitance	f = 1 MHz, See Figure 2	f = 1 MHz, See Figure 2			23		pF
$C_{COM(OFF)}$	COM OFF capacitance	f = 1 MHz, See Figure 2	2	25°C		20		pF
C _{COM(ON)}	COM ON capacitance	f = 1 MHz, See Figure 2	2	25°C		43		рF
BW	Bandwidth	$R_L = 50 \Omega$, Switch ON		25°C		125		MHz
^	OFF isolation ⁽⁷⁾	$R_L = 50 \Omega, C_L = 5 pF,$	f = 10 MHz	2500		-40		٩D
O _{ISO}	OFF ISOIdtion 7	See Figure 3	f = 1 MHz	25°C		-62		dB
V	Crosstalk	$R_L = 50 \Omega, C_L = 5 pF,$	f = 10 MHz	2500		-73		٩D
X _{TALK}	Ciussiaik	See Figure 3	f = 1 MHz	25°C		-95		dB
TUD	Tatal hammania diatantian	f = 20 Hz to 20 kHz,	R _L = 32 Ω	0500		0.04%		
THD	Total harmonic distortion	$V_{COM} = 2 V_{P-P}$	$R_L = 600 \Omega$	25°C		0.003%		
DIGITAL COI	NTROL INPUTS (IN1-IN4)							
V_{IH}	Input logic high			Full	1.4			V
V _{IL}	Input logic low			Full			0.5	V
	Janut Jackson surrent			25°C		0.5	1	- ^
I _{IN}	Input leakage current	$V_I = 0$ or V_{CC}		Full	-20		20	nA
SUPPLY								
V _{CC}	Power-supply range				1.6		3.6	V
_	Dealth a supply supply	V 20VV 2	\/	25°C	25°C (0.075	μА
I _{CC}	Positive-supply current	$v_{CC} = 3.6 \text{ V}, V_{IN} = 0 \text{ or}$	$V_{CC} = 3.6 \text{ V}, V_{IN} = 0 \text{ or } V_{CC}$				0.75	

⁽¹⁾ The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Submit Documentation Feedback

⁽²⁾ Parts are tested at 85°C and specified by design and correlation over the full temperature range.

Typical values are at $V_{CC} = 3 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$. (3)

 $[\]Delta r_{on} = r_{on(max)} - r_{on(min)}$ Flatness is defined as the difference between the maximum and minimum value of r_{on} as measured over the specified analog signal

Leakage parameters are 100% tested at the maximum-rated hot operating temperature and specified by correlation at $T_A = 25$ °C. OFF isolation = $20_{log}10$ (V_{COM}/V_{NO}), $V_{COM} = output$, $V_{NO} = input$ to OFF switch



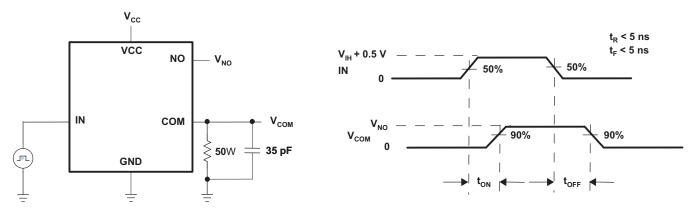


Figure 1. Switching Times

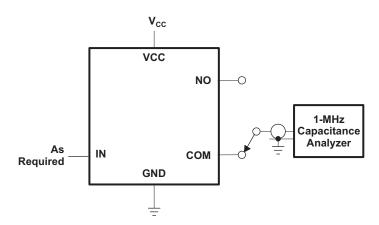
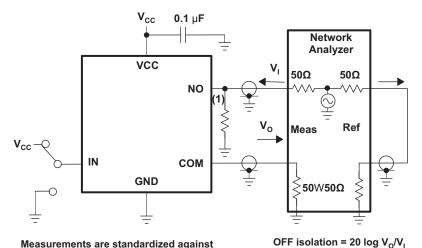


Figure 2. NO and COM Capacitance



Measurements are standardized against short at socket terminals. OFF isolation is measured between COM and OFF terminals on each switch. Bandwidth is measured between COM and ON terminals on each switch. Signal direction through switch is reversed; worst values are recorded.

0 0 1

 $^{(1)}$ Add 50-Ω termination for OFF isolation

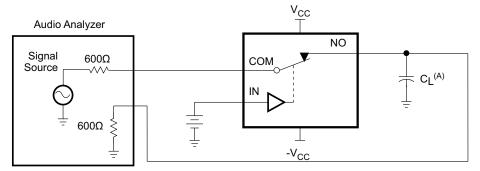
Figure 3. OFF Isolation, Bandwidth, and Crosstalk

Submit Documentation Feedback

Copyright © 2006–2015, Texas Instruments Incorporated

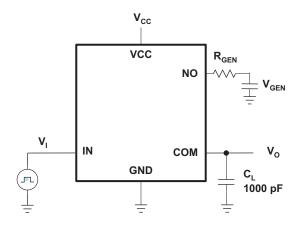


Channel ON: COM to NO V_I = V_{CC} C_L = 50 pF V_{SOURCE} = V_{CC}P-P f_{SOURCE} = 20 Hz to 20 kHz R_L = 600 Ω



A. C_L includes probe and jig capacitance.

Figure 4. Total Harmonic Distortion (THD)



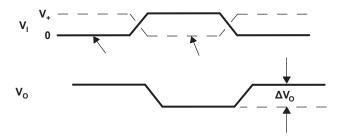
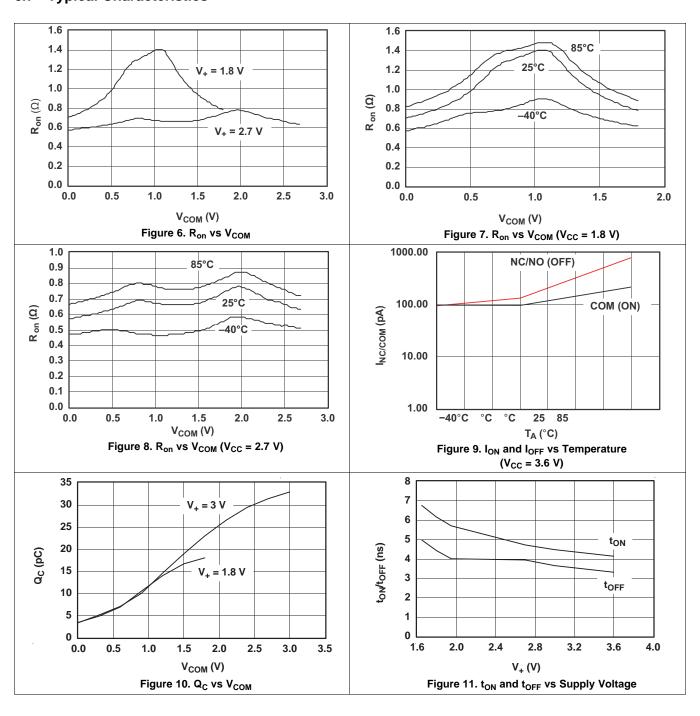


Figure 5. Charge Injection (Q_C)



6.7 Typical Characteristics

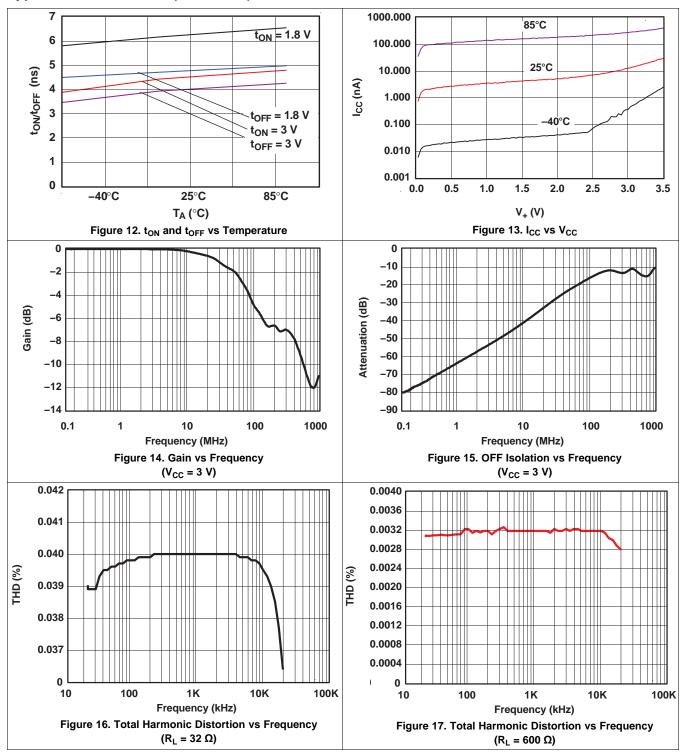


Submit Documentation Feedback

Copyright © 2006–2015, Texas Instruments Incorporated

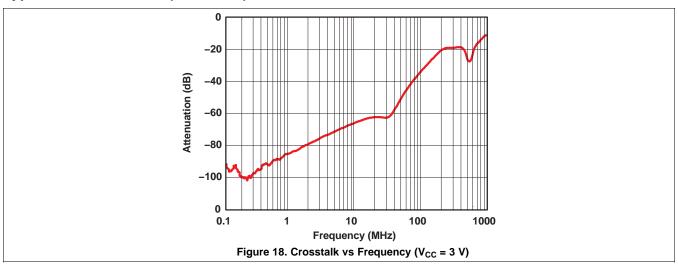


Typical Characteristics (continued)





Typical Characteristics (continued)





7 Detailed Description

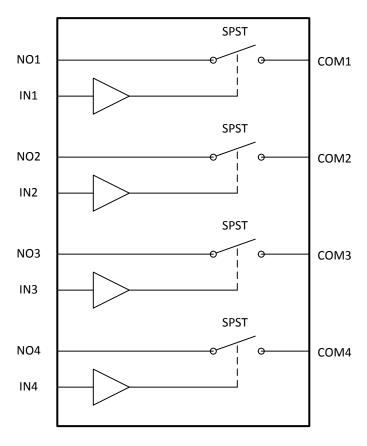
7.1 Overview

The TS3A4751 is a bidirectional, 4-channel, normally open (NO) single-pole single-throw (SPST) analog switch that operates from a single 1.6-V to 3.6-V supply. This device has fast switching speeds, handles rail-to-rail analog signals, and consumes very low quiescent power.

The digital input is 1.8-V CMOS compatible when using a 3-V supply.

The TS3A4751 has four normally open (NO) switches. The TS3A4751 is available in a 14-pin thin shrink small-outline package (TSSOP) and in space-saving 14-pin VQFN (RGY) and micro X2QFN (RUC) packages.

7.2 Functional Block Diagram



7.3 Feature Description

This device has fast switching speeds, handles rail-to-rail analog signals, and consumes very low quiescent power.

The digital input is 1.8-V TTL/CMOS compatible when using a 3-V supply.

7.4 Device Functional Modes

Table 1. Function Table

IN	NO TO COM, COM TO NO
L	OFF
Н	ON



8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Logic Inputs

The TS3A4751 logic inputs can be driven up to 3.6 V, regardless of the supply voltage. For example, with a 1.8-V supply, IN may be driven low to GND and high to 3.6 V. Driving IN rail to rail minimizes power consumption.

8.1.2 Analog Signal Levels

Analog signals that range over the entire supply voltage (V_{CC} to GND) can be passed with very little change in R_{on} (see *Typical Characteristics*). The switches are bidirectional, so NO and COM can be used as either inputs or outputs.

8.2 Typical Application

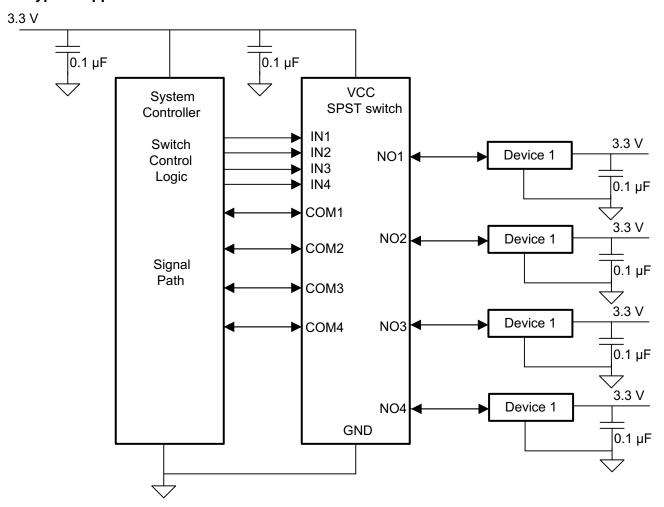


Figure 19. Typical Application Diagram



Typical Application (continued)

8.2.1 Design Requirements

Ensure that all of the signals passing through the switch are with in the specified ranges to ensure proper performance.

8.2.2 Detailed Design Procedure

The TS3A4751 and can be properly operated without any external components. However, it is recommended that unused pins should be connected to ground through a $50-\Omega$ resistor to prevent signal reflections back into the device. It is also recommneded that the digital control pins (INX) be pulled up to V_{CC} or down to GND to avoid undesired switch positions that could result from the floating pin.

8.2.3 Application Curve

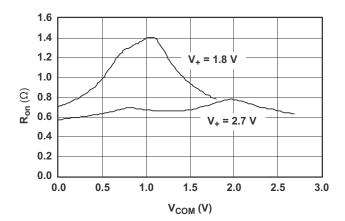


Figure 20. Ron vs V_{COM}



9 Power Supply Recommendations

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V_{CC} on first, followed by NO or COM.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{CC} supply to other components. A 0.1- μ F capacitor, connected from V_{CC} to GND, is adequate for most applications.

10 Layout

10.1 Layout Guidelines

High-speed switches require proper layout and design procedures for optimum performance.

Reduce stray inductance and capacitance by keeping traces short and wide.

Ensure that bypass capacitors are as close to the device as possible.

Use large ground planes where possible.

10.2 Layout Example



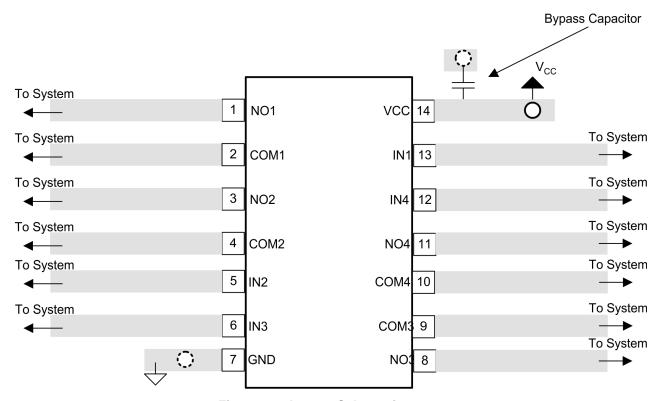


Figure 21. Layout Schematic



11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com 10-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
TS3A4751PWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YC751
TS3A4751PWR.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YC751
TS3A4751RGYR	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YC751
TS3A4751RGYR.B	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YC751
TS3A4751RGYRG4	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YC751
TS3A4751RGYRG4.B	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YC751
TS3A4751RUCR	Active	Production	QFN (RUC) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3МО
TS3A4751RUCR.B	Active	Production	QFN (RUC) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3МО
TS3A4751RUCRG4.B	Active	Production	QFN (RUC) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3МО

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

www.ti.com 10-Nov-2025

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

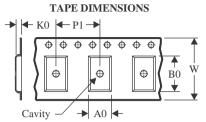
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

www.ti.com 23-Jul-2025

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A4751PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TS3A4751RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TS3A4751RGYRG4	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TS3A4751RUCR	QFN	RUC	14	3000	180.0	9.5	2.2	2.2	0.5	4.0	8.0	Q2

www.ti.com 23-Jul-2025



*All dimensions are nominal

7 till dillitoriolorio di o riorriiridi							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A4751PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TS3A4751RGYR	VQFN	RGY	14	3000	353.0	353.0	32.0
TS3A4751RGYRG4	VQFN	RGY	14	3000	353.0	353.0	32.0
TS3A4751RUCR	QFN	RUC	14	3000	189.0	185.0	36.0

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



INSTRUMENTS www.ti.com



PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
 The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

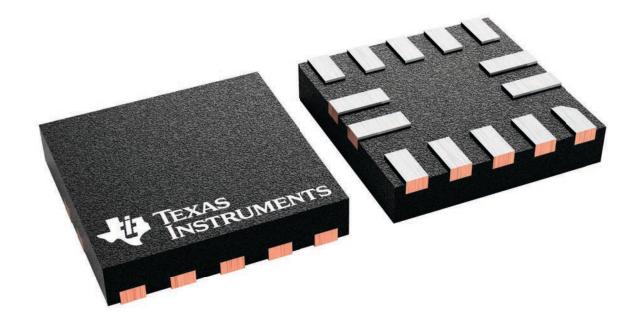
- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



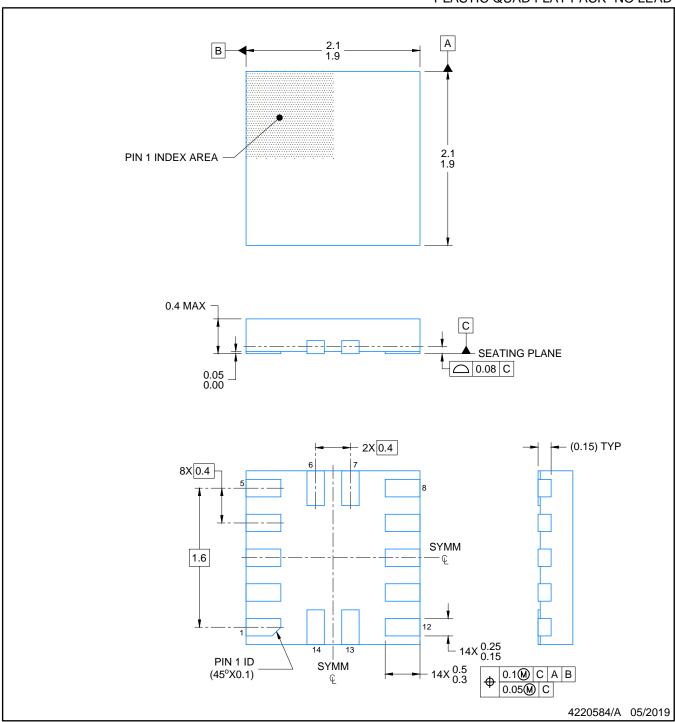
2 x 2, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



PLASTIC QUAD FLAT PACK- NO LEAD

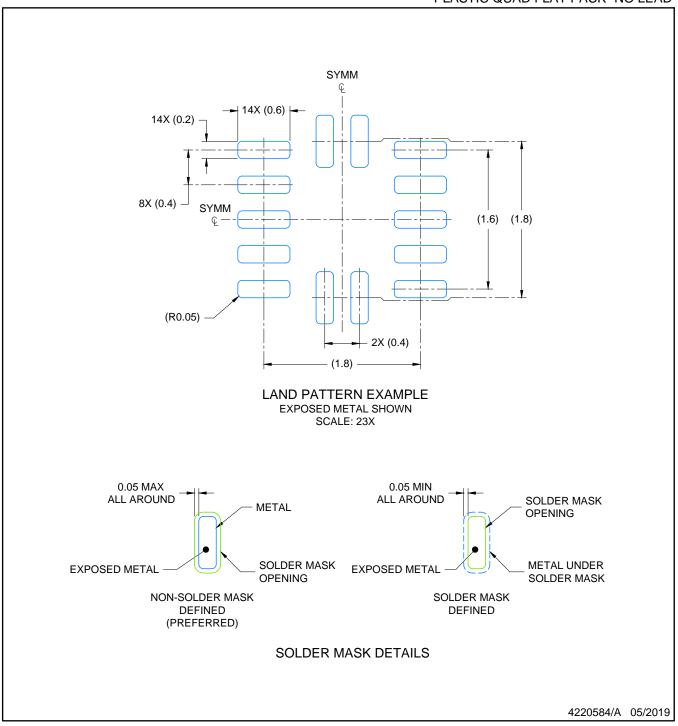


NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



PLASTIC QUAD FLAT PACK- NO LEAD

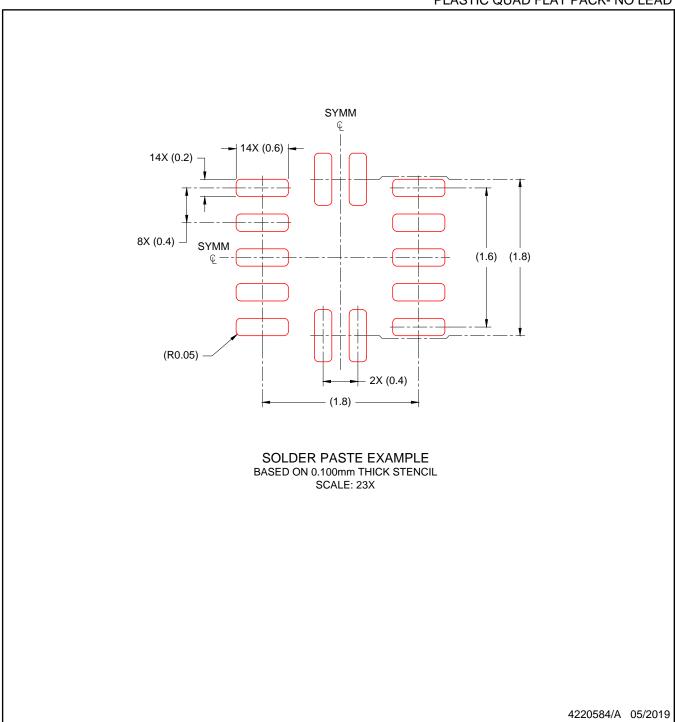


NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



PLASTIC QUAD FLAT PACK- NO LEAD



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025