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# LOW-POWER SINGLE OPERATIONAL AMPLIFIER

#### **FEATURES**

- Qualified for Automotive Applications
- Wide Power-Supply Range
  - Single Supply: 3 V to 30 V
  - Dual Supply: ±1.5 V to ±15 V
- Large Output Voltage Swing:
   0 V to 3.5 V (Min) (V<sub>CC</sub> = 5 V)
- Low Supply Current: 500 μA (Typ)
   Low Input Bias Current: 20 nA (Typ)
- Stable With High Capacitive Loads

# OUT 1 V<sub>cc-</sub> 2 IN+3 4 IN-

# **DESCRIPTION/ORDERING INFORMATION**

The TS321 is a bipolar operational amplifier for cost-sensitive applications in which space savings are important.

## ORDERING INFORMATION(1)

T <sub>A</sub>	PACK	AGE <sup>(2)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING		
-40°C to 125°C	SOT-23-5 - DBV	Reel of 3000	TS321QDBVRQ1	9CNS		

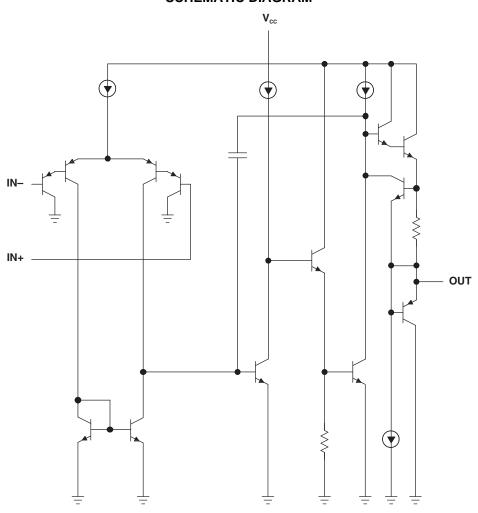
- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



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# **SCHEMATIC DIAGRAM**





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# ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
.,	Supply voltage <sup>(2)</sup>	Single		32	V
V <sub>CC</sub> V <sub>ID</sub> V <sub>I</sub> I <sub>I</sub> t <sub>short</sub>	Supply voltage (	Dual		±16	V
$V_{ID}$	Differential input voltage (3)			32	V
VI	Input voltage range (2)(4)		-0.3	32	V
I	Input current <sup>(4)</sup>			50	mA
t <sub>short</sub>	Duration of output short circuit to ground		U	Inlimited	
$\theta_{JA}$	Package thermal impedance, junction to free air <sup>(5)(6)</sup>	DBV package		206	°C/W
TJ	Operating virtual junction temperature			150	°C
T <sub>stg</sub>	Storage temperature range		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- These voltage values are with respect to the midpoint between V<sub>CC+</sub> and V<sub>CC-</sub>.
- Differential voltages are at IN+ with respect to IN-.
- (4)
- Neither input must ever be more positive than  $V_{CC+}$  or more negative than  $V_{CC-}$ . Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) - T_A)/\theta_{JA}$ . Selecting the maximum of 150°C can affect reliability.
- The package thermal impedance is calculated in accordance with JESD 51-7.

#### RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V <sub>CC</sub>	Cumply voltage	Single supply	3	30	\/
vcc	Supply voltage	Dual supply		±15	V
T <sub>A</sub>	Operating free-air temperature		-40	125	°C

Product Folder Link(s): TS321-Q1

SLOS647-AUGUST 2009 www.ti.com

## **ELECTRICAL CHARACTERISTICS**

 $V_{CC+} = 5 \text{ V}, V_{CC-} = \text{GND}, V_{O} = 1.4 \text{ V} \text{ (unless otherwise noted)}$ 

	PARAMETER	TEST CONDIT	TONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
V	longit offeet veltege	$R_S = 0, 5 \text{ V} < V_{CC+} < 3$	0 V,	25°C		0.5	4	\/
V <sub>IO</sub>	Input offset voltage	$0 < V_{IC} < (V_{CC+} - 1.5 V_{CC+})$	")	Full range			5	mV
	land offers comment		25°C		2	30	^	
I <sub>IO</sub>	Input offset current			Full range			50	nA
	land him summet(1)			25°C		20	150	^
I <sub>IB</sub>	Input bias current <sup>(1)</sup>			Full range			200	nA
^	Large-signal differential voltage	$V_{CC} = 15 \text{ V}, R_L = 2 \text{ k}\Omega$		25°C	50	100		\//m\/
A <sub>VD</sub>	amplification	$V_0 = 1.4 \text{ V to } 11.4 \text{ V}$		Full range	25			V/mV
	Common-mode input voltage <sup>(2)</sup>	V 20 V		25°C	0		V <sub>CC+</sub> – 1.5	V
V <sub>ICR</sub>	Common-mode input voltage	V <sub>CC</sub> = 30 V		Full range	0		V <sub>CC+</sub> – 2	V
			$R_L = 2 k\Omega$	25°C	26	27		
		V 20 V		Full range	25.5			
.,	Liber lavel autout valtage	V <sub>CC</sub> = 30 V	D 401.0	25°C	27	28		V
V <sub>OH</sub>	High-level output voltage		$R_L = 10 \text{ k}\Omega$	Full range	26.5			V
		V 5 V	$R_L = 2 k\Omega$	25°C	3.5			
		$V_{CC} = 5 V$		Full range	3			
	Low lovel output voltogo	$R_1 = 10 \text{ k}\Omega$		25°C		5	15	mV
V <sub>OL</sub>	Low-level output voltage	$K_{\Gamma} = 10 \text{ K}\Omega$	Full range			20	mv	
GBP	Gain bandwidth product		$V_{CC} = 30 \text{ V}, V_I = 10 \text{ mV}, R_L = 2 \text{ k}\Omega,$ f = 100 kHz, $C_L = 100 \text{ pF}$			0.8		MHz
SR	Slew rate	$V_{CC} = 15 \text{ V}, V_{I} = 0.5 \text{ V}$ $R_{L} = 2 \text{ k}\Omega, C_{L} = 100 \text{ pF}$		25°C		0.4		V/μs
φ <sub>m</sub>	Phase margin			25°C		60		0
CMRR	Common-mode rejection ratio	R <sub>S</sub> ≤ 10 kΩ		25°C	65	85		dB
I <sub>SOURCE</sub>	Output source current	$V_{CC} = 15 \text{ V}, V_{O} = 2 \text{ V},$	V <sub>ID</sub> = 1 V	25°C	20	40		mA
	Output sink ourront	V <sub>CC</sub> = 15 V, V <sub>ID</sub> = 1 V	V <sub>O</sub> = 2 V	25°C	10	20		mA
I <sub>SINK</sub>	Output sink current	v <sub>CC</sub> = 15 v, v <sub>ID</sub> = 1 v	$V_0 = 0.2 \text{ V}$	25°C	12	50		μΑ
Io	Short-circuit to GND	V <sub>CC</sub> = 15 V		25°C		40	60	mA
SVR	Supply-voltage rejection ratio	$V_{CC} = 5 \text{ V to } 30 \text{ V}$		25°C	65	110		dB
			$V_{CC} = 5 V$	25°C		500	800	
	Total supply current	No load	$V_{CC} = 30 \text{ V}$	25 C		600	900	μΑ
I <sub>CC</sub>	Total supply current	$V_{CC} = 5 \text{ V}$		Full range		600	900	μΛ
		V <sub>CC</sub> = 30 V		i un range			1000	
THD	Total harmonic distortion	$V_{CC} = 30 \text{ V}, V_{O} = 2 \text{ V}_{pp}$ $R_{L} = 2 \text{ k}\Omega, f = 1 \text{ kHz}, C$	$A_{V} = 20 \text{ dB},$ $A_{L} = 100 \text{ pF}$	25°C		0.015		%
e <sub>N</sub>	Equivalent input noise voltage	$V_{CC} = 30 \text{ V, f} = 1 \text{ kHz,}$	$R_S = 100 \Omega$	25°C		50		nV/√ <del>Hz</del>

<sup>(1)</sup> The direction of the input current is out of the device. This current essentially is constant, independent of the state of the output, so no loading change exists on the input lines.

<sup>(2)</sup> The input common-mode voltage of either input signal should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V<sub>CC+</sub> – 1.5 V, but either or both inputs can go to 32 V without damage.

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
TS321QDBVRQ1	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9CNS
TS321QDBVRQ1.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9CNS

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

- (2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) RoHS values: Yes, No. RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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#### OTHER QUALIFIED VERSIONS OF TS321-Q1:

Catalog: TS321



# **PACKAGE OPTION ADDENDUM**

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NOTE: Qualified Version Definitions:

 $_{\bullet}$  Catalog - TI's standard catalog product

# PACKAGE MATERIALS INFORMATION

www.ti.com 3-Aug-2017

# TAPE AND REEL INFORMATION





A0	
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

# QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



## \*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS321QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

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#### \*All dimensions are nominal

I	Device	Device Package Type		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
I	TS321QDBVRQ1	SOT-23	DBV	5	3000	202.0	201.0	28.0	



SMALL OUTLINE TRANSISTOR



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
  3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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