RS-232 TRANSCEIVER WITH SPLIT SUPPLY PIN FOR LOGIC SIDE

Check for Samples: TRS3386E

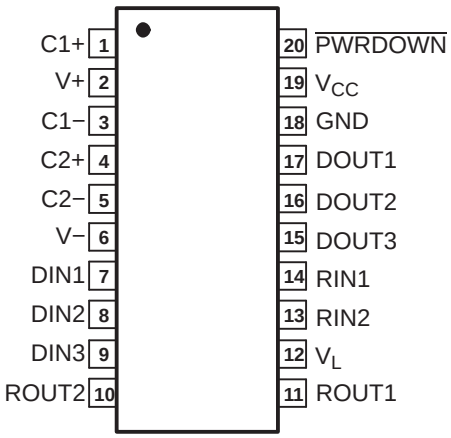
FEATURES

- **V_L Pin for Compatibility With Mixed-Voltage Systems Down to 2.5 V on Logic Side**
- **Enhanced ESD Protection on RIN Inputs and DOUT Outputs**
  - **±15-kV Human-Body Model**
  - **±15-kV IEC 61000-4-2, Air-Gap Discharge**
  - **±8-kV IEC 61000-4-2, Contact Discharge**
- **Low 300-µA Supply Current**
- **Specified 250-kbps Data Rate**
- **1-µA Low-Power Shutdown**
- **Meets EIA/TIA-232 Specifications Down to 3 V**
- **Designed to be Interchangeable With Industry Standard '3386 Devices**

APPLICATIONS

- **Hand-Held Equipment**
- **PDAs**
- **Cell Phones**
- **Battery-Powered Equipment**
- **Data Cables**

PW OR DW PACKAGE
TOP VIEW



DESCRIPTION/ORDERING INFORMATION

The TRS3386E is a three-driver and two-receiver RS-232 interface device, with split supply pins for mixed-signal operations. All RS-232 inputs and outputs are protected to ±15 kV using the IEC 61000-4-2 Air-Gap Discharge method, ±8 kV using the IEC 61000-4-2 Contact Discharge method, and ±15 kV using the Human-Body Model.

The charge pump requires only four small 0.1-µF capacitors for operation from a 3.3-V supply. The TRS3386E is capable of running at data rates up to 250 kbps, while maintaining RS-232-compliant output levels.

The TRS3386E has a unique V_L pin that allows operation in mixed-logic voltage systems. Both driver in (DIN) and receiver out (ROUT) logic levels are pin programmable through the V_L pin. The TRS3386E is available in a space-saving thin shrink small-outline package (TSSOP).

ORDERING INFORMATION

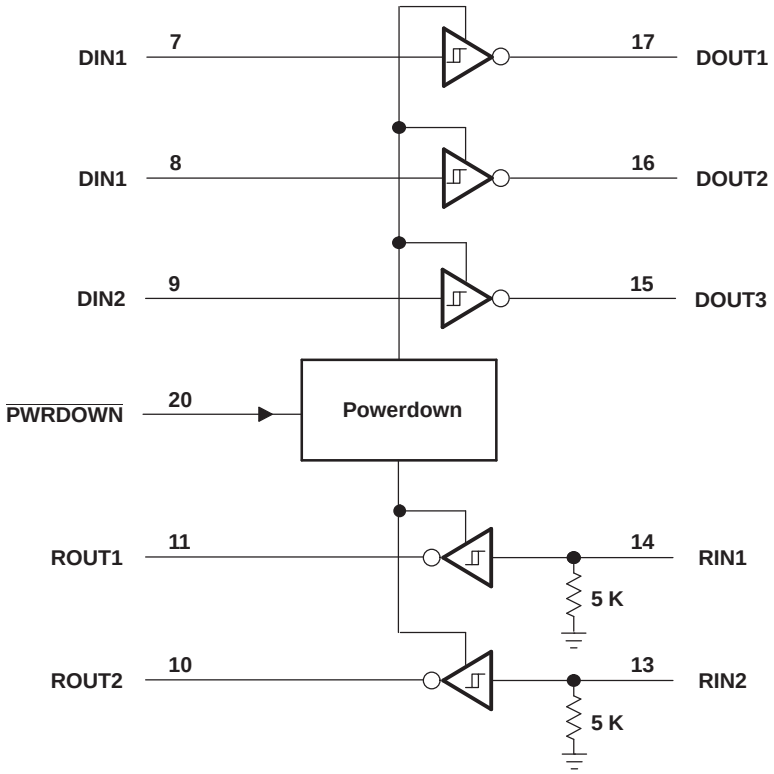
T_A	PACKAGE(1) (2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	TSSOP – PW	TRS3386ECPWR	RV86EC
	SOIC – DW	TRS3386ECDWR	TRS3386EC
–40°C to 85°C	TSSOP – PW	TRS3386EIPWR	RV86EI
	SOIC – DW	TRS3386EIDWR	TRS3386EI

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Table 1. TRUTH TABLE (SHUTDOWN FUNCTION)

$\overline{\text{PWRDWN}}$	DRIVER OUTPUTS	RECEIVER OUTPUTS	CHARGE PUMP
L	High-Z	High-Z	Inactive
H	Active	Active	Active

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
C1+	1	Positive terminal of the voltage-doubler charge-pump capacitor
V+	2	5.5-V supply generated by the charge pump
C1–	3	Negative terminal of the voltage-doubler charge-pump capacitor
C2+	4	Positive terminal of the inverting charge-pump capacitor
C2–	5	Negative terminal of the inverting charge-pump capacitor
V–	6	–5.5-V supply generated by the charge pump
DIN1 DIN2 DIN3	7 8 9	Driver inputs
ROUT2 ROUT1	10 11	Receiver outputs. Swing between 0 and V_L.
V_L	12	Logic-level supply. All CMOS inputs and outputs are referenced to this supply.
RIN2 RIN1	13 14	RS-232 receiver inputs
DOUT3 DOUT2 DOUT1	15 16 17	RS-232 driver outputs
GND	18	Ground
V_{CC}	19	3-V to 5.5-V supply voltage
$\overline{\text{PWRDWN}}$	20	Powerdown input L = Powerdown H = Normal operation

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	V_{CC} to GND		–0.3	6	V
	V_L to GND		–0.3	V_{CC} + 0.3	V
	V+ to GND		–0.3	7	V
	V– to GND		0.3	–7	V
	V+ + |V–|(2)			13	V
V_I	Input voltage	DIN, $\overline{\text{PWRDWN}}$ to GND	–0.3	6	V
		RIN to GND		±25	
V_O	Output voltage	DOUT to GND		±13.2	V
		ROUT	–0.3	V_L + 0.3	
	Short-circuit duration DOUT to GND			Continuous	
	Continuous power dissipation	T_A = 70°C, 20-pin TSSOP (derate 7 mW/°C above 70°C)		559	mW
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C
	Lead temperature (soldering, 10 s)			300	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V+ and V– can have maximum magnitudes of 7 V, but their absolute difference cannot exceed 13 V.

Recommended Operating Conditions

				MIN	MAX	UNIT
V_{CC}	Supply voltage			3	5.5	V
V_L	Supply voltage			2.25	V_{CC}	V
	Input logic threshold low	DIN, $\overline{PWRDWN}$	V_L = 3 V or 5.5 V		0.8	V
			V_L = 2.3 V		0.6	
	Input logic threshold high	DIN, $\overline{PWRDWN}$	V_L = 5.5 V	2.4		V
			V_L = 3 V	2.0		
			V_L = 2.7 V	1.4		
	Operating temperature		TRS3386ECPWR	0	70	°C
			TRS3386EIPWR	–40	85	
	Receiver input voltage			–25	25	V

Electrical Characteristics

over operating free-air temperature range, V_{CC} = V_L = 3 V to 5.5 V, C1–C4 = 0.1 µF (tested at 3.3 V ± 10%), C1 = 0.047 µF, C2–C4 = 0.33 µF (tested at 5 V ± 10%) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
DC Characteristics (V_{CC} = 3.3 V or 5 V, T_A = 25°C)					
Powerdown supply current	$\overline{PWRDWN}$ = GND, All inputs at V_{CC} or GND		1	10	µA
Supply current	$\overline{PWRDWN}$ = V_{CC}, No load		0.3	1	mA

(1) Typical values are at V_{CC} = V_L = 3.3 V, T_A = 25°C.

ESD Protection

PARAMETER	TEST CONDITIONS	TYP	UNIT
RIN, DOUT	Human-Body Model	±15	kV
	IEC 61000-4-2 Air-Gap Discharge	±15	
	IEC 61000-4-2 Contact Discharge	±8	

RECEIVER SECTION

Electrical Characteristics

over operating free-air temperature range, V_{CC} = V_L = 3 V to 5.5 V, C1–C4 = 0.1 µF (tested at 3.3 V ± 10%), C1 = 0.047 µF, C2–C4 = 0.33 µF (tested at 5 V ± 10%), T_A = T_{MIN} to T_{MAX} (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{off}	Output leakage current	ROUT, receivers disabled			±0.05	±10	µA
V_{OL}	Output voltage low	I_{OUT} = 1.6 mA				0.4	V
V_{OH}	Output voltage high	I_{OUT} = –1 mA		V_L – 0.6	V_L – 0.1		V
$V_{IT–}$	Input threshold low	T_A = 25°C	V_L = 5 V	0.8	1.2		V
			V_L = 3.3 V	0.6	1.5		
V_{IT+}	Input threshold high	T_A = 25°C	V_L = 5 V		1.8	2.4	V
			V_L = 3.3 V		1.5	2.4	
V_{hys}	Input hysteresis				0.5		V
	Input resistance	T_A = 25°C		3	5	7	kΩ

(1) Typical values are at V_{CC} = V_L = 3.3 V, T_A = 25°C

Switching Characteristics

over operating free-air temperature range, V_{CC} = V_L = 3 V to 5.5 V, C1–C4 = 0.1 µF (tested at 3.3 V ± 10%), C1 = 0.047 µF, C2–C4 = 0.33 µF (tested at 5 V ± 10%), T_A = T_{MIN} to T_{MAX} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP(1)	UNIT
t_{PHL}	Receiver propagation delay	Receiver input to receiver output, C_L = 150 pF	0.15	µs
t_{PLH}			0.15	
t_{PHL} – t_{PLH}	Receiver skew		50	ns
t_{en}	Receiver output enable time	From $\overline{PWRDWN}$	200	ns
t_{dis}	Receiver output disable time	From $\overline{PWRDWN}$	200	ns

(1) Typical values are at V_{CC} = V_L = 3.3 V, T_A = 25°C.

DRIVER SECTION

Electrical Characteristics

over operating free-air temperature range, V_{CC} = V_L = 3 V to 5.5 V, C1–C4 = 0.1 µF (tested at 3.3 V ± 10%), C1 = 0.047 µF, C2–C4 = 0.33 µF (tested at 5 V ± 10%), T_A = T_{MIN} to T_{MAX} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{OH}	Output voltage swing	All driver outputs loaded with 3 kΩ to ground	±5	±5.4		V
r_O	Output resistance	V_{CC} = V+ = V– = 0, Driver output = ±2 V	300	10M		Ω
I_{OS}	Output short-circuit current	V_{T_OUT} = 0			±60	mA
I_{OZ}	Output leakage current	V_{T_OUT} = ±12 V, Driver disabled, V_{CC} = 0 or 3 V to 5.5 V			±25	µA
	Driver input hysteresis				0.5	V
	Input leakage current	DIN, $\overline{PWRDWN}$		±0.01	±1	µA

(1) Typical values are at V_{CC} = V_L = 3.3 V, T_A = 25°C

Timing Requirements

over operating free-air temperature range, V_{CC} = V_L = 3 V to 5.5 V, C1–C4 = 0.1 µF (tested at 3.3 V ± 10%), C1 = 0.047 µF, C2–C4 = 0.33 µF (tested at 5 V ± 10%), T_A = T_{MIN} to T_{MAX} (unless otherwise noted)

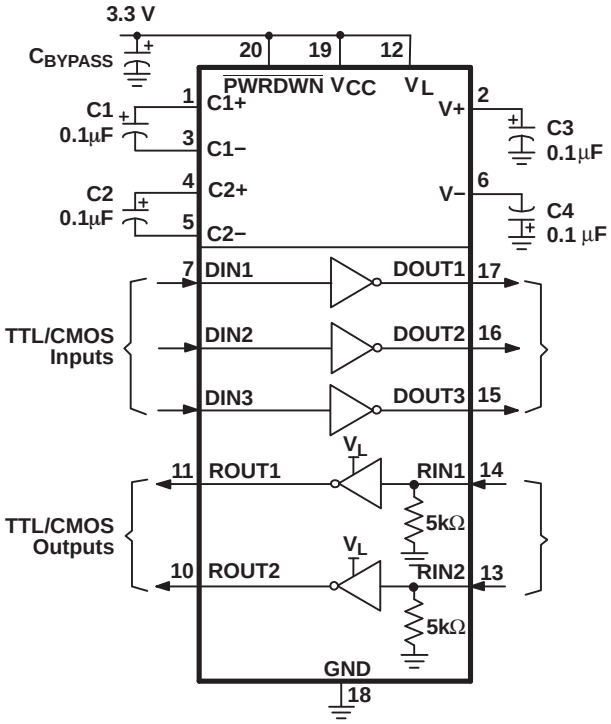
PARAMETER				MIN	TYP(1)	MAX	UNIT
	Maximum data rate	R_L = 3 kΩ, C_L = 1000 pF, One driver switching		250			kbps
	Time-to-exit powerdown	$\|V_{T\_OUT}\|$ > 3.7 V			100		µs
$\|t_{PHL} – t_{PLH}\|$	Driver skew(2)				100		ns
	Transition-region slew rate	V_{CC} = 3.3 V, T_A = 25°C, R_L = 3 kΩ to 7 kΩ, Measured from 3 V to –3 V or –3 V to 3 V	C_L = 150 pF to 1000 pF	6		30	V/µs
			C_L = 150 pF to 2500 pF	4		30	

(1) Typical values are at V_{CC} = V_L = 3.3 V, T_A = 25°C.
(2) Driver skew is measured at the driver zero crosspoint.

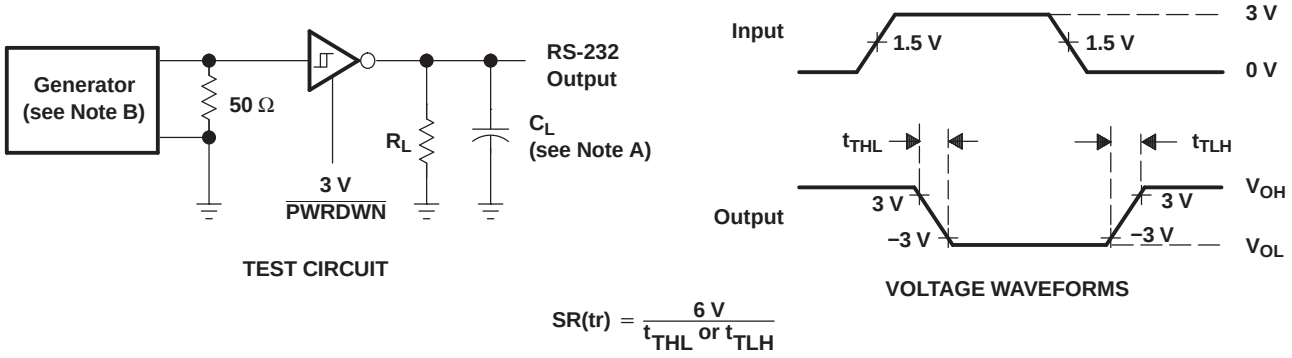
ESD Protection

PARAMETER	TEST CONDITIONS	TYP	UNIT
RIN, DOUT	Human-Body Model	±15	kV
	IEC 61000-4-2 Air-Gap Discharge	±15	
	IEC 61000-4-2 Contact Discharge	±8	

APPLICATION INFORMATION



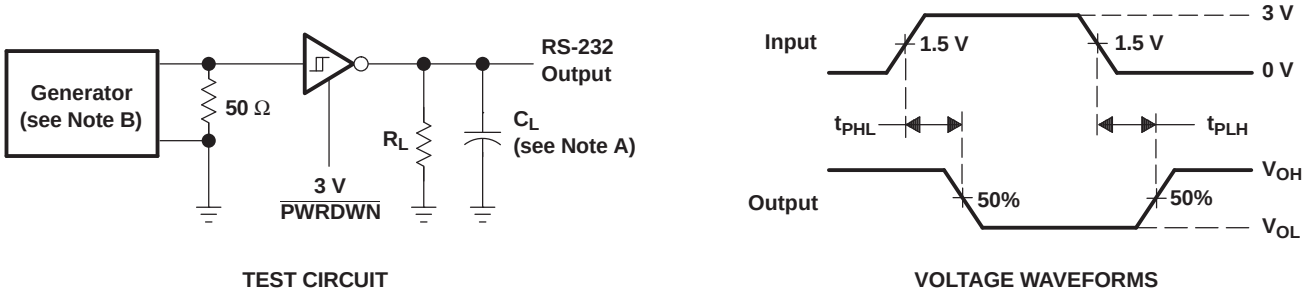
PARAMETER MEASUREMENT INFORMATION



$$SR(tr) = \frac{6\ V}{t_{THL} \text{ or } t_{TLH}}$$

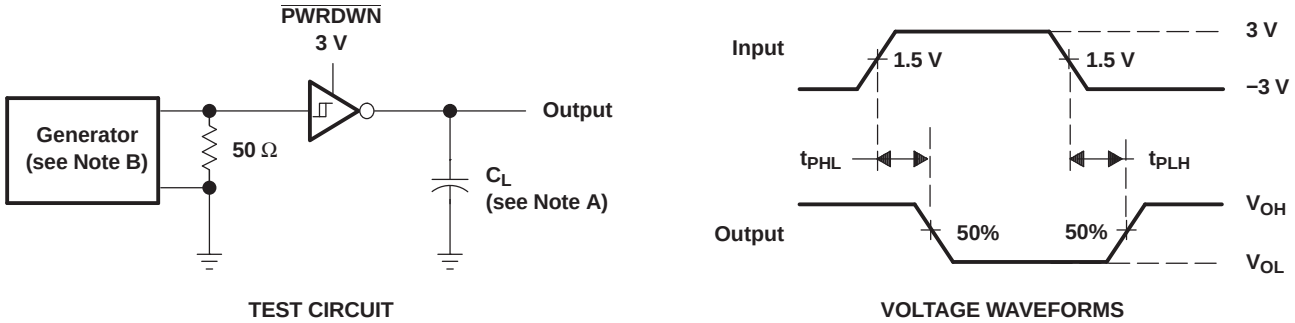
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 1. Driver Slew Rate



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

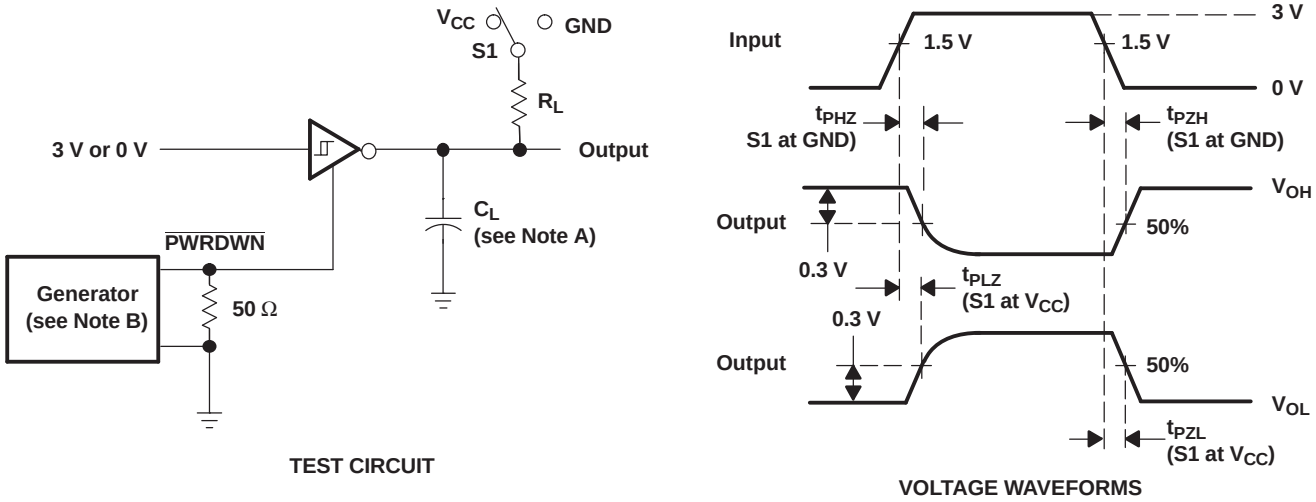
Figure 2. Driver Pulse Skew



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 3. Receiver Propagation Delay Times

PARAMETER MEASUREMENT INFORMATION (Continued)



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 4. Receiver Enable and Disable Times

REVISION HISTORY

Changes from Revision B (April 2009) to Revision C **Page**

- Changed V_L Pin for Compatibility With Mixed-Voltage Systems Down to 2.5 V (originally 1.8 V) on the Logic Side. 1
- Changed V_L Supply MIN value from 1.65 V to 2.25 V. 4
- Deleted V_L = 1.65V parameter from Input logic threshold low. 4
- Deleted V_L = 1.95V parameter from Input logic threshold high. 4

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TRS3386ECDWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3386EC
TRS3386ECDWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3386EC
TRS3386ECPW	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	0 to 70	RV86EC
TRS3386ECPWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	RV86EC
TRS3386ECPWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	RV86EC
TRS3386ECPWRG4	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	RV86EC
TRS3386EIDWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3386EI
TRS3386EIDWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3386EI
TRS3386EIPW	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	-40 to 85	RV86EI
TRS3386EIPWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RV86EI
TRS3386EIPWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RV86EI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

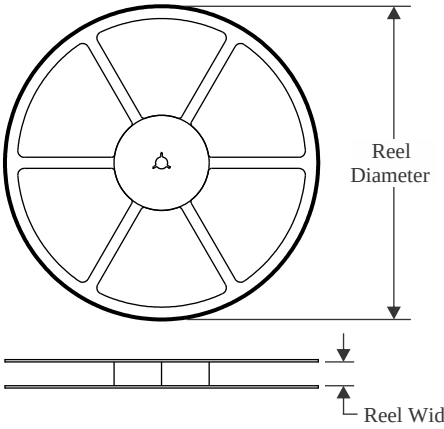
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

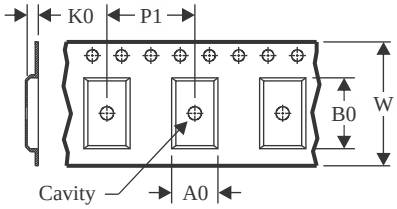
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

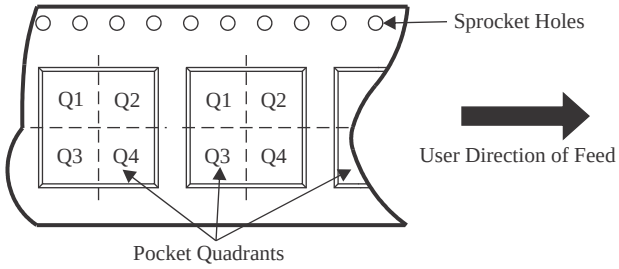


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

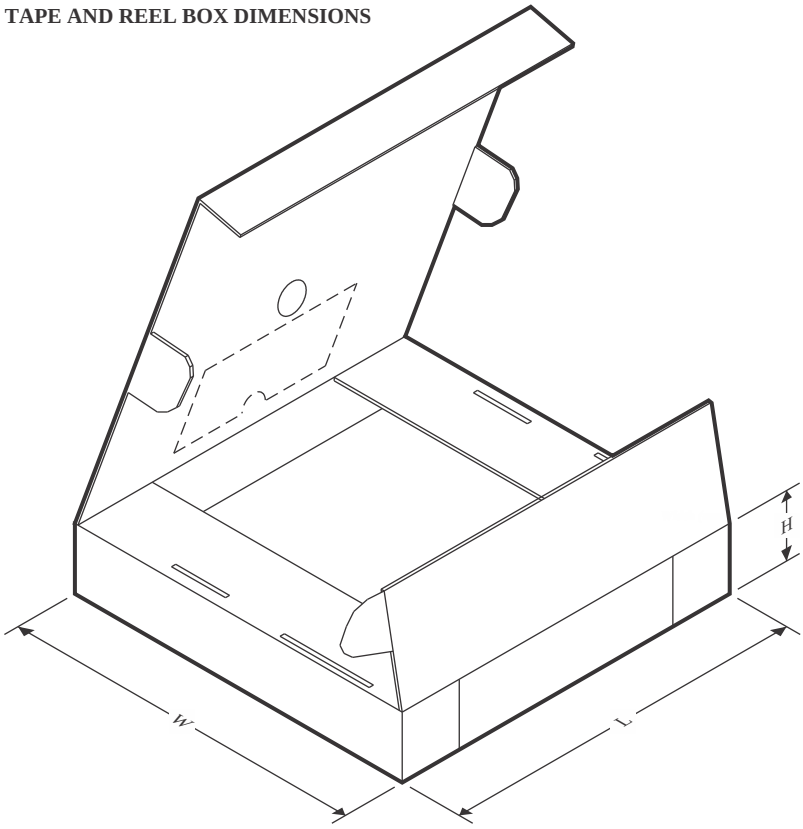
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS3386ECDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TRS3386ECPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
TRS3386EIPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

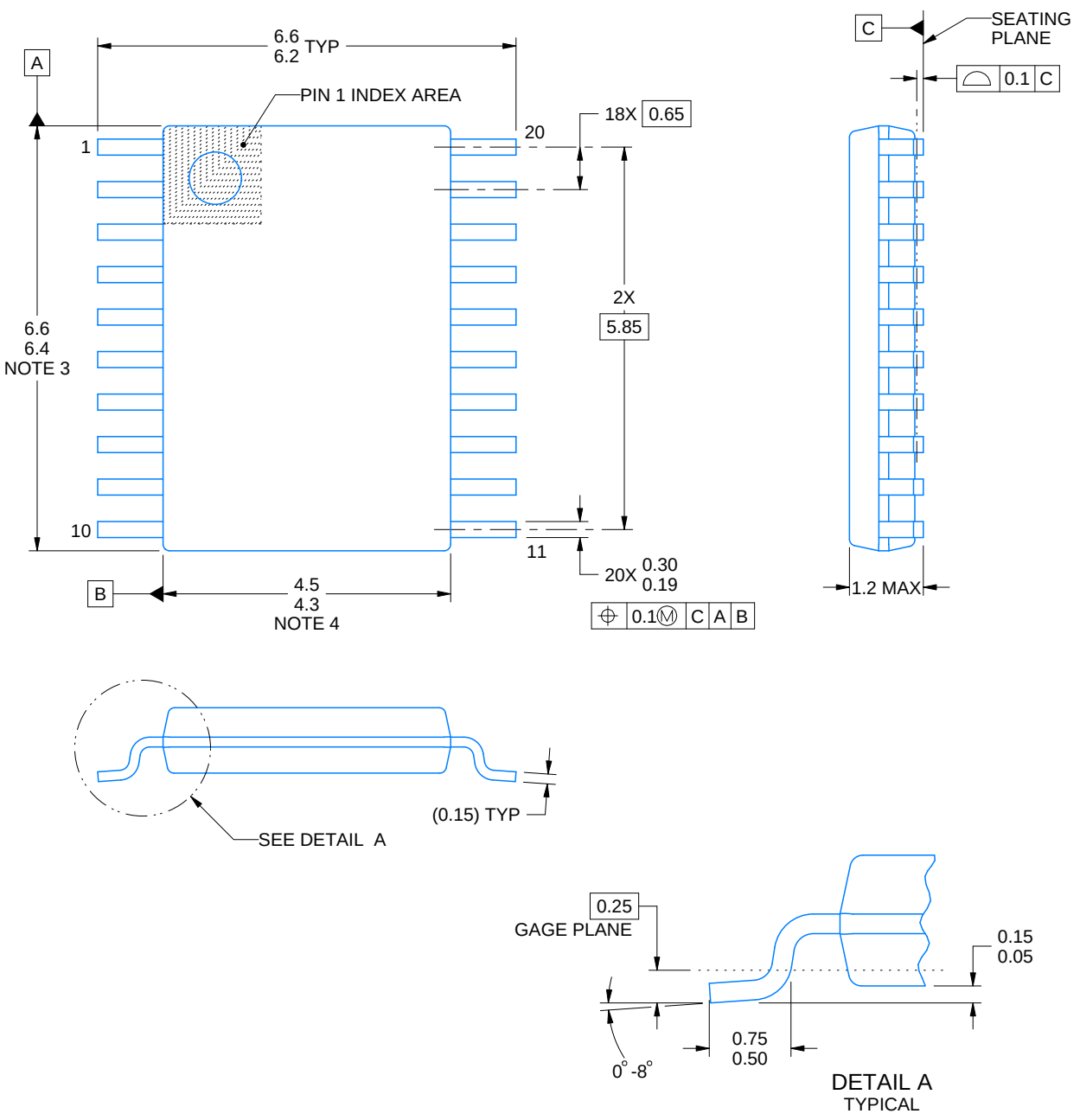
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS3386ECDWR	SOIC	DW	20	2000	356.0	356.0	45.0
TRS3386ECPWR	TSSOP	PW	20	2000	353.0	353.0	32.0
TRS3386EIPWR	TSSOP	PW	20	2000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0020A

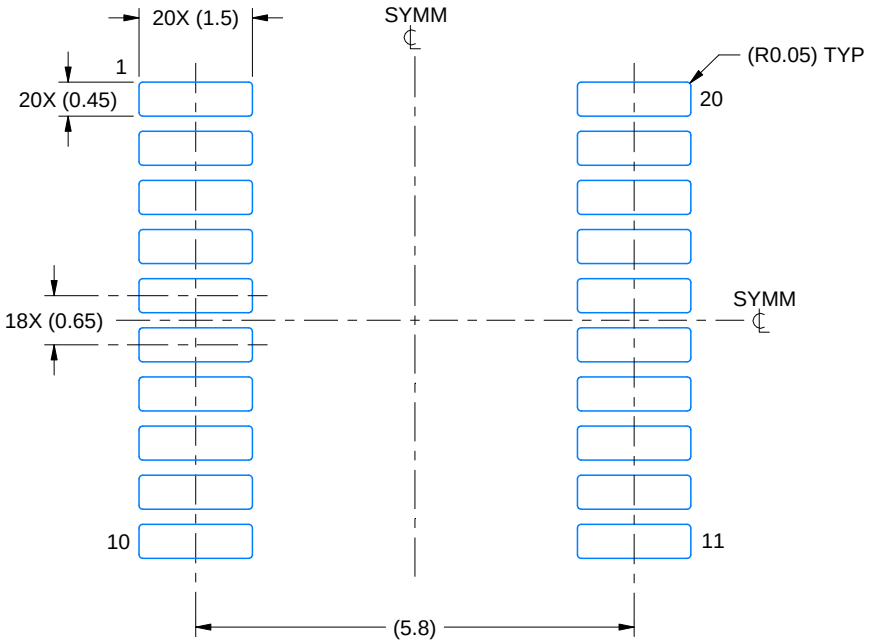
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



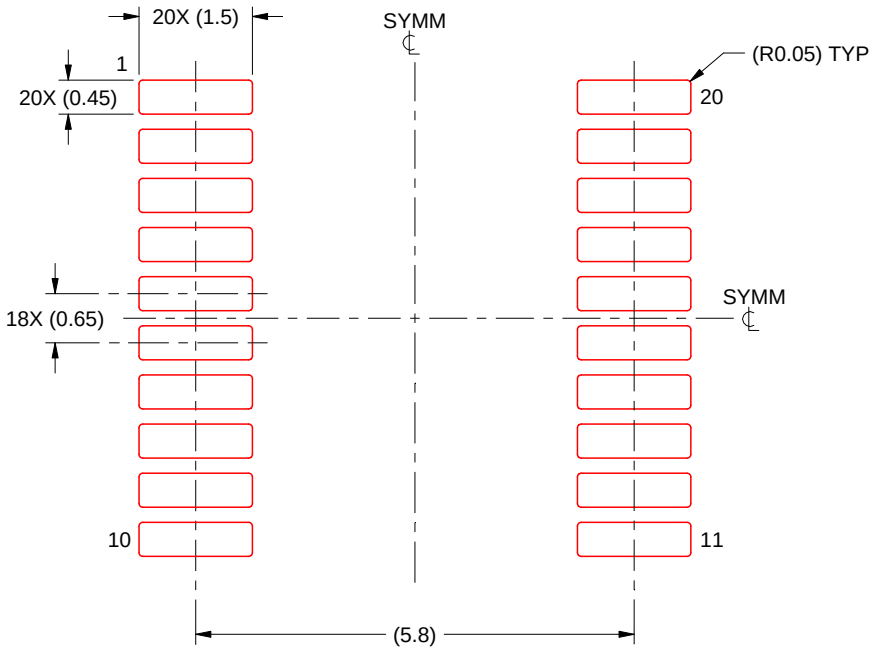
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

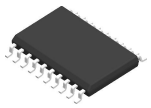


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

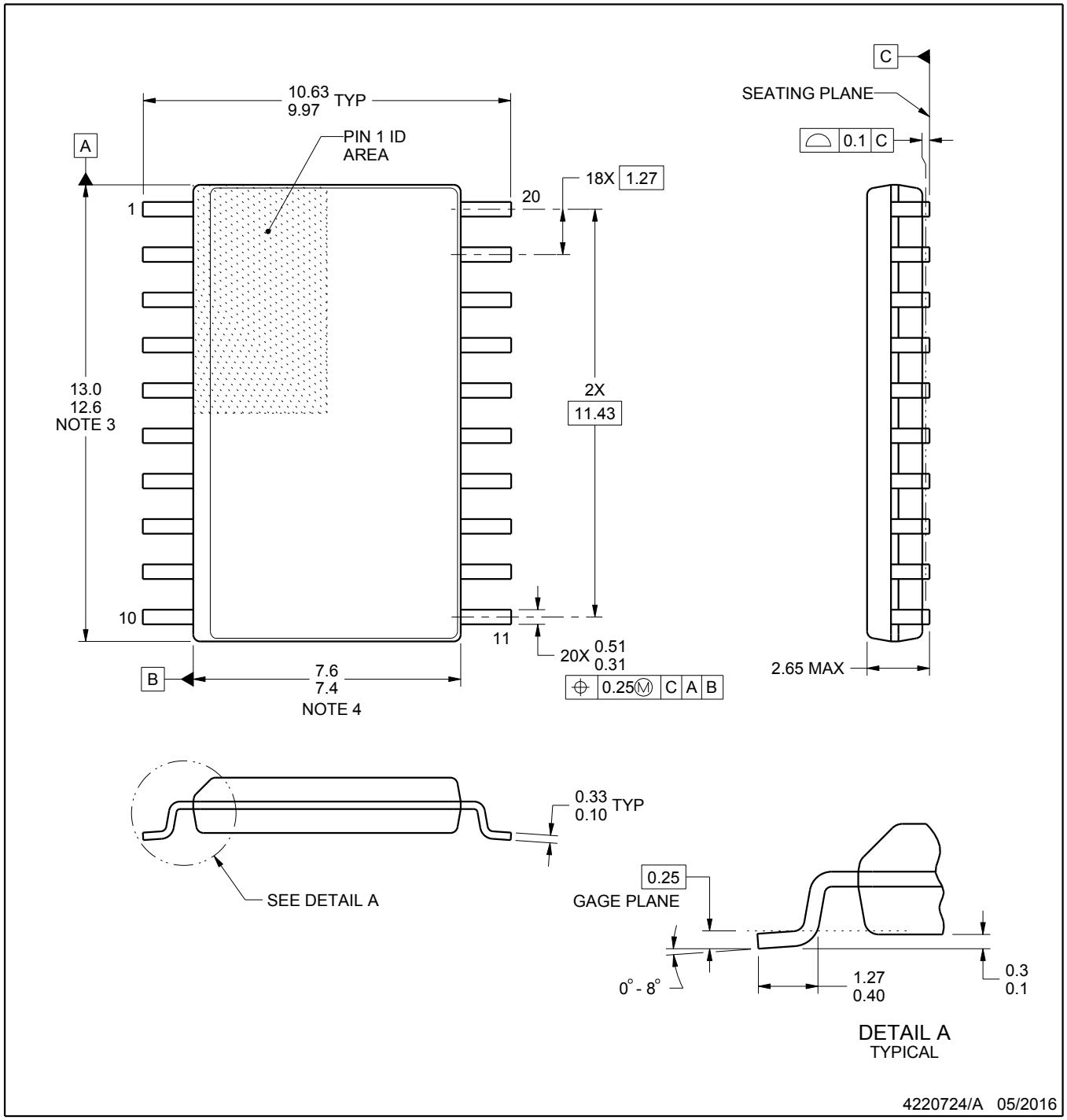


PACKAGE OUTLINE

DW0020A

SOIC - 2.65 mm max height

SOIC



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2. This drawing is subject to change without notice.
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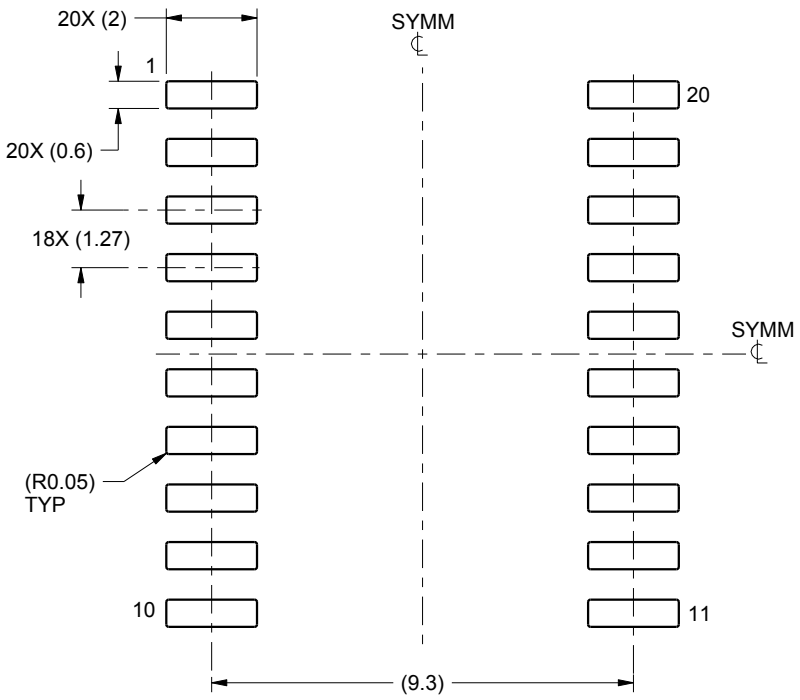
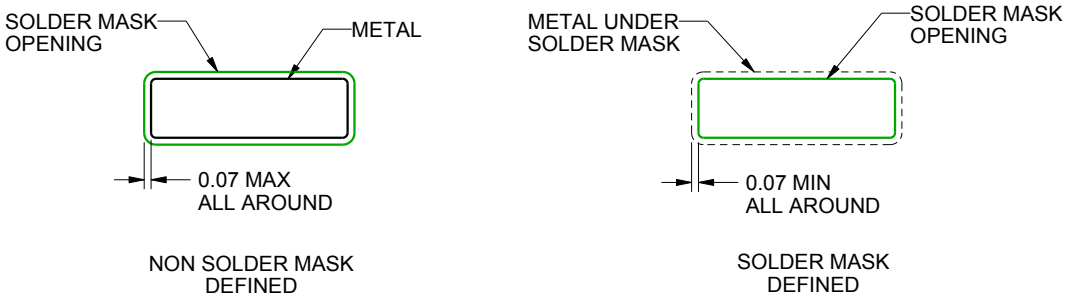
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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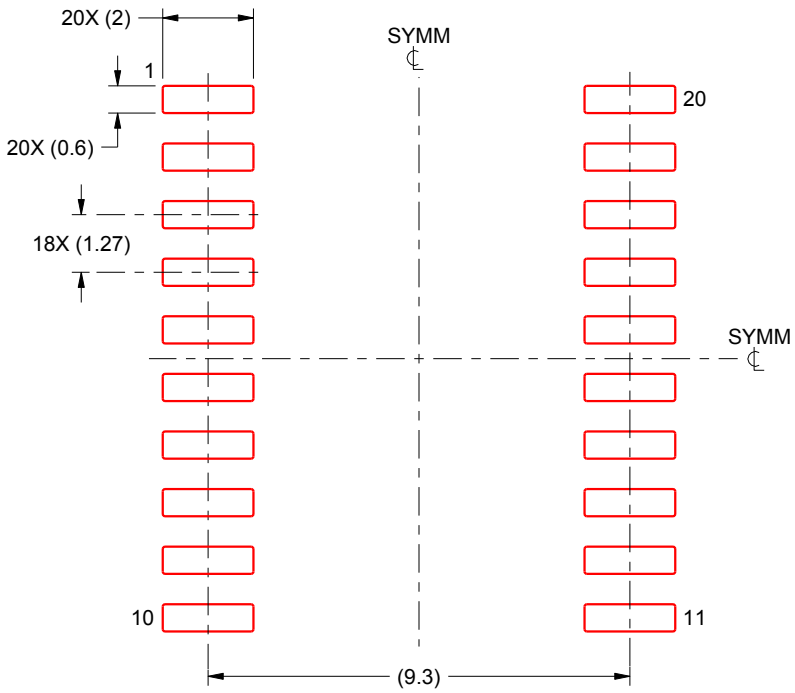
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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