TPSM82850x-Q1 Automotive 2.7V to 6V Input, 1A and 2A Step-Down Power Module With Integrated Inductor

1 Features

- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: –40°C to +125°C T_A
- Optimized for low EMI requirements
  - Pin-selectable pseudo-random spread spectrum (SSC) reduces peak emissions
- T_J = –40°C to +150°C
- Input voltage range: 2.7V to 6V
- Quiescent current: 17μA typical
- Output voltage from 0.6V to 5.5V
- Output voltage accuracy ±1% (PWM operation)
- Forced PWM or PWM/PFM operation
- Adjustable switching frequency: 1.8MHz to 4MHz
- Precise ENABLE input allows:
  - User-defined undervoltage lockout
  - Exact sequencing
- 100% duty cycle mode
- Active output discharge
- Foldback overcurrent protection – optional
- Power-good output with window comparator

2 Applications

- Advanced driver assistance systems (ADAS) camera
- ADAS sensor fusion and surround view ECU
- Hybrid and reconfigurable instrument cluster
- Head unit and telematics control unit
- External audio amplifier

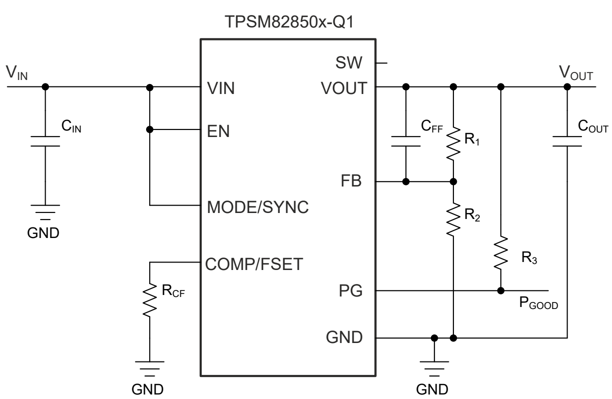
3 Description

TPSM82850x-Q1 is a family of pin-to-pin compatible, 1A, and 2A, automotive high-efficiency and easy to use synchronous step-down DC/DC power modules with integrated inductors. The devices use a fixed-frequency peak current-mode control topology and are suitable for automotive applications with high power density and ease of use requirements. Low resistance switches allow up to 2A continuous output current at high ambient temperatures. The switching frequency can be fixed at 2.25MHz through pin-strapping or selected from a range of 1.8MHz to 4MHz through a set resistor. The module can also be synchronized to an external clock in the range from 1.8MHz to 4MHz. In PFM/PWM mode, the TPSM82850x-Q1 automatically enters power save mode at light loads to maintain high efficiency across the whole load range. The TPSM82850x-Q1 provides a 1% feedback voltage accuracy in PWM mode which helps design a power supply with high output voltage accuracy. The COMP/FSET pin sets the switching frequency, one out of two loop compensation settings and the SSC function for a wide variety of load conditions

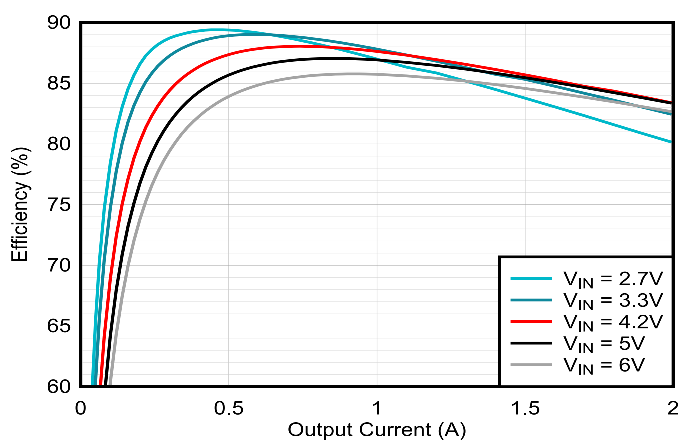
Device Information

PART NUMBER(2)	OUTPUT CURRENT	PACKAGE(1)	BODY SIZE (NOM)
TPSM828500-Q1(3)	0.5A	RDY (QFN-FCMOD, 9)	2.7mm × 3.0mm
TPSM828501-Q1(3)	1A		
TPSM828502-Q1	2A		

(1) For more information, see Section 12.
(2) See the *Device Comparison Table*.
(3) Preview information (not Production Data).



Simplified Schematic



Efficiency vs Output Current; V_{OUT} = 1.1V

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4 Device Comparison Table

DEVICE NUMBER	OUTPUT CURRENT	OUTPUT VOLTAGE	TYPICAL INPUT CAPACITOR	TYPICAL OUTPUT CAPACITOR
TPSM828500WRDYRQ1 (1)	0.5A	Adjustable	2 × 4.7µF	2 × 10µF
TPSM828501WRDYRQ1 (1)	1A			
TPSM828502WRDYRQ1	2A			

(1) Preview information (not Production Data).

5 Pin Configuration and Functions

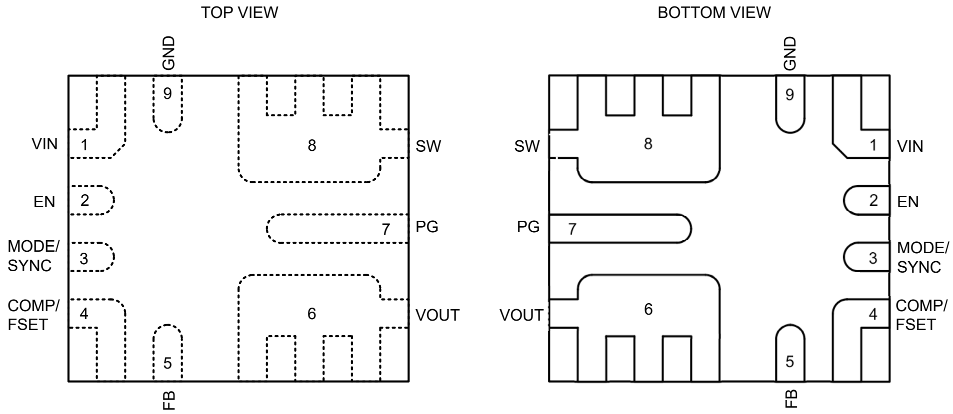


Figure 5-1. 9-Pin RDY QFN-FCMOD Package

Table 5-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
VIN	1	PWR	Power supply input. Connect the input capacitor as close as possible between the VIN and GND pins.
EN	2	I	This pin is the enable pin of the device. Connect to logic low to disable the device. Pull high to enable the device. Do not leave this pin unconnected.
MODE/SYNC	3	I	The device runs in PFM/PWM mode when this pin is pulled low. When the pin is pulled high, the device runs in forced PWM mode. Do not leave this pin unconnected. The MODE/SYNC pin can also be used to synchronize the device to an external frequency. See *Synchronizing to an External Clock*.
COMP/FSET	4	I	Device compensation and frequency set input. A resistor from this pin to GND defines the compensation of the control loop as well as the switching frequency if not externally synchronized.
FB	5	I	Voltage feedback input. Connect the output voltage resistor divider to this pin.
VOUT	6	PWR	Output voltage pin. This pin is internally connected to the integrated inductor.
PG	7	O	Open-drain power-good output with window comparator. This pin is pulled to GND while VOUT is outside the power-good threshold. This pin can be left open or tied to GND if not used. A pullup resistor can be connected to any voltage not larger than VIN.
SW	8	O	This pin is the switch pin of the converter. This pin is connected to the internal power MOSFET and the inductor. Avoid connecting this pin to larger traces as this can increase EMI. This pin can stay unconnected or be soldered to a small pad for thermal improvement.
GND	9	PWR	Ground pin

(1) I = input, O = output, PWR = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin voltage(2)	VIN	–0.3	6.5	V
	SW (DC)	–0.3	V_{IN} + 0.3	V
	SW (AC, less than 10ns)(3)	–3	10	V
	COMP/FSET, PG	–0.3	V_{IN} + 0.3	V
	EN, MODE/SYNC, FB	–0.3	6.5	V
Storage temperature	T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the network ground terminal
(3) While switching

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.7		6	V
V_{OUT}	Output voltage range	0.6		5.5	V
C_{OUT}	Effective output capacitance(1)	8	10	200	µF
C_{IN}	Effective input capacitance(1)	5	10		µF
I_{SINK_PG}	Sink current at PG pin	0		2	mA
T_J	Junction temperature	–40		150	°C

(1) The values given for all the capacitors in the table are effective capacitance, which includes the DC bias effect. Due to the DC bias effect of ceramic capacitors, the effective capacitance is lower than the nominal value when a voltage is applied. Please check the manufacturer´s DC bias curves for the effective capacitance vs DC voltage applied.

6.4 Thermal Information

THERMAL METRIC[1]		TPSM82850x-Q1 RDY (JEDEC)[2] 9 PINS	TPSM82850x-Q1 RDY (EVM) 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.1	54.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	82.7	n/a	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.7	n/a	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14.6	12.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	27.7	28.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) JEDEC standard PCB with 4 layers, no thermal vias

6.5 Electrical Characteristics

Over operating junction remperature range (T_J = –40°C to +150°C) and V_{IN} = 2.7V to 6V. Typical values at V_{IN} = 5V and T_J = 25°C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current	EN = V_{IN}, no load, device not switching, MODE = GND, V_{OUT} = 0.6V		17	36	µA
I_{SD}	Shutdown current	EN = GND, Nominal value at T_J = 25°C, Max value at T_J = 150°C		1.5	48	µA
V_{UVLO}	Undervoltage lock out threshold	V_{IN} rising	2.45	2.6	2.7	V
		V_{IN} falling	2.1	2.5	2.6	V
T_{JSD}	Thermal shutdown threshold	T_J rising		170		°C
	Thermal shutdown hysteresis	T_J falling		15		°C
CONTROL and INTERFACE						
$V_{EN,IH}$	Input threshold voltage at EN, rising edge		1.05	1.1	1.15	V
$V_{EN,IL}$	Input threshold voltage at EN, falling edge		0.96	1.0	1.05	V
V_{IH}	High-level input-threshold voltage at MODE/SYNC		1.1			V
$I_{EN,LKG}$	Input leakage current into EN	V_{IH} = V_{IN} or V_{IL} = GND			125	nA
V_{IL}	Low-level input-threshold voltage at MODE/SYNC				0.3	V
I_{LKG}	Input leakage current into MODE/SYNC				100	nA
t_{Delay}	Enable delay time	Time from EN high to device starts switching; V_{IN} applied already	135	200	520	µs
t_{Delay}	Enable delay time	Time from EN high to device starts switching; V_{IN} applied already, V_{IN} ≥ 3.3V			480	µs
t_{Ramp}	Output voltage ramp time	Time from device starts switching to power good; device not in current limit	0.8	1.3	1.8	ms
f_{SYNC}	Frequency range on MODE/SYNC pin for synchronization		1.8		4	MHz
	Duty cycle of synchronization signal at MODE/SYNC		20		80	%
	Time to lock to external frequency			50		µs
	resistance from COMP/FSET to GND for logic low	internal frequency setting with f = 2.25MHz	0		2.5	kΩ
	Voltage on COMP/FSET for logic high	internal frequency setting with f = 2.25MHz		V_{IN}		V

6.5 Electrical Characteristics (continued)

Over operating junction rremperature range (T_J = –40°C to +150°C) and V_{IN} = 2.7V to 6V. Typical values at V_{IN} = 5V and T_J = 25°C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TH_PG}	UVP power-good threshold voltage; DC level	rising (%V_{FB})	92	95	98	%
V_{TH_PG}	UVP power-good threshold voltage; DC level	falling (%V_{FB})	87	90	93	%
V_{TH_PG}	OVP power-good threshold voltage; DC level	rising (%V_{FB})	107	110	113	%
	OVP power-good threshold voltage; DC level	falling (%V_{FB})	104	107	111	%
$V_{PG,OL}$	Low-level output voltage at PG	I_{SINK_PG} = 2mA		0.07	0.3	V
$I_{PG,LKG}$	Input leakage current into PG	V_{PG} = 5V			100	nA
t_{PG}	PG deglitch time	for a high level to low level transition on the power-good output		40		µs
OUTPUT						
V_{FB}	Feedback voltage, adjustable version			0.6		V
$I_{FB,LKG}$	Input leakage current into FB, adjustable version	V_{FB} = 0.6V		1	70	nA
$I_{FB,LKG}$	Input current into FB, fixed voltage versions			1		µA
V_{FB}	Feedback voltage accuracy	PWM, $V_{IN} \geq V_{OUT}$ + 1V	–1		1	%
V_{FB}	Feedback voltage accuracy	PFM, $V_{IN} \geq V_{OUT}$ + 1V, $V_{OUT} \geq$ 1.0V, $C_{out,eff} \geq$ 10µF, L = 0.47µH	–1		2	%
V_{FB}	Feedback voltage accuracy	PFM, $V_{IN} \geq V_{OUT}$ + 1V, V_{OUT} < 1.0V, $C_{out,eff} \geq$ 15µF, L = 0.47µH	–1		3	%
	Load regulation	PWM		0.05		%/A
	Line regulation	PWM, I_{OUT} = 1A, $V_{IN} \geq V_{OUT}$ + 1V		0.02		%/V
R_{DIS}	Output discharge resistance				100	Ω
f_{SW}	PWM Switching frequency range	MODE = high, see the FSET pin functionality about setting the switching frequency	1.8	2.25	4	MHz
f_{SW}	PWM Switching frequency range	MODE = low, see the FSET pin functionality about setting the switching frequency	1.8		3.5	MHz
f_{SW}	PWM Switching frequency	with COMP/FSET tied to GND or V_{IN}	2.025	2.25	2.475	MHz
f_{SW}	PWM Switching frequency tolerance	using a resistor from COMP/FSET to GND	–12		12	%
$t_{on,min}$	Minimum on-time of high-side FET	V_{IN} = 3.3V, T_J = –40°C to 125°C		35	50	ns
$t_{on,min}$	Minimum on-time of low-side FET			10		ns
R_{DP}	Dropout resistance ($R_{DS(on)}$ high-side FET + DCR of inductor)	$V_{IN} \geq$ 5V		95	150	mΩ
	High-side MOSFET leakage current	T_J = 85°C		2.5		µA
	High-side MOSFET leakage current			0.01	44	µA
	Low-side MOSFET leakage current	T_J = 85°C		3.7		µA
	Low-side MOSFET leakage current			0.01	70	µA
	SW leakage	V(SW) = 0.6V, current into SW pin		–0.01	11	µA
I_{LIMH}	High-side FET switch current limit	DC value, for TPSM828502; V_{IN} = 3V to 6V	2.85	3.4	3.9	A
I_{LIMH}	High-side FET switch current limit	DC value, for TPSM828501; V_{IN} = 3V to 6V	2.1	2.6	3.0	A

6.5 Electrical Characteristics (continued)

Over operating junction remperature range (T_J = –40°C to +150°C) and V_{IN} = 2.7V to 6V. Typical values at V_{IN} = 5V and T_J = 25°C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LIMNEG}	Low-side FET negative current limit	DC value		–1.8		A

6.6 Typical Characteristics

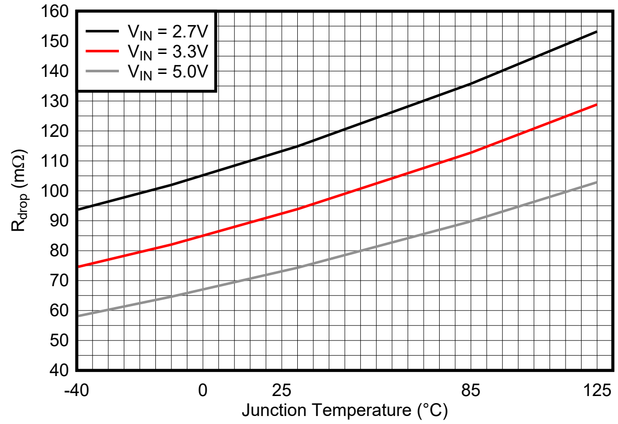


Figure 6-1. Dropout Resistance

7 Parameter Measurement Information

7.1 Schematic

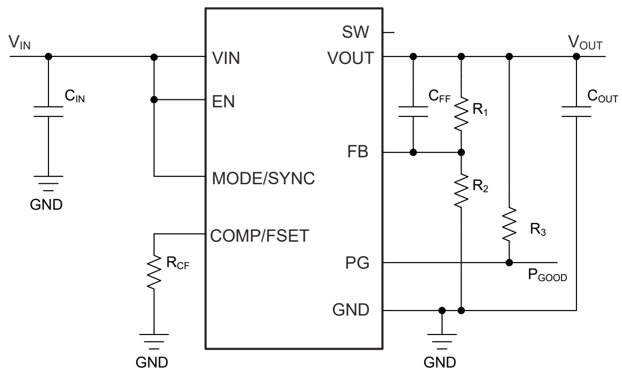


Figure 7-1. Measurement Setup for TPSM82850x-Q1

Table 7-1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER (1)
IC	TPSM828510 / TPSM828511 / TPSM828512	Texas Instruments
C_{IN}	2 × 10µF / 6.3V / GRM188D70J106MA73	Murata
C_{OUT}	2 × 10µF / 6.3V / GRM188D70J106MA73	Murata
C_{FF}	10pF	Any
R_1	Depending on VOUT	Any
R_2	Depending on VOUT	Any
R_3	100 kΩ	Any

(1) See the *Third-party Products Disclaimer*.

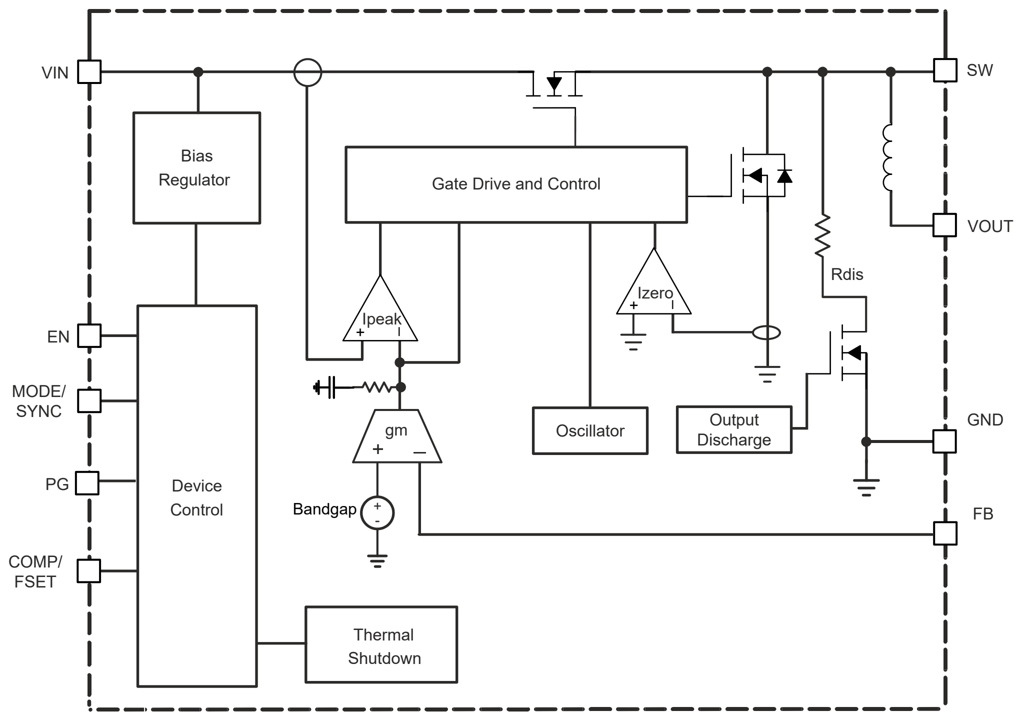
8 Detailed Description

8.1 Overview

The TPSM82850x-Q1 synchronous, switch mode, DC/DC converter power modules are based on a fixed-frequency peak current-mode control topology. The control loop is internally compensated. The compensation select pin COMP/FSET allows optimization of the control loop for a wide range of output capacitance. The regulation network achieves fast and stable operation with small external components and low-ESR ceramic output capacitors.

The devices support fixed-frequency forced PWM operation with the MODE/SYNC pin tied to a logic high level. When the MODE/SYNC pin is set to a logic low level, the device operates in power save mode (PFM) at low-output currents and automatically transitions to fixed-frequency PWM mode at higher output currents. In PFM mode, the switching frequency decreases linearly based on the load to sustain high efficiency down to very low output currents. The device can be synchronized to an external clock signal in a range from 1.8MHz to 4MHz applied to the MODE/SYNC pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Precise Enable (EN)

The voltage applied at the enable pin of the TPSM82850x-Q1 is compared to a fixed threshold of 1.1V for a rising voltage. This comparison allows the user to drive the pin by a slowly changing voltage and enables the use of an external RC network to achieve a power-up delay.

The precise enable input provides a user-programmable undervoltage lockout by adding a resistor divider to the input of the Enable pin.

The enable input threshold for a falling edge is typically 100mV lower than the rising edge threshold. The TPSM82850x-Q1 starts operation when the rising threshold is exceeded. For proper operation, terminate and do not leave the enable (EN) pin floating. Pulling the enable pin low forces the device into shutdown, with a shutdown current of typically 1µA. In this mode, the internal high-side and low-side MOSFETs are turned off and the entire internal control circuitry is switched off. See also *Achieving a Clean Start-up by Using a DC/DC Converter with a Precise Enable-pin Threshold* analog design journal.

8.3.2 COMP/FSET

This pin allows to set three different parameters:

- Internal compensation settings for the control loop (two settings available)
- The switching frequency in PWM mode from 1.8MHz to 4MHz
- Enable/disable spread spectrum clocking (SSC)

A resistor from COMP/FSET to GND changes the compensation as well as the switching frequency. The change in compensation allows the user to adopt the device to different values of output capacitance. The resistor must be placed close to the pin to keep the parasitic capacitance on the pin to a minimum. The compensation setting is sampled at start-up of the converter, so a change in the resistor during operation only has an effect on the switching frequency but not on the compensation.

To save external components, the pin can also be directly tied to VIN or GND to set a pre-defined setting. Do not leave the pin floating.

The switching frequency must be selected based on the input voltage and the output voltage to meet the specifications for the minimum on-time and minimum off-time.

Example: V_{IN} = 5V, V_{OUT} = 0.6V --> duty cycle = 0.6V / 5V = 0.12

- --> $t_{on,min}$ = 1 / fs × 0.12
- --> $f_{sw,max}$ = 1 / $t_{on,min}$ × 0.12 = 1 / 0.05μs × 0.12 = 2.4MHz

The compensation range must be chosen based on the minimum capacitance used. The capacitance can be increased from the minimum value as given in Table 8-1, up to the maximum as per Section 6.3 in both compensation ranges. If the capacitance of an output changes during operation, for example, when load switches are used to connect or disconnect parts of the circuitry, the compensation must be chosen for the minimum capacitance on the output. With large output capacitance, the compensation must be done based on that large capacitance to get the best load transient response. Compensating for large output capacitance but placing less capacitance on the output can lead to instability.

Table 8-1. Switching Frequency, Compensation, and Spread Spectrum Clocking

R_{CF}	COMPENSATION	SWITCHING FREQUENCY	MINIMUM OUTPUT CAPACITANCE FOR VOUT < 1V	MINIMUM OUTPUT CAPACITANCE FOR 1V ≤ VOUT < 3.3V	MINIMUM OUTPUT CAPACITANCE FOR VOUT ≥ 3.3V
10kΩ .. 4.5kΩ	For smallest output capacitance (comp setting 1) SSC disabled	$R_{CF}(k\Omega) = \frac{18MHz \times k\Omega}{f_S(MHz)}$	15μF	10μF	8μF
33kΩ .. 15kΩ	For best transient response (larger output capacitance) (comp setting 2) SSC enabled	$R_{CF}(k\Omega) = \frac{60MHz \times k\Omega}{f_S(MHz)}$	30μF	18μF	15μF
100kΩ .. 45kΩ	For best transient response (larger output capacitance) (comp setting 2) SSC disabled	$R_{CF}(k\Omega) = \frac{180MHz \times k\Omega}{f_S(MHz)}$	30μF	18μF	15μF
tied to GND	For smallest output capacitance (comp setting 1) SSC disabled	internally fixed 2.25MHz	15μF	10μF	8μF
tied to V_{IN}	For best transient response (larger output capacitance) (comp setting 2) SSC enabled	internally fixed 2.25MHz	30μF	18μF	15μF

See also Section 9.2.2.4 for further details on the output capacitance required depending on the output voltage.

A resistor value that is too high for R_{CF} is decoded as "tied to V_{IN}", a value below the lowest range is decoded as "tied to GND". The minimum output capacitance in Switching Frequency, Compensation, and

Spread Spectrum Clocking is for capacitors close to the output of the device. If the capacitance is distributed, a lower compensation setting can be required.

8.3.3 MODE/SYNC

When MODE/SYNC is set low, the device operates in PWM or PFM mode, depending on the output current. The MODE/SYNC pin forces PWM mode when set high. The pin also allows you to apply an external clock in a frequency range from 1.8MHz to 4MHz for external synchronization. When an external clock is applied, the device operates in PWM mode. As with the switching frequency selection, the specification for the minimum on-time has to be observed when applying the external clock signal. The synchronization to the external clock is done on the falling edge of the applied clock to the rising edge of the internal SW pin. The MODE/SYNC pin can be changed during operation.

8.3.4 Spread Spectrum Clocking (SSC)

These devices offer spread spectrum clocking, where the switching frequency is randomly changed in PWM mode when the internal clock is used. The frequency variation is typically between the nominal switching frequency and up to 288kHz above the nominal switching frequency. When the device is externally synchronized, the TPSM82850x-Q1 follows the external clock and the internal spread spectrum block is turned off. SSC is also disabled during soft start.

8.3.5 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents misoperation of the device by switching off both the MOSFETs. The device is fully operational for voltages above the rising UVLO threshold and turns off if the input voltage goes below the falling threshold.

8.3.6 Power-Good Output (PG)

Power good is an open-drain output that requires a pullup resistor to any voltage up to the recommended input voltage level. Power good is driven by a window comparator. PG is held low when the device is disabled, in undervoltage lockout in thermal shutdown, and not in soft start. When the output voltage is in regulation hence, within the window defined in the electrical characteristics, the output is high impedance.

V_{IN} must remain present for the PG pin to stay low. If the power-good output is not used, TI recommends to tie to GND or leave open. The PG indicator features a deglitch, as specified in the electrical characteristics, for the transition from *high impedance* to *low* of the output.

Table 8-2. PG Status

EN	DEVICE STATUS	PG STATE
X	V_{IN} < 2V	undefined
low	V_{IN} ≥ 2V	low
high	2V ≤ V_{IN} ≤ UVLO OR in thermal shutdown OR V_{OUT} not in regulation OR device in soft start	low
high	V_{OUT} in regulation	high impedance

8.3.7 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 170°C (typ), the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and PG goes low. When T_J decreases below the hysteresis amount of typically 15°C, the converter resumes normal operation, beginning with soft start. During PFM, the thermal shutdown is not active.

8.4 Device Functional Modes

8.4.1 Pulse Width Modulation (PWM) Operation

The TPSM82850x-Q1 family has two operating modes: forced PWM mode and PFM/PWM mode.

With the MODE/SYNC pin set to high, the TPSM82850x-Q1 family operates with pulse width modulation in continuous conduction mode (CCM). The switching frequency is 2.25MHz or defined by an external clock signal applied to the MODE/SYNC pin. With an external clock applied to MODE/SYNC, the TPSM82850x-Q1 devices follow the frequency applied to the pin. In general, the frequency range in forced PWM mode is 1.8MHz to 4MHz. However, the frequency must be in a range the TPSM82850x-Q1 can operate at, taking the minimum on-time into account.

8.4.2 Power Save Mode Operation (PFM/PWM)

When the MODE/SYNC pin is low, power save mode is allowed. The device operates in PWM mode as long as the peak inductor current is above the PFM threshold of about 0.8A. When the peak inductor current drops below the PFM threshold, the device starts to skip switching pulses. In power save mode, the switching frequency decreases with the load current maintaining high efficiency.

8.4.3 100% Duty-Cycle Operation

The duty cycle of a buck converter operated in PWM mode is given as D = VOUT / VIN. The duty cycle increases as the input voltage comes close to the output voltage and the off-time gets smaller. When the minimum off-time of typically 10ns is reached, the TPSM82850x-Q1 devices skip switching cycles while approaching 100% mode. In 100% mode, the device keeps the high-side switch on continuously. The high-side switch stays turned on as long as the output voltage is below the target. This feature is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The following equation gives the minimum input voltage to maintain a minimum output voltage:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT(min)} \times R_{DP} \tag{1}$$

where

- R_{DP} is the resistance from V_{IN} to V_{OUT}, which includes the high-side MOSFET on-resistance and DC resistance of the inductor.
- $V_{OUT\ (min)}$ is the minimum output voltage the load can accept.

8.4.4 Current Limit and Short-Circuit Protection

The TPSM82850x-Q1 devices are protected against overload and short-circuit events. If the inductor current exceeds the current limit I_{LIMH}, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. The high-side MOSFET turns on again only if the current in the low-side MOSFET has decreased below the low-side current limit. Due to internal propagation delays, the actual current can exceed the static current limit. The following equation gives the dynamic current limit:

$$I_{peak} = I_{LIMH} + \frac{V_L}{L} \times t_{PD} \tag{2}$$

where

- I_{LIMH} is the static current limit, as specified in the electrical characteristics
- L is the effective inductance of the internal inductor (typical 0.47μH)
- V_L is the voltage across the inductor ($V_{IN} – V_{OUT}$)
- t_{PD} is the internal propagation delay of typically 50ns

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. Calculate the dynamic high-side switch peak current as follows:

$$I_{peak} = I_{LIMH} + \frac{V_{IN} - V_{OUT}}{L} \times 50ns \tag{3}$$

8.4.5 Output Discharge

The purpose of the discharge function is to make sure a defined down-ramp of the output voltage when the device is disabled and keep the output voltage close to 0V when the device is off. The output discharge feature is only active after the TPSM82850x-Q1 devices have been enabled at least once since the supply voltage was applied. The discharge function is enabled as soon as the device is disabled, in thermal shutdown, or in undervoltage lockout. The minimum supply voltage required for the discharge function to remain active is typically 2V. Output discharge is not activated during a current limit event.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPSM82850x-Q1 are synchronous, step-down, converter power modules. The required power inductor is integrated in a shielded version inside the TPSM82850x-Q1. The TPSM82850x-Q1 family members are pin-to-pin and BOM-to-BOM compatible, differing only in the rated output current.

9.2 Typical Application

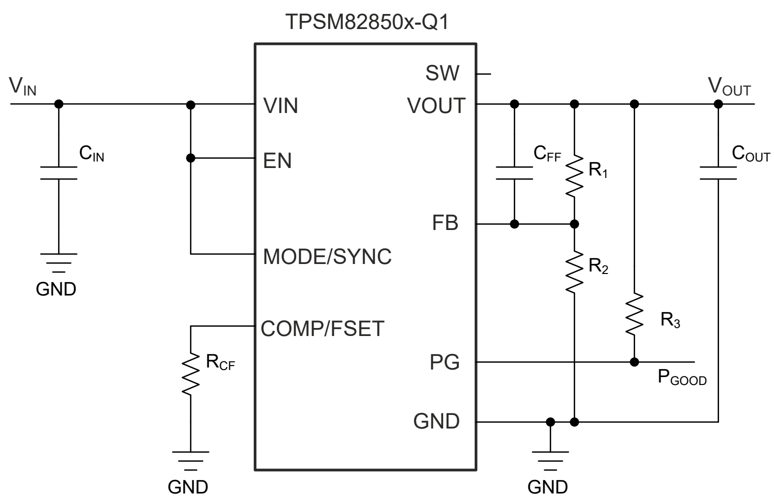


Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

The design guidelines provide a component selection to operate the device within the recommended operating conditions.

9.2.2 Detailed Design Procedure

9.2.2.1 Setting the Output Voltage

The output voltage of the TPSM82850x-Q1 devices is adjustable. Choose resistors R1 and R2 to set the output voltage within a range of 0.6V to 5.5V according to Equation 4. To keep the feedback (FB) net robust from noise, set R2 equal to or lower than 100kΩ to have at least 6µA of current in the voltage divider. Lower values of FB resistors achieve better noise immunity, and lower light load efficiency, as explained in the *Design Considerations for a Resistive Feedback Divider in a DC/DC Converter* analog design journal.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) \quad (4)$$

With V_{FB} = 0.6V:

Table 9-1. Setting the Output Voltage

NOMINAL OUTPUT VOLTAGE V_{OUT}	R_1	R_2	C_{FF}	EXACT OUTPUT VOLTAGE
0.8V	16.9kΩ	51kΩ	10pF	0.7988V
1.0V	20kΩ	30kΩ	10pF	1.0V
1.1V	39.2kΩ	47kΩ	10pF	1.101V
1.2V	68kΩ	68kΩ	10pF	1.2V
1.5V	76.8kΩ	51kΩ	10pF	1.5V
1.8V	80.6kΩ	40.2kΩ	10pF	1.803V
2.5V	47.5kΩ	15kΩ	10pF	2.5V
3.3V	88.7kΩ	19.6kΩ	10pF	3.315V

9.2.2.2 Feedforward Capacitor

TI recommends a feedforward capacitor (C_{FF}) in parallel with R_1 to improve the transient response. Regardless of the FB resistor values, the C_{FF} value must always be 10pF.

9.2.2.3 Input Capacitor

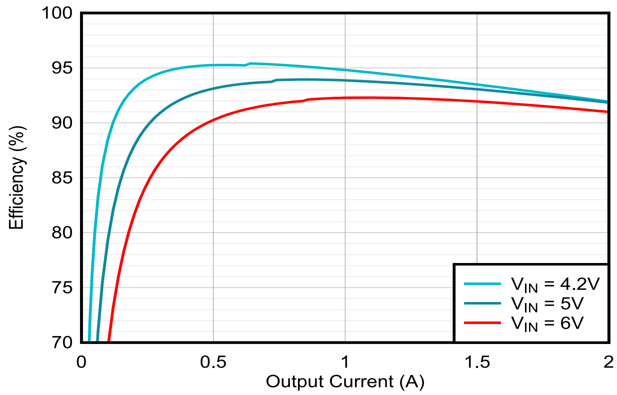
For most applications, 10µF nominal is sufficient and recommended. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. TI recommends a low-ESR multilayer ceramic capacitor (MLCC) for best filtering and must be placed between VIN and GND as close as possible to those pins.

9.2.2.4 Output Capacitor

The architecture of the TPSM82850x-Q1 family allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and TI recommends them. To keep low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends to use X7R or X5R dielectric. Using a higher value has advantages like smaller voltage ripple and a tighter DC output accuracy in power save mode.

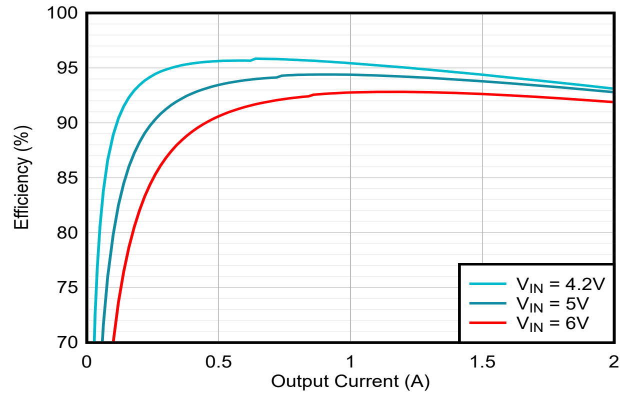
9.2.3 Application Curves

T_A = 25°C, V_{IN} = 5V, V_{OUT} = 1.8V, 1.8MHz, PWM mode, BOM = Table 7-1 unless otherwise noted.



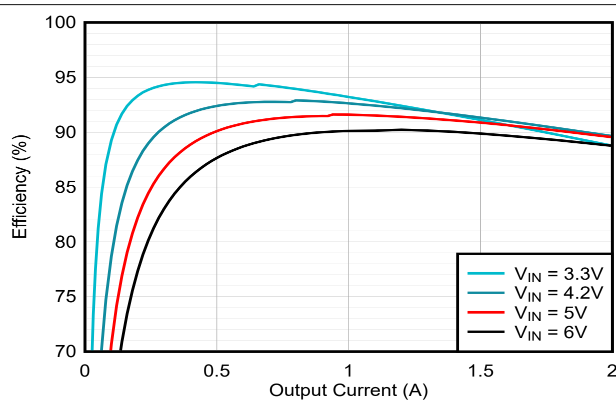
V_{OUT} = 3.3V PWM T_A = 85°C

Figure 9-2. Efficiency versus Output Current



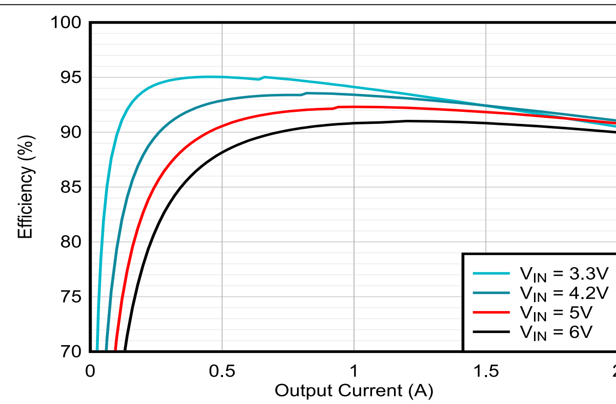
V_{OUT} = 3.3V PWM T_A = 25°C

Figure 9-3. Efficiency versus Output Current



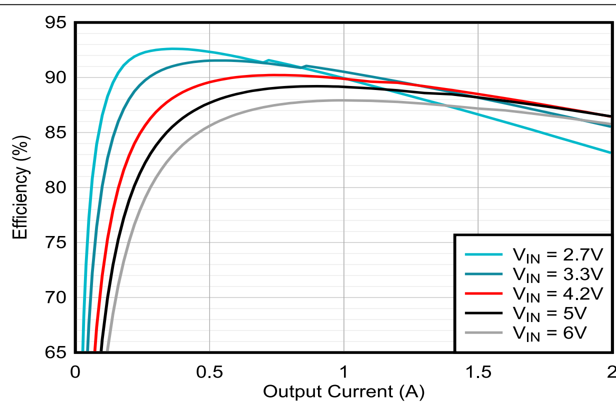
V_{OUT} = 2.5V PWM T_A = 85°C

Figure 9-4. Efficiency versus Output Current



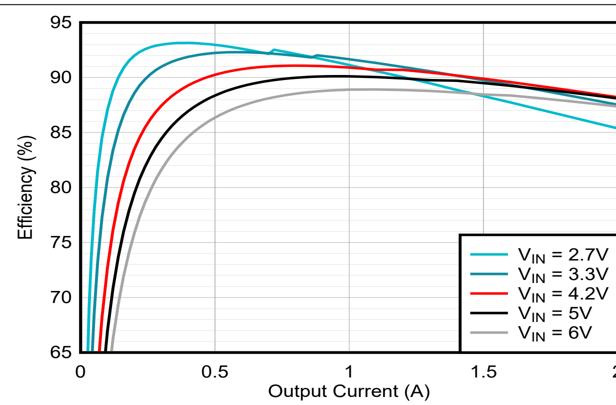
V_{OUT} = 2.5V PWM T_A = 25°C

Figure 9-5. Efficiency versus Output Current



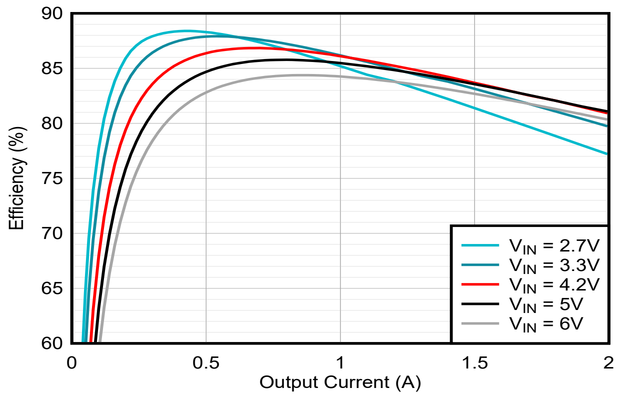
V_{OUT} = 1.8V PWM T_A = 85°C

Figure 9-6. Efficiency versus Output Current



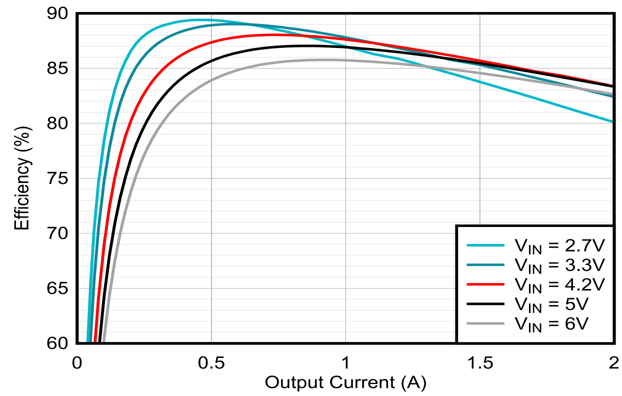
V_{OUT} = 1.8V PWM T_A = 25°C

Figure 9-7. Efficiency versus Output Current



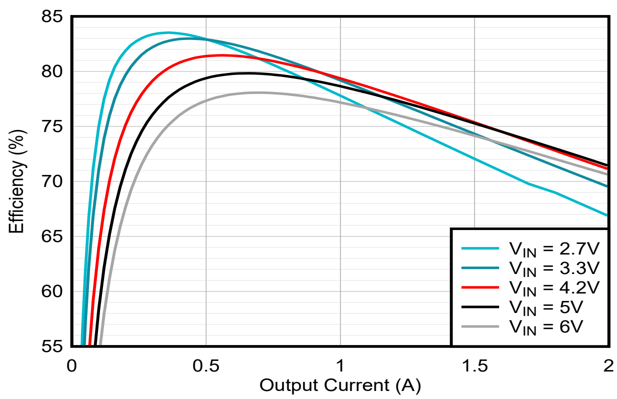
V_{OUT} = 1.1V PWM T_A = 85°C

Figure 9-8. Efficiency versus Output Current



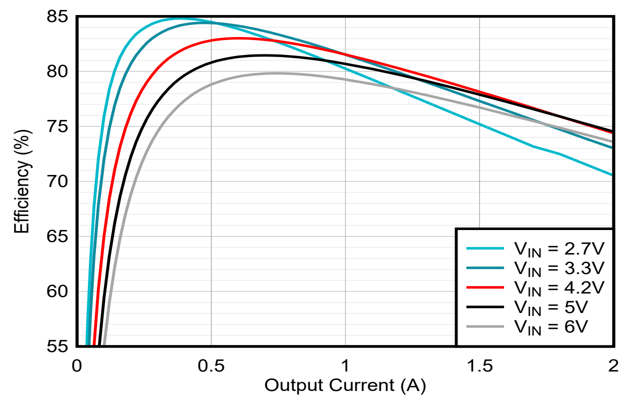
V_{OUT} = 1.1V PWM T_A = 25°C

Figure 9-9. Efficiency versus Output Current



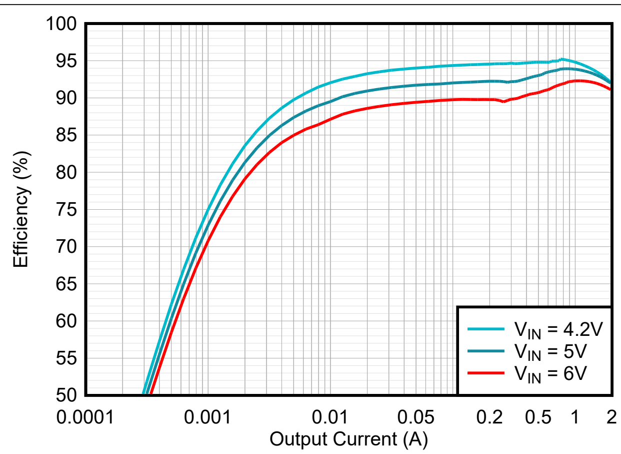
V_{OUT} = 0.6V PWM | T_A = 85°C

Figure 9-10. Efficiency versus Output Current



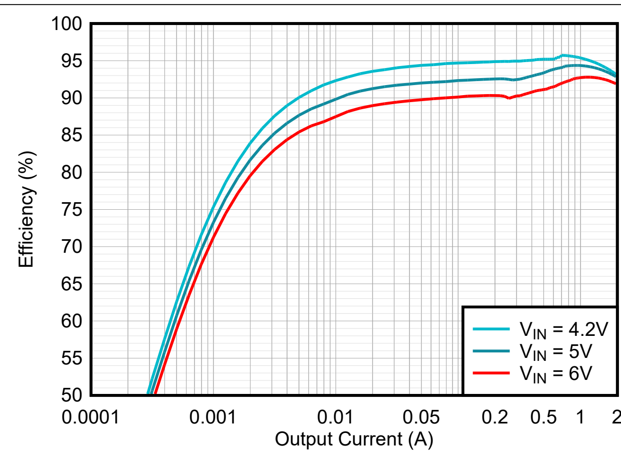
V_{OUT} = 0.6V PWM | T_A = 25°C

Figure 9-11. Efficiency versus Output Current



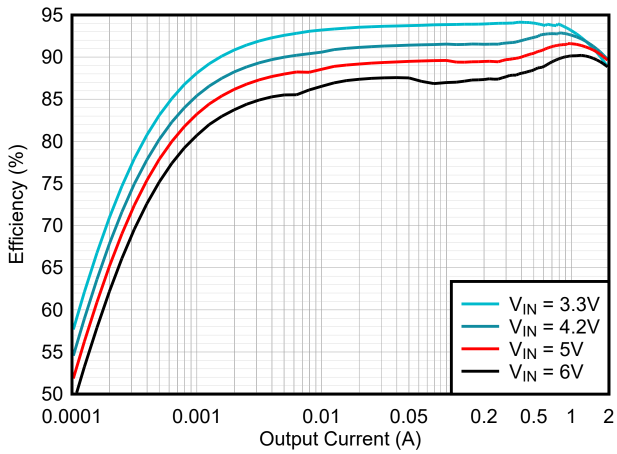
V_{OUT} = 3.3V PFM T_A = 85°C

Figure 9-12. Efficiency versus Output Current



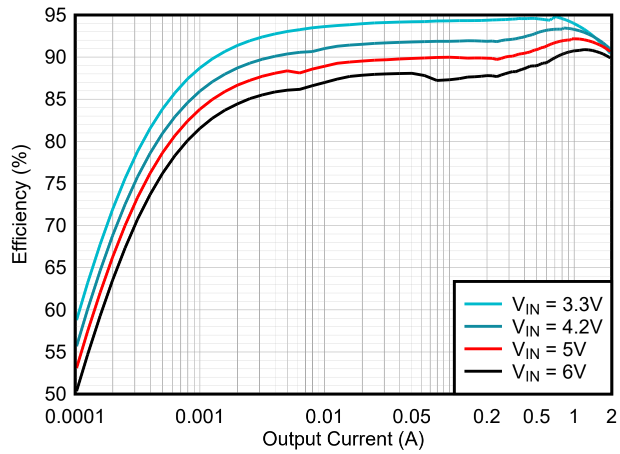
V_{OUT} = 3.3V PFM T_A = 25°C

Figure 9-13. Efficiency versus Output Current



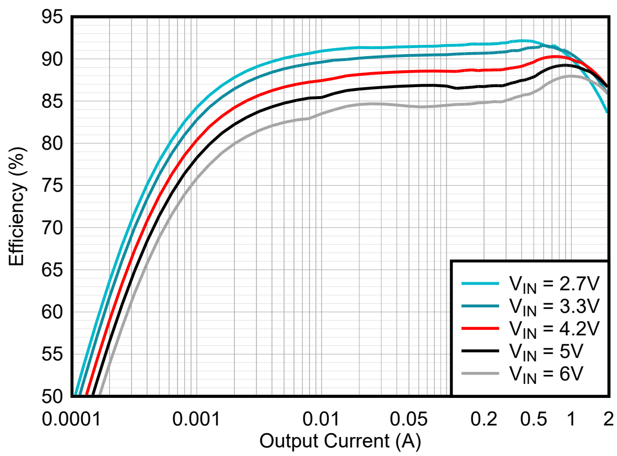
V_{OUT} = 2.5V PFM T_A = 85°C

Figure 9-14. Efficiency versus Output Current



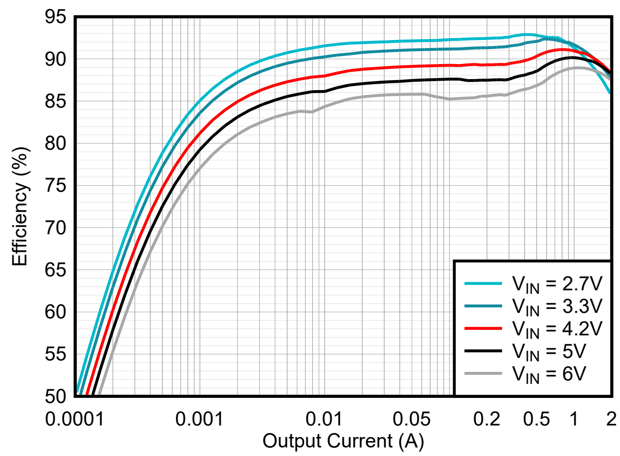
V_{OUT} = 2.5V PFM T_A = 25°C

Figure 9-15. Efficiency versus Output Current



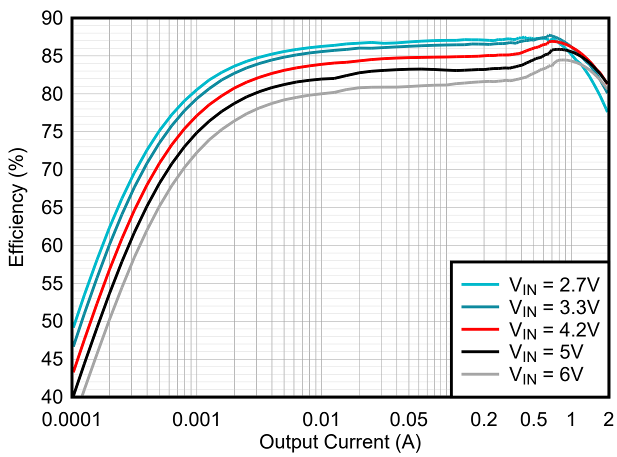
V_{OUT} = 1.8V PFM T_A = 85°C

Figure 9-16. Efficiency versus Output Current



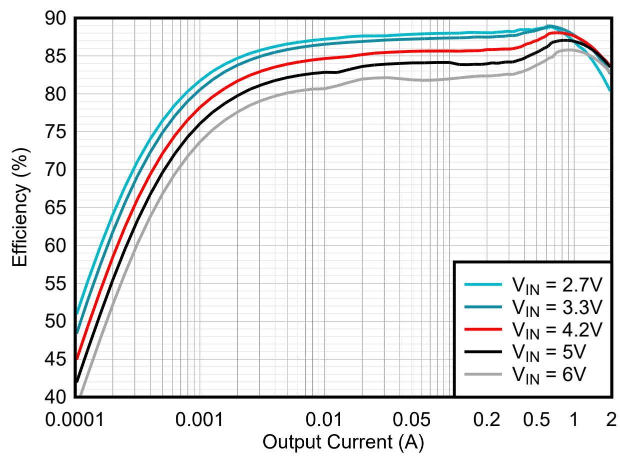
V_{OUT} = 1.8V PFM T_A = 25°C

Figure 9-17. Efficiency versus Output Current



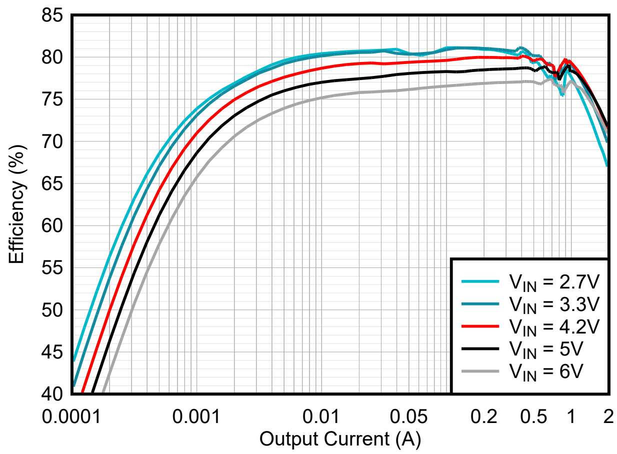
V_{OUT} = 1.1V PFM T_A = 85°C

Figure 9-18. Efficiency versus Output Current



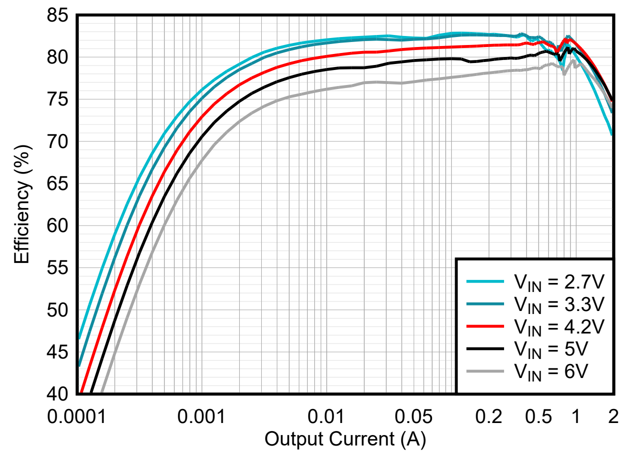
V_{OUT} = 1.1V PFM T_A = 25°C

Figure 9-19. Efficiency versus Output Current



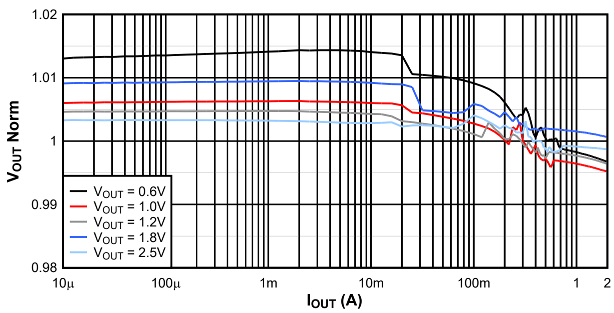
V_{OUT} = 0.6V PFM | T_A = 85°C

Figure 9-20. Efficiency versus Output Current



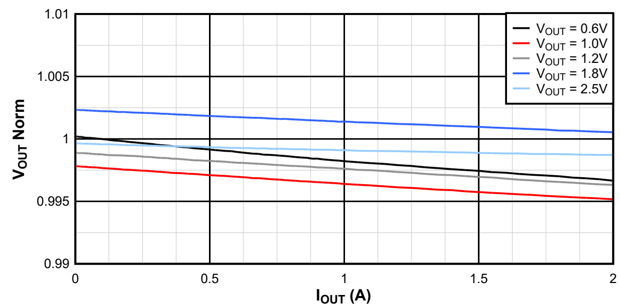
V_{OUT} = 0.6V PFM | T_A = 25°C

Figure 9-21. Efficiency versus Output Current



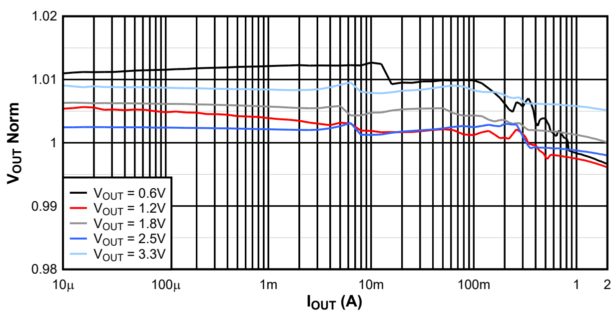
PFM Mode T_A = 25°C

Figure 9-22. Load Regulation V_{IN} = 3.3V



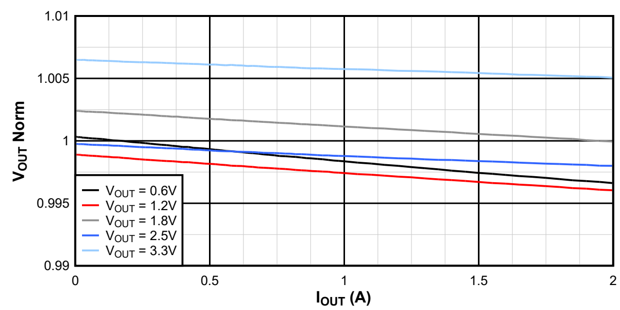
PWM Mode T_A = 25°C

Figure 9-23. Load Regulation V_{IN} = 3.3V



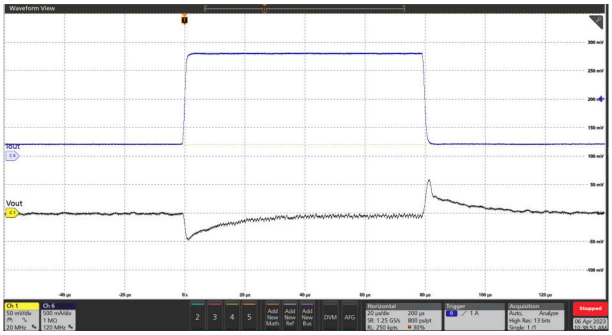
PFM Mode T_A = 25°C

Figure 9-24. Load Regulation V_{IN} = 5V



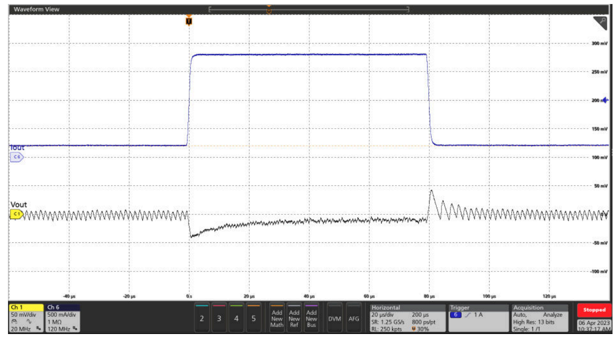
PWM Mode T_A = 25°C

Figure 9-25. Load Regulation V_{IN} = 5V



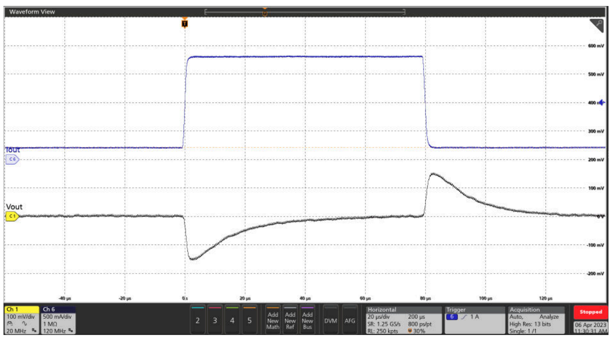
V_{OUT} = 0.6V PWM T_A = 25°C
V_{IN} = 3.3V I_{OUT} = 0.2A to 1.8A

Figure 9-26. Load Transient Response



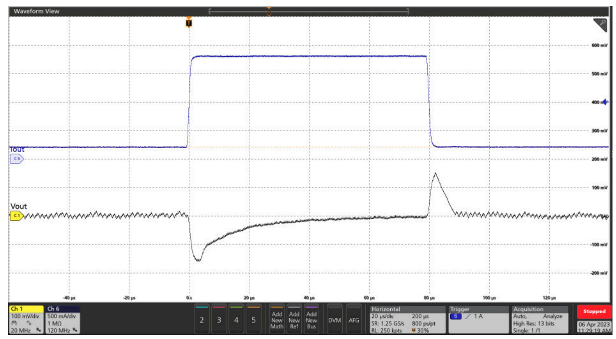
V_{OUT} = 0.6V PFM T_A = 25°C
V_{IN} = 3.3V I_{OUT} = 0.2A to 1.8A

Figure 9-27. Load Transient Response



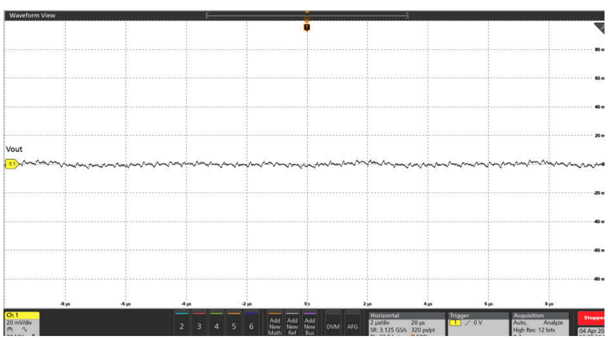
V_{OUT} = 3.3V PWM T_A = 25°C
V_{IN} = 5.0V I_{OUT} = 0.2A to 1.8A

Figure 9-28. Load Transient Response



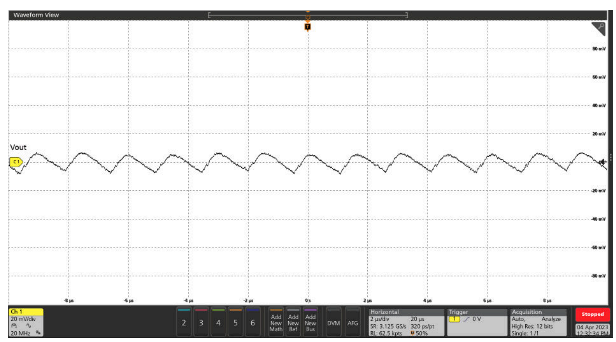
V_{OUT} = 3.3V PFM T_A = 25°C
V_{IN} = 5.0V I_{OUT} = 0.2A to 1.8A

Figure 9-29. Load Transient Response



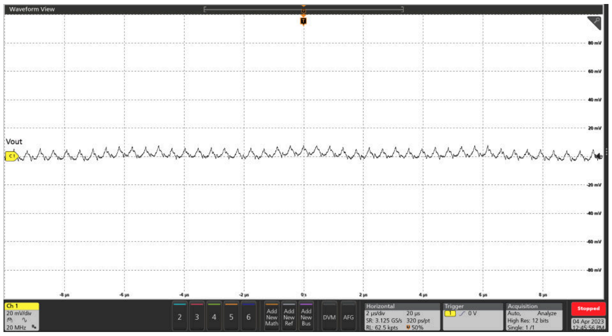
V_{OUT} = 0.6V PWM T_A = 25°C
I_{OUT} = 0.2A V_{IN} = 3.3V BW = 20MHz

Figure 9-30. Output and Input Voltage Ripple



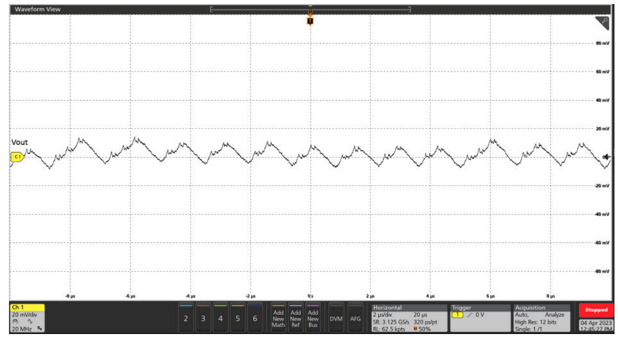
V_{OUT} = 0.6V PFM T_A = 25°C
I_{OUT} = 0.2A V_{IN} = 3.3V BW = 20MHz

Figure 9-31. Output and Input Voltage Ripple



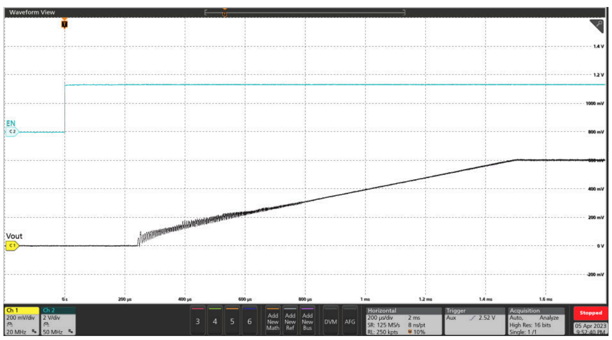
V_{OUT} = 3.3V | PWM | T_A = 25°C
I_{OUT} = 0.2A | V_{IN} = 5.0V | BW = 20MHz

Figure 9-32. Output and Input Voltage Ripple



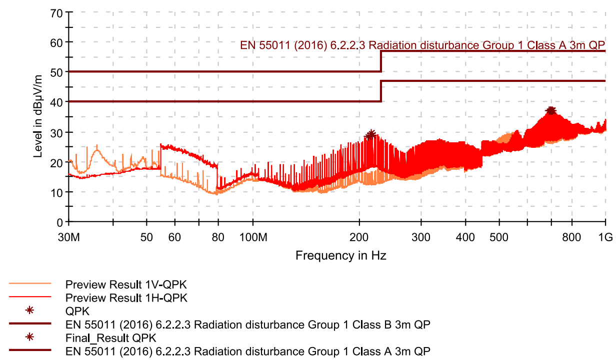
V_{OUT} = 3.3V | PFM | T_A = 25°C
I_{OUT} = 0.2A | V_{IN} = 5.0V | BW = 20MHz

Figure 9-33. Output and Input Voltage Ripple



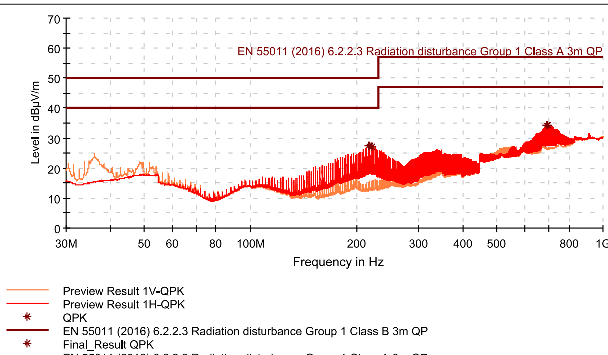
V_{OUT} = 0.6V | PWM/PFM | T_A = 25°C
I_{OUT} = 2A | V_{IN} = 3.3V | C_{SS} = 4.7nF

Figure 9-34. Start-Up Timing



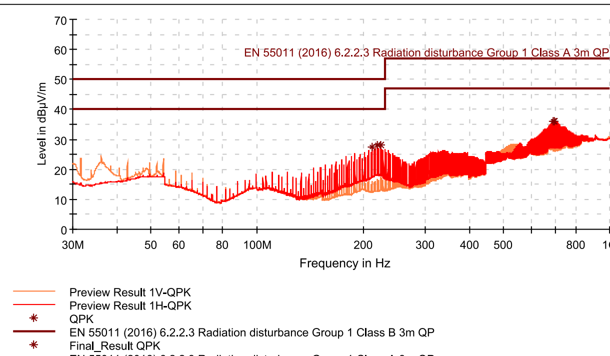
V_{OUT} = 1.2V | PWM | T_A = 25°C
I_{OUT} = 2A | V_{IN} = 6V | measured on TPSM828512EVM

Figure 9-35. Radiated Emissions



V_{OUT} = 1.8V | PWM | T_A = 25°C
I_{OUT} = 2A | V_{IN} = 6V | measured on TPSM828512EVM

Figure 9-36. Radiated Emissions



V_{OUT} = 3.3V | PWM | T_A = 25°C
I_{OUT} = 2A | V_{IN} = 6V | measured on TPSM828512EVM

Figure 9-37. Radiated Emissions

9.3 System Examples

9.3.1 Synchronizing to an External Clock

The TPSM82850x-Q1 devices can be synchronized by applying a clock on the MODE/SYNC pin. There is no need for any additional circuitry. See Figure 9-38. The clock can be applied, changed, and removed during operation. TI recommends the value of the R_{CF} resistor to be chosen such that the internally defined frequency and the externally-applied frequency are close to each other to have a fast settling time to the external clock. Synchronizing to a clock is not possible, if the COMP/FSET pin is connected to Vin or GND. Figure 9-39 and Figure 9-40 show the external clock being applied and removed. When an external clock is applied, the device operates in PWM mode.

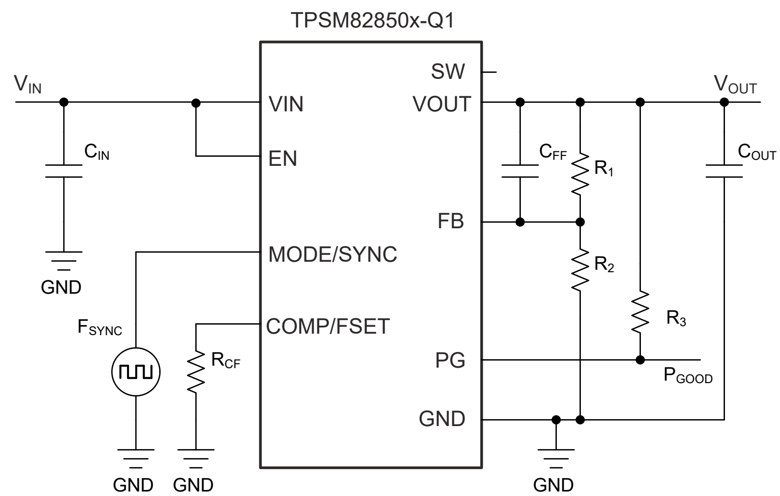
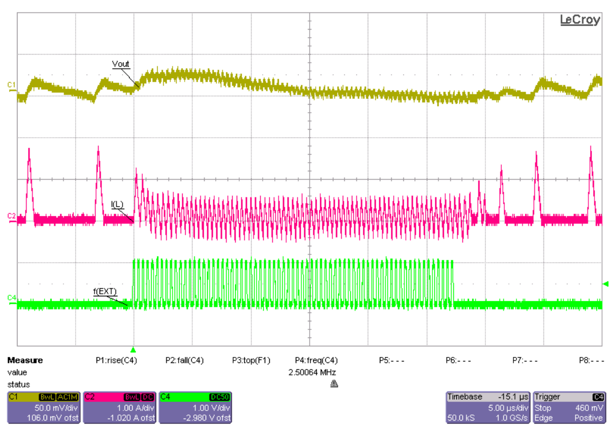
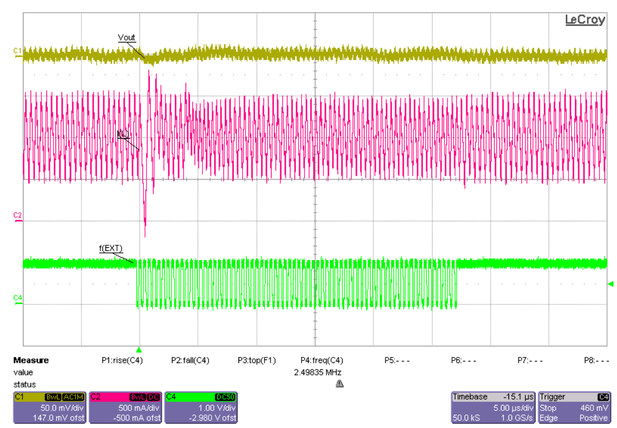


Figure 9-38. Frequency Synchronization



V_{IN} = 5V R_{CF} = 8.06kΩ I_{OUT} = 0.1A
V_{OUT} = 1.8V f_{EXT} = 2.5MHz

Figure 9-39. Applying and Removing the Synchronization Signal (PFM)



V_{IN} = 5V R_{CF} = 8.06kΩ I_{OUT} = 1A
V_{OUT} = 1.8V f_{EXT} = 2.5MHz

Figure 9-40. Applying and Removing the Synchronization Signal (FPWM)

9.4 Power Supply Recommendations

The TPSM82850x-Q1 device family has no special requirements for the input power supply. Rate the output current of the input power supply according to the supply voltage, output voltage, and output current of the TPSM82850x-Q1.

9.5 Layout

9.5.1 Layout Guidelines

A proper layout is critical for the operation of any switched mode power supply, especially at high switching frequencies. Therefore, the PCB layout of the TPSM82850x-Q1 demands careful attention to make sure of best performance. A poor layout can lead to issues like bad line and load regulation, instability, increased EMI radiation, and noise sensitivity. Refer to the *Five Steps to a Great PCB Layout for a Step-Down Converter* analog design journal for a detailed discussion of general best practices. Specific recommendations for the device are listed below.

- Place the input capacitor as close as possible to the VIN and GND pins of the device. This placement is the most critical component placement. Route the input capacitor directly to the VIN and GND pins avoiding vias.
- Place the output capacitor ground close to the VOUT and GND pins and route directly avoiding vias.
- Place the FB resistors, R1 and R2, and the feedforward capacitor C_{FF} close to the FB pin and place C_{SS} close to the SS/TR pin to minimize noise pickup.
- The recommended layout is implemented on the EVM and shown in *TPSM828502QEVM-159 Evaluation Module* EVM user's guide and in *Layout Example*.
- See the recommended land pattern for the TPSM82850x-Q1 at the end of this data sheet. For best manufacturing results, create the pads as solder mask defined (SMD), when some pins (such as VIN, VOUT, and GND) are connected to large copper planes. Using SMD pads keeps each pad the same size and avoids solder pulling the device during reflow.

9.5.2 Layout Example

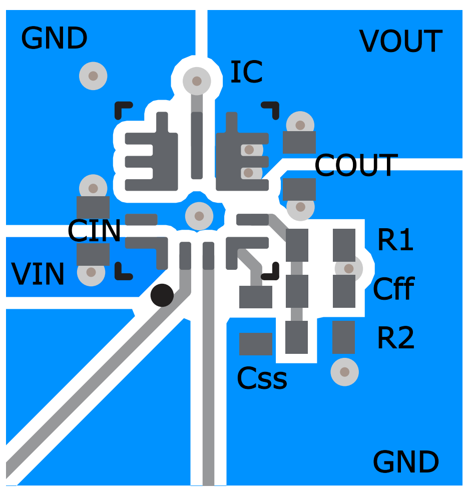


Figure 9-41. Example Layout

9.5.2.1 Thermal Consideration

The TPSM82850x-Q1 module temperature must be kept less than the maximum rating of 125°C. The following are three basic approaches for enhancing thermal performance:

- Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the component to the PCB.
- Introduce airflow into the system.

To estimate the approximate module temperature of the TPSM82850x-Q1, apply the typical efficiency stated in this data sheet to the desired application condition to compute the power dissipation of the module. Then, calculate the module temperature rise by multiplying the power dissipation by the power dissipation thermal resistance. For more details on how to use the thermal parameters in real applications, see the application notes: *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* and *Semiconductor and IC Package Thermal Metrics*.

The thermal values in *Thermal Information* used the recommended land pattern, shown at the end of this data sheet, including the 18 vias as shown. The TPSM82850x-Q1 was simulated on a PCB defined by JEDEC 51-7. The 9 vias on the GND pins are connected to copper on other PCB layers, while the remaining 9 vias are not connected to other layers.

10 Device and Documentation Support

10.1 Device Support

10.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPSM828502QEVM-159 Evaluation Module* EVM user's guide
- Texas Instruments, *Five Steps to a Great PCB Layout for a Step-Down Converter analog design journal*
- Texas Instruments, *Design Considerations for a Resistive Feedback Divider in a DC/DC Converter* analog design journal
- Texas Instruments, *Achieving a Clean Start-up by Using a DC/DC Converter with a Precise Enable-pin Threshold* analog design journal
- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* application note

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

DATE	REVISION	NOTES
November 2025	*	Initial release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSM828502WRDYRQ1	Active	Production	QFN-FCMOD (RDY) | 9	3000 | LARGE T&R	Yes	Call TI	Call TI	-40 to 125	88502

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

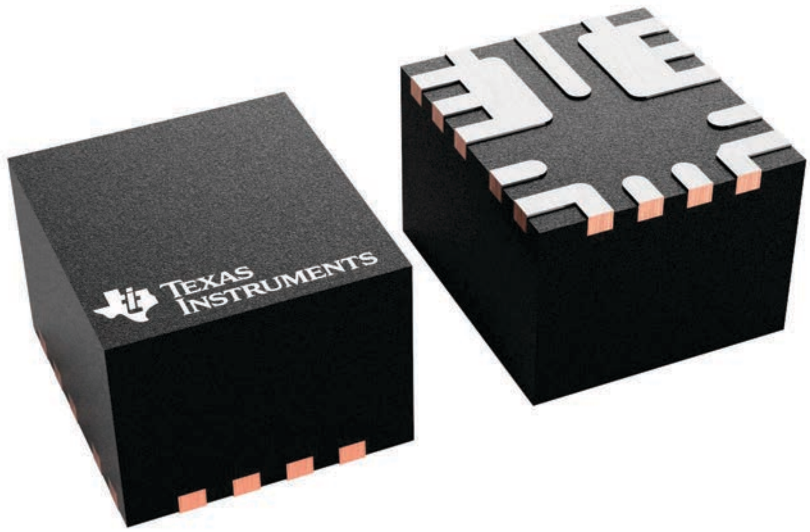
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

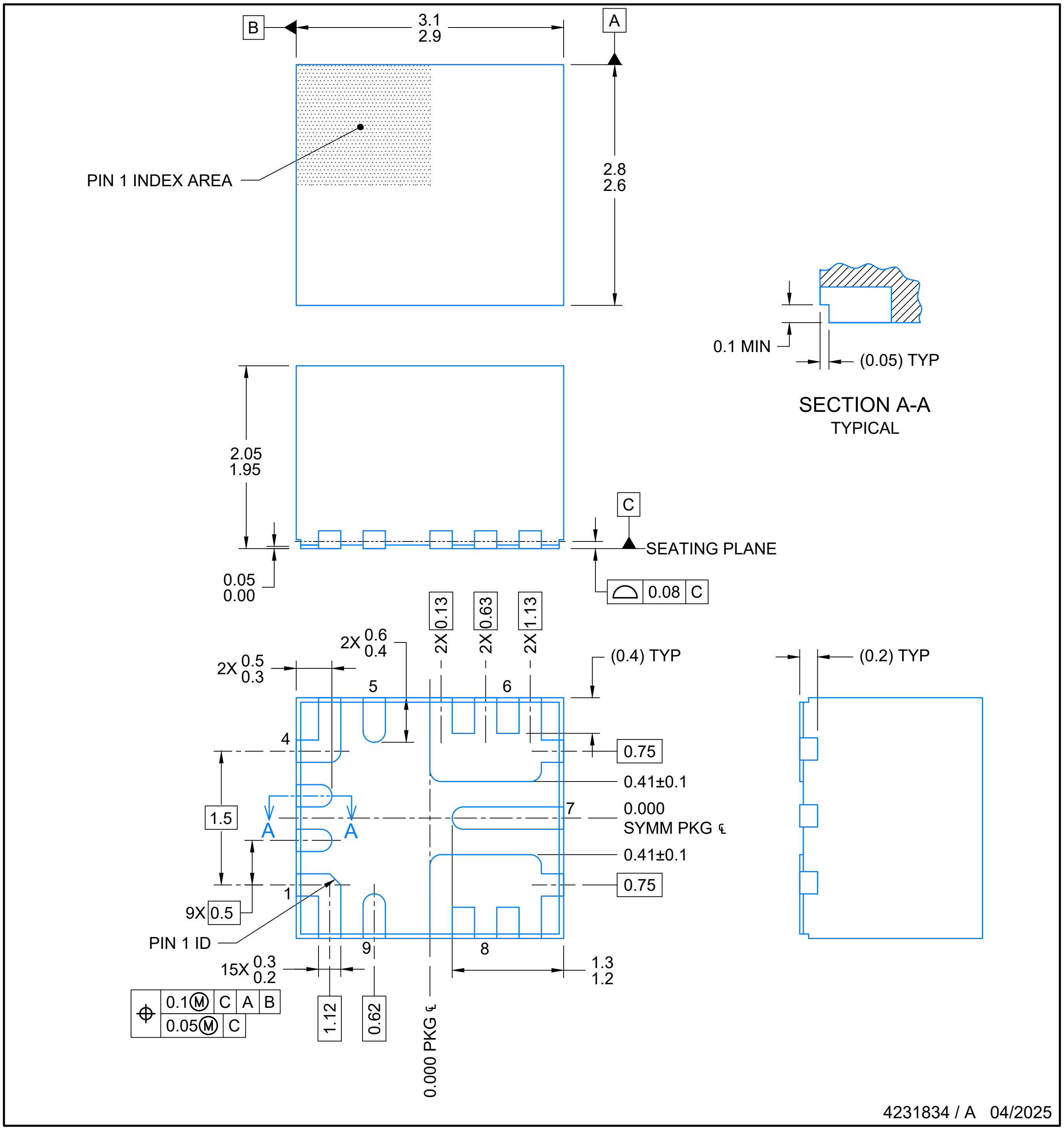
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

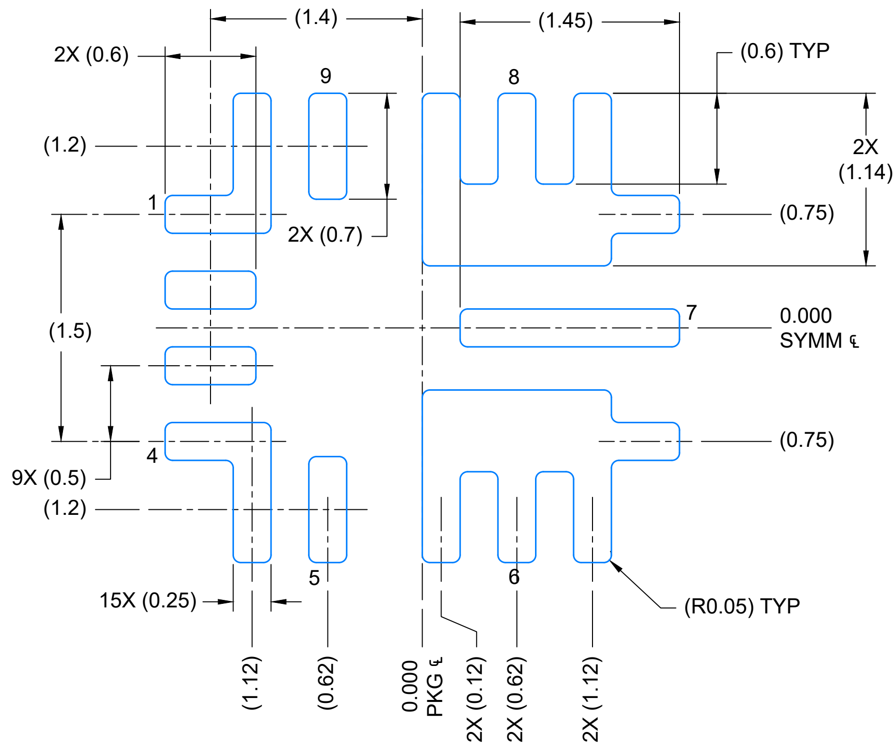
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



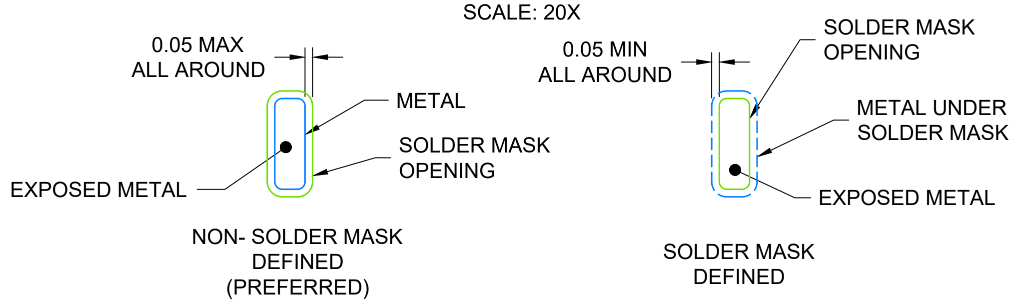


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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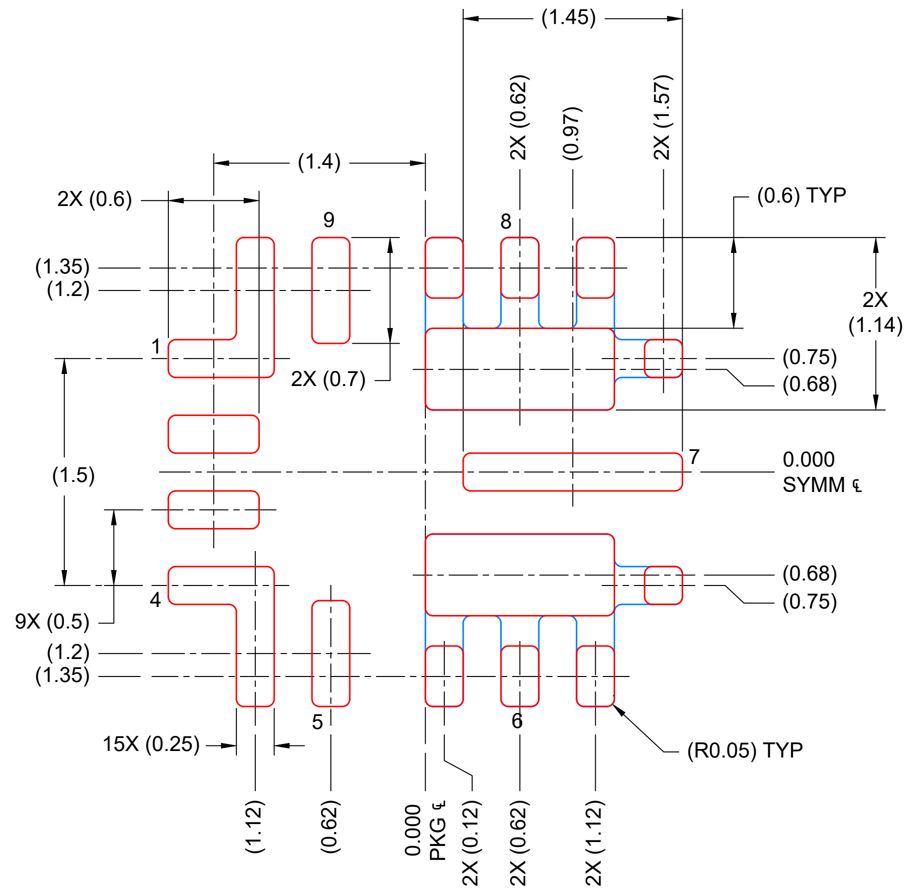
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 6 & 8 = 84%
SCALE: 20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..