# TPS92642-Q1 Automotive Synchronous Buck Infrared LED Driver

## 1 Features

- AEC-Q100 qualified for automotive applications
  - Grade 1: –40°C to 125°C ambient operating temperature
  - Device HBM classification level H1C
  - Device CDM classification level C5
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Input voltage range: 5.5 V to 36 V
  - Operation down to 5.15 V after start-up
- Up to 5-A pulsed output current with 4% accuracy
- Adaptive on-time current control
  - Low offset high-side current sense amplifier
  - Stable with any combination of ceramic, and aluminum capacitors
- Programmable switching frequency from 100 kHz to 2.2 MHz
- Advanced dimming operation
  - 1000:1 precision PWM dimming
  - 15:1 precision analog dimming
- Internal maximum duty cycle limit
- Cycle-by-cycle switch overcurrent protection
- Open-drain fault indicator output
  - LED short circuit, open circuit and cable harness fault indication
- Thermal shutdown protection

## 2 Applications

- Driver Monitoring Systems (DMS)
- IR LED and laser driver

## 3 Description

The TPS92642-Q1 is a monolithic, synchronous Buck LED driver with a wide 5.5-V to 36-V operating input voltage range and 40-V tolerance that supports load dump for duration of 400 ms. The TPS92642-Q1 implements an adaptive on-time average current mode control based on inductor valley current detection. The adaptive on-time control provides near constant switching frequency that can be set between 100 kHz and 2.2 MHz. Inductor current sensing and closed-loop feedback enables better than ±4% accuracy over wide input, output and ambient temperature.

The high-performance infrared LED driver can independently modulate LED current using both analog or PWM dimming techniques. Linear analog dimming range with over 15:1 range is obtained by setting the IADJ voltage. PWM dimming of LED current is achieved by directly modulating the UDIM input pin with desired duty cycle. The device incorporates an internal pulse monitoring circuit that limits the maximum pulse duty cycle.

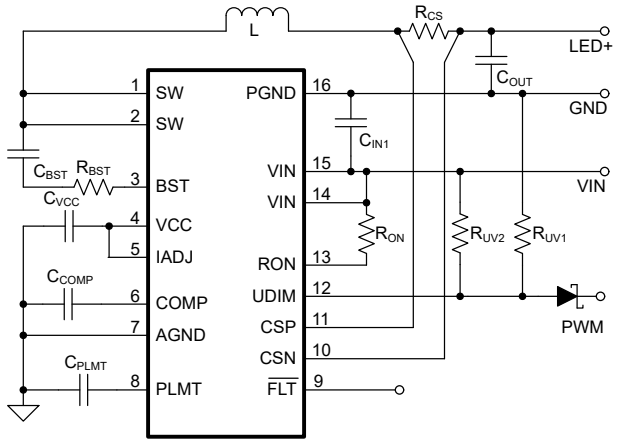
The TPS92642-Q1 incorporates advanced diagnostic and fault protection featuring: cycle-by-cycle switch current limit, bootstrap undervoltage, LED open, LED short and thermal shutdown.

The TPS92642-Q1 is available in a 6.6-mm × 5.1-mm thermally-enhanced 16-pin HTSSOP package with 0.65-mm lead pitch.

**Device Information**

| PART NUMBER | PACKAGE (1) | BODY SIZE (NOM) |
|---|---|---|
| TPS92642-Q1 | HTSSOP (16) | 6.60 mm × 5.10 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




**Typical Buck LED Driver Application Schematic**

**LED Pulse Limit**

Ch1: UDIM input  Ch2: PLMT voltage  Ch4: LED current

# Table of Contents

# 4 Pin Configuration and Functions

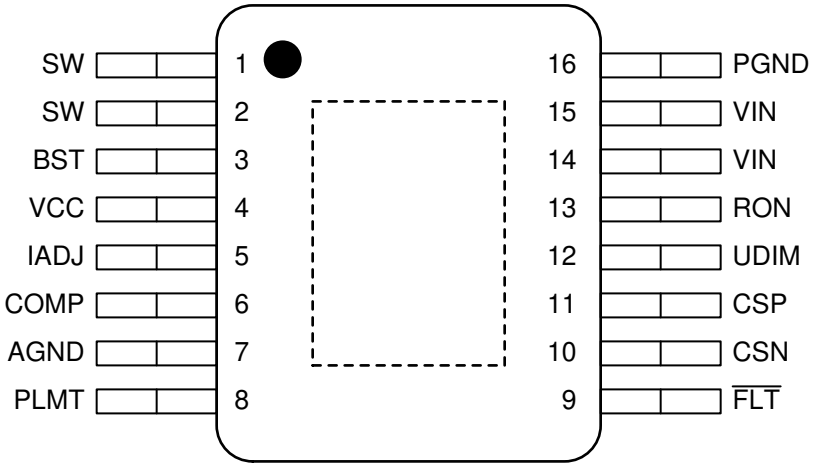



**Figure 4-1. PWP Package, 16-Pin HTSSOP with PowerPAD, Top View**

**Table 4-1. Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 7 | AGND | — | Analog ground. Return for the internal voltage reference and analog circuit. Connect to circuit ground, GND, to complete return path. |
| 3 | BST | I | Supply input for high-side MOSFET gate drive circuit. Connect a ceramic capacitor between BST and SW pins. An internal diode is connected between VCC and BST pins. |
| 6 | COMP | O | Output of internal transconductance error amplifier. Connect an integral compensation network to ensure stability. |
| 10 | CSN | I | Negative input (–) of internal rail-to-rail transconductance error amplifier. Connect directly to the negative node of the LED current sense resistor, $R_{CS}$. |
| 11 | CSP | I | Positive input (+) of internal rail-to-rail transconductance error amplifier. Connect directly to the positive node of the LED current sense resistor, $R_{CS}$. |
| 9 | $\overline{FLT}$ | O | Open-drain fault indicator. Connect to VCC with a resistor to create an active low fault signal output. |
| 5 | IADJ | I | Analog adjust input. Input below 100 mV disables the output. The analog input can be varied between 140 mV to 2.4 V to set current reference from 10 mV to 175 mV. Connect a 0.1-µF capacitor from pin to AGND. |
| 16 | PGND | — | Ground returns for low-side MOSFETs |
| 8 | PLMT | I | Pulse limit pin. Connect a capacitor from the PLMT pin to GND to set minimum period allowed of the external PWM pulse. |
| 13 | RON | I | On-time programming pin. Connect a resistor to VIN based on the desired pseudo-fixed switching frequency. |
| 1,2 | SW | I | Switching output of the regulator. Internally connected to both power MOSFETs. Connect to the power inductor. |
| 12 | UDIM | I | Undervoltage lockout and external PWM dimming input. Connect to VIN through a resistor divider to implement input undervoltage protection. Diode couple external PWM signal to enable dimming. Do not float. |
| 4 | VCC | O | VCC bias supply pin. Locally decouple to AGND using a 2.2-µF to 4.7-µF ceramic capacitor located close to the controller. |
| 14,15 | VIN | I | Power input and connection to high-side MOSFET drain node. Connect to the power supply and bypass capacitors $C_{IN}$. The path from the VIN pin to the high frequency bypass capacitor and PGND must be as short as possible. |
| PowerPAD | | — | The AGND and PGND pin must be connected to the exposed PowerPAD for proper operation. This PowerPAD must be connected to PCB ground plane using multiple vias for good thermal performance. |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input Voltage | $V_{IN}$ | –0.3 | 36 | V |
| | $V_{IN}$ (< 400 ms) | | 40 | V |
| Bias supply voltage, VCC | $V_{VCC}$ | –0.3 | 5.5 | V |
| Boot voltage, BST | BST to SW | –0.3 | 5.5 | V |
| | BST to GND | –0.3 | 41.5 | V |
| Switch node voltage | $V_{SW}$ to GND | –0.5 | 36 | V |
| | $V_{SW}$ to GND (< 400 ms) | –0.5 | 40 | V |
| | $V_{SW}$ to GND (< 10 ns) | –3.5 | 40 | V |
| Inputs | CSP, CSN | –0.5 | 36 | V |
| | RON | –0.1 | 36 | V |
| | $I_{RON}$ | | 500 | µA |
| | $V_{(CSP-CSN)}$ | –0.3 | 0.3 | mV |
| | UDIM to GND | –0.3 | $V_{VIN}$ | V |
| | IADJ | –0.1 | 5.5 | V |
| | COMP, PLMT | –0.3 | 5.5 | V |
| Outputs | $\overline{FLT}$ | –0.3 | 20 | V |
| Ground | PGND to AGND | –0.5 | 0.5 | V |
| | PGND to AGND (< 10 ns) | –3.5 | 3.5 | V |
| $T_J$ | Junction temperature | –40 | 150 | °C |
| $T_{stg}$ | Storage temperature | –40 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the *Recommended Operating Conditions* but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

## 5.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002(1) | | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | Corner pins (SW, DLMT, $\overline{FLT}$ and PGND) | ±750 | |
| | | | Other pins | ±500 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{VIN}$ | Input Voltage | 5.5 | | 36 | V |
| $V_{(CSP-CSN)}$ | Sensed inductor current ripple voltage | 10 | | | mV |
| $dV_{CSP}/dt$ | CSP slew-rate | | | 10 | V/µs |
| $I_{LED}$ | LED Current (Pulse < 4 ms) | | | 5 | A |
| $V_{UDIM}$ | Digital PWM Input | –0.3 | | $V_{VIN}$ | |
| $\overline{FLT}$ | Fault Output | –0.3 | | 18 | |
| $f_{SW}$ | Switching Frequency | 400 | | 2200 | kHz |
| $T_A$ | Ambient temperature | –40 | | 125 | °C |
| $T_J$ | Junction temperature | –40 | | 150 | °C |

## 5.4 Thermal Information

| THERMAL METRIC[1] | | DEVICE | UNIT |
|---|---|---|---|
| | | PKG (HTSSOP) | |
| | | PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 38.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 24.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 19.9 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.7 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 19.7 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 1.7 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 5.5 Electrical Characteristics

–40°C < $T_J$ < 150°C, $V_{IN}$ = 14V, $V_{UDIM}$ = 5V, $V_{IADJ}$ = 2.1V, $C_{VCC}$ = 2.2µF, $C_{BST}$ = 1nF, $C_{COMP}$ = 1nF, $R_{CS}$ = 100mΩ, $R_{ON}$ = 401kΩ, , $C_{PLMT}$ = 680nF, $f_{SW}$ = 200 kHz

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT VOLTAGE (VIN)** | | | | | | |
| $V_{DO}$ | LDO dropout voltage | $I_{VCC}$ = 20 mA, $V_{VIN}$ = 5 V | | 315 | | mV |
| $I_{SW}$ | Input switching current | | | 10 | 17.6 | mA |
| $I_{OP}$ | Input operating current | Not switching, $V_{IADJ}$ = $V_{VCC}$ | | 2 | 4 | mA |
| **BIAS SUPPLY (VCC)** | | | | | | |
| $VCC_{(UVLO-RISE)}$ | Rising threshold | VCC rising threshold, $V_{VIN}$ = 8 V | | 4.40 | 4.58 | V |
| $VCC_{(UVLO-FALL)}$ | Falling threshold | VCC falling threshold, $V_{VIN}$ = 8 V | 3.9 | 4.2 | | V |
| $VCC_{(UVLO-HYS)}$ | | Hysteresis | | 200 | | mV |
| $VCC_{(REG)}$ | Regulation voltage | No Load | 4.75 | 5.00 | 5.25 | V |
| $I_{CC(LIMIT)}$ | Supply current Limit | $V_{VCC}$ = 0 V | 45 | 56 | 76 | mA |
| **HIGH-SIDE FET (SW, BOOT)** | | | | | | |
| $R_{DS(ON-HS)}$ | High-side MOSFET on resistance | $I_{LED}$ = 100 mA | | 65 | 130 | mΩ |
| $V_{BST(UV)}$ | Bootstrap gate drive UVLO | $V_{(BST-SW)}$ rising | 3.24 | 3.4 | 3.54 | V |
| $V_{BST(HYS)}$ | Bootstrap gate drive UVLO hysteresis | Hysteresis | 175 | 207 | 240 | mV |
| $I_{Q(BST)}$ | Bootstrap pin quiescent current | $V_{SW}$ = 0V, $V_{UDIM}$ = 0 V, $V_{BOOT}$ = 5 V | 215 | 280 | 350 | µA |
| **LOW-SIDE FET (SW)** | | | | | | |
| $R_{DS(ON-LS)}$ | Low-side MOSFET on resistance | $I_{LED}$ = 100 mA | | 67 | 130 | mΩ |
| **HIGH SIDE FET CURRENT LIMIT** | | | | | | |
| $I_{LIM(HS)}$ | High-side current limit threshold | | 6.1 | 8.6 | 10.3 | A |
| $t_{(HS-BLANK)}$ | High-side current sense blanking period | | | 60 | | ns |
| **LOW SIDE FET CURRENT LIMIT** | | | | | | |
| $I_{SINK(LS)}$ | Sinking current limit | | 2.0 | 3.2 | 4.3 | A |
| $t_{BLANK}$ | Blanking time | | | 71 | | ns |
| **ERROR AMPLIFIER (CSP, CSN, COMP)** | | | | | | |
| $V_{(CSP-CSN)}$ | Current sense threshold | $V_{IADJ}$ = $V_{CC}$, $V_{CSP}$ = 3 V, $I_{COMP}$ = 0 V | 168 | 175 | 182 | mV |
| | | $V_{IADJ}$ = 2.1 V, $V_{CSP}$ = 3 V, $I_{COMP}$ = 0 V | | 150 | | mV |
| $I_{CSP}$ | CSP bias current | $V_{IADJ}$ = 150 mV | | 10 | | µA |
| $g_M$ | Transconductance | | | 450 | | µA/V |
| $I_{COMP(SRC)}$ | COMP current source capacity | $V_{IADJ}$ = 2.5 V, $V_{(CSP-CSN)}$ = 0 V | | 200 | | µA |
| $I_{COMP(SINK)}$ | COMP current sink capacity | $V_{IADJ}$ = 150 mV, $V_{(CSP-CSN)}$ = 300 mV | | 140 | | µA |
| $V_{COMP(RISE)}$ | COMP startup threshold | Rising | | 2.45 | | V |
| $V_{COMP(HYS)}$ | COMP startup comparator hysteresis | | | 440 | | mV |
| $EA_{(BW)}$ | Bandwidth | Unity gain bandwidth | | 3 | | MHz |
| $I_{COMP(LKG)}$ | Comp leakage current | $V_{UDIM}$ = 0 V | | 2.5 | | nA |
| $V_{COMP(RST)}$ | COMP pin reset voltage | $V_{VCC}$ dropping from 5 V to 0 V | | 100 | | mV |
| $R_{COMP(DCH)}$ | COMP discharge FET resistance | | | 230 | | Ω |
| $V_{COMP(OV)}$ | COMP overvoltage protection threshold | | 2.9 | 3.2 | | V |
| $V_{COMP(OV-HYS)}$ | COMP overvoltage protection hysteresis | | | 60 | | mV |
| $V_{CSP(SHORT)}$ | Output short circuit detection threshold | Falling | | 1.5 | | V |
| | | Rising | | 1.6 | | V |

–40°C < $T_J$ < 150°C, $V_{IN}$ = 14V, $V_{UDIM}$ = 5V, $V_{IADJ}$ = 2.1V, $C_{VCC}$ = 2.2µF, $C_{BST}$ = 1nF, $C_{COMP}$ = 1nF, $R_{CS}$ = 100mΩ, $R_{ON}$ = 401kΩ, , $C_{PLMT}$ = 680nF, $f_{SW}$ = 200 kHz

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ANALOG ADJUST INPUT (IADJ)** | | | | | | |
| $V_{IADJ(CLAMP)}$ | IADJ internal clamp voltage | | | 2.45 | | V |
| $V_{IADJ(DIS)}$ | Disable threshold voltage | Rising | | 133 | | mV |
| $V_{IADJ(DIS)}$ | Disable threshold voltage | Falling | | 100 | | mV |
| **VALLEY CURRENT COMPARATOR** | | | | | | |
| $g_{M(LV)}$ | Level shift amplifier transconductance | | | 50 | | µA/V |
| $t_{DEL}$ | $V_{(CSP-CSN)}$ falling to gate rising delay | | | 65 | | ns |
| **ON-TIME GENERATOR (RON)** | | | | | | |
| $t_{ON(MIN)}$ | Minimum on-time | | 85 | 101 | 117 | ns |
| $t_{ON}$ | Programmed on-time | $V_{VIN}$ = 14 V, $V_{CSP}$ = 5 V, $R_{ON}$ = 35 kΩ | | 150 | | ns |
| | | $V_{VIN}$ = 10 V, $V_{CSP}$ = 8 V, $R_{ON}$ = 35 kΩ | | 336 | | ns |
| | | $V_{VIN}$ = 14 V, $V_{CSP}$ = 3 V, $R_{ON}$ = 400 kΩ | | 0.95 | | µs |
| | | $V_{VIN}$ = 10 V, $V_{CSP}$ = 8 V, $R_{ON}$ = 400 kΩ | | 3.55 | | µs |
| **MINIMUM OFF-TIME** | | | | | | |
| $t_{OFF(MIN)}$ | Minimum off-time | $V_{(CSP-CSN)}$ = 0 V, VCOMP = 2.5 V | 63 | 78 | 93 | ns |
| **PWM DIMMING and PROGRAMMABLE UVLO INPUT (UDIM)** | | | | | | |
| $I_{UDIM(DO)}$ | UDIM source current (UVLO hysteresis) | $V_{UDIM}$ > 2.45 V | 6.5 | 10 | 13 | µA |
| $V_{UDIM(EN,RISE)}$ | Undervoltage lockout rising threshold | $V_{UDIM}$ rising | | 1.22 | 1.27 | V |
| $V_{UDIM(EN,FALL)}$ | Undervoltage lockout falling threshold | $V_{UDIM}$ falling | 1.075 | 1.120 | | V |
| $t_{UDIM(RISE)}$ | UDIM to SW pin rising delay | | | 1200 | | ns |
| $t_{UDIM(FALL)}$ | UDIM pin SW pin falling delay | | | 105 | | ns |
| **DUTY CYCLE LIMIT** | | | | | | |
| $R_{PLMT(PU)}$ | PLMT Pull-Up Resistor | | 19.2 | 22.7 | 28.3 | kΩ |
| $R_{PLMT(PD)}$ | PLMT Pull-Down Resistor | | 75.0 | 91.8 | 110.0 | kΩ |
| $R_{PLMT(DIS)}$ | PLMT Discharge Resistor | | | 48 | | Ω |
| $V_{PLMT(PK)}$ | PLMT Peak Voltage | | 2.340 | 2.439 | 2.540 | V |
| $V_{PLMT(VAL)}$ | PLMT Valley Voltage | | 786 | 819 | 851 | mV |
| **FAULT INDICATION (nFLT)** | | | | | | |
| $R_{(\overline{FLT})}$ | Fault pin pull-down resistance | $I_{FLT}$ = 20 mA | | 2.5 | 7 | Ω |
| $T_{OC}$ | Hiccup retry delay time | | | 5.5 | | ms |
| $T_{UC(BLANK)}$ | Undercurrent reporting blanking period | | | 20 | | µs |
| $I_{\overline{FLT}(LKG)}$ | Fault pin leakage current | | | | 100 | nA |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{SD}$ | Thermal shutdown threshold | | | 175 | | °C |
| $T_{SD(HYS)}$ | Thermal shutdown hysteresis | | | 15 | | °C |

## 5.6 Typical Characteristics

–40°C < $T_J$ < 150°C, $V_{IN}$ = 14 V, $V_{UDIM}$ = 5 V, $V_{IADJ}$ = 2.1V , $C_{VCC}$ = 2.2 µF, $C_{BST}$ = 1 nF, $C_{COMP}$ = 1 nF, $R_{CS}$ = 100 mΩ, $R_{ON}$ = 401 kΩ, , $C_{PLMT}$ = 680 nF, $f_{SW}$ = 200 kHz

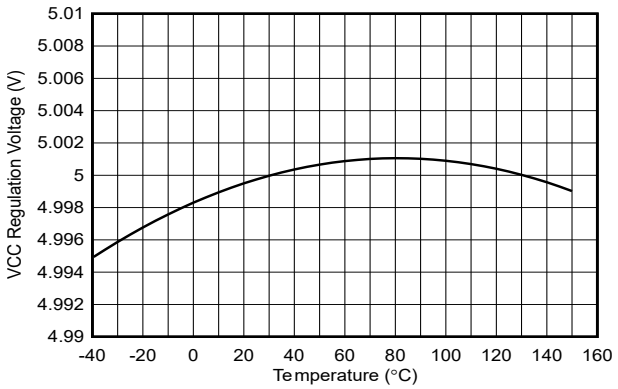



**Figure 5-1. VCC Regulation Voltage vs Temperature**

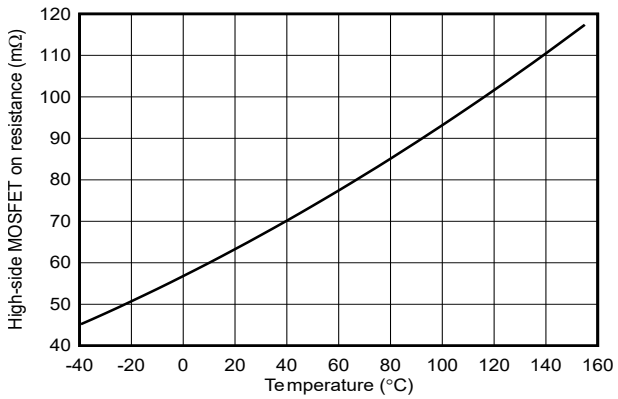



**Figure 5-2. High-Side MOSFET On Resistance vs Temperature**

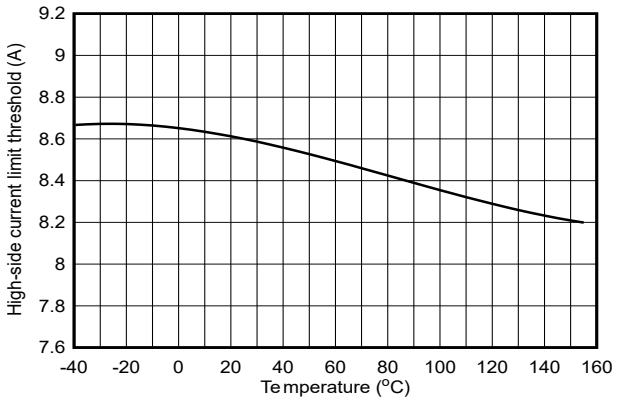



**Figure 5-3. High-Side Current Limit Threshold vs Temperature**

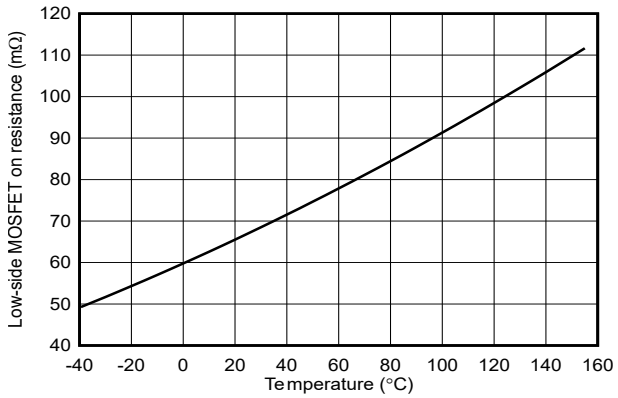



**Figure 5-4. Low-Side MOSFET On Resistance vs Temperature**

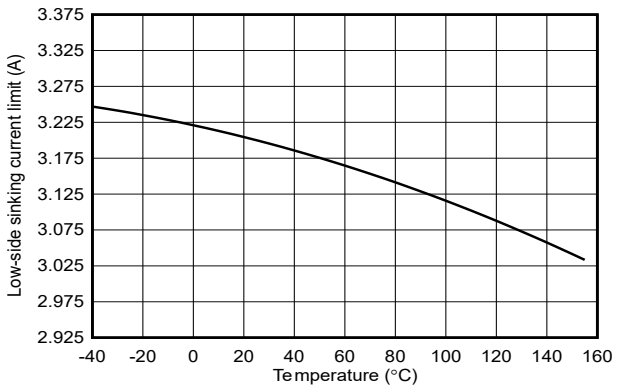



**Figure 5-5. Low-Side Sinking Current Limit vs Temperature**

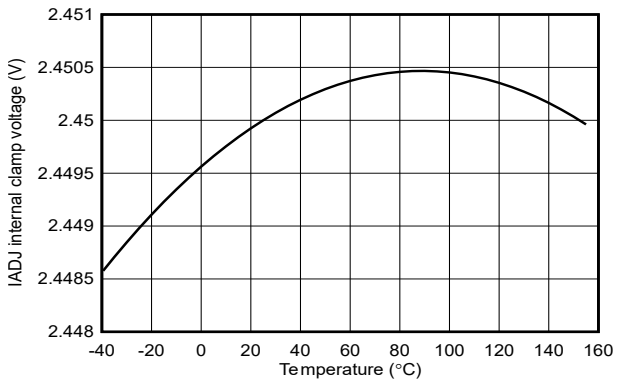



**Figure 5-6. IADJ Internal Clamp Voltage vs Temperature**

## 5.6 Typical Characteristics (continued)

–40°C < $T_J$ < 150°C, $V_{IN}$ = 14 V, $V_{UDIM}$ = 5 V, $V_{IADJ}$ = 2.1V , $C_{VCC}$ = 2.2 µF, $C_{BST}$ = 1 nF, $C_{COMP}$ = 1 nF, $R_{CS}$ = 100 mΩ, $R_{ON}$ = 401 kΩ, , $C_{PLMT}$ = 680 nF, $f_{SW}$ = 200 kHz

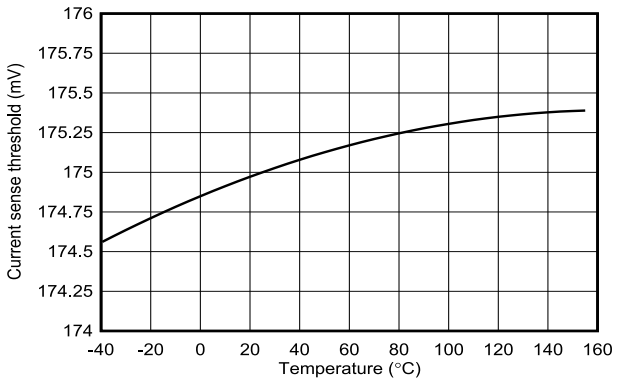



**Figure 5-7. $V_{(CSP-CSN)}$ Sense Threshold vs Temperature**

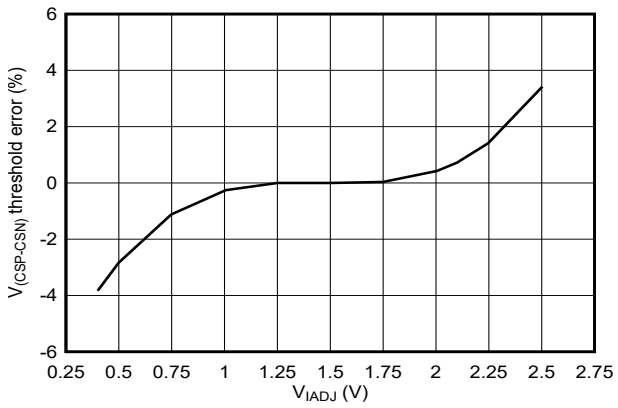



**Figure 5-8. $V_{(CSP-CSN)}$ Sense Error vs IADJ Setpoint**

# 6 Detailed Description

## 6.1 Overview

The TPS92642-Q1 is a wide input, synchronous buck LED driver. The device can deliver up to 5 A of continuous current and power a single string of one to 10 series-connected LEDs. The device implements an adaptive on-time current regulation control technique to achieve fast transient response. This architecture uses a comparator and a one-shot on-timer that varies inversely with input and output voltage to maintain a near-constant frequency. The integrated low offset rail-to-rail error amplifier enables closed-loop regulation of LED current and ensures better than 4% accuracy over a wide input, output, and temperature range. The LED current reference is set by the IADJ pin and is programmed by a voltage divider to achieve over a 15:1 linear analog dimming range. The high impedance IADJ input simplifies LED current binning and thermal protection.

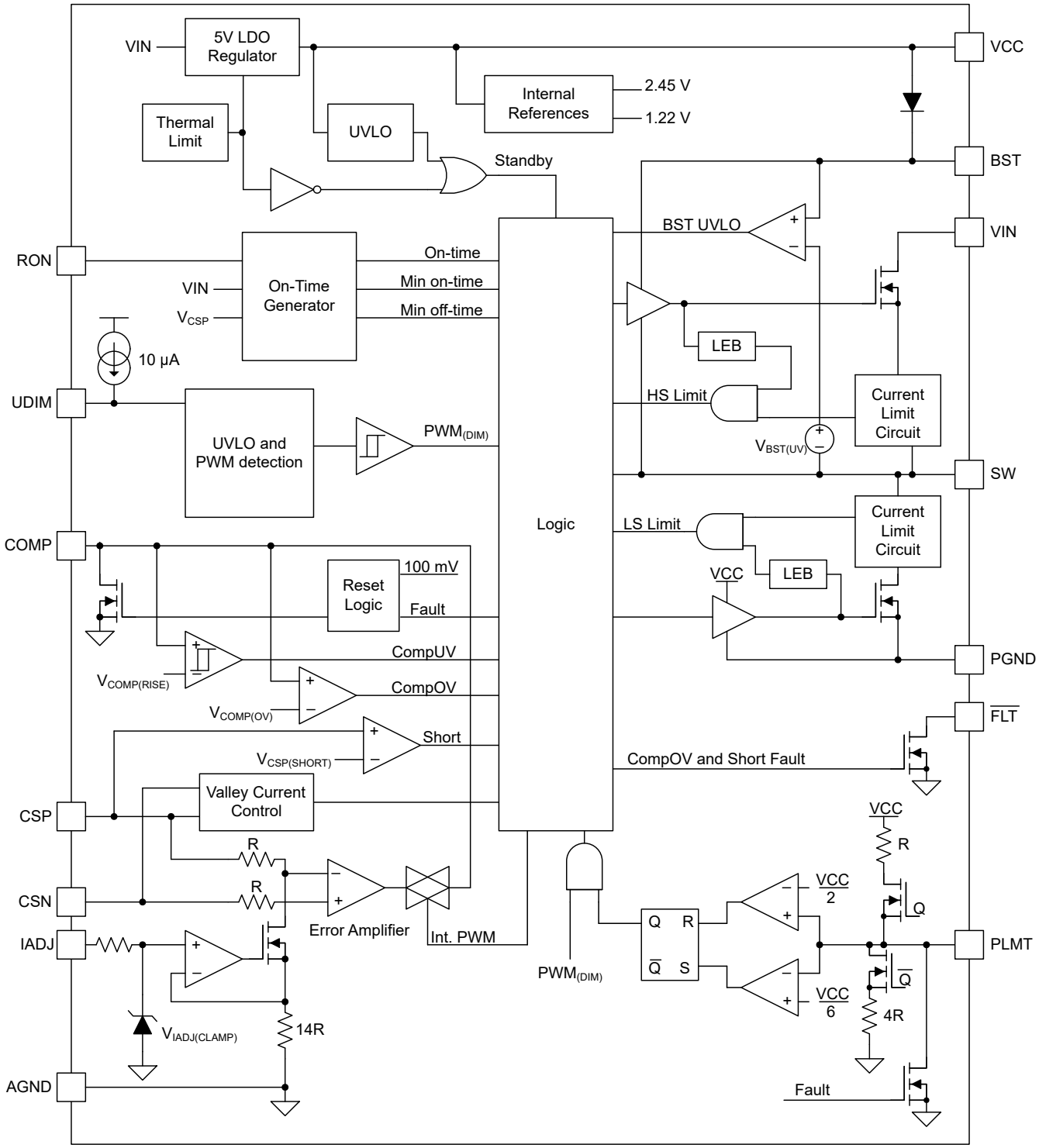
The TPS92642-Q1 device incorporates an internal pulse generator to implement a maximum LED pulse duty cycle limit. The maximum PWM duty cycle, $D_{PLMT}$, is internally fixed to 13.6% (typical) of the PWM period. This PWM period is set using external capacitor, $C_{PLMT}$, connected from the PLMT pin to GND. The LED current can be pulse width modulated by the external pulsed signal connected to the UDIM input for any duration less than the limit, $t_{PWM\_ON(LMT)}$, set by the internal pulse generator circuit. The maximum on-time, $t_{PWM_ON(LMT)}$is fixed at $D_{PLMT} \times t_{PLMT}$ where $t_{PLMT}$ is the period set by the external $C_{PLMT}$ capacitor. In addition, the internal pulse generator also behaves as a one-shot timer and blocks any subsequent UDIM pulses until the end of the period, $t_{PLMT}$. The internal pulse generator circuit and maximum duty cycle limit function can be disabled by connecting PLMT pin to GND. This device optimizes the inductor current response and is capable of responding to an input PWM signal with a minimum pulse width of 10 µs.

The device incorporates enhanced fault features, including the following:

- Cycle-by-cycle switch overcurrent limit
- Input undervoltage protection
- Boot undervoltage protection
- Comp overvoltage warning
- LED short-circuit indication

In addition, thermal shutdown (TSD) protection is implemented to limit the junction temperature at 175°C (typical).

## 6.2 Functional Block Diagram



## 6.3 Feature Description

### 6.3.1 Internal Regulator

The TPS92642-Q1 incorporates a 36-V rated linear regulator to generate the 5-V (typical) $V_{CC}$ bias supply and other internal reference voltages. The $V_{CC}$ output is monitored internally to by a UVLO circuit. Operation is enabled when $V_{CC}$ exceeds the $V_{CC(UVLO)}$ rising threshold and is disabled when $V_{CC}$ drops below $V_{CC(UVLO)}$ falling threshold. The comparator provides 200 mV of hysteresis to avoid chatter during transitions. The $V_{CC}$ UVLO thresholds are internally fixed and cannot be adjusted. An internal current limit circuit is implemented to protect the device during VCC pin short-circuit conditions. The $V_{CC}$ supply powers the internal circuitry, the low-side gate driver and the bootstrap supply for high-side gate driver. Place a bypass capacitor (4.7 µF to 10 µF) between VCC pin and AGND as close to the device as possible. The capacitor must be five times larger than the bootstrap capacitor, $C_{BST}$ to support proper operation. The regulator operates in dropout when input voltage, $V_{IN}$, falls below 5 V, forcing $V_{CC}$ to be lower than $V_{IN}$ by $V_{DO}$ for a 20-mA supply current. The $V_{CC}$ is a regulated output of the internal regulator and is not recommended to be driven from an external power supply.

### 6.3.2 Buck Converter Switching Operation

The following operating description of the TPS92642-Q1 refers to the *Functional Block Diagram* and the waveforms in Figure 6-1. The main control loop of the TPS92642-Q1 is based on an adaptive on-time pulse width modulation (PWM) technique that combines a constant on-time control with an inductor valley current sense circuit for pseudo-fixed frequency operation. This proprietary control technique enables closed-loop regulation of LED current and fast dynamic response necessary to meet the requirements for driver monitoring systems (DMS) using infrared and laser diodes.

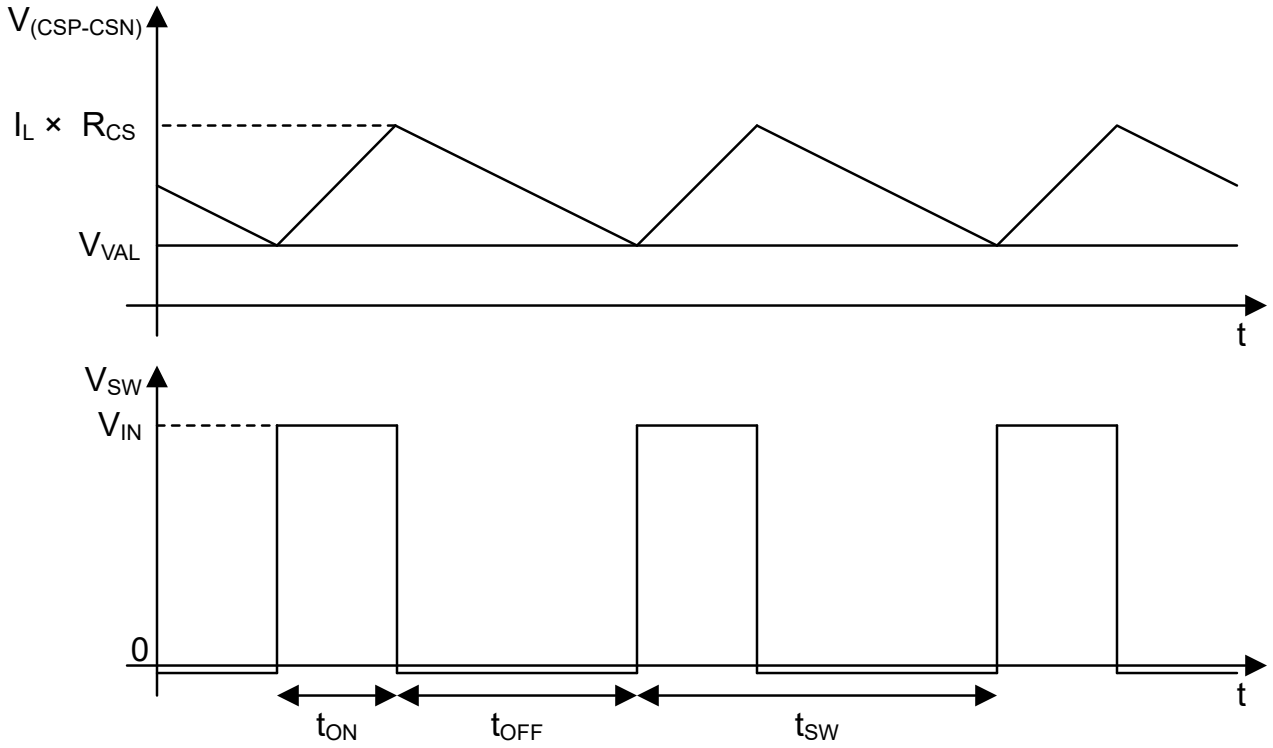



**Figure 6-1. Adaptive On-Time Buck Converter Waveforms**

In steady state, the high-side MOSFET is turned on at the beginning of each cycle. The on-time duration of this MOSFET is controlled by an internal one-shot timer and the high-side MOSFET is turned off after the timer expires. The one-shot timer duration is set by the output voltage measured at the CSP pin, $V_{CSP}$, and the input voltage measured at the VIN pin, $V_{IN}$, to maintain a pseudo-fixed frequency. During the on-time interval, the inductor current increases with a slope proportional to the voltage applied across its terminals ($V_{IN} – V_{CSP}$).

The low-side MOSFET is turned on after a fixed dead time and the inductor current then decreases with the constant slope proportional to the output voltage, $V_{CSP}$. Inductor current measured by the external sense resistor is compared to the valley threshold, $V_{VAL}$, by an internal high-speed comparator. This MOSFET is turned off and the one-shot timer is initiated when the sensed inductor current falls below the valley threshold voltage. The high-side MOSFET is turned on again after a fixed dead time.

The internal rail-to-rail error amplifier sets the valley threshold voltage and regulates the average inductor current based on a reference value set by $V_{IADJ}$ pin. A simple integral loop compensation circuit consisting of a capacitor connected from the COMP pin to GND provides a stable and high-bandwidth response. As the inductor current is directly sensed by an external resistor, the device operation is not sensitive to the ESR of the output capacitors and is compatible with common multilayered ceramic capacitors (MLCC).

### *6.3.3 Bootstrap Supply*

The TPS92642-Q1 contains both high-side and low-side N-channel MOSFETs. The high-side gate driver works in conjunction with an internal bootstrap diode and an external bootstrap capacitor, $C_{BST}$. During the on-time of the low-side MOSFET, the SW pin voltage is approximately 0 V and $C_{BST}$ is charged from the VCC supply through the internal diode and external $R_{BST}$ resistor. TI recommends a 33-nF to 100-nF capacitor between the BST and SW pins.

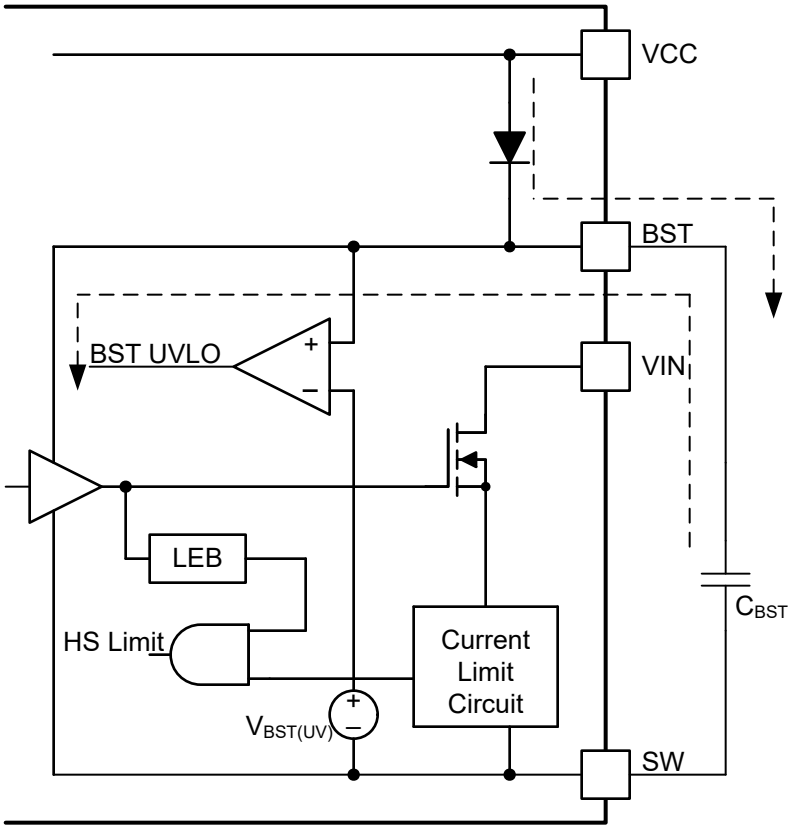



**Figure 6-2. Bootstrap Network**

### 6.3.4 Switching Frequency and Adaptive On-Time Control

The TPS92642-Q1 uses an adaptive on-time control scheme and does not have a dedicated on-board oscillator. The one-shot timer is programmed by the $R_{ON}$ resistor. The on-time is calculated internally using Equation 1 and is inversely proportional to the measured input voltage, $V_{IN}$, and directly proportional to the measured CSP voltage, $V_{CSP}$.

$$t_{ON} = 10 \times 10^{-12} \times R_{ON} \times \left(\frac{V_{CSP}}{V_{IN}}\right) \quad (1)$$

Given the duty ratio of the buck converter is $V_{CSP}/V_{IN}$, the switching period, $T_{SW}$, remains nearly constant over different operating points. Use Equation 2 to calculate the switching period.

$$T_{SW} = t_{ON} \times \left(\frac{V_{IN}}{V_{CSP}}\right) = 10 \times 10^{-12} \times R_{ON} \quad (2)$$

The switching frequency is calculated internally using Equation 3.

$$f_{SW} = \frac{1}{10 \times 10^{-12} \times R_{ON}} \quad (3)$$

The minimum or maximum duty cycle is limited to finite minimum on-time, $T_{ON(MIN)}$ and minimum off-time, $T_{OFF(MIN)}$, respectively. As on-time is constant, the frequency is also a dependent on the efficiency of the device, $\eta_{REG}$, excluding inductor and sense resistor losses.

$$f_{SW} = \frac{1}{10 \times 10^{-12} \times R_{ON} \times \eta_{REG}} \quad (4)$$

TI recommends a switching frequency setting between 100 kHz and 2.2 MHz.

### 6.3.5 Minimum On-Time, Off-Time, and Inductor Ripple

Buck converter operation is impacted by minimum on-time, minimum off-time, and minimum peak-to-peak inductor ripple limitations. The converter reaches the minimum on-time of 96 ns (typical) when operating with high input voltage and low-output voltage. In this control scheme, the off-time continues to increase and the switching frequency reduces to regulate the inductor current and LED current to the desired value.

$$f_{SW(MIN)} = \frac{V_{OUT(MIN)}}{T_{ON(MIN)} \times V_{IN(MAX)}}; t_{ON} = t_{ON(MIN)} \quad (5)$$

The converter reaches the minimum off-time of 91 ns (typical) when operating in dropout (low input voltage and high output voltage). As the on-time and off-time are fixed, the duty cycle is constant and the buck converter operates in open-loop mode. The inductor current and LED current are not in regulation.

The behavior and response of valley comparator is dependent on sensed peak-to-peak voltage ripple, $\Delta V_{(CSP-CSN)}$, and is a function of current sense resistor, $R_{CS}$, and peak-to-peak inductor current ripple, $\Delta i_{L(PK-PK)}$. To ensure periodic switching, the sensed peak-to-peak ripple must exceed the minimum value. At high (near 100%) or low (near 0%) duty cycles, the inductor current ripple may not be sufficient to ensure periodic switching. Under such operating conditions, the converter transitions from periodic switching to a burst sequence, forcing multiple on-time and off-time cycles at a rate higher than the programmed frequency. Although the converter may not operate in a periodic manner, the closed-loop control continues regulating the average LED current with a larger ripple value corresponding to higher peak-to-peak inductor ripple. TI recommends choosing an inductor, output capacitor, and switching frequency to ensure minimum sensed peak-to-peak ripple voltage under nominal operating condition is greater than 8 mV. The *Application and Implementation* section summarizes the detailed design procedure.

### 6.3.6 LED Current Regulation and Error Amplifier

The reference voltage, $V_{IADJ}$, set by the $V_{IADJ}$ and is internally scaled by a gain factor of 1/14 through a resistor network. An internal rail-to-rail error amplifier generates an error signal proportional to the difference between the scaled reference voltage ($V_{IADJ}$ / 14) and the inductor current measured by the differential voltage drop between CSP and CSN, $V_{(CSP-CSN)}$. This error drives the COMP pin voltage, $V_{COMP}$, and directly controls the valley threshold of the inductor current. Zero average DC error and closed-loop regulation is achieved by implementing an integral compensation network consisting of a capacitor connected from the output of the error amplifier to GND. As a good starting point, TI recommends a capacitor value between 1 nF and 10 nF between the COMP pin and GND. The choice of compensation network must ensure a minimum of 60° of phase margin and 10 dB of gain margin.

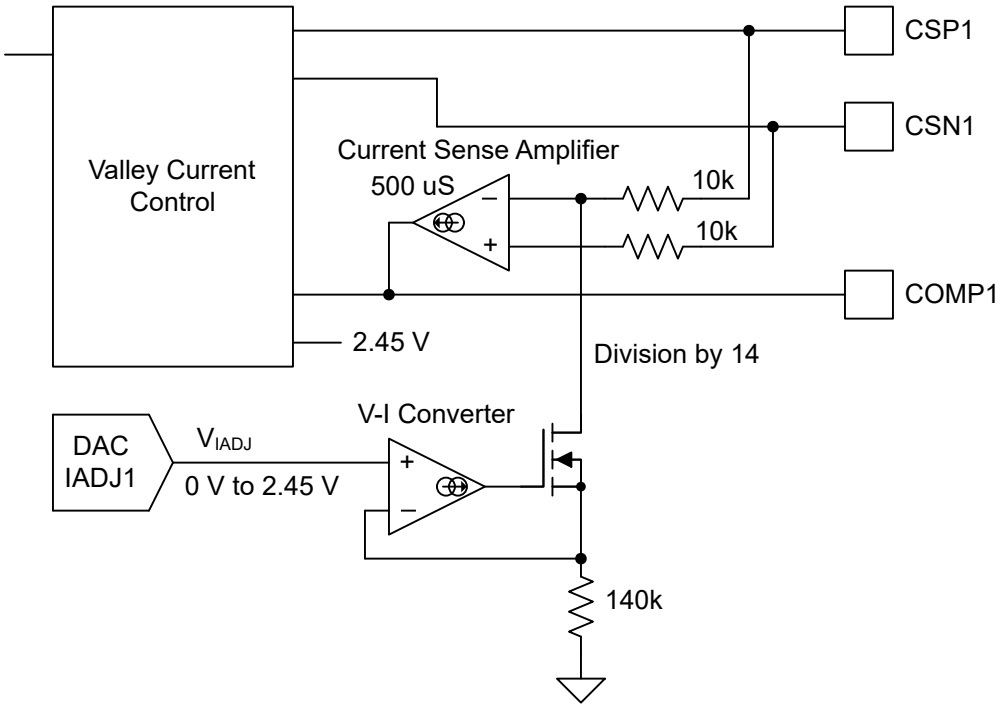



**Figure 6-3. Closed-Loop LED Current Regulation**

LED current is dependent on the current sense resistor, $R_{CS}$. Use Equation 17 to calculate the LED current.

TI recommends a Schottky diode connected from PGND to SW placed close to the device for LED current greater than 4-A and operating frequency is above 1-MHz. The diode reduces the impact of high frequency noise on PGND from impacting the valley detection circuit. The diode only conducts for a brief period of time and hence the impact on efficiency is negligible.

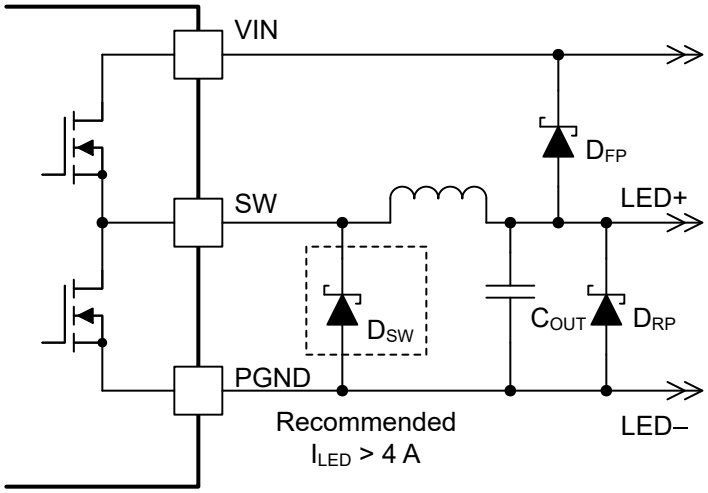



**Figure 6-4. Switch node Schottky diode connection**

LED current accuracy is a function of the tolerance of the external sense resistor, $R_{CS}$, and the variation in the sense threshold, $V_{(CSP-CSN)}$, caused by internal mismatch and temperature dependency of the analog components. The TPS92642-Q1 incorporates low offset rail-to-rail amplifiers, and is capable of achieving LED current accuracy of ±4% over common-mode range and a junction temperature range of –40°C to 150°C.

### 6.3.7 Start-Up Sequence

The start-up circuit allows the COMP pin voltage to gradually increase, thus reducing the LED current overshoot and current surges. The switching operation is initiated after the COMP pin voltage exceeds 2.45 V. A 440-mV hysteresis window allows the device to operate when COMP voltage is within the expected operating range of 2.2 V to 2.7 V. Switching is disabled on detection of low COMP voltage to avoid excessive negative inductor current.

The duration of soft start, $t_{ss}$, depends on the size of the compensation capacitor and the error amplifier source current, $I_{COMP(SRC)}$.

$$t_{SS} = \frac{2.45 \times C_{COMP}}{I_{COMP(SRC)}} \quad (6)$$

The source current, $I_{COMP(SRC)}$ is a function of the transconductance, $g_M$, of the error amplifier and error generated between the reference and the current sensed voltage.

$$I_{COMP(SRC)} = g_M \times \left(\frac{V_{IADJ}}{14} - V_{(CSP-CSN)}\right) \quad (7)$$

With no current flowing through the LEDs, the soft start duration depends on the choice of compensation capacitor, $C_{COMP}$, and the reference voltage, $V_{IADJ}$.

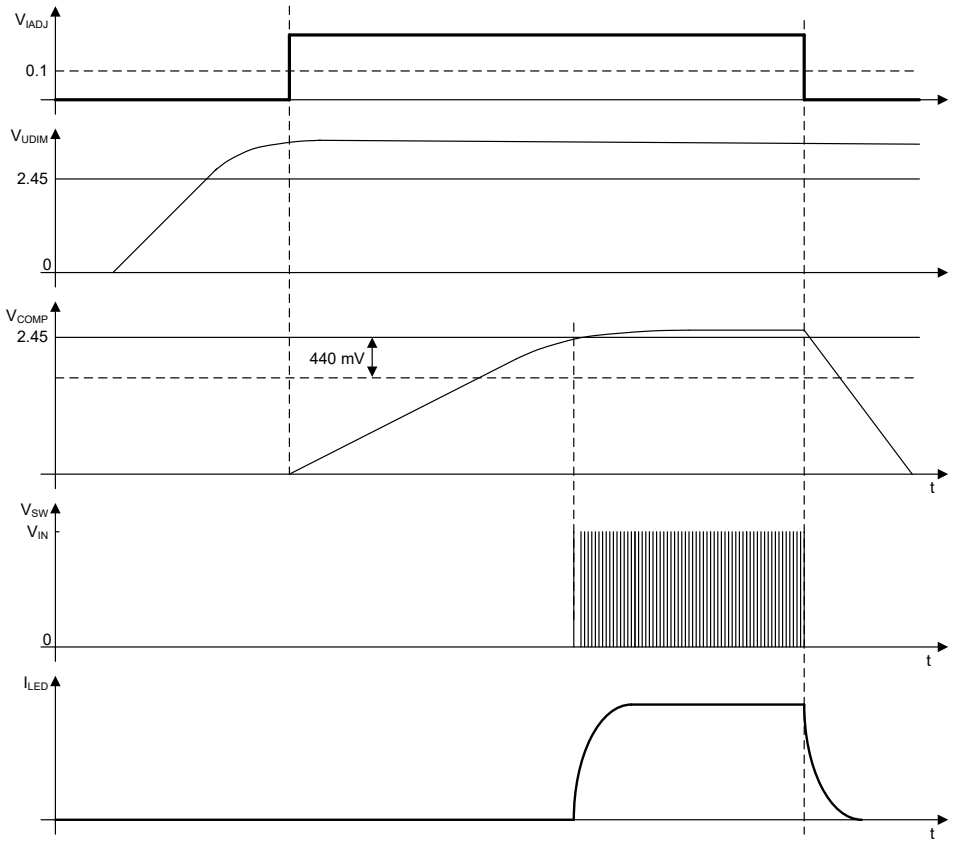



**Figure 6-5. Soft-Start Sequence**

The open drain fault indicator, $\overline{FLT}$, is set low when the COMP voltage deviates from the nominal range and exceeds $V_{COMP(OV)}$ threshold. This setting indicates a fault condition where the converter is operating in open-loop and the LED current is out of regulation. The device can be disabled by setting IADJ input below 100 mV or controlling the UDIM input.

### 6.3.8 Analog Dimming and Forced Continuous Conduction Mode

Analog dimming is accomplished by the voltage on IADJ pin, $V_{IADJ}$. The TPS92642-Q1 improves the linear range of analog dimming by supporting forced continuous conduction mode of operation. With synchronous MOSFETs, the inductor current is allowed to go negative for part of the switching cycle, thus enabling linear dimming with over 15:1 dimming range. TI recommends a 10-nF capacitor from IADJ pin to AGND pin to improve noise sensitivity.

### 6.3.9 External PWM Dimming and Input Undervoltage Lockout (UVLO)

The UDIM pin is a multifunction input that features an accurate input voltage detection based on band-gap thresholds with programmable hysteresis as shown in Figure 6-6. This pin functions as the external PWM dimming input for the LEDs and monitors VIN to detect dropout and undervoltage conditions. When the rising pin voltage exceeds the 1.22-V threshold, 10 µA (typical) of current is driven out of the UDIM pin into the resistor divider providing programmable hysteresis. TI recommends a bypass capacitor value of 1 nF between the UDIM pin and GND to improve noise immunity.

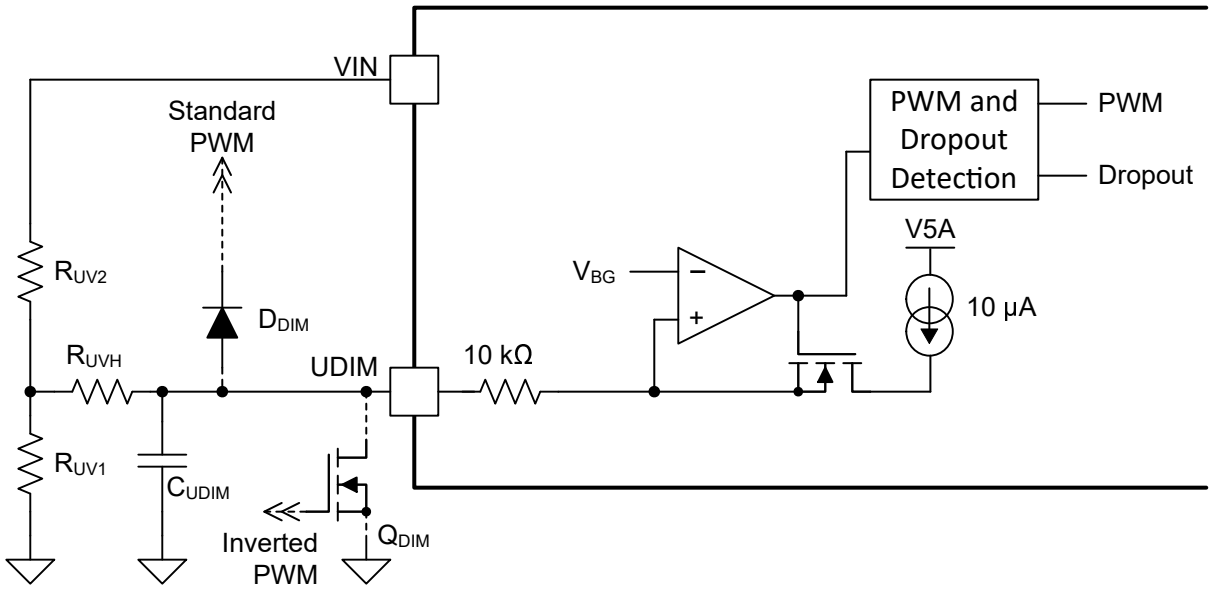



**Figure 6-6. External PWM Dimming**

The brightness of LEDs can be varied by modulating the duty cycle of the signal directly connected to the UDIM input. In addition, either an n-channel MOSFET or a Schottky diode can be used to couple an external PWM signal when using UDIM input in conjunction with UVLO functionality. With an n-channel MOSFET, the brightness is proportional to the negative duty cycle of the external PWM signal. With a Schottky diode, the brightness is proportional to the positive duty cycle of the external PWM signal.

Dropout and input undervoltage protection is achieved by connecting the resistor divider network from VIN to UDIM pin and UDIM pin to GND. Dropout protection is activated when UDIM pin voltage drops below $V_{UDIM(EN,\ FALL)}$ threshold. The minimum input voltage, below which drop protection is activated is programmed using Equation 8.

$$V_{IN(DO,FALL)} = V_{IN(DO,RISE)} - I_{UDIM(DO)} \times \left( R_{UV2} + \frac{\left(R_{UVH} + 10 \times 10^{3}\right) \times \left(R_{UV1} + R_{UV2}\right)}{R_{UV1}} \right) \quad (8)$$

$$V_{IN(DO,RISE)} = V_{UDIM(EN,RISE)} \times \frac{R_{UV1} + R_{UV2}}{R_{UV1}} \quad (9)$$

Additional hysteresis to internal 100 mV is programmed by connecting an external resistor, $R_{UVH}$ in series with UDIM pin. This connection allows the standard resistor divider to have smaller values, minimizing PWM delays.

Input undervoltage protection is triggered when UDIM pin voltage drops below $V_{UDIM(EN)}$ thresholds. The device responds to very low VIN voltage or to the external PWM input signal by disabling the error amplifier, disconnecting the COMP pin and tri-stating the switch node. With switch disabled, inductor current and the LED current drops to zero and the charge on the compensation network is maintained. On rising edge of PWM or when VIN exceeds the internal hysteresis of 100 mV, the converter resumes switching operation. The inductor current quickly ramps to the previous steady-state value.

### 6.3.10 Pulse Duty Cycle Limit Circuit

The TPS92642-Q1 features an internal analog circuit to impose a limit on the on-time, $t_{PWN(ON)}$ and off-time, $t_{PWM(OFF)}$, of the output current, $I_{LED}$. As illustrated in Figure 6-7, the device is controlled by external UDIM pulses with widths less than $t_{PWM\_ON(LMT)}$. Any external UDIM pulses that are longer than $t_{PWM(LMT)}$ are truncated to maintain a maximum fixed duty ratio of $D_{PLMT}$. The device also rejects any spurious pulses that can be present on the external UDIM input by blanking the UDIM signal during the PLMT off time. The off time is a function of the period, $t_{PLMT}$, set by the external capacitor, $C_{PLMT}$. This mechanism is designed to help limit overexposure to infrared lights due to error conditions in DMS applications. The relationship between $t_{PLMT}$, $t_{PWM\_ON(LMT)}$ and $D_{PLMT}$ is given in Equation 10.

$$t_{PWM\_ON(LMT)} = D_{PLMT} \times t_{PLMT} \quad (10)$$

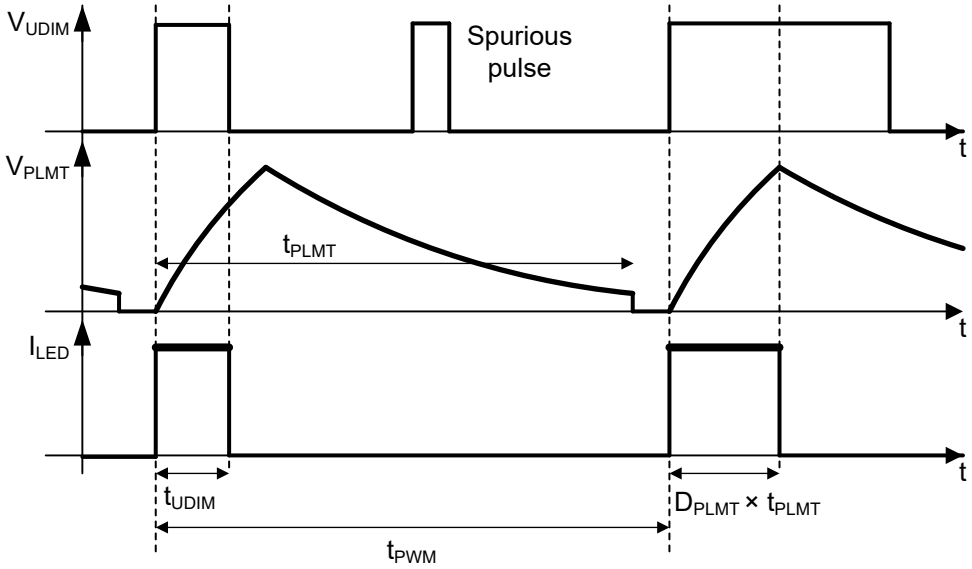



**Figure 6-7. Duty Cycle Limit Function Using Internal Pulse Generator**

The desired pulse period, $t_{PLMT}$, is set by external capacitor, $C_{PLMT}$.

$$t_{PLMT} = 1.168 \times 10^{5} \times C_{PLMT} \quad (11)$$

The maximum pulse on-duration, $t_{PWM\_ON(LMT)}$, and minimum off-duration, $t_{PWM\_OFF(LMT)}$, is given in Equation 12 and Equation 13.

$$t_{PWM\_ON(LMT)} = 0.6931 \times R_{PLMT(PU)} \times C_{PLMT} \quad (12)$$

$$t_{PW\backslash M\_OFF(LMT)} = 1.1 \times R_{PLMT(PD)} \times C_{PLMT} \quad (13)$$

For LED current set point greater than 2.5 A, the maximum pulse-duration is impacted due to the switching noise in the system. The maximum pulse-duration as a function of LED current is given in Equation 14. Because the off-duration, $t_{OFF}$, does not change, the duty cycle ratio reduces with increase in LED current.

$$t_{PWM\_ON(LMT)} = 0.6931 \times R_{PLMT(PU)} \times C_{PLMT} - 1.76 \times 10^{-2} \times (I_{LED} - 2.5) \times t_{PLMT} \quad (14)$$

As an alternative, the PLMT pin can be externally driven by an external pulse generator or microcontroller to set the maximum on-duration and minimum off-duration, independent of the external UDIM input. In this case, the circuit functionality remains unchanged, however ,the pulse parameters are set by external pulse signal driving PLMT pin. The relationship between external PLMT signal and UDIM signal is shown in the following figure.

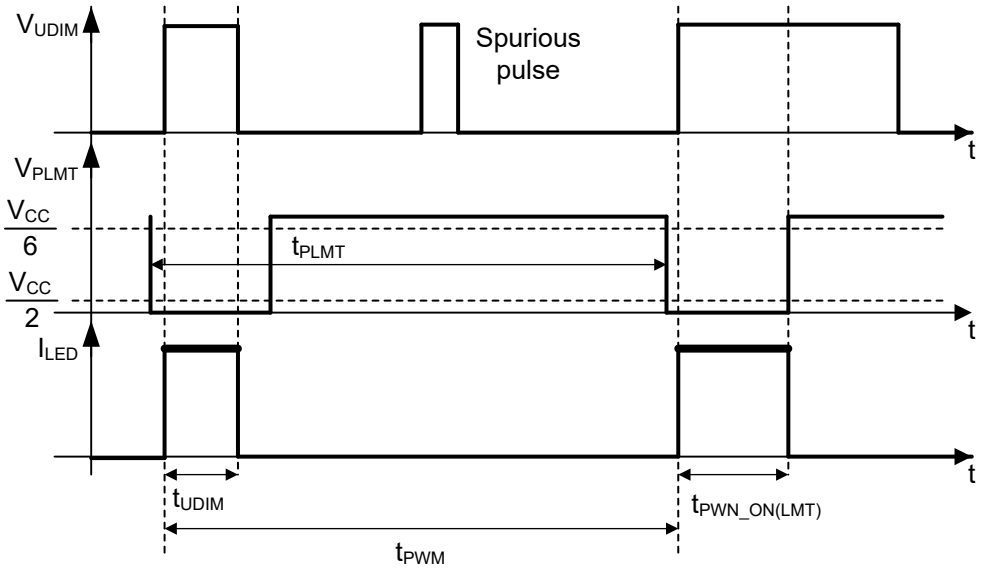



**Figure 6-8. Duty Cycle Limit Function Using External Pulse Generator**

The pulse duty cycle limit function is disabled by connecting PLMT pin to GND. The LED current is controlled directly by the PWM signal connected to UDIM input.

### 6.3.11 Output Short and Open-Circuit Faults

The TPS92642-Q1 monitors the CSN voltage to detect output short circuit faults. A short failure is indicated by open drain $\overline{FLT}$ output when the CSN voltage drops below 1.5 V (typical). The device continues to regulate current and operate without interruption in case of short circuit. A short-circuit fault does not impact the device behavior. The device continues to operate and regulate current without interruption.

An LED open-circuit fault ultimately causes the output voltage to increase and settle close to the input voltage. When this event occurs, the TPS92642-Q1 switching operation is then controlled by the fixed on-time and minimum off-time resulting in a duty cycle close to 100%. The COMP pin voltage exceeds the COMP overvoltage threshold, $V_{COMP(OV)}$, and the fault in indicated by $\overline{FLT}$ output. However, during open circuit, the dynamic behavior of the device and buck converter is influenced by the input voltage, $V_{IN}$, and the output capacitor, $C_{OUT}$, value. The device response to open circuit can be categorized into the following two distinct cases.

Case 1: For a Buck converter design with a small output capacitor, the switching operation in open load condition excites the tank resonance forcing the output voltage to oscillate. The frequency and amplitude of the oscillation are based on the resonant frequency and Q-factor of the second order tank network.

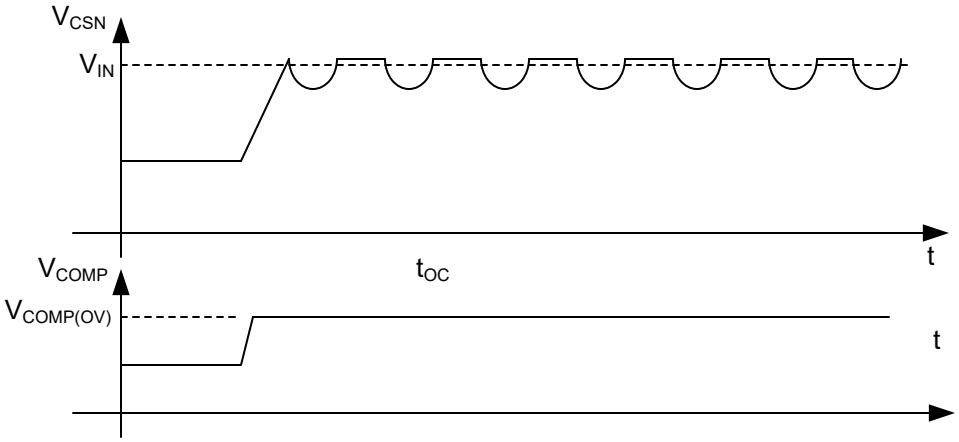



**Figure 6-9. Open-Circuit Condition with Output Voltage Oscillation**

Case 2: For a buck converter design with large output capacitor the inductor Q-factor and resonant frequency are much lower than the switching frequency. In this case, output voltage rises to input voltage and the converter continues to switch with minimum off-time.

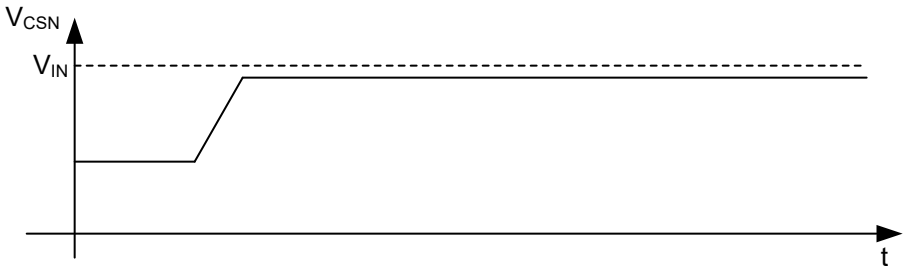



**Figure 6-10. Open-Circuit Condition with Minimum Off-Time Operation**

The voltage transient imposed on CSP and CSN inputs during short circuit and open circuit is dependent on the output capacitance and is influenced by the cable harness impedance. The inductance associated with a long cable harness resonates with the charge stored on the output capacitor and forces CSP and CSN voltage to ring above VIN and below ground. The magnitude of the voltage overshoot above VIN and below ground are dependent on the parasitic cable harness inductance and resistance.

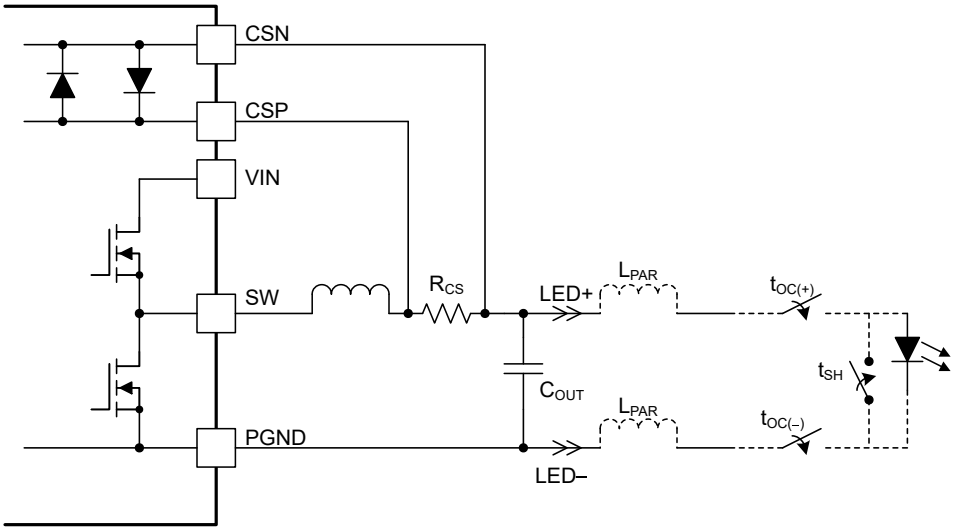



**Figure 6-11. Cable Harness Parasitic Inductance**

When using a long cable harness, TI recommends diodes to clamp the voltage across CSP and CSN input, as shown in Figure 6-12. TI recommends a low forward voltage Schottky diode or a fast recovery silicon diode with reverse blocking voltage rating greater than the maximum output voltage. The diode is required to be placed close to the output capacitor.

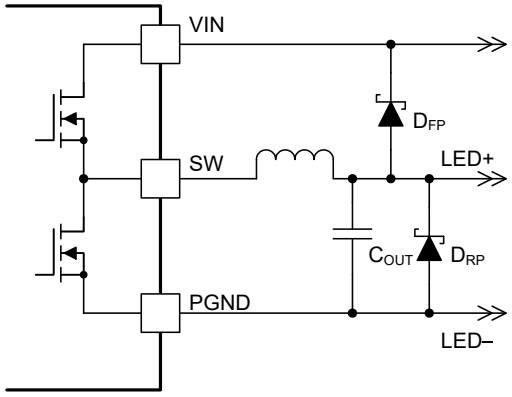



**Figure 6-12. Transient Protection Using an External Diode**

### 6.3.12 Overcurrent Protection

The device is protected from overcurrent conditions with cycle-by-cycle current limiting on both the high-side and the low-side MOSFETs.

The device turns off the high-side MOSFET and discharges the COMP capacitor when the drain current exceeds 7.7-A typical. The low-side switch is turned on to discharge the inductor current and output capacitor.

When the low-side switch is turned on, the switch current is also sensed and monitored. The device turns off both high-side and low-side MOSFETs and discharges the COMP capacitor when the drain current (from drain to PGND) exceeds 3.2-A typical.

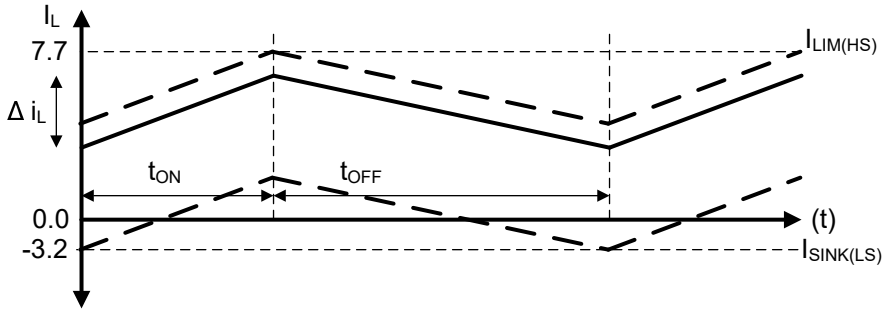



**Figure 6-13. Overcurrent Protection Thresholds**

The device employs hiccup mode overcurrent protection. In hiccup mode, the device shuts itself down and attempts to start after $T_{OC}$. Hiccup mode helps reduce the device power dissipation under severe overcurrent conditions.

### 6.3.13 Thermal Shutdown

Thermal shutdown prevents the device from extreme junction temperatures by turning off the internal switches when the IC junction temperature exceeds 175℃ (typical). Thermal shutdown does not trigger below 158℃. After thermal shutdown occurs, hysteresis prevents the device from switching until the junction temperature drops to approximately 160℃. When the junction temperature falls below 160℃ (typical), the device attempts to start up.

### 6.3.14 Fault Indicator and Diagnostics Summary

Table 6-1 summarizes the device behavior under fault conditions.

**Table 6-1. Fault Description**

| FAULT | DETECTION | DESCRIPTION |
|---|---|---|
| **Thermal protection** | $T_J$ > 175°C | The thermal protection is activated in the event the maximum MOSFET temperature exceeds the typical value of 175°C. This feature is designed to prevent overheating and damage to the internal switching MOSFETs. |
| **VCC undervoltage lockout** | $V_{CC(RISE)}$ < 4.4 V | The device enters the Undervoltage Lockout (UVLO). The switching operation is disabled, the COMP capacitor is discharged. |
| | $V_{CC(FALL)}$ < 4.2 V | |
| **VIN undervoltage lockout** | $V_{UDIM}$ < 1.12 V | The device disables switching operation for the corresponding channel. Switching is enabled when the input voltage rises above the turn-on threshold, $V_{IN(DO,RISE)}$ . |
| **BST undervoltage lockout** | $V_{BST(RISE)}$ < 3.4 V | The device turns off the high-side MOSFET and turns on the low-side MOSFET for the corresponding channel. Normal switching operation is resumed after the bootstrap voltage exceeds 3.2 V. |
| | $V_{BST(FALL)}$ < 3.2 V | |
| **COMP overvoltage** | $V_{COMP}$ > 3.2 V | The $\overline{FLT}$ flag is set low to indicate that the COMP voltage exceeded the normal operating range. This condition indicates output open-circuit fault. |
| **Short output** | $V_{CSN}$ < 1.5 V | The $\overline{FLT}$ flag is set low to indicate an output short-circuit condition based on sensed CSN voltage. |
| **High-side switch current limit** | $I_{HS}$ > 8.6 A | The device turns off the high-side MOSFET, turns on low-side MOSFET and discharges the COMP capacitor. The device attempts to restart after a delay of 5.5 ms. |
| **Low-side switch current limit** | $I_{LS}$ > 3.2 A | The device turns off both high-side and low-side MOSFETs and discharges the COMP capacitor. The device attempts to restart after a delay of 5.5 ms. |

Output open and short circuit faults force the $\overline{FLT}$ pin low when biased through an external resistor and connected to a 5-V supply. The $\overline{FLT}$ output can be used in conjunction with a microcontroller or system basis chip (SBC) as an interrupt and aid in fault diagnostics.

## 6.4 Device Functional Modes

This device has no additional functional modes.

# 7 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

Figure 7-1 shows a schematic of a typical application for the TPS92642-Q1.

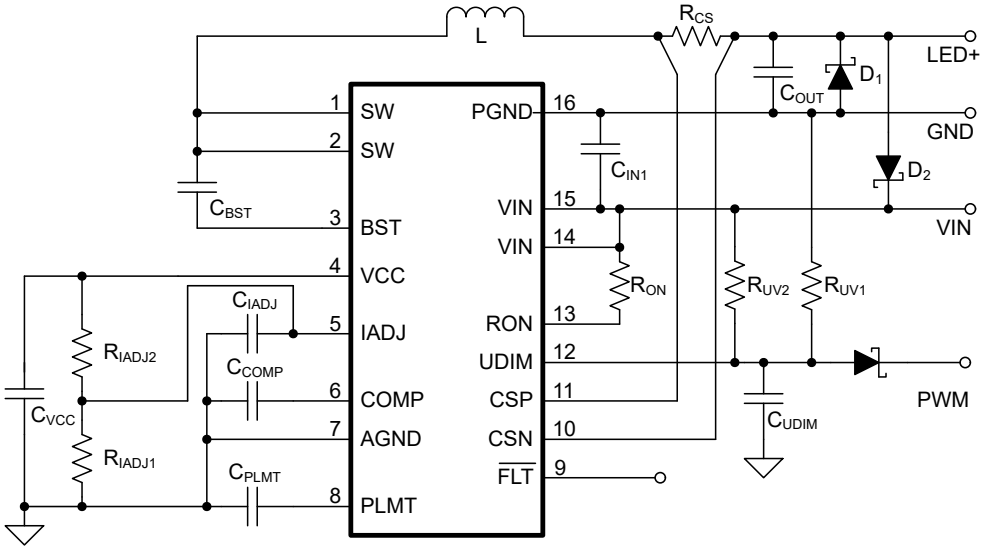



**Figure 7-1. Typical Application Schematic**

The TPS92642-Q1 controller is suitable for implementation of step-down LED driver topology. Use the following design procedure to select component values for the TPS92642-Q1 device. This section presents a simplified discussion of the design process for the Buck converter.

### 7.1.1 Duty Cycle Considerations

The switch duty cycle, D, defines the converter operation and is a function of the input and output voltages. In steady state, the duty cycle is defined using Equation 15:

$$D = \frac{V_{CSN}}{V_{IN}} \quad (15)$$

The buck converter maximum operating duty cycle, $D_{MAX}$, at minimum input voltage, $V_{IN,MIN}$ and maximum LED voltage, $V_{CSN,MAX}$.

$$D_{MAX} = \frac{V_{CSN,\,MAX}}{V_{IN,\,MIN}} \quad (16)$$

There is no limitation for small duty cycles, because at low duty cycles, the switching frequency is reduced as needed to always ensure current regulation. The maximum duty cycle attainable is limited by the minimum off-time duration and is a function of switching frequency.

### 7.1.2 Switching Frequency Selection

Nominal switching frequency is set by programming the $R_{ON}$ resistor. The switching varies slightly over operating range and temperature based on converter efficiency. Table 7-1 shows common switching frequencies and corresponding $R_{ON}$ resistor values.

**Table 7-1. Switching Frequency Setting**

| $R_{ON}$ (kΩ) | SWITCHING FREQUENCY (kHz) |
|---|---|
| 267 | 400 |
| 243 | 435 |
| 221 | 480 |
| 50 | 2000 |
| 44.2 | 2200 |

### 7.1.3 LED Current Programming

The LED current is set by the external current sense resistor, $R_{CS}$, and the analog adjust voltage, $V_{IADJ}$. The LED current can be programmed by varying $V_{IADJ}$ between 140 mV to 2.3 V. The LED current can be calculated using Equation 17:

$$I_{LED} = \frac{V_{IADJ}}{14 \times R_{CS}} \quad (17)$$

The LED current can be programmed by varying $V_{IADJ}$ between 140 mV and 2.3 V. TI recommends a 10-nF capacitor from IADJ pin to AGND pin to filter high frequency switching noise.

### 7.1.4 Inductor Selection

The inductor is sized to meet the ripple specification at maximum operating duty cycle. TI recommends a minimum sensed peak-to-peak voltage ripple ($\Delta V_{(CSP-CSN)}$) of 8 mV and typical voltage ripple of 20 mV to ensure periodic switching operation under.

$$\Delta V_{(CSP-CSN)} = \Delta i_L \times R_{CS} \quad (18)$$

Use Equation 19 to calculate the inductor value.

$$L = \frac{V_{IN,MIN} - V_{CSN,MAX}}{\Delta i_L \times f_{SW}} \times \frac{V_{CSN,MAX}}{V_{IN,MIN}} \quad (19)$$

The maximum inductor current ripple occurs at 50% duty cycle. Use Equation 20 to calculate the maximum peak-to-peak inductor current ripple, $\Delta i_{L(MAX)}$.

$$\Delta i_{L(MAX)} = \frac{V_{IN(TYP)}}{4 \times L \times f_{SW}} \quad (20)$$

Use Equation 21 and Equation 22 to calculate the RMS and peak currents through the inductor. Make sure that the inductor is rated to handle these currents.

$$i_{L(RMS)} = \sqrt{\left(I_{LED(MAX)}^2 + \frac{\Delta I_{L(MAX)}^2}{12}\right)} \quad (21)$$

$$i_{L(PK)} = I_{LED(MAX)} + \frac{\Delta i_{L(MAX)}}{2} \quad (22)$$

### 7.1.5 Output Capacitor Selection

The output capacitor value depends on the total series resistance of the LED string, $r_D$, and the switching frequency, $f_{SW}$. The capacitance required for the target LED ripple current, $\Delta i_{LED}$, is calculated using Equation 23.

$$C_{OUT} = \frac{\Delta i_{L(MAX)}}{8 \times f_{SW} \times r_D \times \Delta i_{LED}} \quad (23)$$

When choosing the output capacitors, consider the ESR and ESL characteristics because they directly impact the LED current ripple. Ceramic capacitors are the best choice due to the following:

- Low ESR
- High ripple current rating
- Long lifetime
- Good temperature performance

With ceramic capacitor technology, consider the derating factors associated with higher temperature and DC bias operating conditions. TI recommends an X7R dielectric with a voltage rating greater than maximum LED stack voltage.

### 7.1.6 Input Capacitor Selection

The input capacitor buffers the input voltage for transient events and decouples the converter from the supply. TI recommends a 10-µF input capacitor across the VIN pin and PGND placed close to the device, and connected using wide traces. X7R-rated ceramic capacitors are the best choice due to the low ESR, high ripple current rating, and good temperature performance.

In addition, a small case size 100-nF ceramic capacitor must be used across VIN to PGND, immediately adjacent to the device. This usage provides a high-frequency bypass for the control circuits internal to the device. These capacitors also suppress SW node ringing, which reduces the maximum voltage present on the SW node and EMI.

The capacitance can be increased to further limit the input voltage deviation during PWM dimming operation.

### 7.1.7 Bootstrap Capacitor Selection

The bootstrap capacitor biases the high-side gate driver during the high-side FET on-time. TI recommends that a 100-nF capacitor rated for 10 V or higher is used. The $V_{BSTI(UV)}$ threshold is designed to maintain proper high-side FET switching operation. If the $C_{BST}$ capacitor voltage drops below $V_{BST(UV)}$, then the device initiates a charging sequence, turning on the low-side FET before attempting to turn on the high-side FET. For a very low PWM frequency, the charging sequence is initiated on the rising edge of the PWM pulse. The duration of the low-side switch turn-on as a function of pulse width can be tuned by increasing the value of bootstrap capacitor, $C_{BSTI}$, depending on the application.

### 7.1.8 Compensation Capacitor Selection

TI recommends a simple integral compensator to achieve stable operation across the wide operating range. The buck converter behaves as a single pole system with additional phase lag caused by the switching behavior. The gain and phase margin are, consequently determined by the choice of the switching frequency and are independent of other design parameters. TI recommends a 1-nF to 10-nF capacitor to achieve bandwidth between 4 kHz and 40 kHz. The choice of compensation capacitor impacts the transient response and PWM dimming performance. TI recommends a larger compensation capacitor (lower bandwidth) to limit the LED current overshoot on the rising edge of internal or external PWM signal.

**Table 7-2. Compensation Capacitor Value**

| BANDWIDTH (kHz) | COMPENSATION CAPACITOR (nF) |
|---|---|
| 40 | 1 |
| 18 | 2.2 |
| 12 | 3.3 |
| 8.5 | 4.7 |
| 5.8 | 6.8 |
| 4.8 | 8.2 |
| 4 | 10 |

### 7.1.9 Input Dropout and Undervoltage Protection

Figure 7-1 shows that the undervoltage protection threshold is programmed using a resistor divider, $R_{UV1}$ and $R_{UV2}$, from the input voltage, $V_{IN}$ to PGND. Use Equation 24 and Equation 25 to calculate the resistor values.

$$R_{UV2} = \frac{V_{IN(DO,\,RISE)}}{I_{UDIM(DO)}} - \frac{V_{IN(DO,\,FALL)}}{I_{UDIM(DO)}} - 10 \times 10^{3} \quad (24)$$

$$R_{UV1} = \frac{V_{UDIM(EN,\,RISE)}}{V_{IN(DO,\,RISE)} - V_{UDIM(EN,\,RISE)}} \times R_{UV2} \quad (25)$$

A capacitor of 1 nF from UDIM pin to GND is placed close to device to improve noise immunity.

### 7.1.10 Pulse Duty Cycle Limit Circuit

The period of internal pulse generator ($t_{PLMT}$) is set by the $C_{PLMT}$ capacitor. The period, $t_{PLMT}$ defines the minimum repetition rate of LED current pulses allowed based on external UDIM signal and is set based on the maximum PWM frequency, $f_{PWM(MAX)}$. An additional margin in design is necessary to compensate for the component tolerances and noise in the system. The $t_{PLMT}$ period is determined using Equation 26.

$$t_{PLMT} = \frac{0.9}{f_{PWM(MAX)}} \quad (26)$$

The pulse limit capacitor, $C_{PLMT}$, capacitor is calculated using Equation 27.

$$C_{PLMT} = \frac{t_{PLMT}}{1.168 \times 10^5} \quad (27)$$

Table 7-3 summarizes the TI recommended pulse limit capacitor value for different PWM frequencies. A single capacitor or parallel combination of capacitors must be rated for 6.3 V or higher and with tolerance lower than 10%.

**Table 7-3. Pulse Limit Capacitor Value**

| PWM DIMMING FREQUENCY (Hz) | PLMT CAPACITOR (µF) |
|---|---|
| 30 | 0.25 |
| 50 | 0.15 |
| 60 | 0.12 |

### 7.1.11 Protection Diodes

External Schottky diodes are required to protect the CSP / CSN node by clamping the voltage during short circuit and open-circuit transients. The Schottky diode must be selected based on the length of the cable harness and the choice of output capacitor. TI recommends a Schottky diode with low forward voltage drop at room-temperature and non-repetitive peak surge current rating of 10 A for duration of 5 µs. The diodes from CSN to VIN and GND to CSN must be located close to the pin.

## 7.2 Typical Application

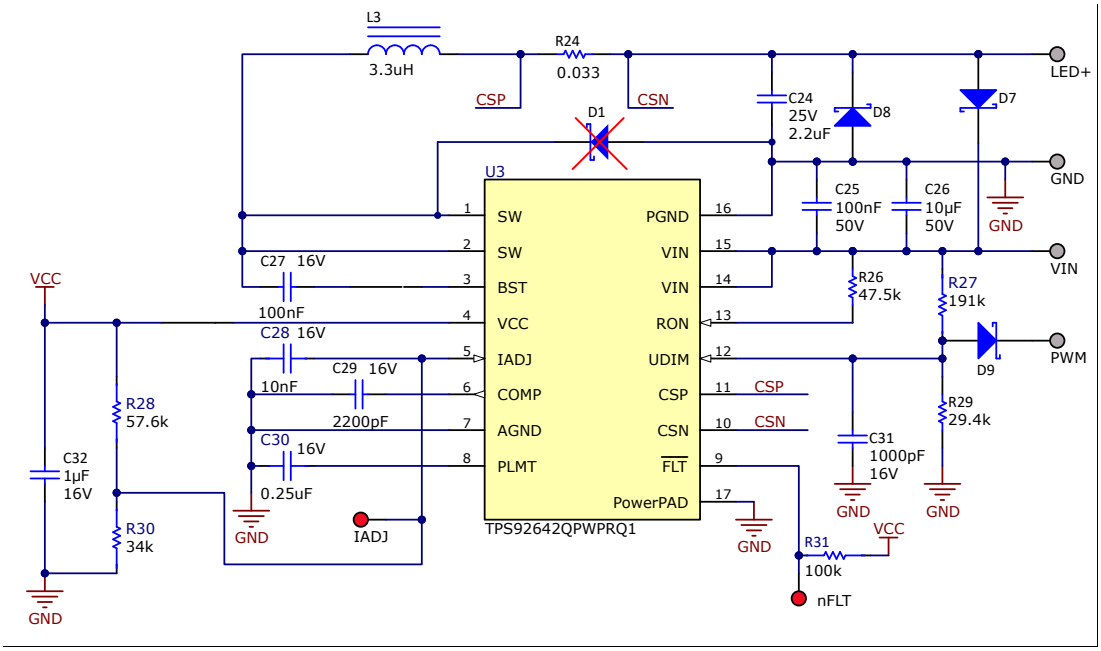



**Figure 7-2. Application Schematic**

### 7.2.1 Design Requirements

**Table 7-4. Design Parameters**

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | | 22 | 24 | 26 | V |
| $N_S$ | Number of LEDs | | | 2 | | |
| $V_{FLED}$ | LED forward voltage drop | | 3.5 | 4.2 | 5.0 | V |
| $r_D$ | LED string series resistance | $N \times r_{D(LED)}$ | 200 | | 500 | mΩ |
| $V_{CSN}$ | Output voltage | $Ns \times V_{FLED}$ | 7.0 | 8.4 | 10.0 | V |
| $I_{LED}$ | LED current | | 2500 | 4000 | 5000 | mA |
| $\Delta i_{LED}$ | LED current ripple | | | | 80 | mA |
| $\Delta V_{(CSP-CSN)}$ | Sensed voltage ripple | | | 20 | | mV |
| $V_{IN(DO,RISE)}$ | Start input voltage | Input voltage rising | | 9 | | V |
| $V_{IN(DO,FALL)}$ | Stop input voltage | Input voltage falling | | 7 | | V |
| $f_{PWM}$ | PWM frequency | | 29 | 30 | 31 | Hz |
| $D_{PWM}$ | PWM dimming duty cycle | Internaly fixed by pulse duty cycle circuit | | | 13.62 | % |
| $f_{SW}$ | Switching frequency | | | 2100 | | kHz |
| $T_A$ | Ambient temperature | | | 25 | | °C |

### 7.2.2 Detailed Design Procedure

#### 7.2.2.1 Calculating Duty Cycle

Solve for duty cycle D, $D_{MAX}$, and $D_{MIN}$:

$$D_{MAX} = \frac{V_{CSN(MAX)}}{V_{IN(MIN)}} = \frac{10}{22} = 0.4545 \quad (28)$$

$$D_{MIN} = \frac{V_{CSN(MIN)}}{V_{IN(MAX)}} = \frac{7}{26} = 0.2692 \quad (29)$$

#### 7.2.2.2 Calculating Minimum On-Time and Off-Time

Solve for minimum on-time, $t_{ON(DMIN)}$, at minimum duty cycle and minimum off-time, $t_{OFF(DMAX)}$, at maximum duty cycle:

$$t_{ON(DMAX)} = \frac{V_{CSN(MAX)}}{V_{IN(MIN)}} \times \frac{1}{f_{sw}} = \frac{10}{22} \times \frac{1}{2100 \times 10^3} = 216 \text{ ns} \quad (30)$$

$$t_{ON(DMIN)} = \frac{V_{CSN(MIN)}}{V_{IN(MAX)}} \times \frac{1}{f_{sw}} = \frac{7}{26} \times \frac{1}{2100 \times 10^3} = 128 \text{ ns} \quad (31)$$

#### 7.2.2.3 Minimum Switching Frequency

Confirm minimum switching frequency at $t_{ON(DMIN)}$, $f_{SW(MIN)}$:

$$f_{sw(MIN)} = \frac{V_{CSN(MIN)}}{t_{ON(DMIN)} \times V_{IN(MAX)}} = \frac{7}{128 \times 10^{-9} \times 26} = 2100 \text{ kHz} \quad (32)$$

For the design specification, $t_{ON(DMIN)} > t_{ON(MIN)}$ and $f_{SW(MIN)} = f_{SW}$.

#### 7.2.2.4 LED Current Set Point

Solve for sense resistor, $R_{CS}$:

$$R_{CS} = \frac{V_{IADJ(MAX)}}{14 \times I_{LED(MAX)}} = \frac{2.3}{14 \times 5} = 0.0329 \quad (33)$$

A standard resistor of 33 mΩ with tolerance better than 1% and low temperature coefficient is selected. The power dissipated in $R_{CS}$ is calculated:

$$P_{sense} = D_{PLMT} \times R_{CS} \times I^2_{LED(MAX)} = 0.1362 \times 0.033 \times 5^2 = 0.1124 \text{ W} \quad (34)$$

A resistor with rated power of 250 mW and above must be selected.

A resistor divider network, with standard values 57.6 kΩ and 34 kΩ, from VCC pin to GND sets the nominal LED current reference voltage of 1.856 V. A 10-nF capacitor from IADJ pin to AGND pin is included to filter high frequency switching noise.

#### 7.2.2.5 Inductor Selection

The inductor is selected to meet the recommended peak-to-peak voltage ripple, $\Delta V_{(CSP-CSN)}$ of 20 mV:

$$L = \frac{V_{IN,MIN} - V_{CSN,MAX}}{\Delta i_L \times f_{SW}} \times \frac{V_{CSN,MAX}}{V_{IN,MIN}} = \frac{22 - 10}{800 \times 10^{-3} \times 2100 \times 10^{3}} \times \frac{10}{22} = 3.247 \times 10^{-6} \quad (35)$$

The closest standard capacitor is 3.3 µH.

- Lower inductor values increase the peak-to-peak inductor current, which minimizes size and cost at the expense of reduced efficiency and larger output capacitor.
- Higher inductance values decrease the peak-to-peak inductor current, which increases efficiency but reduces the operating range based on minimum sense voltage ripple, $\Delta V_{(CSP-CSN)}$ specification.

#### 7.2.2.6 Output Capacitor Selection

The minimum output capacitance is selected to meet the LED current ripple specification:

$$C_{OUT} = \frac{\Delta i_{L(MAX)}}{8 \times f_{SW} \times r_{D(MAX)} \times \Delta i_{LED}} = \frac{0.608}{8 \times 2100 \times 10^{3} \times 0.5 \times 80 \times 10^{-3}} = 2.261 \times 10^{-6} \quad (36)$$

A standard 2.2-µF, 25-V X7R capacitor is selected.

#### 7.2.2.7 Bootstrap Capacitor Selection

A standard 0.1-µF, 16-V X7R capacitor is selected to support 2100-kHz switching frequency.

#### 7.2.2.8 Compensation Capacitor Selection

A compensation capacitor of 2.2 nF is selected to achieve balanced transient response between PWM dimming and shunt FET dimming.

#### 7.2.2.9 VIN Dropout Protection and PWM Dimming

The resistor divider, $R_{UV1}$ and $R_{UV2}$, is set to meet $V_{IN(UVLO,RISE)}$ and $V_{IN(DO,FALL)}$ thresholds.

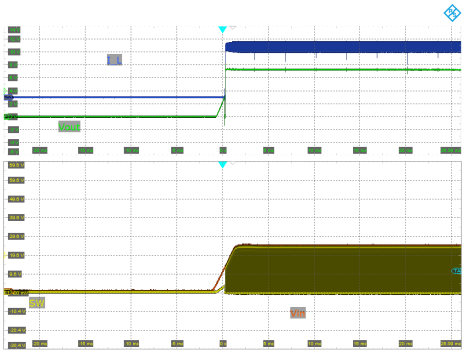
$$R_{UV2} = \frac{9}{10 \times 10^{-6}} - \frac{7}{10 \times 10^{-6}} - 10 \times 10^{3} = 190 \times 10^{3} \quad (37)$$

$$R_{UV1} = \frac{1.22}{9 - 1.22} \times 190 \times 10^{3} = 29.8 \times 10^{3} \quad (38)$$

A standard value resistors of 191 kΩ and 29.4 kΩ are selected for $R_{UV2}$ and $R_{UV1}$, respectively.

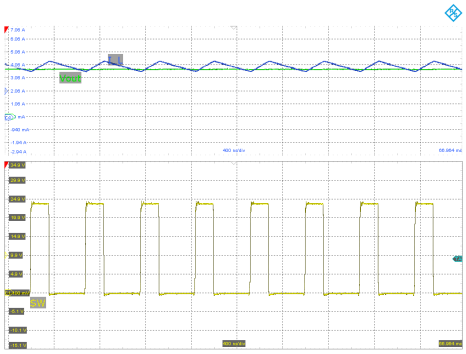
The external PWM dimming is achieved by controlling UDIM input. The device modulates the LED current based on the PWM duty cycle of the external signal, coupled through external diode.

### 7.2.3 Application Curves



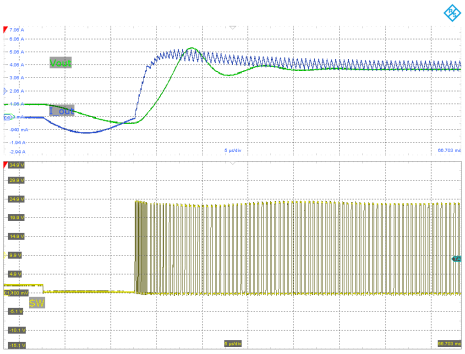
Ch1: SW voltage (10 V/div); Ch2: Output voltage (1 V/div); Ch3: Inductor current (1 A/div); Ch4: VIN voltage (10 V/div); Time: 5 ms/div

**Figure 7-3. Start-up Transient**



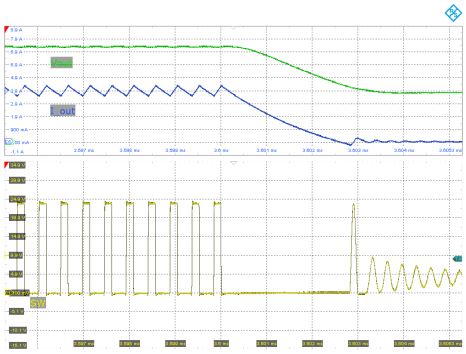
Ch1: SW voltage (5 V/div); Ch2: Output voltage (2 V/div); Ch3: LED current (1 A/div); Time: 400 ns/div

**Figure 7-4. Normal Operation**



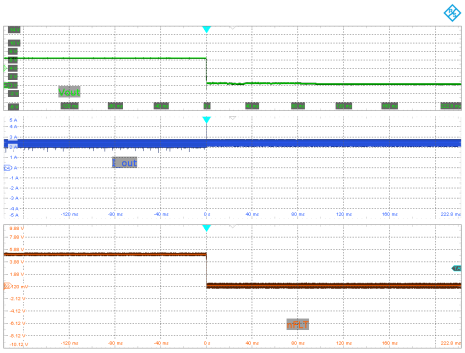
Ch1: SW voltage (5 V/div); Ch2: Output voltage (2 V/div); Ch3: Inductor current (1 A/div); Time: 5 µs/div

**Figure 7-5. PWM Dimming (Rising Edge)**



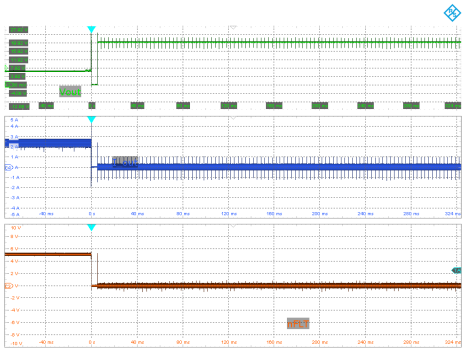
Ch1: SW voltage (5 V/div); Ch2: Output voltage (2 V/div); Ch3: Inductor current (1 A/div); Time: 1 µs/div

**Figure 7-6. PWM Dimming (Falling Edge)**



Ch2: Output voltage (4 V/div); Ch3: LED current (1 A/div); Ch4: $\overline{FLT}$ voltage (2 V/div); Time: 40 ms/div

**Figure 7-7. Output Short-Circuit Fault**



Ch2: Output voltage (4 V/div); Ch3: LED current (1 A/div); Ch4: $\overline{FLT}$ voltage (2 V/div); Time: 40 ms/div

**Figure 7-8. Output Open-Circuit Fault**

## 7.3 Power Supply Recommendations

The characteristics of the input supply must be compatible with *Absolute Maximum Ratings* and *Recommended Operating Conditions* in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded converter.

If the converter is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the converter. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an under-damped resonant circuit, resulting in overvoltage transients at the input to the converter or tripping UVLO. Additional bulk capacitance or an input filter can be required in addition to the ceramic bypass capacitors to address converter stability, noise, and EMI concerns.

## 7.4 Layout

### *7.4.1 Layout Guidelines*

The performance of any switching converter depends as much on the layout of the PCB as the component selection. The following guidelines can help design a PCB with the best power converter performance.

- Place ceramic high-frequency bypass capacitors as close as possible to the TPS92642-Q1 VIN and PGND pins. Grounding for both the input and output capacitors must consist of localized top side planes that connect to the PGND pin.
- Place bypass capacitors for VCC close to the pins and ground the capacitors to device ground.
- Use wide traces for the $C_{BST}$ capacitor and $R_{BST}$ resistor. Place $R_{BST}$ and $C_{BST}$ network as close as possible to BST pin and SW pin.
- Differentially route the CSP and CSN pins to sense resistor. Route the traces away from noisy nodes, preferably through a layer on the other side of a shielding/ground layer.
- Use ground plane in one of the middle layers for noise shielding.
- Make VIN and ground connection as wide as possible. This action reduces any voltage drops on the input of the converter and maximizes efficiency.
- Keep switch area small. Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time, the total area of this node must be minimized to help reduce radiated EMI.

#### 7.4.1.1 Compact Layout for EMI Reduction

Radiated EMI is generated by the high di/dt from pulsing currents in switching converters. The larger the area covered by the path of a pulsing current, the more electromagnetic emission is generated. The key to minimize radiated EMI is to identify the pulsing current path and minimize the area of the path. In buck converters, the pulsing current path is from the VIN side of the input capacitors through the HS switch, through the LS switch, and then returns to the ground of the input capacitor.

High-frequency ceramic bypass capacitors at the input side provide primary path for the high di/dt components of the pulsing current. Placing ceramic capacitors as close as possible to the VIN and PGND pins is the key to EMI reduction.

The PCB copper connection of the SW pin to the inductor must be as short as possible and just wide enough to carry the LED current without excessive heating. Short, thick traces or, copper pours (shapes), must be used for high current conduction path to minimize parasitic resistance. Place the output capacitor close to the CSN pin and grounded closely to the PGND pin.

##### *7.4.1.1.1 Ground Plane*

TI recommends using one of the middle layers as a solid ground plane. The ground plane provides shielding for sensitive circuits and traces. the ground plane also provides a quiet reference potential for the control circuitry. Connect the GND, AGND and PGND pins to the ground plane using via right next to the bypass capacitors. PGND pins are connected to the source of the internal LS switch. They must be connected directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce due to load variations.

### 7.4.2 Layout Example

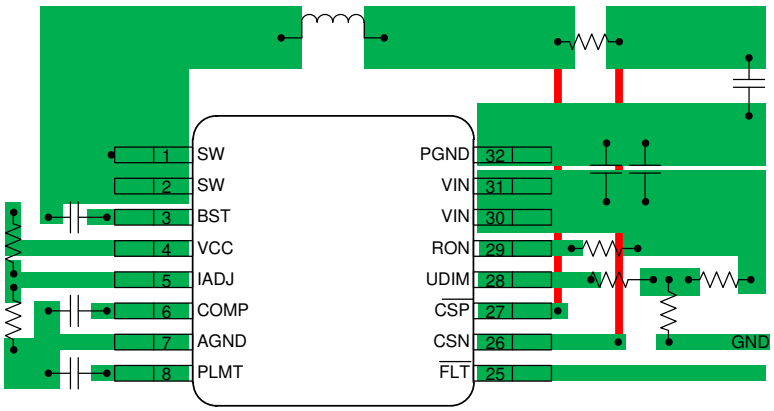



**Figure 7-9. TPS92642-Q1 Layout Example**

# 8 Device and Documentation Support

## 8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 9 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| November 2023 | * | Initial release |

## 10 Mechanical, Packaging, and Orderable Information

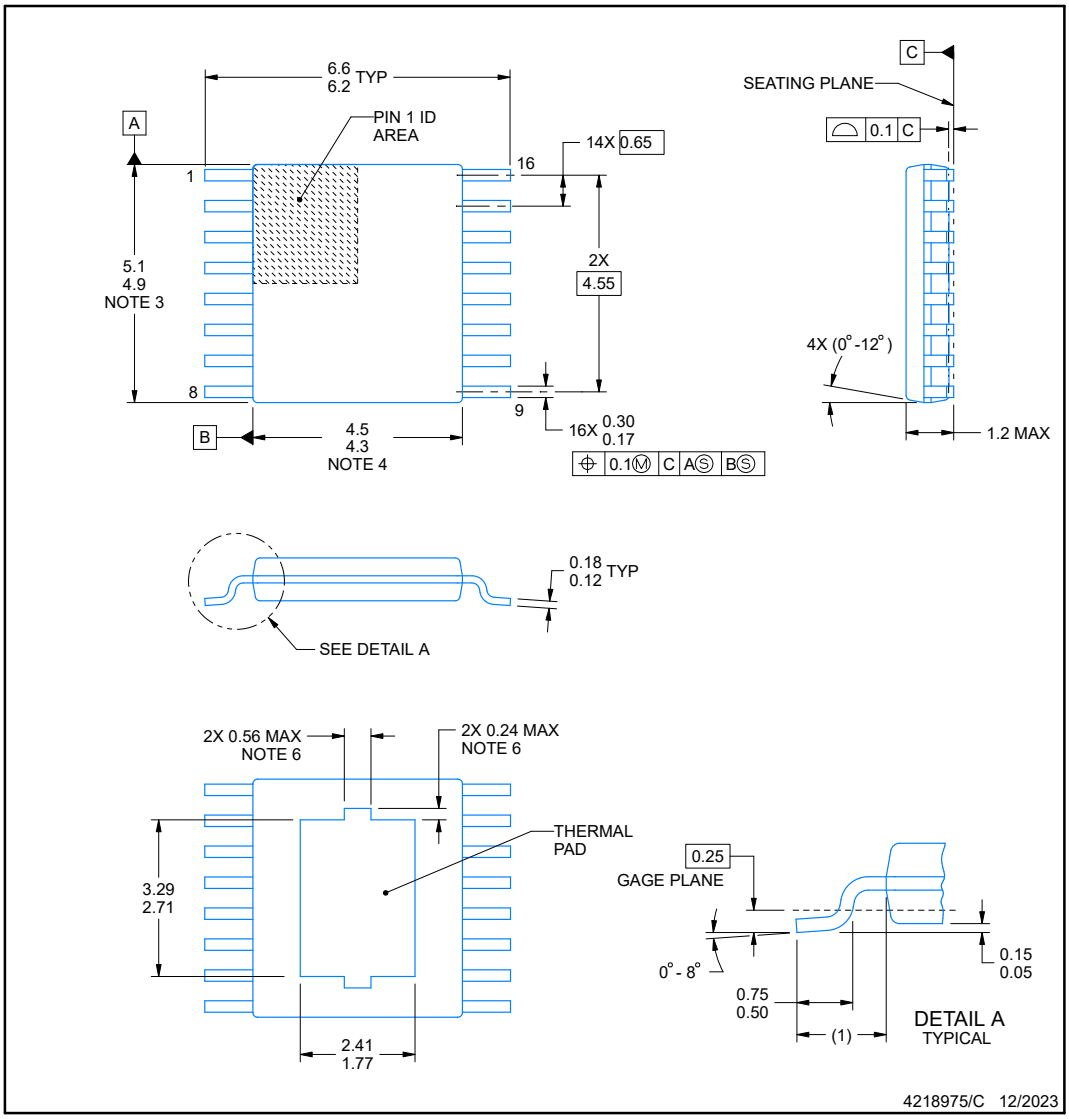
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

# PACKAGE OUTLINE

## PWP0016G

## PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE




PowerPAD is a trademark of Texas Instruments.

NOTES:

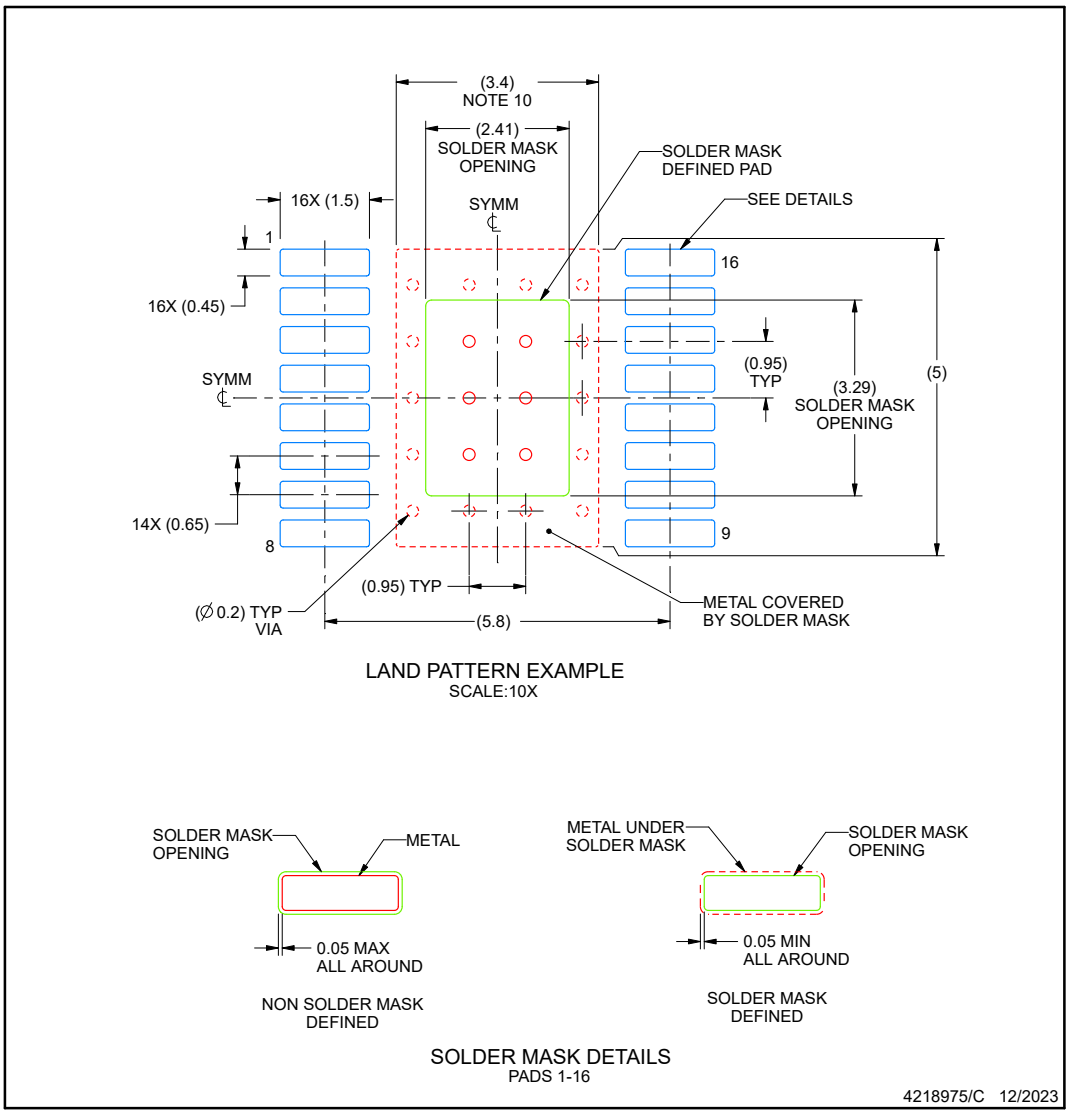
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.
6. Features may not present.

## EXAMPLE BOARD LAYOUT

### PWP0016G

**PowerPAD ™ TSSOP - 1.2 mm max height**

PLASTIC SMALL OUTLINE



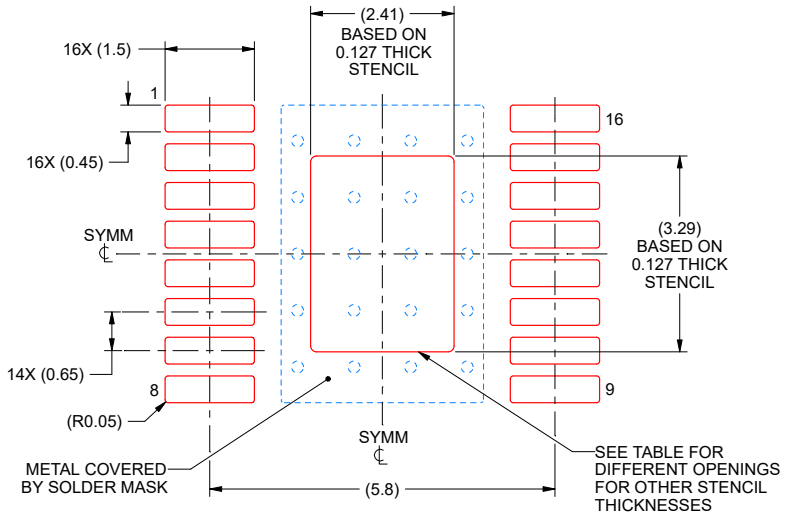

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
10. Size of metal pad may vary due to creepage requirement.

## EXAMPLE STENCIL DESIGN

**PWP0016G** — **PowerPAD ™ TSSOP - 1.2 mm max height**

PLASTIC SMALL OUTLINE




SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 2.69 X 3.68 |
| 0.127 | 2.41 X 3.29 (SHOWN) |
| 0.152 | 2.20 X 3.00 |
| 0.178 | 2.04 X 2.78 |

4218975/C 12/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS92642QPWPRQ1 | Active | Production | HTSSOP (PWP) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 642Q1 |
| TPS92642QPWPRQ1.A | Active | Production | HTSSOP (PWP) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 642Q1 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

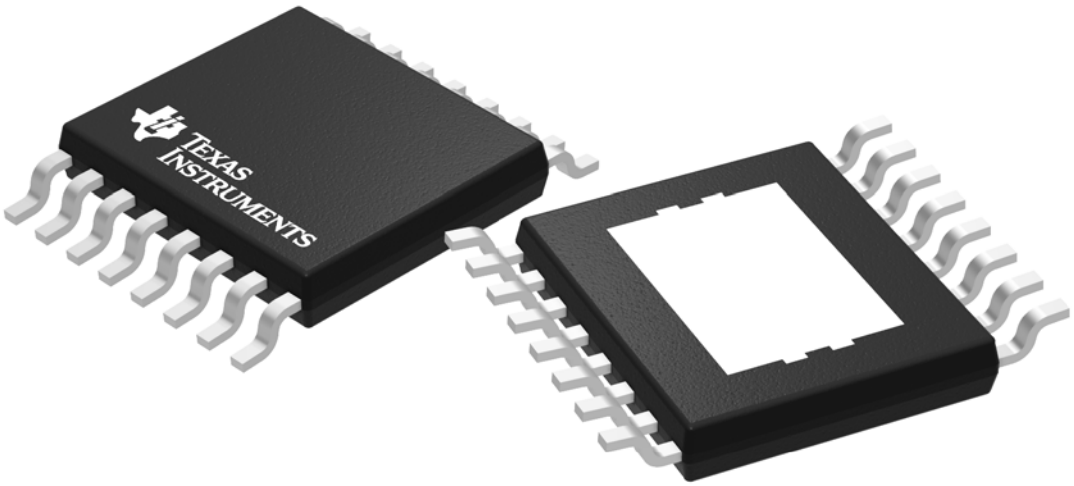
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

# PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265