











TPS7H1101-SP

SLVSD81A - JANUARY 2016-REVISED FEBRUARY 2017

TPS7H1101-SP 1.5-V to 7-V Input, 3-A, Radiation-Hardened **Ultra-Low Dropout (LDO) Regulator**

Features

- 5962R13202:
 - Radiation Hardness Assurance (RHA) up to TID 100 krad (Si)
 - Total Ionizing Dose 100 krad (Si)
 - ELDRS-Free 100 krad (Si)
 - Dose Rate 10 mRAD (si)/s
 - Single Event Latchup (SEL) Immune to $LET = 85 \text{ MeV-cm}^2/\text{mg}$
 - SEB and SEGR Immune to $LET = 85 \text{ MeV-cm}^2/\text{mg}$
 - SET/SEFI Onset Threshold > 40 MeV-cm²/mg, See Radiation Report for Details
 - Specifically Designed to Always Upset Low to Avoid Damage to Critical Downstream Component
 - SET/SEFI Cross-Section Plot, See Radiation Report for Details
- Ultra-Low V_{IN} Range: 1.5 V to 7 V
- 3-A Maximum Output Current
- Current Share/Parallel Operation to Provide up to 6-A Output Current
- Stable With Ceramic Output Capacitor
- ±2% Accuracy Over Line, Load, and Temperature
- Programmable Soft-Start Through External Capacitor
- Input Enable and Power-Good Output for Power Sequencing
- Ultra-Low Dropout LDO Voltage: 62 mV at 1 A (25°C), $V_{OUT} = 1.8 \text{ V}$
- Low Noise: $20.33 \mu VRMS V_{IN} = 2 V, V_{OUT} = 1.8 V at 3 A$
- PSRR: Over 45 dB at 1 kHz
- Excellent Load/Line Transient Response
- Foldback Current Limit
- See the Tools & Software Tab
- Thermally-Enhanced CFP Package (0.6°C/W $R_{\theta JC}$

2 Applications

- Space Satellite Point of Load Supply for FPGAs, Microcontrollers, ASICs, and Data Converters
- Space Satellite Payloads
- Radiation-Hardened Low-Noise Linear Regulator Power Supply for RF, VCOs, Receivers, and **Amplifiers**
- Clean Analog Supply Requirements
- Available in Military (-55°C to 125°C) Temperature Range
- Engineering Evaluation (/EM) Samples are Available⁽¹⁾

3 Description

The TPS7H1101-SP is a radiation-hardened LDO linear regulator that uses a PMOS pass element configuration. This device operates over a wide range of input voltage, from 1.5 V to 7 V while offering excellent PSRR. The TPS7H1101-SP features a precise and programmable foldback current limit implementation with a very-wide adjustment range. To support the complex power requirements of FPGAs, DSPs, or microcontrollers, the TPS7H1101-SP provides enable on and off functionality, programmable SoftStart, current sharing capability, and a PowerGood open-drain output.

Device Information⁽²⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7H1101-SP	CFP (16)	11.00 mm × 9.60 mm

- (1) These units are intended for engineering evaluation only. They are processed to a noncompliant flow (that is, no burnin, and so forth) and are tested to a temperature rating of 25°C only. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full MIL specified temperature range of -55°C to 125°C or operating life.
- (2) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit

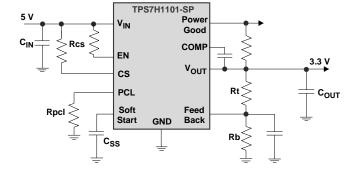


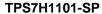


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4 Revision History

Cł	nanges from Original (January 2016) to Revision A	Page
•	Changed accuracy over line, load, and temperature from ±1.25% : to ±2% in the Features section	1
•	Added I/O values in the Pin Functions table	4
•	Changed COMP pin description	4
•	Deleted peak output current spec in Absolute Maximum Ratings table	5
•	Changed max output voltage from V _{IN} : to 7.5 V	5
•	Added rise time specification for EN signal in Recommended Operating Conditions table	5
•	Added rise time specification for VIN signal in Recommended Operating Conditions table	5
•	Deleted unnecessary DC input line regulation data in the Electrical Characteristics table	6
•	Deleted worst case dropout voltage specifications Electrical Characteristics table	6
•	Deleted redundant operating junction temperature in the <i>Electrical Characteristics</i> table	6
•	Changed output voltage range from V _{IN} – 0.35 V : to V _{IN}	6
•	Changed min and typ CSR values from 47500 A/A and 47394 A/A: to 47394 A/A and 47500 A/A, respectively	7
•	Added PSRR curve to Typical Characteristics section	g
•	Changed typo regarding capacitor from CS: to SS in the Soft Start section	12
•	Added clarification on PG functionality and removed reference to sequencing SS terminal in Power Good (PG) sect	tion . 12
•	Deleted description for disable using SS terminal in the Enable/Disable section	13
•	Changed Stability section	15
•	Changed Equation 2 (group delay equation)	15
•	Added resistor between V _{IN} and EN in Figure 12 as recommended	16
•	Changed values in Table 2 with more accurate output voltages	17
•	Added clarity to current foldback feature in Current Foldback section	19
•	Changed channel labels to match scope captures in Transient Response section	20
•	Added parallel operation block diagram to Current Sharing section	21
•	Added compensation example feedback resistor value (R _{bottom}) to Compensation section	23
•	Changed organization of information in Capacitors section	24
•	Deleted redundant curves in the Application Curves section	25



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Revision History (continued)

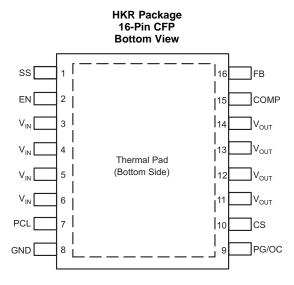
•	Added information to Layout Guidelines section	26
•	Added Receiving Notification of Documentation Updates section to Device and Documentation Support section	27



5 Description (continued)

The TPS7H1101-SP is available in a thermally-enhanced 16-pin ceramic flatpack package (CFP).

6 Pin Configuration and Functions



Pin Functions

PIN		1/0	DESCRIPTION		
NAME	NO.	1/0	DESCRIPTION		
SS	1	0	Soft-start terminal. Connecting an external capacitor slows down the output voltage ramp rate after enable event. The soft-start terminal can be used to disable the device as described in the Soft Start section.		
EN 2 I disables the device. V _{IN} voltage must be greater than 3.5 terminal cannot be used to disable the device.		1	Enable terminal. Driving this terminal to logic high enables the device; driving the terminal to logic low disables the device. $V_{\rm IN}$ voltage must be greater than 3.5 V when using the EN pin. For $V_{\rm IN}$ < 3.5 V, enable terminal cannot be used to disable the device. TI recommends to connect the enable terminal to $V_{\rm IN}$.		
	3				
V	4	1	Unrequiated cumply voltage. Three monde to connect an input capacitor as a good analog circuit practice.		
V _{IN}	5		'	Jnregulated supply voltage. TI recommends to connect an input capacitor as a good analog circuit practic	
	6				
PCL	Programmable current limit. A resistor to GND sets the overcurrent limit activation point. The range of resistor that can be used on the PCL terminal to GND is 8.2 kΩ to 160 kΩ.				
GND	8	_	Ground/thermal pad. (1)		
PG/OC	9	0	Power Good terminal. PG is an open-drain output to indicate the output voltage reaches 90% of target. PG terminal is also used as indicator when an overcurrent condition is activated. PG pin should have a pull-up resistor to the V _{OUT} pin.		
CS	10	0	Current sense terminal. Resistor connected from CS to V _{IN} . CS terminal indicates voltage proportional to output current. CS terminal low: Foldback current limit disabled CS terminal high: Foldback current limit enabled		
	11				
\	12		Dogulated autout		
V _{OUT}	13	0	Regulated output.		
	14				
COMP	15	1	Internal compensation point for error amplifier.		
FB	16	I	The output voltage feedback input through voltage dividers. See <i>Adjustable Output Voltage (Feedback Circuit)</i> section.		

(1) Thermal pad must be connected to GND.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
long tradtage	V _{IN} , PG	-0.3	7.5	V
Input voltage	FB, COMP, PCL, CS, EN	-0.3	$V_{IN} + 0.3$	V
Output voltage	V _{OUT} , SS	-0.3	7.5	V
PG terminal sink current		0.001	5	mA
Maximum operating juncti	on temperature, T _J	-55	150	°C
Storage temperature, T _{stg}		-55	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
V	Electrostatic	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	.,
V _(ESD)	discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±1000	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM MAX	UNIT
T _J	Operating junction temperature	-55	125	ô
t _R EN	Rise time (10% to 90%) for EN signal	100		μs
t _R VIN	Rise time (10% to 90%) for VIN = EN	1		ms

7.4 Thermal Information

		TPS7H1101-SP	
	THERMAL METRIC (1)(2)	HKR (CFP)	UNIT
		16 PINS	
R ₀ JC(bot)	Junction-to-case (bottom) thermal resistance	0.6	°C/W

⁽¹⁾ Do not allow package body temperature to exceed 265°C at any time or permanent damage may result.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

⁽²⁾ Maximum power dissipation may be limited by overcurrent protection.



7.5 Electrical Characteristics

 $1.5~V \le V_{IN} \le 7~V,~V_{OUT(target)} = V_{IN} - 0.35~V,~I_{OUT} = 10~mA,~V_{EN} = 1.1~V,~C_{OUT} = 22~\mu F,~PG$ terminal pulled up to V_{IN} with 50 k Ω , over operating temperature range ($T_J = -55^{\circ}C$ to 125°C), unless otherwise noted. Typical values are at $T_J = 25^{\circ}C$.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IN}	Input voltage range		1.5		7	V
V_{FB}	Feedback terminal voltage ⁽¹⁾	0 A ≤ I _{OUT} ≤ 3 A, 1.5 V ≤ V _{IN} ≤ 7 V	0.594	0.605	0.616	V
V _{OUT}	Output voltage range		0.8		V _{IN}	V
	Output voltage accuracy ⁽¹⁾	$0 \text{ A} \le I_{OUT} \le 3 \text{ A}, 1.5 \text{ V} \le V_{IN} \le 7 \text{ V}, V_{OUT} = 0.8 \text{ V}, 1.2 \text{ V}, 1.8 \text{ V}, 6.65 \text{ V}$	-2%		2%	
$\Delta V_{OUT}\%/$ ΔV_{IN}	Line regulation	1.5 V ≤ V _{IN} ≤ 7 V	-0.07	0.01	0.07	%/V
$\Delta V_{OUT}\%/$ ΔI_{OUT}	Load regulation	$0.8 \text{ V} \le \text{V}_{\text{OUT}} \le 6.65 \text{ V}, 0 \le \text{I}_{\text{Load}} \le 3 \text{ A}$		0.08		%/A
		$I_{0UT} = 10 \text{ mA}, T_{J} = -55^{\circ}C^{(2)}$		0.5	3	
ΔV_{OUT}	DC input line regulation	$I_{0UT} = 10 \text{ mA}, T_{J} = 25^{\circ}C^{(2)}$		0.2	0.6	mV
		$I_{0.0T} = 1.5 \text{ V} \le V_{IN} \le 7 \text{ V}, V_{0.0T} = 0.8 \text{ V}, 1.2 \text{ V}, 1.8 \text{ V}, V_{0.0T} = 10 \text{ mA}, T_{J} = 125^{\circ}C^{(2)}$		0.2	1.0	

 ⁽¹⁾ The output voltage accuracy of condition at I_{OUT} = 2 A and I_{OUT} = 3 A is specified by characterization, but not production tested.
 (2) Line and load regulations done under pulse condition for t < 10 ms.



Electrical Characteristics (continued)

 $1.5~V \le V_{IN} \le 7~V,~V_{OUT(target)} = V_{IN} - 0.35~V,~I_{OUT} = 10~mA,~V_{EN} = 1.1~V,~C_{OUT} = 22~\mu F,~PG$ terminal pulled up to V_{IN} with 50 k Ω , over operating temperature range ($T_J = -55^{\circ}C$ to 125°C), unless otherwise noted. Typical values are at $T_J = 25^{\circ}C$.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		$V_{OUT} = 0.8 \text{ V}, 0 \le I_{Load} \le 1 \text{ A}, T_{J} = -55^{\circ}C^{(2)}$		0.4	1.0	
		$V_{OUT} = 0.8 \text{ V}, 0 \le I_{Load} \le 1 \text{ A}, T_{J} = 25^{\circ}C^{(2)}$		0.6	1.1	
		$V_{OUT} = 0.8 \text{ V}, 0 \le I_{Load} \le 1 \text{ A}, T_{J} = 125^{\circ}C^{(2)}$		0.8	1.3	
		$V_{OUT} = 0.8 \text{ V}, 0 \le I_{Load} \le 2 \text{ A}, T_{J} = -55^{\circ} \text{C}^{(2)}$		0.8	1.8	
		$V_{OUT} = 0.8 \text{ V}, 0 \le I_{Load} \le 2 \text{ A}, T_{J} = 25^{\circ}\text{C}^{(2)}$		1.3	1.8	
		$V_{OUT} = 0.8 \text{ V}, 0 \le I_{Load} \le 2 \text{ A}, T_{J} = 125 ^{\circ}\text{C}^{(2)}$		1.6	2.4	
		$V_{OUT} = 0.8 \text{ V}, 0 \le I_{Load} \le 3 \text{ A}, T_{J} = -55^{\circ} C^{(2)}$		1.1	1.9	
		$V_{OUT} = 0.8 \text{ V}, 0 \le I_{Load} \le 3 \text{ A}, T_{J} = 25^{\circ}\text{C}^{(2)}$		1.9	2.6	
		$V_{OUT} = 0.8 \text{ V}, 0 \le I_{Load} \le 3 \text{ A}, T_{J} = 125^{\circ}\text{C}^{(2)}$		2.5	3.4	
		$V_{OUT} = 1.2 \text{ V}, 0 \le I_{Load} \le 1 \text{ A}, T_{J} = -55^{\circ}\text{C}^{(2)}$		0.3	1.2	
		$V_{OUT} = 1.2 \text{ V}, 0 \le I_{Load} \le 1 \text{ A}, T_{J} = 25^{\circ}\text{C}^{(2)}$		0.5	1.3	
		$V_{OUT} = 1.2 \text{ V}, 0 \le I_{Load} \le 1 \text{ A}, T_J = 125^{\circ}\text{C}^{(2)}$		0.6	1.3	
	$V_{OUT} = 1.2 \text{ V}, 0 \le I_{Load} \le 2 \text{ A}, T_{J} = -55^{\circ}\text{C}^{(2)}$		0.8	1.6		
		$V_{OUT} = 1.2 \text{ V}, 0 \le I_{Load} \le 2 \text{ A}, T_{J} = 25^{\circ}\text{C}^{(2)}$		1.1	2.1	
		$V_{OUT} = 1.2 \text{ V}, 0 \le I_{Load} \le 2 \text{ A}, T_J = 125^{\circ}\text{C}^{(2)}$		1.5	2.1	
		$V_{OUT} = 1.2 \text{ V}, 0 \le I_{Load} \le 3 \text{ A}, T_{J} = -55^{\circ}\text{C}^{(2)}$		1.0	1.7	
		$V_{OUT} = 1.2 \text{ V}, 0 \le I_{Load} \le 3 \text{ A}, T_J = 25^{\circ}\text{C}^{(2)}$		1.1	2.4	
A \ /	(3)	$V_{OUT} = 1.2 \text{ V}, 0 \le I_{Load} \le 3 \text{ A}, T_J = 125^{\circ}\text{C}^{(2)}$		2.2	3.5	
Vo	DC output load regulation (3)	$V_{OUT} = 1.8 \text{ V}, 0 \le I_{Load} \le 1 \text{ A}, T_{J} = -55^{\circ}\text{C}^{(2)}$		0.1	0.9	mV
		$V_{OUT} = 1.8 \text{ V}, 0 \le I_{Load} \le 1 \text{ A}, T_J = 25^{\circ}\text{C}^{(2)}$		0.3	0.9	
		$V_{OUT} = 1.8 \text{ V}, 0 \le I_{Load} \le 1 \text{ A}, T_J = 125^{\circ}\text{C}^{(2)}$		0.4	1.2	
		$V_{OUT} = 1.8 \text{ V}, 0 \le I_{Load} \le 2 \text{ A}, T_{J} = -55^{\circ}\text{C}^{(2)}$		1.4	2.4	
		$V_{OUT} = 1.8 \text{ V}, 0 \le I_{Load} \le 2 \text{ A}, T_J = 25^{\circ}\text{C}^{(2)}$		0.7	1.4	
		$V_{OUT} = 1.8 \text{ V}, 0 \le I_{Load} \le 2 \text{ A}, T_J = 125^{\circ}\text{C}^{(2)}$		0.6	1.9	
		$V_{OUT} = 1.8 \text{ V}, 0 \le I_{Load} \le 3 \text{ A}, T_{J} = -55^{\circ}\text{C}^{(2)}$		2.5	3.9	
		$V_{OUT} = 1.8 \text{ V}, 0 \le I_{Load} \le 3 \text{ A}, T_{J} = 25^{\circ}\text{C}^{(2)}$		1.2	2.1	
		$V_{OUT} = 1.8 \text{ V}, 0 \le I_{Load} \le 3 \text{ A}, T_J = 125^{\circ}\text{C}^{(2)}$		1.2	2.5	
		$V_{OUT} = 6.65 \text{ V}, 0 \le I_{Load} \le 1 \text{ A}, T_{J} = -55^{\circ}\text{C}^{(2)}$		1.5	2.9	
		$V_{OUT} = 6.65 \text{ V}, 0 \le I_{Load} \le 1 \text{ A}, T_{J} = 25^{\circ}\text{C}^{(2)}$		0.4	2.6	
		$V_{OUT} = 6.65 \text{ V}, 0 \le I_{Load} \le 1 \text{ A}, T_J = 125^{\circ}C^{(2)}$		2.8	3.5	
		$V_{OUT} = 6.65 \text{ V}, 0 \le I_{Load} \le 2 \text{ A}, T_{J} = -55^{\circ}\text{C}^{(2)}$		3.5	5.9	ı
		$V_{OUT} = 6.65 \text{ V}, 0 \le I_{Load} \le 2 \text{ A}, T_{J} = 25^{\circ}\text{C}^{(2)}$		1.1	4.7	
		$V_{OUT} = 6.65 \text{ V}, 0 \le I_{Load} \le 2 \text{ A}, T_{J} = 125^{\circ}\text{C}^{(2)}$		5.8	8.0	
		$V_{OUT} = 6.65 \text{ V}, 0 \le I_{Load} \le 3 \text{ A}, T_{J} = -55^{\circ}\text{C}^{(2)}$		5.6	9.3	
		$V_{OUT} = 6.65 \text{ V}, 0 \le I_{Load} \le 3 \text{ A}, T_{J} = 25^{\circ}C^{(2)}$		3.7	8.0	
		$V_{OUT} = 6.65 \text{ V}, 0 \le I_{Load} \le 3 \text{ A}, T_J = 125^{\circ}\text{C}^{(2)}$		13.0	25	
00	Dropout voltage ⁽³⁾	$I_{OUT} = 3 \text{ A, } V_{OUT} = 1.3 \text{ V, } V_{IN} = V_{OUT} + V_{DO}$		210	335	mV
	Programmable output current	V_{IN} = 1.5 V, V_{OUT} = 1.2 V , PCL resistance = 47 k Ω	500		750	
L	limit range	V _{IN} = 1.5 V, V _{OUT} = 1.2 V , PCL resistance varies	200		3500 ⁽⁴⁾	mA
CS	Operating voltage range at CS		0.3		V _{IN}	V
SR	Current sense ratio	I _{LOAD} / I _{CS} , V _{IN} = 2.3 V, V _{OUT} = 1.9 V	47394	47500	56000	A/A

³⁾ The parameter is specified to the limit in characterization, but not production tested.

⁽⁴⁾ The maximum limit of the I_{CL}parameter is specified to the limit in characterization, but not production tested.



Electrical Characteristics (continued)

 $1.5~V \leq V_{IN} \leq 7~V,~V_{OUT(target)} = V_{IN} - 0.35~V,~I_{OUT} = 10~mA,~V_{EN} = 1.1~V,~C_{OUT} = 22~\mu F,~PG~terminal~pulled~up~to~V_{IN}~with~50~k\Omega,~terminal~pulled~up~to~V_{IN}~with~terminal~pulled~up~to~V_{IN}~with~terminal~pulled~up~to~V_{IN}~with~terminal~pulled~up~to~V_{IN}~with~terminal~pulled~up~to~V_{IN}~with~terminal~pulled~up~to~V_{IN}~with~terminal~pulled~up~to~V_{IN}~with~terminal~pulled~up~to~V_{IN}~with~terminal~pulled~up~to~V_{IN}~with~terminal~pulled~up~to~V_{IN}~with~terminal~pulled~up~to~V_{IN}~with~terminal~pulled~up~to~V_{IN}~with~terminal$

	PARAMETER	TEST CONDITIO	NS	MIN	TYP	MAX	UNIT
I _{GND}	GND terminal current	V _{IN} = 1.5 V, V _{OUT} = 1.2 V, I _{OU}	T = 2 A		10	16	mA
IQ	Quiescent current (no load)	$V_{IN} = V_{OUT} + 0.5 \text{ V}, I_{OUT} = 0 \text{ A}$	\		7	10	mA
		1.5 V ≤ V _{IN} ≤ 7 V			26	230	μA
I _{SHDN}	Shutdown current	1.5 V \leq V _{IN} \leq 7 V, post 100 kR 25°C ⁽⁵⁾	Rads (si), T _J =			1400	μA
I _{SNS} , I _{FB}	FB/SNS terminal current	V _{IN} = 7 V, V _{OUT} = 6.65 V	V _{IN} = 7 V, V _{OUT} = 6.65 V		1	5	nA
I _{EN}	EN terminal input current	$V_{IN} = 7 \text{ V}, V_{EN} = 7 \text{ V}, V_{OUT} = 6$	6.65 V		20	150	nA
V _{ILEN}	EN terminal input low (disable)	3.5 V < V _{IN} < 7 V		(0.30 × V _{IN}		V
V _{IHEN}	EN terminal input high (enable)	3.5 V < V _{IN} < 7 V		(0.75 × V _{IN}		V
Eprop Dly	Enable terminal propagation delay	V _{IN} = 2.2 V, EN rise to I _{OUT} rise			650	1000	μs
T _{EN}	Enable terminal turn-on delay	$V_{IN} = 2.2 \text{ V}, V_{OUT} = 1.8 \text{ V}, I_{LOAD} = 1 \text{ A},$ $C_{OUT} = 220 \mu\text{F}, C_{SS} = 2 \text{ nF}$			1.4	1.6	ms
V_{THPG}	PG threshold	No load, 0.8 V ≤ V _{OUT} ≤ 6.65 V		86%	90%		
V _{THPGHYS}	PG hysteresis	1.5 V ≤ V _{IN} ≤ 7 V			2%		
V _{OLPG}	PG terminal output low	$I_{PG} = -1$ mA to 0 mA			120	300	mV
	DC towning look on a compart	$V_{OUT} > V_{THPG}$, $V_{PG} = 1.2 \text{ V}$		0.2		1.5	
I _{LKGPG}	PG terminal leakage current	$V_{OUT} > V_{THPG}, V_{PG} = 7 V$			0.5	2.5	μΑ
I _{SS}	SS terminal charge current	V _{IN} = 1.5 V to 7 V			2.5	3.5	μΑ
I _{SSdisb}	SS terminal disable current	V _{IN} = 1.5 V to 7 V			5	10	μΑ
V _{SS}	SS terminal voltage (device enabled) (6)	V _{IN} = 1.5 V to 7 V				1.232	V
V _{SSdisb}	SS terminal low-level input voltage to disable device	V _{IN} = 1.5 V to 7 V				0.4	V
DCDD	Davies aventural atlant	V _{IN} = 2.5 V, V _{OUT} = 1.8 V,	1 kHz		48		4D
PSRR	Power-supply rejection ratio	C _{OUT} = 220 µF	100 kHz		25		dB
V _N	Output noise voltage	BW = 10 Hz to 100 kHz, I _{OUT} = 3 A, V _{IN} = 2 V, V _{OUT} = 1.8 V			20.33		μV_{RMS}
TSD	Thermal shutdown temperature				185		°C

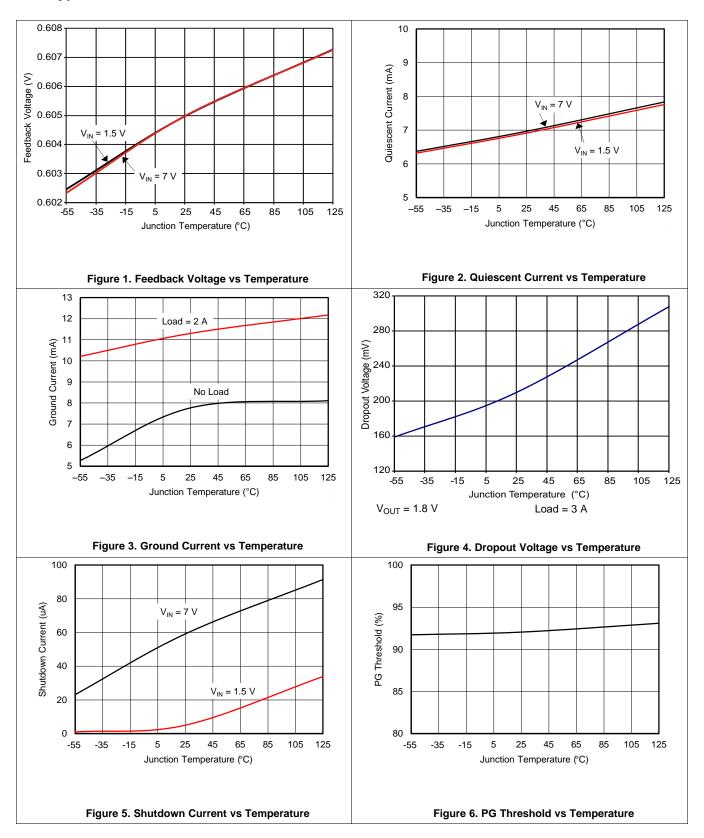
⁽⁵⁾ This maximum limit applies to SMD 5962R13202 post 100 kRads (Si) test at 25°C.

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⁽⁶⁾ Any external pullup voltage should not exceed 1.188 V.



7.6 Typical Characteristics

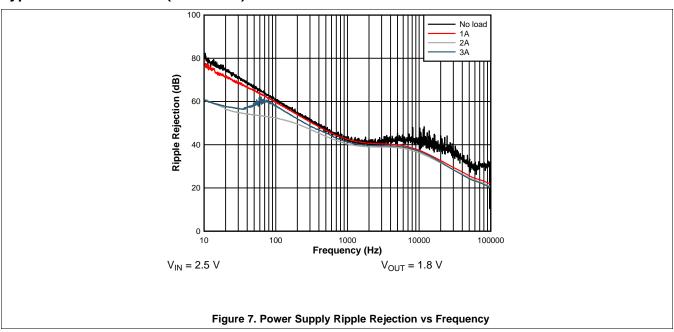


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Typical Characteristics (continued)





8 Detailed Description

8.1 Overview

The TPS7H1101-SP is 3-A, 1.5-V to 7-V LDO linear regulator that uses PMOS pass element configuration.

It uses TI's proprietary process to achieve low noise, high PSRR combined with high thermal performance in a 16-pin ceramic flatpack package (HKR).

A number of features are incorporated in the design to provide high reliability and system flexibility. Current foldback, current limit, and thermal protection are incorporated in the design to make it viable for harsh environments.

The device also has a current sense monitoring feature. A resistor connected from the current sense (CS) terminal to VIN indicates voltage proportional to the output current. When CS is held high, foldback current limit is enabled. Shorting CS low disables the foldback current limit.

A resistor connected from the programmable current limit (PCL) terminal to ground sets the over current limit activation point. When overcurrent limit activation point is reached, it results in LDO going into current foldback mode. Output current is reduced to approximately 50% of the current limit set point. *PCL* section provides a detailed description of this feature.

TPS7H1101-SP incorporates thermal protection, which disables the output when the junction temperature rises approximately 185°C, allowing the device to cool. Cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

A resistor connected from the CS terminal to VIN indicates voltage proportional to the output load current.

To provide system flexibility for demanding current needs, the LDO can be configured in parallel operation as indicated in Figure 22. *Current Sharing* section provides detailed parallel operation information.

An enable feature is incorporated in the design allowing the user to enable or disable the LDO. Power Good, an open-drain connection, indicates the status of the output voltage. These provide the customers system flexibility in monitoring and controlling the LDO operation. When using the Enable function, V_{IN} voltage must be > 3.5 V. For V_{IN} from 1.5 V to 7 V, TPS7H1101-SP can be disabled using the soft-start (SS) terminal as described in *Enable/Disable* section.



8.2 Functional Block Diagram

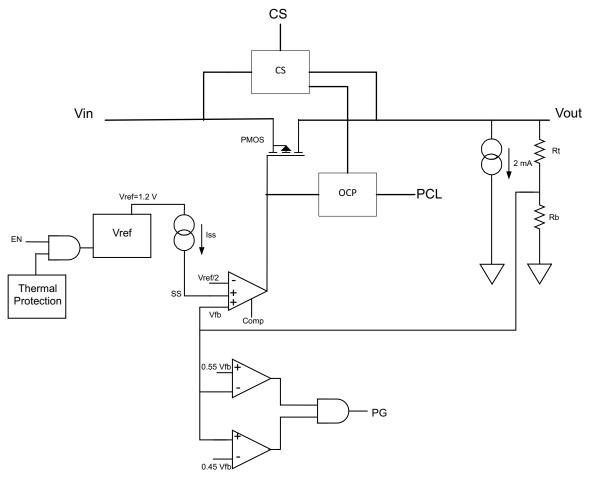


Figure 8. Block Diagram

8.3 Feature Description

8.3.1 Soft Start

Connecting a capacitor from the SS terminal to GND (C_{SS}) slows down the output voltage ramp rate. The soft-start capacitor charges up to 1.2 V.

$$C_{SS} = \frac{t_{SS} \cdot I_{SS}}{V_{FR}}$$

where

• t_{ss} = Soft-start time

•
$$V_{FB} = V_{REF} / 2 = 0.605 \text{ V}$$
 (1)

8.3.2 Power Good (PG)

Power Good terminal (9) is an open-drain connection and can be used to sequence multiple LDOs. Figure 9 shows typical connection for $V_{\text{IN}} > 3.5 \text{ V}$. The PG terminal will be pulled low until the output voltage reaches 90% of its maximum level. At that point, the PG pin will be pulled up. Since the PG pin is open drain, it can be pulled up to any voltage as long as it does not exceed the absolute max of 7.5 V listed in the *Electrical Characteristics* table.

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Feature Description (continued)

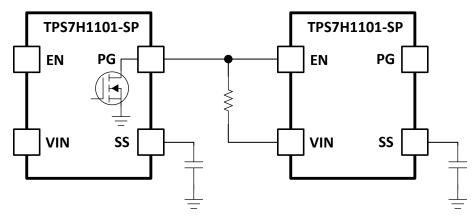


Figure 9. Sequencing LDOs with Power Good

NOTE

For PSpice models, WEBENCH, and mini-POL reference design, see the *Tools & Software* tab.

- 1. PSpice average model (stability bode plot)
- 2. PSpice transient model (switching waveforms)
- 3. WEBENCH design tool (www.ti.com/product/TPS7H1101-SP/toolssoftware)

8.4 Device Functional Modes

8.4.1 Enable/Disable

For V_{IN} from 1.5 V to 7 V, TPS7H1101-SP can be disabled using the SS terminal. The minimum soft-start pulldown current is 10 μ A, with soft start to ground voltage of 400 mV or lower. External voltage applied to the SS terminal must be limited to 1.2-V maximum. Removing the logic-low condition on soft start enables the device allowing the soft-start capacitor to get charged by the internal current source. Alternatively, for $V_{IN} > 3.5$ V, the device can be disabled by pulling the enable terminal to logic low. In all other cases, the enable terminal should be connected to VIN.

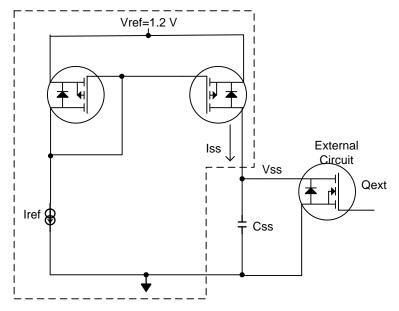


Figure 10. Enable/Disable

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Device Functional Modes (continued)

The circuit shown in Figure 10 highlights the SS terminal 1 along with block diagram of internal circuitry. Circuitry in dashed outline is internal to the IC composed of PMOSFET current mirror. The PMOS current mirror sources current from the positive supply and external circuitry composed of Qext is used to sink current from SS terminal 1. As highlighted in the *Electrical Characteristics* table, typical ISS = 2.5 μ A and max ISS = 3.5 μ A for TPS7H1101-SP. If ISS current is exceeded, such as sinking higher current in excess of max ISS, this disables the LDO. See the *Electrical Characteristics* table for the external sink current from SS terminal necessary to disable the IC. Exceeding maximum external sink current does not damage the device.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS7H1101-SP LDO linear regulator is targeted to harsh environment applications. This regulator has various features such as low dropout, soft start, output current foldback, high-side current sensing (where sensing voltage at CS pin provides voltage proportional to output current), and current sharing.

9.1.1 Stability

Conventional Bode plots are a standard approach in assessing stability as shown in Figure 11. This approach requires that we have a single feedback path where an AC signal is injected across a resistor (typically 50 Ω) and measurements are taken on either side of the resistor. From this, loop gain and phase plots can be generated. Crossover frequency, $f_{\rm C}$, is defined as the frequency where the magnitude of the loop gain is unity and phase margin is evaluated at the crossover frequency $f_{\rm C}$.

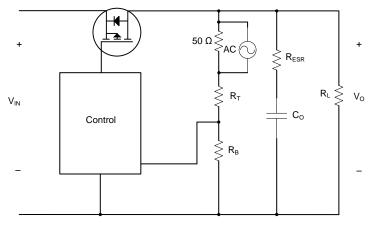


Figure 11. Conventional Bode Plot

However, there are conditions where the feedback loop is not accessible or there may be multiple feedback paths, as with the TPS7H1101-SP. When there are multiple feedback loops the conventional bode plot approach will not be representative of the device's true response. The TPS7H1101-SP uses a conventional feedback loop in addition to an inner fast loop that injects current into the error amplifier, which in turn greatly improves the transient response of the device. The Bode plot method can still be used to understand the behavior of the main loop, but this will show a lower crossover frequency and thus imply a slower transient response than the actual performance of the device. Fortunately, accurate and quantitative stability metrics can still be assessed from output impedance measurements and simulations.

There are multiple ways output impedance can be measured. One approach is to inject a small current at the output of the regulator and compare it to the resulting voltage response. The variation in the phase of the output impedance across frequency can be related to the phase margin through the group delay.

Group delay, T_g , is the rate of change of phase with respect to frequency as shown in Equation 2. Most SPICE simulation packages can plot this parameter and certain frequency analyzers boast software that supports a direct measurement. Using this software, phase margin can be extracted from the group delay plot. The phase margin and crossover frequency reported from these measurements will include the effects of both feedback loops.

$$T_{g} = \frac{d\phi}{d\omega} \tag{2}$$



Application Information (continued)

The stability of the device can be qualitatively validated by applying a step load to the output and observing the response. The SPICE models for the device can be found in *Tools & Software* on the product page. To simulate impedance measurements, the transient model should be used. For a more detailed explanation of this approach and how to use the model to simulate the output impedance and group delay, please see reference (1).

9.2 Typical Application

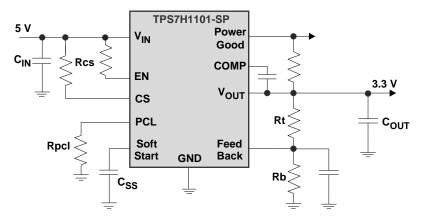


Figure 12. Typical Application Circuit

9.2.1 Design Requirements

Table 1 shows the design parameters.

Table 1. Design Parameters

PARAMETER	VALUE			
Input voltage	1.5 V to 7 V			
Output voltage	User programmable			
Output current	3-A max			



9.2.2 Detailed Design Procedure

9.2.2.1 Adjustable Output Voltage (Feedback Circuit)

The output voltage of the TPS7H1101-SP can be set to a user-programmable level between 0.8 V and 6.65 V. Achieve this by using a resistor divider connected between V_{OUT} , FB, and GND terminals. R_{TOP} connected between V_{OUT} and V_{FB} , and R_{BOTTOM} connected between V_{FB} and GND.

Use Equation 3 to determine V_{OUT}.

$$V_{\scriptscriptstyle OUT} = \frac{(R_{\scriptscriptstyle TOP} + R_{\scriptscriptstyle BOTTOM}) \bullet V_{\scriptscriptstyle FB}}{R_{\scriptscriptstyle BOTTOM}}$$

where

•
$$V_{FB} = 0.605 \text{ V}$$
 (3)

Table 2. Resistor Values for Typical Voltages

				_	
V	Standard	1% Resistors	Standard 0.1% Resistors		
V _{OUT}	R _{TOP}	R _{BOTTOM}	R _{TOP}	R _{BOTTOM}	
0.8 V	10.7 kΩ	33.2 kΩ	10.7 kΩ	33.2 kΩ	
1 V	13.7 kΩ	21 kΩ	12.6 kΩ	19.3 kΩ	
1.2 V	11.3 kΩ	11.5 kΩ	11.8 kΩ	12 kΩ	
1.5 V	15.8 kΩ	10.7 kΩ	18.2 kΩ	12.3 kΩ	
1.8 V	23.2 kΩ	11.8 kΩ	32 kΩ	16.2 kΩ	
2.5 V	10.7 kΩ	3.4 kΩ	37.9 kΩ	12.1 kΩ	
3.3 V	51.1 kΩ	11.5 kΩ	10.2 kΩ	2.29 kΩ	
4 V	13.3 kΩ	2.37 kΩ	31.2 kΩ	5.56 kΩ	
5 V	11.5 kΩ	1.58 kΩ	16.2 kΩ	2.23 kΩ	
5.5 V	17.4 kΩ	2.15 kΩ	89.8 kΩ	11.1 kΩ	
6 V	90.9 kΩ	10.2 kΩ	10.7 kΩ	1.2 kΩ	
6.5 V	26.7 kΩ	2.74 kΩ	15.2 kΩ	1.56 kΩ	
6.6 V	11.3 kΩ	1.15 kΩ	22.1 kΩ	2.23 kΩ	
6.7 V	39.2 kΩ	3.92 kΩ	13.8 kΩ	1.37 kΩ	
· · · · ·	33.2 142	3.32 141	. 5.5 142		

9.2.2.2 PCL

PCL resistor, R_{pcl}, sets the overcurrent limit activation point and can be calculated per Equation 4.

$$R_{pcl} = (CSR \times V_{ref}) / (I_{CL} - 0.0403)$$

where

- $V_{ref} = 0.605 \text{ V}$
- I_{CL} = Programmable current limit (A)
- Current sense ratio (CSR) is the ratio of output load current to I_{CS}. The typical value of the CSR is 47394. (4)

Figure 13 shows the output load current (I_{OUT}) versus PCL terminal current (I_{CL})

A suitable resistor R_{pcl} must be chosen to ensure the CS terminal is within its operating range of 0.3 V to V_{IN} .

The maximum PCL is 3.5 A. The range of resistor that can be used on the PCL terminal to GND is 8.2 k Ω to 160 k Ω .

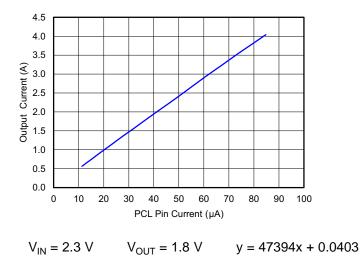


Figure 13. I_{OUT} (A) vs I_{PCL} (μ A)

9.2.2.3 High-Side Current Sense

Figure 14 shows the cascode NMOS current mirror. V_{cs} must be in the range as specified in the *Electrical Characteristics* table. The following example shows the typical calculation of R_{cs} .

$$I_{CS} = \frac{I_{LOAD} + I_{offset}}{CSR}$$

$$R_{CS} = \frac{V_{IN} - V_{CS}}{I_{CS}}$$
(5)

where

- I_{LOAD} is the output load current.
- CSR is the current sense ratio.
 (6)

When V_{IN} = 2.3 V, select V_{CS} = 2.05 V, I_{LOAD} = 3 A, CSR = 47394, and I_{offset} = 0.1899 A, then I_{CS} = 67.306 μ A and R_{CS} = 3.714 $k\Omega$.

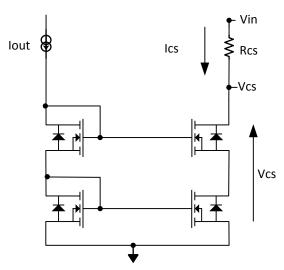


Figure 14. Cascode NMOS Current Mirror

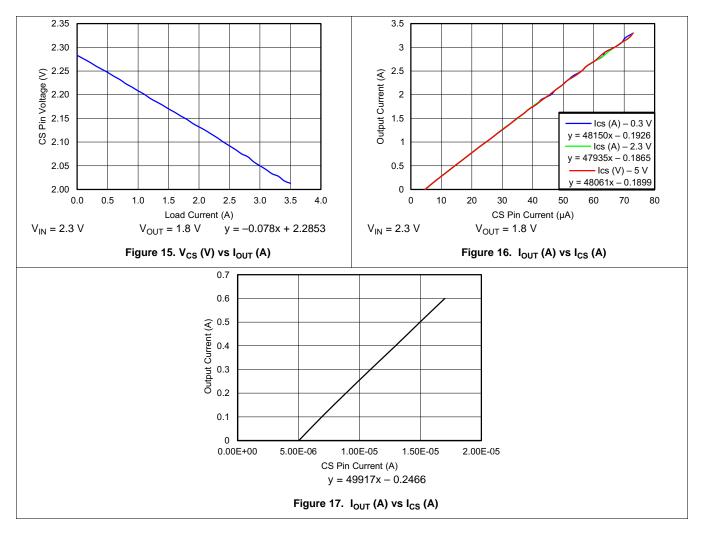
For TPS7H1101-SP, Figure 15 shows the typical curve V_{CS} vs I_{OUT} for V_{IN} = 2.28 V and R_{CS} = 3.65 k Ω . A resistor connected from the CS terminal to V_{IN} indicates voltage proportional to the output current.

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Monitoring current in the CS terminal (I_{CS} vs I_{OUT}) indicates the current sense ratio between the main PMOSFET and the current sense MOSFET as shown in Figure 16.

Figure 17 shows I_{OUT} vs I_{CS} when the voltage on CS terminal is varied from 0.3 V to 7 V.



9.2.2.4 Current Foldback

- 1. The TPS7H1101-SP has a current foldback feature which can be enabled when the CS terminal is held high. Shorting CS low disables the foldback current limit. If the foldback current limit is disabled, then the LDO will begin regulating again as soon as the current falls below the clamp threshold.
- 2. With foldback current limit enabled, when current limit trip point is activated,
 - (a) Output voltage drops low.
 - (b) Output current folds back to approximately 50% of the current limit trip point.

This results in minimizing the power loss under fault conditions. Monitoring the voltage at the CS terminal indicates voltage proportional to the output current.



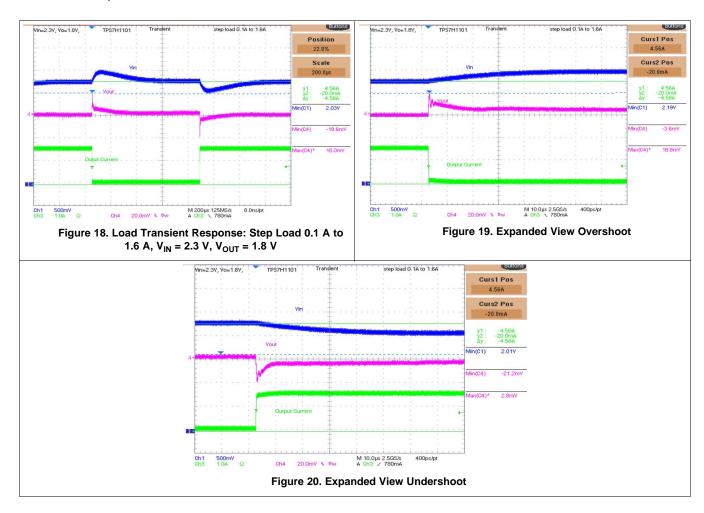
9.2.2.5 Transient Response

Figure 18, Figure 19, and Figure 20 indicate the transient response behavior of the LDO for 50% step load change.

Channel 1: Input Voltage

Channel 2: Output voltage overshoot/undershoot

Channel 3: Step load in current



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9.2.2.6 Current Sharing

For demanding load requirements, multiple LDOs can be paralleled as indicated in Figure 22. In parallel mode, the CS terminal of LDO1 must be connected to the PCL terminal of LDO2 via a series resistor R_{CL} , and CS terminal of LDO2 must be connected to PCL terminal of LDO1 via series resistor R_{CL} . The typical value of R_{CL} in parallel operation is 3.75 k Ω for current limit > 6 A. In parallel configuration, R_{CL} (resistor from PCL to GND) and R_{CS} (resistor from CS terminal to V_{IN}) must be left open (unpopulated). The R_{CL} value must be selected so that the operating condition of the CS terminal is maintained, as specified in the *Electrical Characteristics* table. The current from PCL through RCL of LDO1 is determined by the output load current of LDO2 divided by the CSR. Hence, the voltage at CS terminal of the LDO1 is 0.605 V – ((output load current of LDO2 + 0.2458) / CSR × R_{CL}).

Alternately, it can also provide twice the output current to meet system needs. When using two LDOs in parallel operation for higher output load current, use POL TPS50601-SP as an input source.

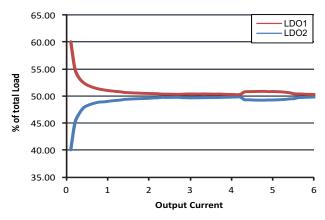


Figure 21. LDO Current Share



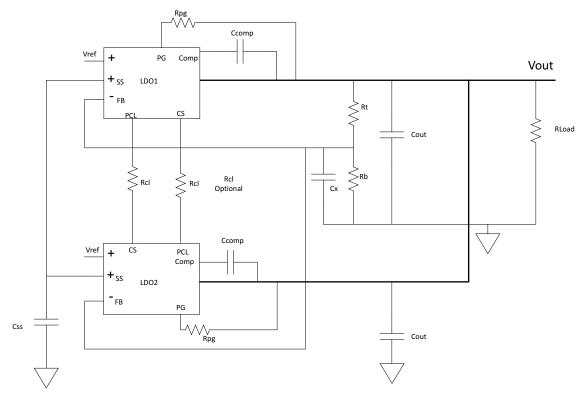


Figure 22. Block Diagram (Parallel Operation)



9.2.2.7 Compensation

Figure 23 shows a generic block diagram for TPS7H1101-SP LDO with external compensation components. LDO incorporates nested loops, thus providing the high gain necessary to meet design performance.

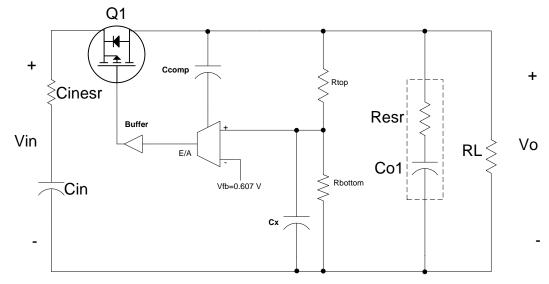


Figure 23. TPS7H1101-SP Compensation

Resistor divider composed of R_{top} and R_{bottom} determine the output voltage set points as indicated by Equation 3. Output capacitor C_{OUT} introduces a pole and a zero as shown in the following.

$$F_{p_co} = \frac{1}{2 \cdot \pi \cdot C_o \cdot R_L}$$

$$F_{z_co} = \frac{1}{2 \cdot \pi \cdot C_o \cdot C_{esr}}$$
(8)

The TPS7H1101-SP was designed so that the ESR of the output capacitor will not have a strong influence on the response of the LDO. However, an optional capacitor, C_x , can be added in parallel with the bottom feedback resistor to introduce a pole to cancel F_{z_co} . Equation 9 shows how to calculate the location of the pole introduced by C_x . To cancel the zero directly, F_p should be equal to F_{z_co} .

$$F_p = \frac{1}{2 \cdot \pi \cdot C_x \cdot R_{bottom}} \tag{9}$$

 C_x is calculated to be 1000 pF for $C_0 = 220 \mu F$, $C_{esr} = 45 \text{ m}\Omega$, and $R_{bottom} = 10 \text{ k}\Omega$.

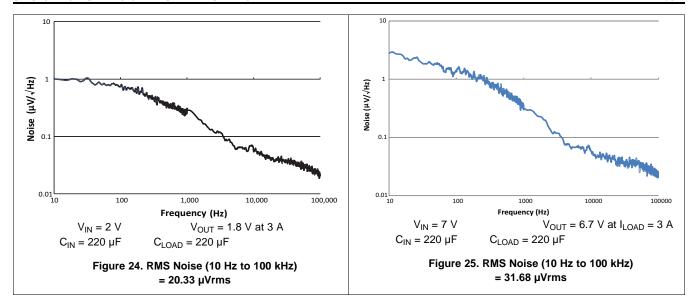
Internal compensation in the LDO cancels the output capacitor pole introduced by C_{OUT} and R_L.

C_{comp} introduces a dominant pole at low frequency. TI recommends that a C_{comp} value of 10 nF.

9.2.2.8 Output Noise

Output noise is measured using an HP3495A. Figure 24, Figure 25, , and show noise of the TPS7H1101-SP in $\mu V/\sqrt{Hz}$ vs frequency.





9.2.2.9 Capacitors

TPS7H1101-SP requires the use of a combination of tantalum and ceramic capacitors to achieve good volume to capacitance ratio. Table 3 highlights some of the capacitors used in the device. TI recommends to follow proper derating guidelines as recommended by the capacitor manufacturer based upon output voltage and operating temperature.

Note that polymer-based tantalum capacitors must be derated to at least 60% of rated voltage, whereas manganese oxide (MnO₂) based tantalum capacitors should be derated to 33% of rated voltage depending upon the operating temperature.

TI recommends to use a tantalum capacitor along with a 0.1- μ F ceramic capacitor. The device is stable for input and output tantalum capacitor values of 10 to 220 μ F with the ESR range of 10 m Ω to 2 Ω . However, the dynamic performance of the device varies based on load conditions and the capacitor values used.

TI recommends a minimum output capacitor of 22 μF with ESR of 1 Ω or less to prevent oscillations. X7R dielectrics are preferred. See Table 3 for various capacitor recommendations.

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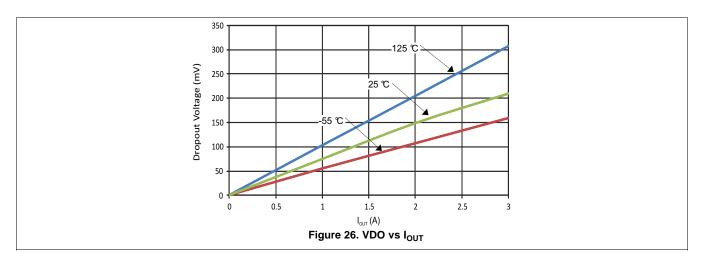


Table 3. TPS7H1101-SP Capacitors

CAPACITOR PART NUMBER	CAPACITOR DETAILS (CAPACITOR, VOLTAGE, ESR)	TYPE	VENDOR
T493X107K016CH612A ⁽¹⁾	100 μF, 16 V, 100 mΩ	Tantalum - MnO2	Kemet
T493X226M025AH6x20 ⁽¹⁾	22 μF, 25 V, 35 m Ω	Tantalum - MnO2	Kemet
T525D476M016ATE035 ⁽¹⁾	47 μF, 10 V, 35 m Ω	Tantalum - Polymer	Kemet
T540D476M016AH6520 ⁽¹⁾	47 μF, 16 V, 20 mΩ	Tantalum - Polymer	Kemet
T525D107M010ATE025 ⁽¹⁾	100 μF, 10 V, 25 mΩ	Tantalum - Polymer	Kemet
T541X337M010AH6720 ⁽¹⁾	330 μF, 10 V, 6 mΩ	Tantalum - Polymer	Kemet
T525D227M010ATE025 ⁽¹⁾	220 μF, 10 V, 25 mΩ	Tantalum - Polymer	Kemet
T495X107K016ATE100 ⁽¹⁾	100 μF, 16 V, 100 mΩ	Tantalum - MnO2	Kemet
CWR29FK227JTHC ⁽¹⁾	220 μF, 10 V, 180 mΩ	Tantalum - MnO2	AVX
THJE107K016AJH	100 μF, 16 V, 58 mΩ	Tantalum	AVX
THJE227K010AJH	220 μF, 10 V, 40 mΩ	Tantalum	AVX
SMX33C336KAN360	33 μF, 25 V	Stacked ceramic	AVX
SR2225X7R335K1P5#M123	3.3 μF, 25 V, 10 mΩ	Ceramic	Presidio Components Inc

⁽¹⁾ Operating temperature is -55° C to 125° C.

9.2.3 Application Curves





10 Power Supply Recommendations

This device is designed to operate with an input voltage supply up to 7 V. The minimum input voltage should provide adequate headroom greater than the dropout voltage for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

11 Layout

11.1 Layout Guidelines

- For best performance, all traces should be as short as possible, and no longer than 5 cm.
- Use wide traces for IN, Out and GND to minimize the parasitic electrical effects.
- Place the output capacitors (COUT) as close as possible to the OUT pin of the device.

11.2 Layout Example

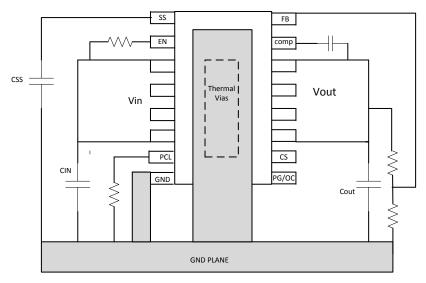


Figure 27. PCB Layout Example



12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

(1) Stability Assessment of Fixed Regulators - Tom Boehler, Paul Ho, AEi Systems

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community T's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.



13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Device Nomenclature

KGD Known good die

RHA Radiation hardness assurance for space systems

5962R13202 Same device as TPS50601-SP, shown with standard microcircuit drawing (SMD)

TPS7H1101-SP Same device as 5962R10221, shown with TI package drawing

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
5962-1320201VXC	NRND	Production	CFP (HKR) 16	25 TUBE	ROHS Exempt	NIAU	N/A for Pkg Type	-55 to 125	5962-1320201VXC TPS7H1101-SP
5962R1320201VXC	NRND	Production	CFP (HKR) 16	25 TUBE	ROHS Exempt	NIAU	N/A for Pkg Type	-55 to 125	5962R1320201VXC TPS7H1101-RHA

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE MATERIALS INFORMATION

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TUBE

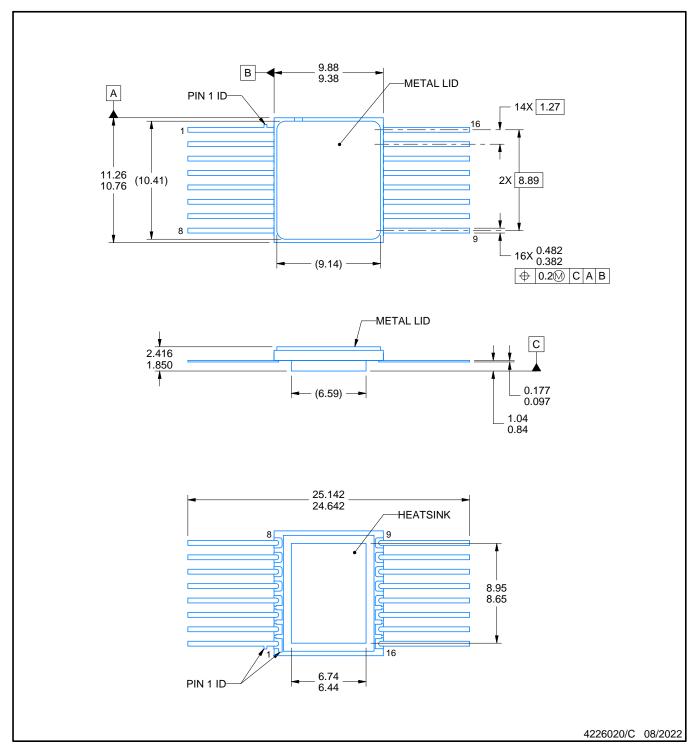


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-1320201VXC	HKR	CFP	16	25	506.98	26.16	6220	NA
5962R1320201VXC	HKR	CFP	16	25	506.98	26.16	6220	NA



CERAMIC DUAL FLATPACK

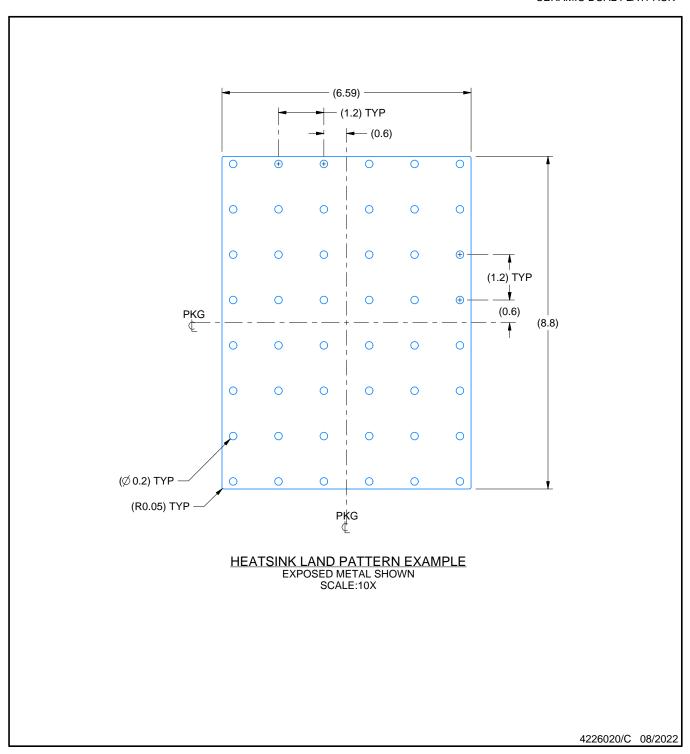


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
 This package is hermetically sealed with a metal lid. Lid is connected to Heatsink.
- 4. The terminals are gold plated.
- 5. Falls within MIL-STD-1835 CDFP-F11A.



CERAMIC DUAL FLATPACK



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