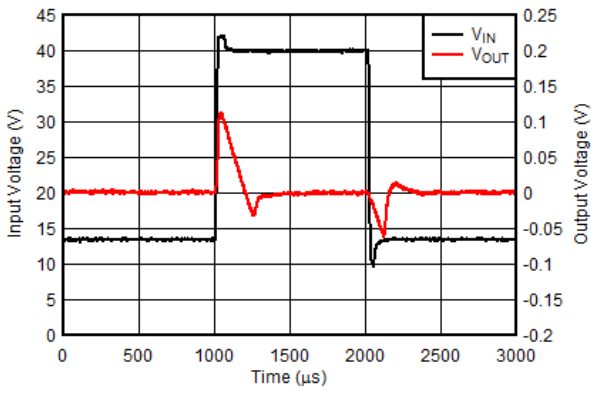
TPS7B87-Q1 Automotive, 500mA, 40V, Low-Dropout Regulator With Power-Good

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
  - Junction temperature: –40°C to +150°C, T_J
- Input voltage range: 3V to 40V (42V max)
- Output voltage range: 3.3V and 5V (fixed)
- Maximum output current: 500mA
- Output voltage accuracy: ±0.85% (max)
- Low dropout voltage:
  - 475mV (max) at 450mA
- Low quiescent current:
  - 17µA (typ) at light loads
- Excellent line transient response:
  - ±2% V_{OUT} deviation during cold-crank
  - ±2% V_{OUT} deviation (1V/µs V_{IN} slew rate)
- Power-good with programmable delay period
- Stable with a 2.2µF or larger capacitor
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Package options:
  - 5-pin TO-252 package: 29.7°C/W $R_{\theta JA}$
  - 8-pin HSOIC-8 package with thermal pad: 41.8°C/W $R_{\theta JA}$

2 Applications

- Reconfigurable instrument clusters
- Body control modules (BCM)
- Always-on battery-connected applications:
  - Automotive gateways
  - Remote keyless entries (RKE)



Line Transient Response (3V/µs V_{IN} Slew Rate)

3 Description

The TPS7B87-Q1 is a low-dropout linear regulator designed to connect to the battery in automotive applications. The device has an input voltage range extending to 40V, which allows the device to withstand transients (such as load dumps) that are anticipated in automotive systems. With only a 17µA quiescent current at light loads, the device is designed for powering always-on components such as microcontrollers (MCUs) and controller area network (CAN) transceivers in standby systems.

The device has state-of-the-art transient response that allows the output to quickly react to changes in load or line (for example, during cold-crank conditions). Additionally, the device has a novel architecture that minimizes output overshoot when recovering from dropout. During normal operation, the device has a tight DC accuracy of ±0.85% over line, load, and temperature.

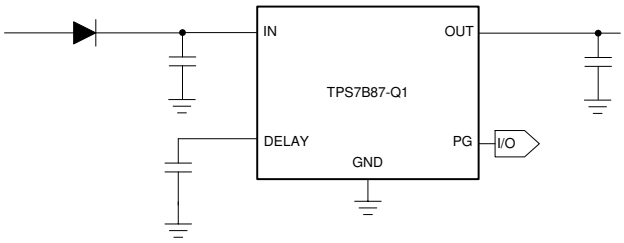
The power-good delay can be adjusted by external components, allowing the delay time to be configured to fit application-specific systems.

The device is available in thermally conductive packaging to allow the device to efficiently transfer heat to the circuit board.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS7B87-Q1	DDA (HSOIC, 8)	4.90mm × 6.00mm
	KVU (TO-252, 5)	6.60mm × 10.11mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Output Equal to Reference Voltage

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4 Pin Configuration and Functions

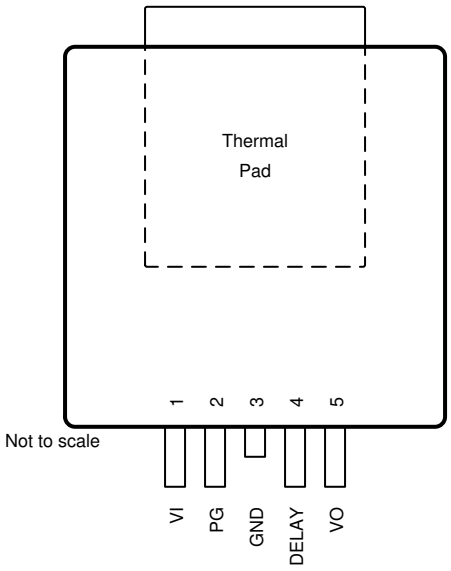


Figure 4-1. KVU Package, 5-Pin TO-252, Top View

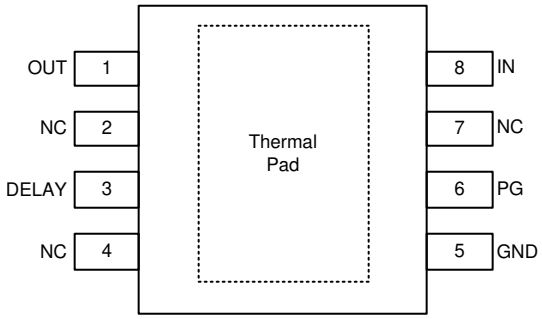


Figure 4-2. DDA Package, 8-Pin HSOIC, Top View

Table 4-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	KVU	DDA		
DELAY	4	3	I	Power-good delay adjustment pin. Connect a capacitor from this pin to GND to set the PG reset delay. Leave this pin floating for a default ($t_{(DLY\_FIX)}$) delay. See the *Power-Good (PG)* section for more information. If this functionality is not desired, leave this pin floating because connecting this pin to GND causes a permanent increase in the GND current.
GND	3	5	G	Ground reference
NC	—	2, 4, 7	—	No internal connection. This pin can be left floating or tied to GND for best thermal performance.
PG	2	6	I	Power-good pin. This pin has an internal pullup resistor. Do not connect this pin to V_{OUT} or any other biased voltage rail. V_{PG} is logic level high when V_{OUT} is above the power-good threshold. See the *Power-Good (PG)* section for more information.
IN	1	8	P	Input power-supply voltage pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to GND as listed in the *Recommended Operating Conditions* table and the *Input Capacitor* section. Place the input capacitor as close to the input of the device as possible.
OUT	5	1	O	Regulated output voltage pin. A capacitor is required from OUT to GND for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to GND; see the *Recommended Operating Conditions* table and the *Output Capacitor* section. Place the output capacitor as close to output of the device as possible. If using a high equivalent series resistance (ESR) capacitor, decouple the output with a 100nF ceramic capacitor.
Thermal pad	Pad	Pad	—	Connect the thermal pad to a large area GND plane for improved thermal performance.

(1) I = input; O = output; P = power; G = ground.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Unregulated input	–0.3	42	V
V_{OUT}	Regulated output	–0.3	V_{IN} + 0.3V(2)	V
Delay	Reset delay input, power-good adjustable threshold	–0.3	6	V
PG	Power-good output	–0.3	20	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

(2) The absolute maximum rating is VIN + 0.3V or 20V, whichever is smaller

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordancewith the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	3		40	V
V_{OUT}	Output voltage	1.2		18	V
I_{OUT}	Output current	0		500	mA
V_{Delay}	Delay pin voltage, power-good adjustable threshold	0		5.5	V
V_{PG}	Power-good output pin	0		18	V
C_{OUT}	Output capacitor(2)	2.2		220	µF
ESR	Output capacitor ESR requirements	0.001		2	Ω
C_{IN}	Input capacitor(1)	0.1	1		µF
C_{Delay}	Power-good delay capacitor			1	µF
T_J	Operating junction temperature	–40		150	°C

(1) For robust EMI performance the minimum input capacitance is 500nF.
(2) Effective output capacitance of 1 µF minimum required for stability.

5.4 Thermal Information

THERMAL METRIC(1) (2)		TPS7B87-Q1			UNIT
		KVU	DDA		
		5 PINS	8 PINS (ASO : ASE) (3)	8 PINS (ASO : FMX) (3)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.7	41.8	42.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.2	55	57.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.6	17.3	17.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.9	4.5	5.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.5	17.3	17.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.5	5.7	7.5	°C/W

(1) The thermal data is based on the JEDEC standard high K profile, JESD 51-7. Two-signal, two-plane, four-layer board with 2oz. copper. The copper pad is soldered to the thermal land pattern. Also, correct attachment procedure must be incorporated.
(2) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(3) See nomenclature table for more information regarding ASO

5.5 Electrical Characteristics

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 0mA, C_{OUT} = 2.2 µF, 1mΩ < C_{OUT} ESR < 2Ω, C_{IN} = 1 µF typical values are at T_J = 25°C

PARAMETER		Test Conditions		MIN	TYP	MAX	UNIT
V_{OUT}	Regulated output	V_{IN} = V_{OUT} + 1V to 40V, I_{OUT} = 100 µA to 450mA, T_J = 25ºC(1)		–0.85		0.85	%
		V_{IN} = V_{OUT} + 1V to 40V, I_{OUT} = 100 µA to 500mA, T_J = 25ºC(1)		–0.85		0.85	
		V_{IN} = V_{OUT} + 1V to 40V, I_{OUT} = 100 µA to 450mA(1)		–1.15		1.15	
		V_{IN} = V_{OUT} + 1V to 40V, I_{OUT} = 100 µA to 500mA(1)		–1.15		1.15	
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation (B Version)	V_{IN} = V_{OUT} + 1V, I_{OUT} = 100 µA to 450mA , V_{OUT} ≥ 3.3V				0.45	%
		V_{IN} = V_{OUT} + 1V, I_{OUT} = 100 µA to 500mA , V_{OUT} ≥ 3.3V				0.475	%
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	V_{IN} = V_{OUT} + 1V, I_{OUT} = 100 µA to 450mA , V_{OUT} ≥ 3.3V				0.425	%
		V_{IN} = V_{OUT} + 1V, I_{OUT} = 100 µA to 500mA , V_{OUT} ≥ 3.3V				0.45	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	V_{IN} = V_{OUT} + 1V to 40V, I_{OUT} = 100 µA				0.2	%
ΔV_{OUT}	Load transient response settling time(2)	t_R = t_F = 1 µs; C_{OUT} = 10 µF, V_{OUT} ≥ 3.3V				100	µs
ΔV_{OUT}	Load transient response overshoot, undershoot(2)	t_R = t_F = 1 µs; C_{OUT} = 10 µF	I_{OUT} = 150mA to 350mA	–2%			%V_{OUT}
			I_{OUT} = 350mA to 150mA			10%	
			I_{OUT} = 0mA to 500mA	–10%			
I_Q	Quiescent current	V_{IN} = V_{OUT} + 1V to 40V, I_{OUT} = 0mA, T_J = 25ºC(3)			17	21	µA
		V_{IN} = V_{OUT} + 1V to 40V, I_{OUT} = 0mA(3)				26	
		I_{OUT} = 500 µA				35	
V_{DO}	Dropout voltage fixed output voltages (DDA Package)	I_{OUT} ≤ 1mA, V_{OUT} ≥ 3.3V, V_{IN} = $V_{OUT(NOM)}$ x 0.95				43	mV
		I_{OUT} = 315mA, V_{OUT} ≥ 3.3V, V_{IN} = $V_{OUT(NOM)}$			260	360	
		I_{OUT} = 450mA, V_{OUT} ≥ 3.3V, V_{IN} = $V_{OUT(NOM)}$			335	475	
		I_{OUT} = 500mA, V_{OUT} ≥ 3.3V, V_{IN} = $V_{OUT(NOM)}$			360	535	
V_{DO}	Dropout voltage fixed output voltages (KVU Package)	I_{OUT} ≤ 1mA, V_{OUT} ≥ 3.3V, V_{IN} = $V_{OUT(NOM)}$ x 0.95				46	mV
		I_{OUT} = 315mA, V_{OUT} ≥ 3.3V, V_{IN} = $V_{OUT(NOM)}$			275	400	
		I_{OUT} = 450mA, V_{OUT} ≥ 3.3V, V_{IN} = $V_{OUT(NOM)}$			360	525	
		I_{OUT} = 500mA, V_{OUT} ≥ 3.3V, V_{IN} = $V_{OUT(NOM)}$			390	575	
$V_{UVLO(RISING)}$	Rising input supply UVLO	V_{IN} rising		2.6	2.7	2.82	V
$V_{UVLO(FALLING)}$	Falling input supply UVLO	V_{IN} falling		2.38	2.5	2.6	V
$V_{UVLO(HYST)}$	$V_{UVLO(IN)}$ hysteresis				230		mV
I_{CL}	Output current limit	V_{IN} = V_{OUT} + 1V, V_{OUT} short to 90% x $V_{OUT(NOM)}$		540		780	mA
PSRR	Power supply rejection ratio	V_{IN} - V_{OUT} = 1V, frequency = 1kHz, I_{OUT} = 450mA			70		dB
R_{PG}	Power-good internal pull up resistor			10	30	50	kΩ
$V_{PG(OL)}$	PG pin low level output voltage	V_{OUT} ≤ 0.83x V_{OUT}				0.4	V
$V_{PG(TH,RISING)}$	Default power-good threshold	V_{OUT} rising		85		95	%V_{OUT}
$V_{PG(TH,FALLING)}$	Default power-good threshold	V_{OUT} falling		83		93	
$V_{PG(HYST)}$	Power-good hysteresis				2		
$V_{DLY(TH)}$	Threshold to release power-good high	Voltage at DELAY pin rising		1.17	1.21	1.25	V
$I_{DLY(CHARGE)}$	Delay capacitor charging current	Voltage at DELAY pin = 1V		1	1.5	2	µA
T_J	Junction temperature			–40		150	°C
$T_{SD(SHUTDOWN)}$	Junction shutdown temperature				175		°C
$T_{SD(HYST)}$	Hysteresis of thermal shutdown				20		°C

(1) Power dissipation is limited to 2W for device production testing purposes. The power dissipation can be higher during normal operation. See the thermal dissipation section for more information on how much power the device can dissipate while maintaining a junction temperature below 150°C.
(2) Specified by design.
(3) For the adjustable output this is tested in unity gain and resistor current is not included.

5.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIMING POWER-GOOD						
$t_{(DLY\_FIX)}$	Power-good propagation delay	No capacitor connect at DELAY pin		100		µs
$t_{(Deglitch)}$	Power-good deglitch time	No capacitor connect at DELAY pin		90		µs
$t_{(DLY)}$	Power-good propagation delay	Delay capacitor value: $C_{(DELAY)}$ = 100nF		80		ms

5.7 Typical Characteristics

specified at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT} ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted)

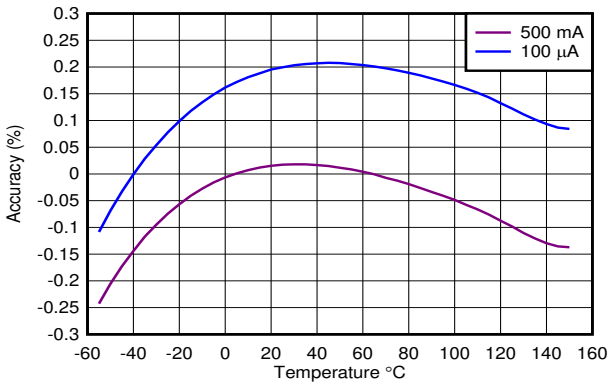
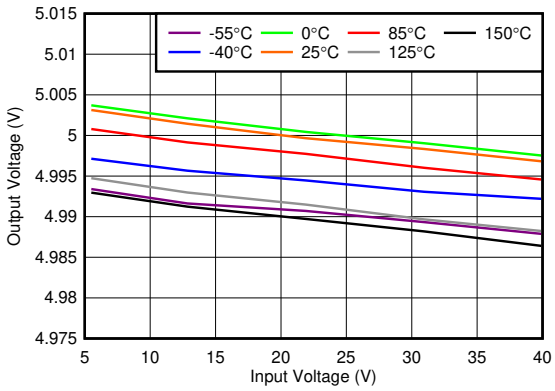
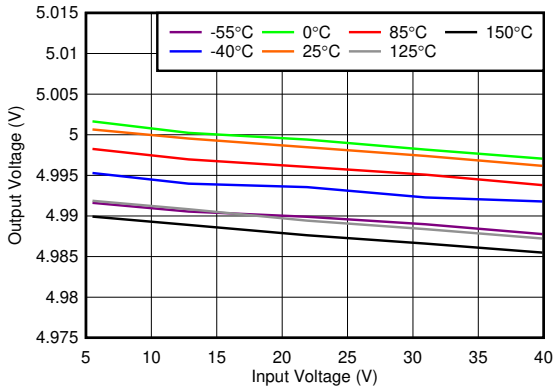


Figure 5-1. Accuracy vs Temperature



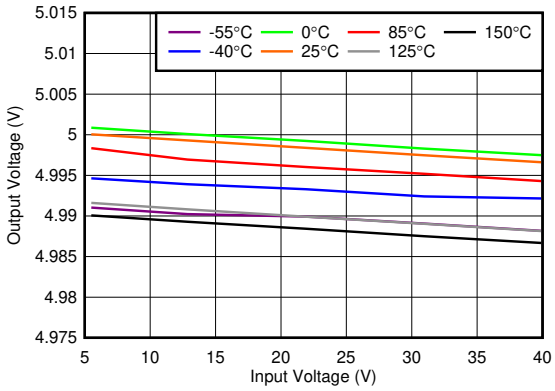
V_{OUT} = 5V, I_{OUT} = 150mA

Figure 5-2. Line Regulation vs V_{IN}



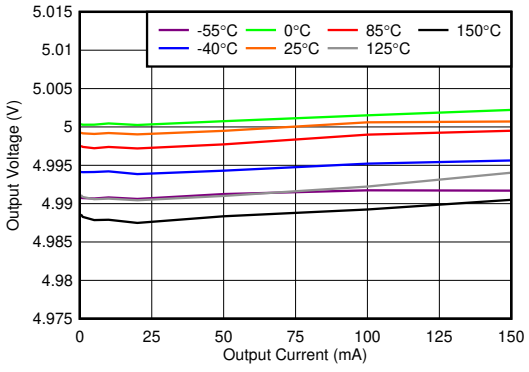
V_{OUT} = 5V, I_{OUT} = 5mA

Figure 5-3. Line Regulation vs V_{IN}



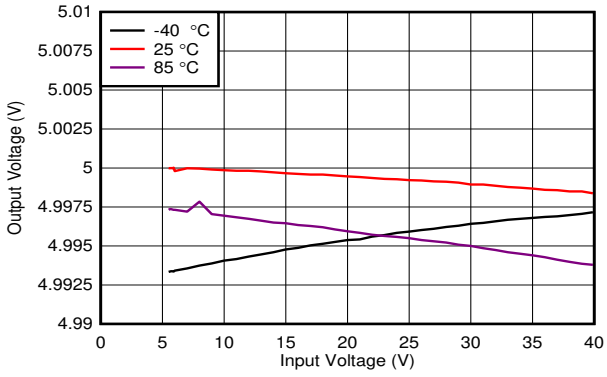
V_{OUT} = 5V, I_{OUT} = 1mA

Figure 5-4. Line Regulation vs V_{IN}



V_{OUT} = 5V

Figure 5-5. Load Regulation vs I_{OUT}

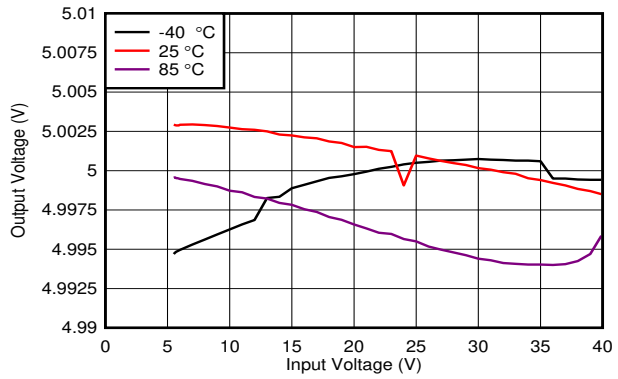


C_{OUT} = 10µF, V_{OUT} = 5V

Figure 5-6. Line Regulation at 50mA

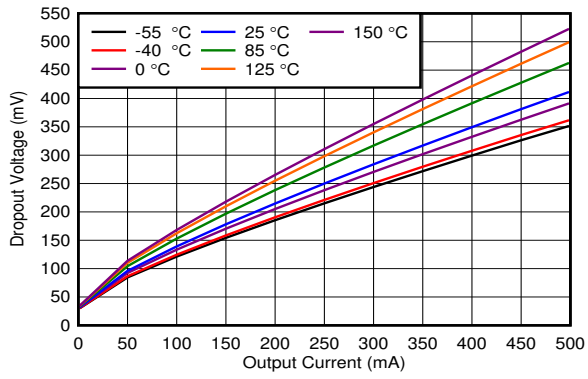
5.7 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT} ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted)



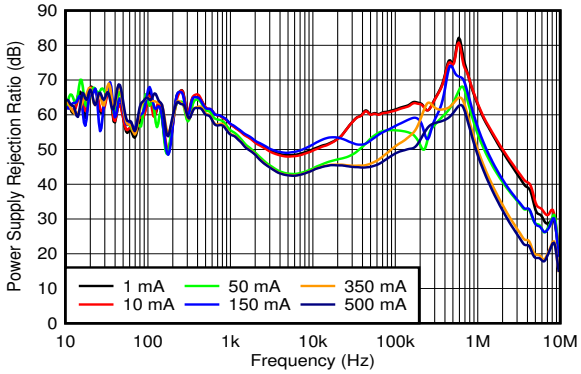
C_{OUT} = 10µF, V_{OUT} = 5V

Figure 5-7. Line Regulation at 100mA



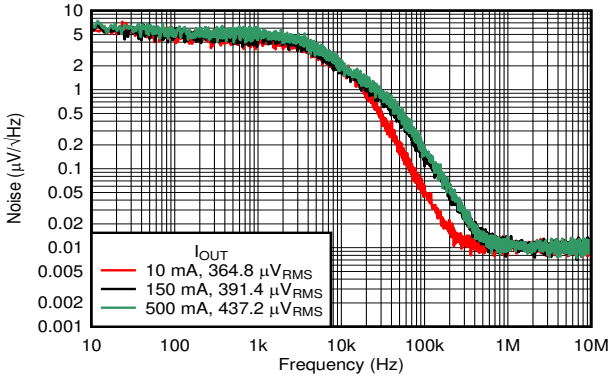
V_{IN} = 3V

Figure 5-8. Dropout Voltage (V_{DO}) vs I_{OUT}



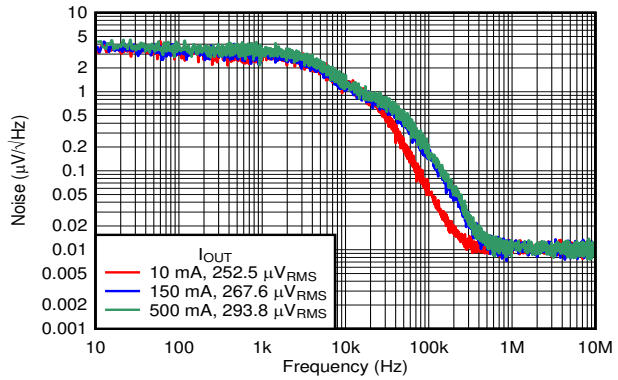
C_{OUT} = 10µF (X7R 50V), V_{OUT} = 5V

Figure 5-9. PSRR vs Frequency and I_{OUT}



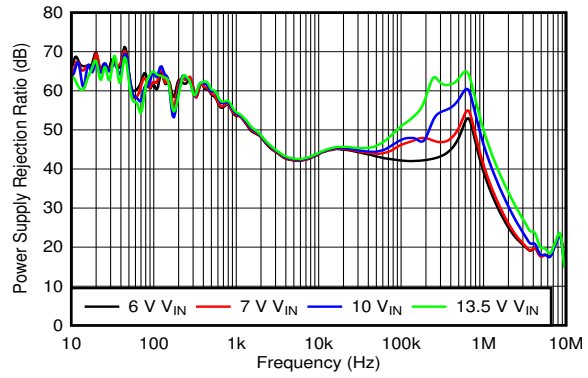
C_{OUT} = 10µF (X7R 50V), V_{OUT} = 5V

Figure 5-10. Noise vs Frequency



C_{OUT} = 10µF (X7R 50V), V_{OUT} = 3.3V

Figure 5-11. Noise vs Frequency

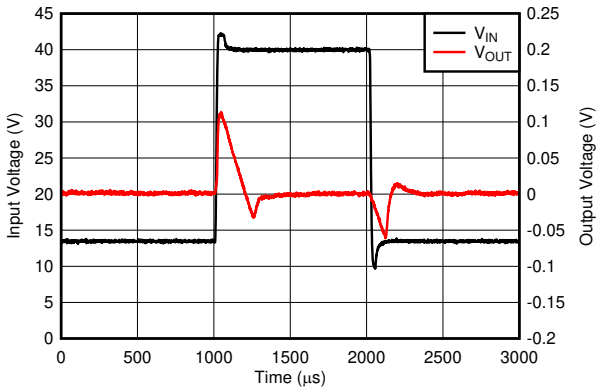


C_{OUT} = 10µF (X7R 50V), I_{OUT} = 500mA, V_{OUT} = 5V

Figure 5-12. PSRR vs Frequency and V_{IN}

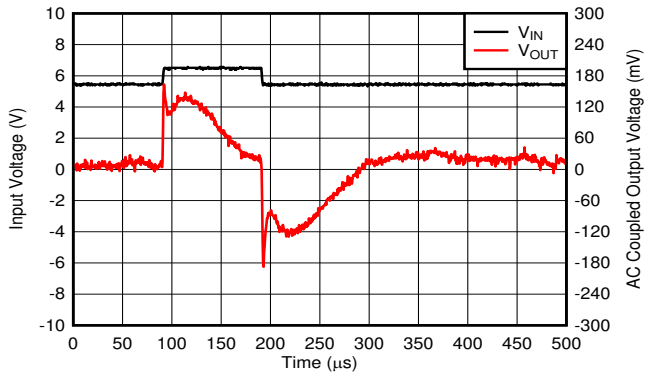
5.7 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT} ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted)



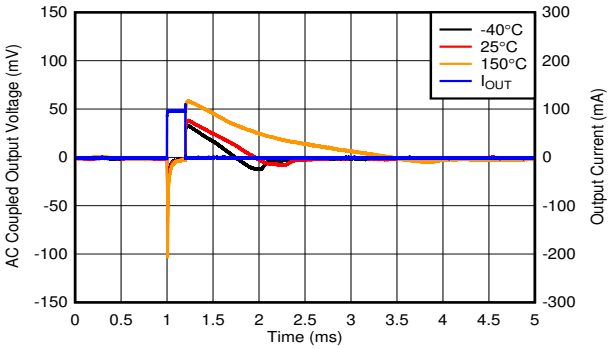
V_{OUT} = 5V, I_{OUT} = 1mA, V_{IN} = 13.5V to 45V, slew rate = 2.7V/µs

Figure 5-13. Line Transients



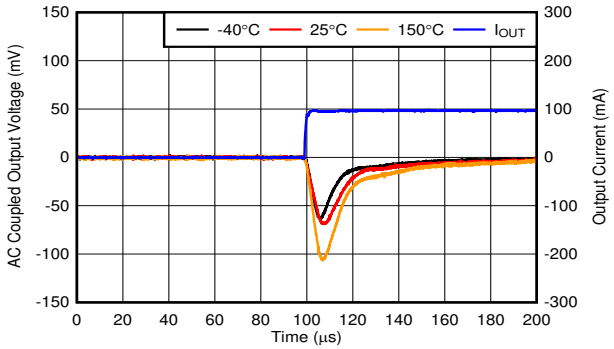
V_{OUT} = 5V, I_{OUT} = 100mA, V_{IN} = 5.5V to 6.5V, rise time = 1µs

Figure 5-14. Line Transients



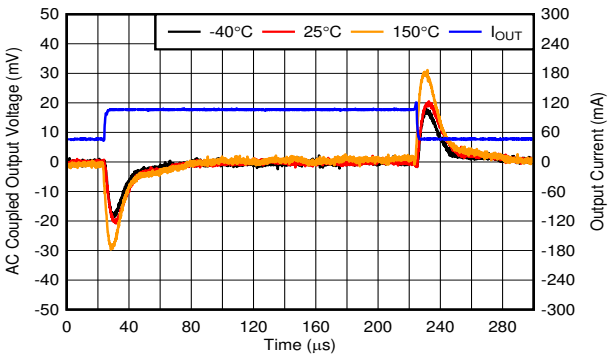
V_{OUT} = 5V, I_{OUT} = 0mA to 100mA, slew rate = 1A/µs, C_{OUT} = 10µF

Figure 5-15. Load Transient, No Load to 100mA



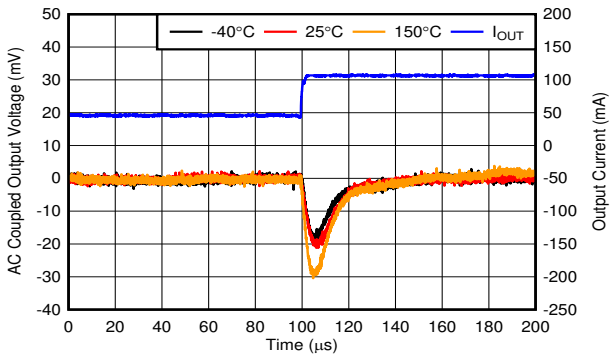
V_{OUT} = 5V, I_{OUT} = 0mA to 100mA, slew rate = 1A/µs, C_{OUT} = 10µF

Figure 5-16. Load Transient, No Load to 100mA Rising Edge



V_{OUT} = 5V, I_{OUT} = 45mA to 105mA, slew rate = 0.1A/µs, C_{OUT} = 10µF

Figure 5-17. Load Transient, 45mA to 105mA

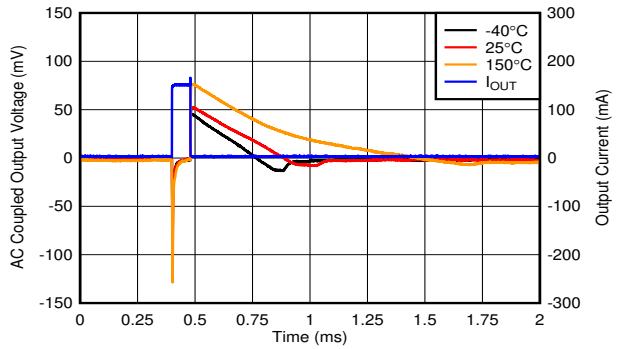


V_{OUT} = 5V, I_{OUT} = 45mA to 105mA, slew rate = 0.1A/µs, C_{OUT} = 10µF

Figure 5-18. Load Transient, 45mA to 105mA Rising Edge

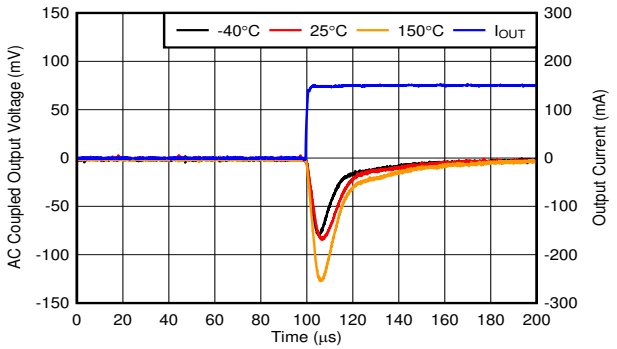
5.7 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT} ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted)



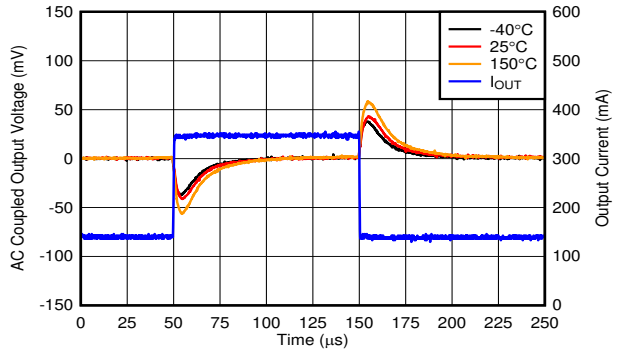
V_{OUT} = 5V, I_{OUT} = 0mA to 150mA, slew rate = 1A/µs, C_{OUT} = 10µF

Figure 5-19. Load Transient, No Load to 150mA



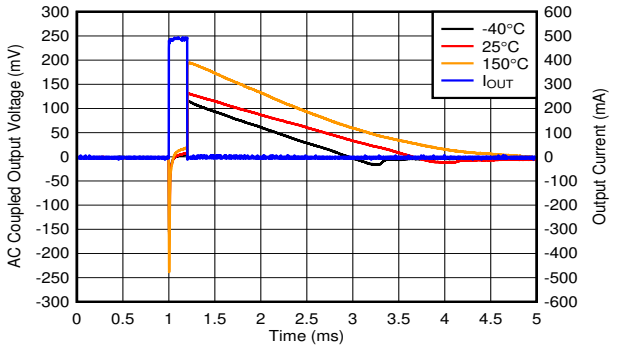
V_{OUT} = 5V, I_{OUT} = 0mA to 150mA, slew rate = 1A/µs, C_{OUT} = 10µF

Figure 5-20. Load Transient, No Load to 150mA Rising Edge



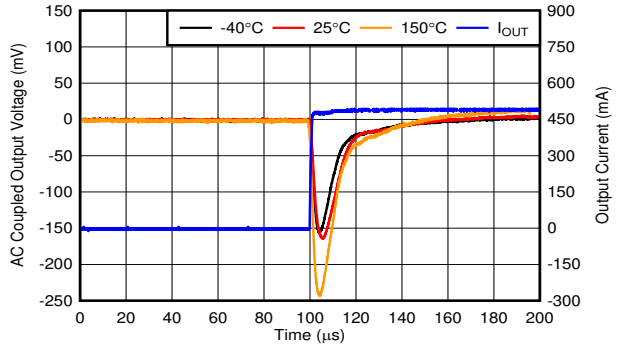
V_{OUT} = 5V, I_{OUT} = 150mA to 350mA, slew rate = 0.1A/µs, C_{OUT} = 10µF

Figure 5-21. Load Transient, 150mA to 350mA



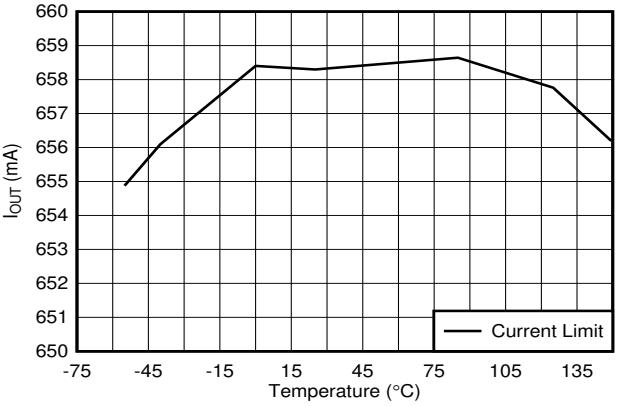
V_{OUT} = 5V, I_{OUT} = 0mA to 500mA, slew rate = 1A/µs, C_{OUT} = 10µF

Figure 5-22. Load Transient, No Load to 500mA



V_{OUT} = 5V, I_{OUT} = 0mA to 500mA, slew rate = 1A/µs, C_{OUT} = 10µF

Figure 5-23. Load Transient, No Load to 500mA Rising Edge



V_{IN} = V_{OUT} + 1V, V_{OUT} = 90% × $V_{OUT(NOM)}$

Figure 5-24. Output Current Limit vs Temperature

5.7 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT} ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted)

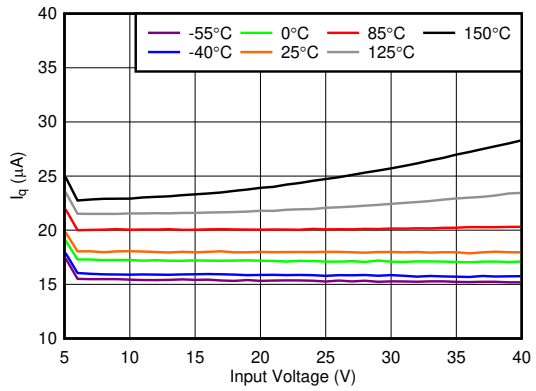


Figure 5-25. Quiescent Current (I_Q) vs V_{IN}

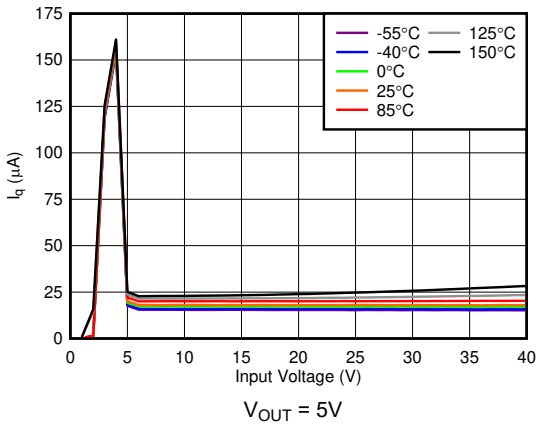


Figure 5-26. Quiescent Current (I_Q) vs V_{IN}

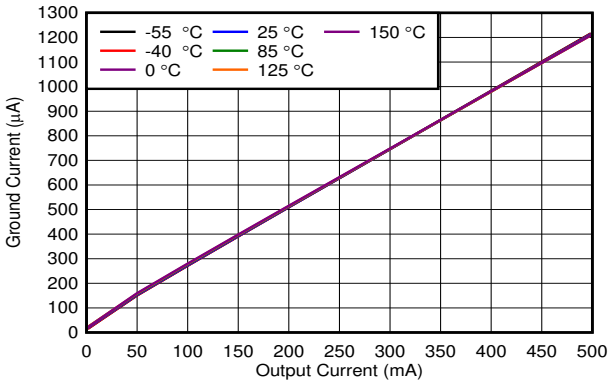


Figure 5-27. Ground Current (I_{GND}) vs I_{OUT}

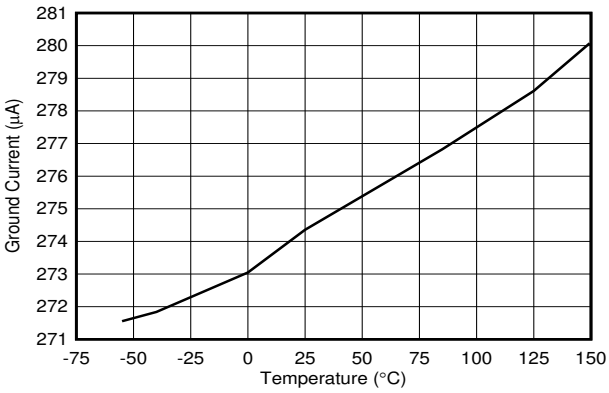


Figure 5-28. Ground Current at 100mA

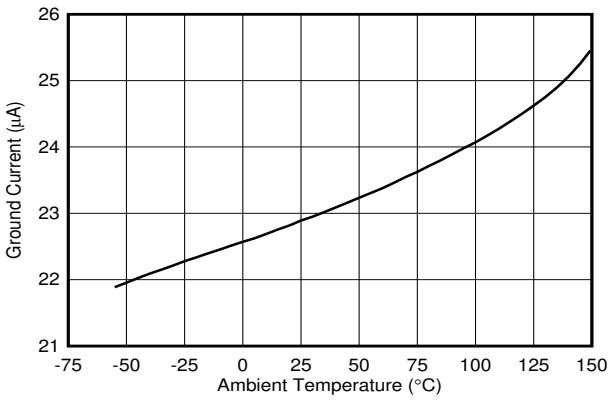


Figure 5-29. Ground Current at 500µA

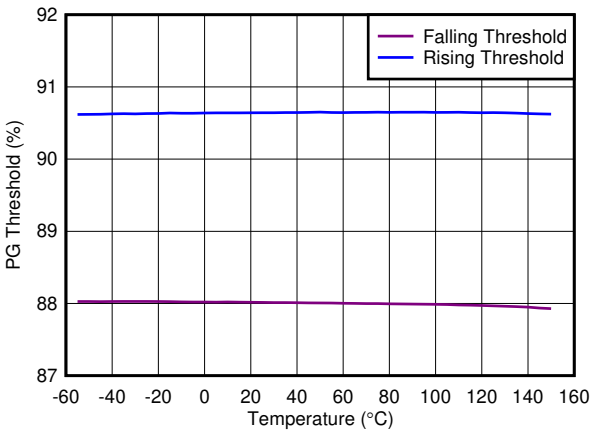
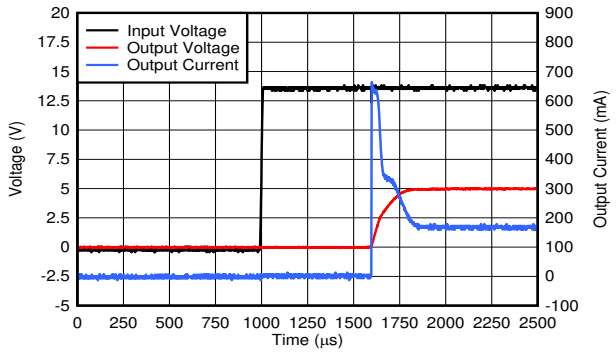


Figure 5-30. PG Threshold vs Temperature

5.7 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT} ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted)



V_{IN} = 13.5V, V_{OUT} = 5V, I_{OUT} = 150mA, C_{OUT} = 10µF

Figure 5-31. Start-Up Plot Inrush Current

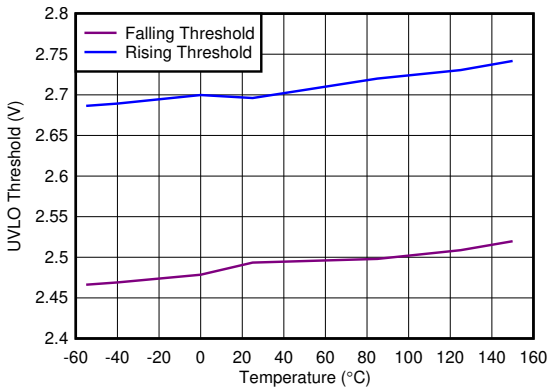
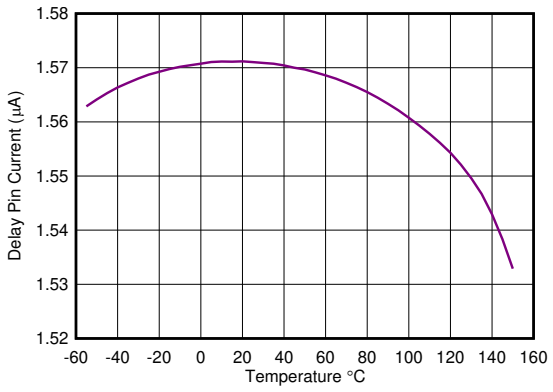


Figure 5-32. Undervoltage Lockout (UVLO) Threshold vs Temperature



V_{DELAY} = 1V

Figure 5-33. Delay Pin Current vs Temperature

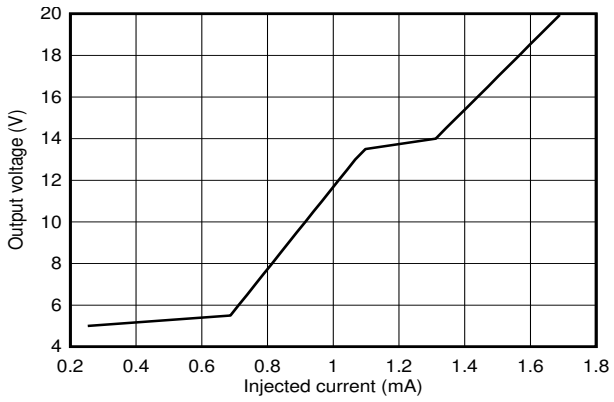


Figure 5-34. Output Voltage vs Injected Current

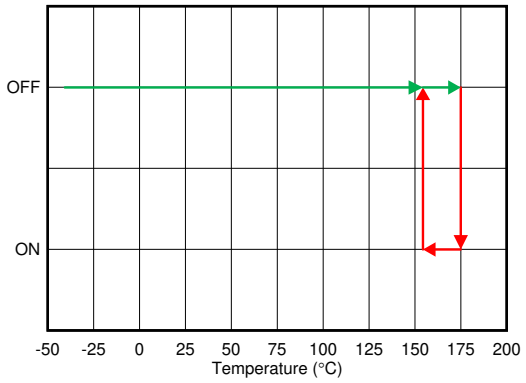


Figure 5-35. Thermal Shutdown

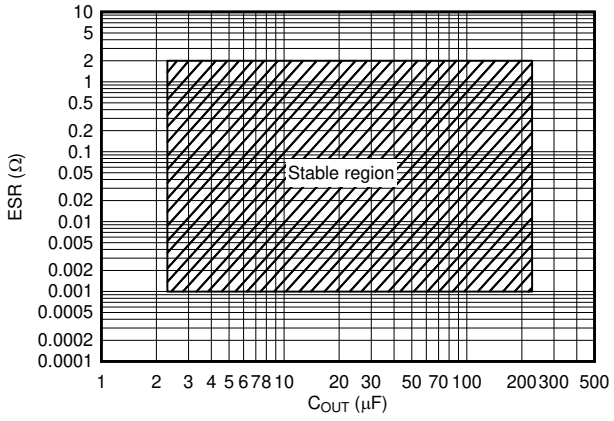


Figure 5-36. Stability, ESR vs C_{OUT}

6 Detailed Description

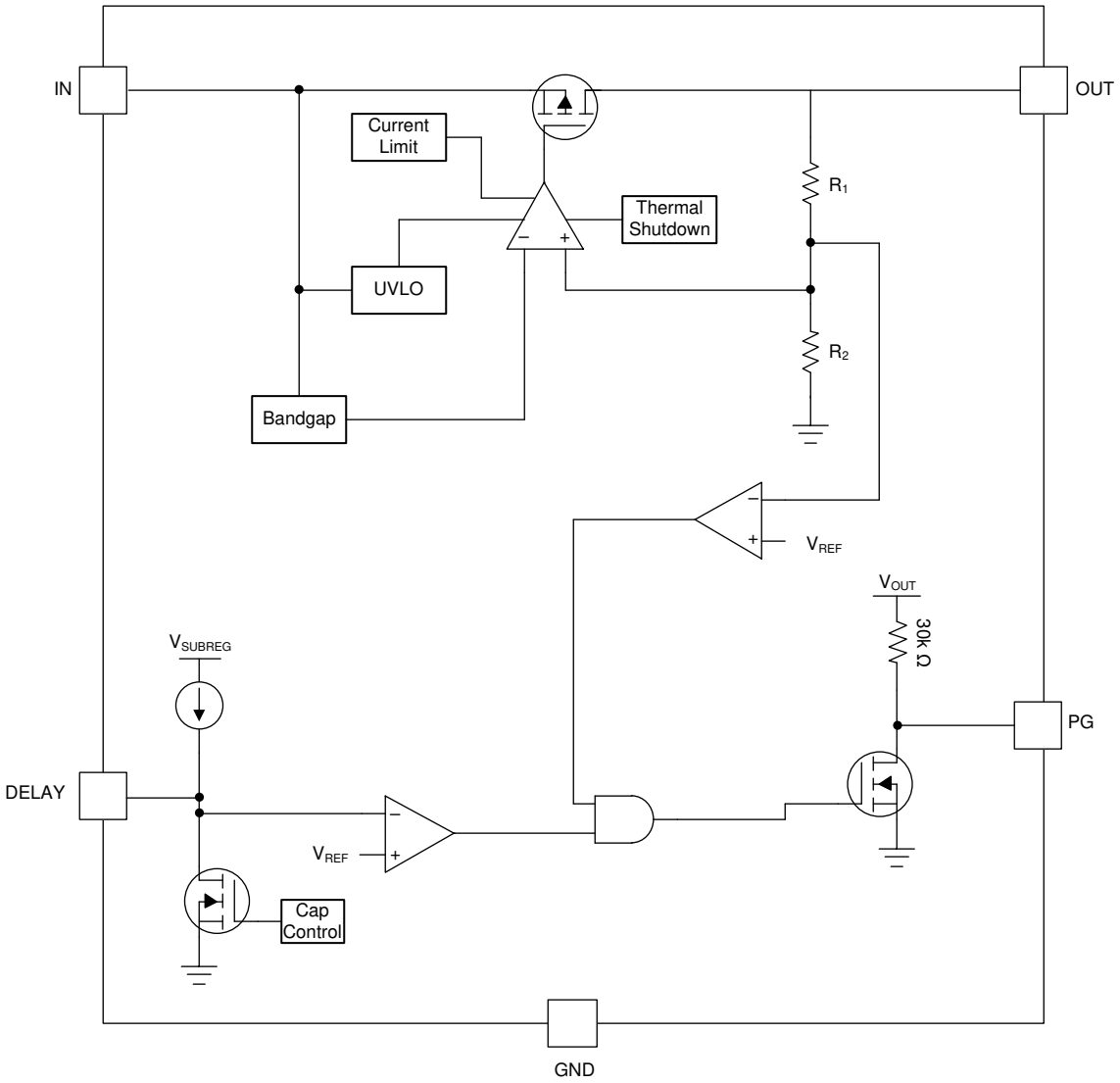
6.1 Overview

The TPS7B87-Q1 is a low-dropout linear regulator (LDO) with improved transient performance that allows for quick response to changes in line or load conditions. The device also features a novel output overshoot reduction feature that minimizes output overshoot during cold-crank conditions.

The integrated power-good and delay features allow for the system to notify down-stream components when the power is good and assist in sequencing requirements.

During normal operation, the device has a tight DC accuracy of ±0.85% over line, load, and temperature. The increased accuracy allows for the powering of sensitive analog loads or sensors.

6.2 Functional Block Diagrams



6.3 Feature Description

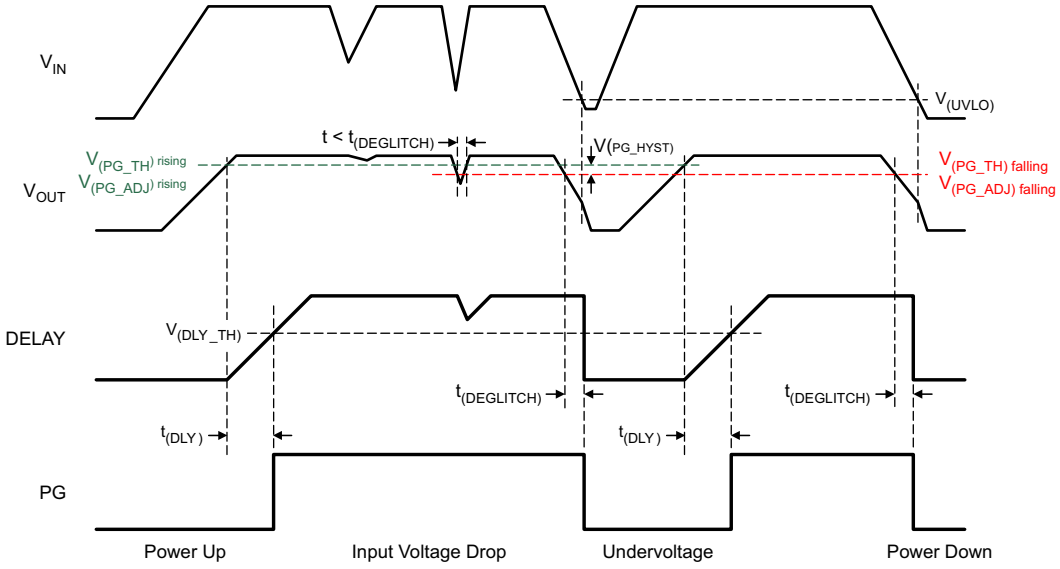
6.3.1 Power-Good (PG)

The power-good (PG) pin is an open-drain output and can be connected to a regulated supply through an external pullup resistor. The maximum pullup voltage is listed as V_{PG} in the *Recommended Operating Conditions* table. For the PG pin to have a valid output, the voltage on the IN pin must be greater than $V_{UVLO(RISING)}$, as listed in the *Electrical Characteristics* table. When V_{OUT} exceeds $V_{PG(TH,\ RISING)}$, the PG output is high impedance and the PG pin voltage pulls up to the connected regulated supply. When the regulated output falls below $V_{PG(TH,\ FALLING)}$, the open-drain output turns on and pulls the PG output low. If output voltage monitoring is not needed, the PG pin can be left floating or connected to ground.

By connecting a pullup resistor to an external supply, any downstream device can receive power-good (PG) as a logic signal that can be used for sequencing. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device.

6.3.2 Adjustable Power-Good Delay Timer (DELAY)

The power-good delay period is a function of the external capacitor on the DELAY pin. The adjustable delay configures the amount of time required before the PG pin becomes high. This delay is configured by connecting an external capacitor from this pin to GND. Figure 6-1 shows the typical timing diagram for the power-good delay pin. If the DELAY pin is left floating, the power-good delay is $t_{(DLY\_FIX)}$. For more information on how to program the PG delay, see the *Setting the Adjustable Power-Good Delay* section.



$V_{(PG\_TH)\ falling} = V_{(PG\_TH)\ rising} - V_{(PG\_HYST)}$.

Figure 6-1. Typical Power-Good Timing Diagram

6.3.3 Undervoltage Lockout

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

6.3.4 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis verifies that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device can cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start-up can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.3.5 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Figure 6-2 shows a diagram of the current limit.

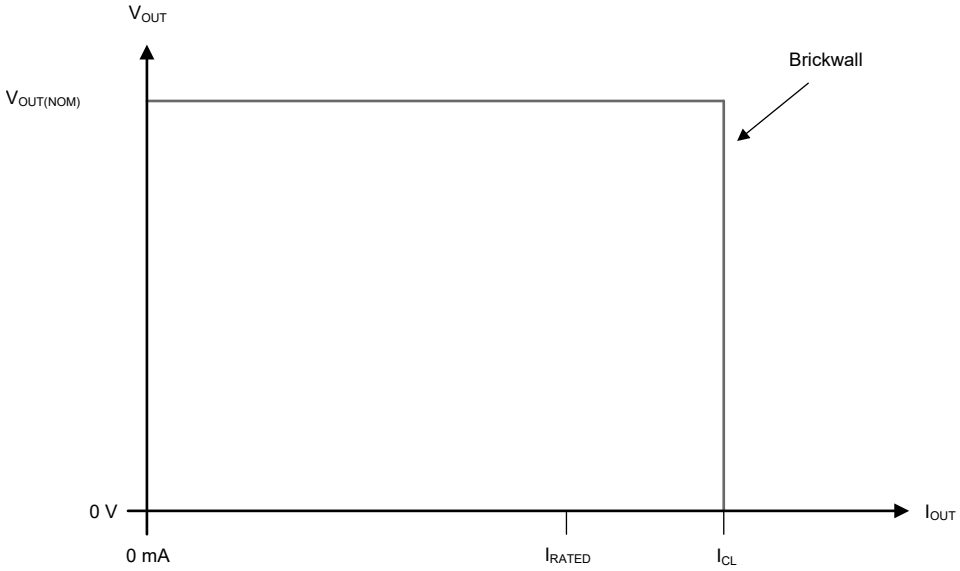


Figure 6-2. Current Limit

6.4 Device Functional Modes

6.4.1 Device Functional Mode Comparison

Table 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER		
	V_{IN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	Not applicable	$T_J > T_{SD(shutdown)}$

6.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)

6.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

6.4.4 Disabled

The output of the device can be shutdown by forcing the input voltage below the UVLO falling threshold (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off and internal circuits are shutdown.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Input and Output Capacitor Selection

The TPS7B87-Q1 requires an output capacitor of 2.2µF or larger (1µF or larger capacitance) for stability and an equivalent series resistance (ESR) between 0.001Ω and 2Ω. For best transient performance, use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and ESR over temperature. When choosing a capacitor for a specific application, be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitance is 220µF.

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

7.1.2 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} – V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

7.1.3 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3V$.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection is recommended to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

7.1.4 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

Note

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (3)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

7.1.4.1 Thermal Performance Versus Copper Area

The most used thermal resistance parameter $R_{\theta JA}$ is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard (see Figure 7-1), PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper.

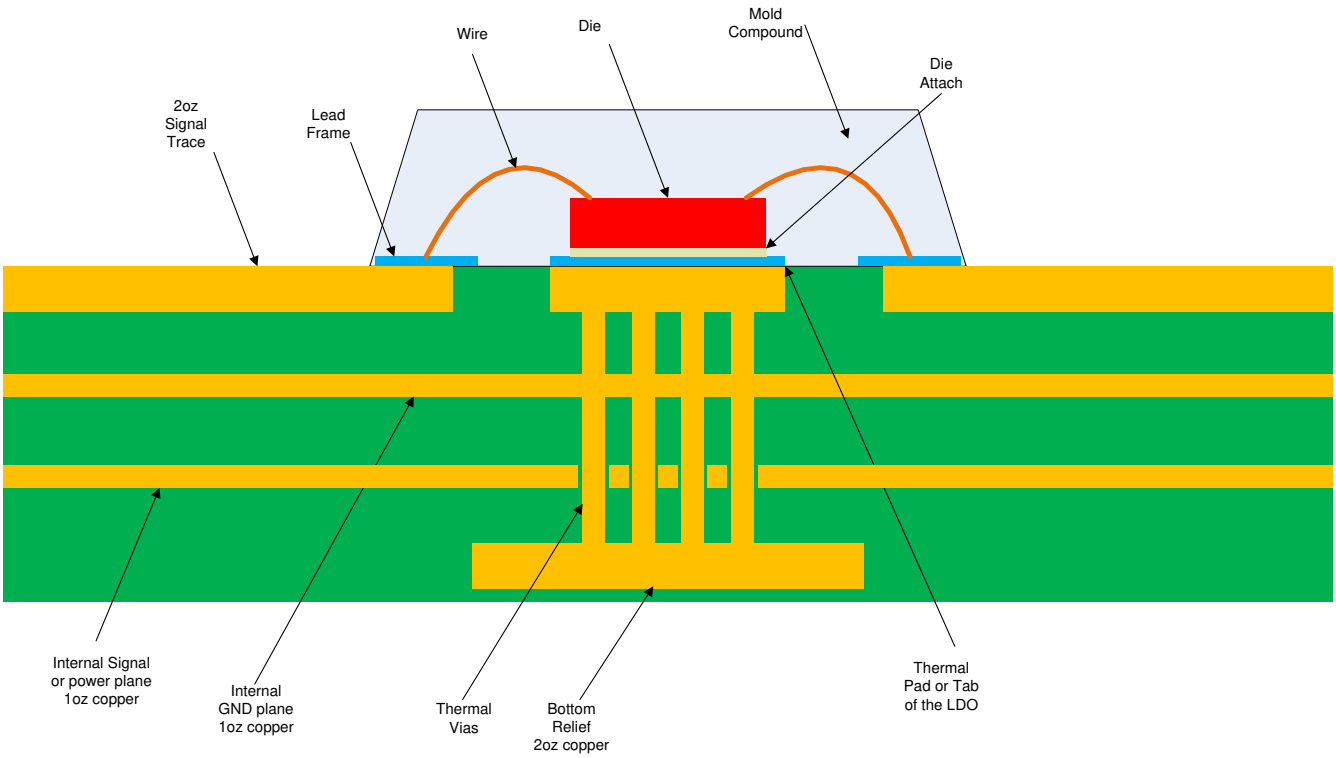


Figure 7-1. JEDEC Standard 2s2p PCB

Figure 7-2 through Figure 7-5 illustrate the functions of $R_{\theta JA}$ and ψ_{JB} versus copper area and thickness. These plots are generated with a 101.6mm × 101.6mm × 1.6mm PCB of two and four layers. For the 4-layer board, inner planes use 1oz copper thickness. Outer layers are simulated with both 1oz and 2oz copper thickness. A 2 × 3 (DDA package) or a 3 × 4 (KVU package) array of thermal vias with a 300µm drill diameter and 25µm copper plating is located beneath the thermal pad of the device. The thermal vias connect the top layer, the bottom layer and, in the case of the 4-layer board, the first inner GND plane. Each of the layers has a copper plane of equal area.

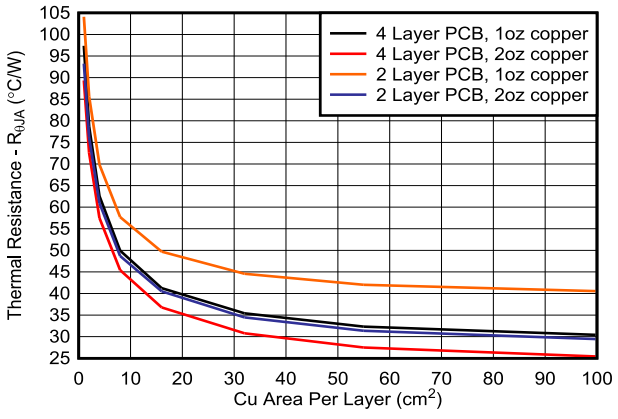


Figure 7-2. $R_{\theta JA}$ vs Copper Area (DDA Package)

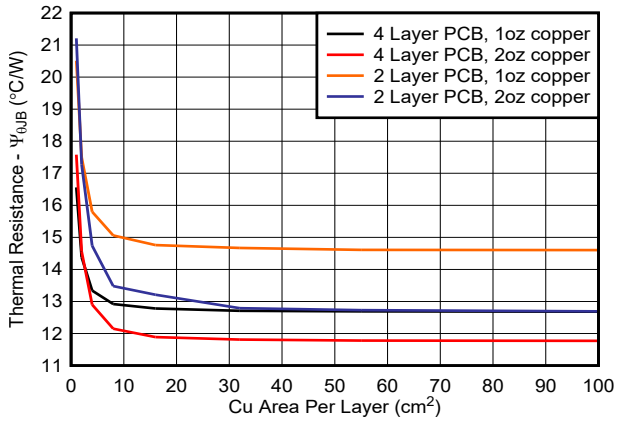


Figure 7-3. ψ_{JB} vs Copper Area (DDA Package)

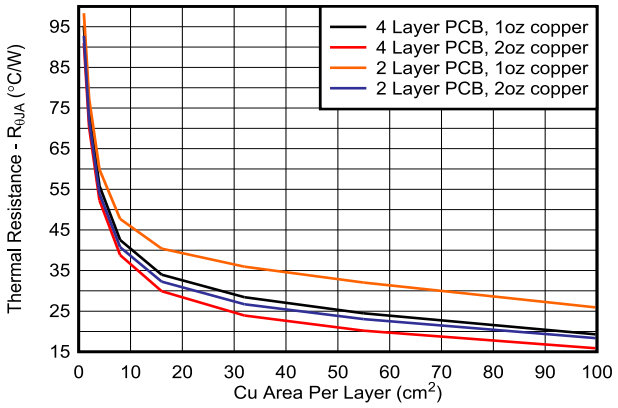


Figure 7-4. $R_{\theta JA}$ vs Copper Area (KVU Package)

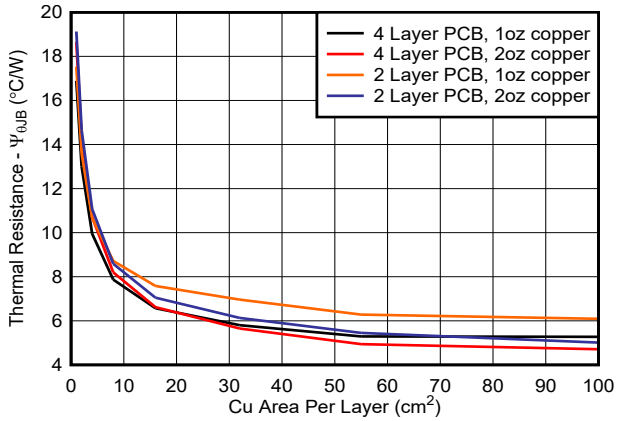


Figure 7-5. ψ_{JB} vs Copper Area (KVU Package)

7.1.4.2 Power Dissipation Versus Ambient Temperature

Figure 7-6 is based off of a JESD51-7 4-layer, high-K board. The allowable power dissipation is estimated using the following equation. As discussed in the *An empirical analysis of the impact of board layout on LDO thermal performance* application note, thermal dissipation can be improved in the JEDEC high-K layout by adding top layer copper and increasing the number of thermal vias. If a good thermal layout is used, the allowable thermal dissipation can be improved by up to 50%.

$$T_A + R_{\theta JA} \, x \, P_D \leq 150 \, °C \tag{4}$$

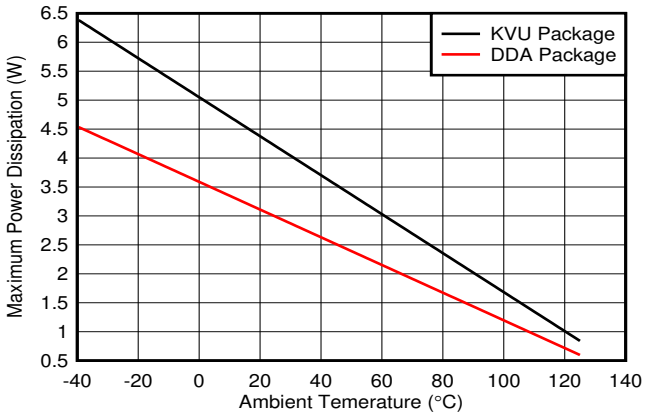


Figure 7-6. TPS7B87-Q1 Allowable Power Dissipation

7.1.5 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (5)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (6)$$

where

- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

7.1.6 Pulling Up the PG Pin to a Different Voltage

Because the power-good (PG) pin is pulled up internally to the output rail, this pin cannot be pulled up to any external voltage like a typical open-drain PG output can be. If this signal must be pulled up to another logic level then an external circuit can be implemented using a PMOS transistor and a pullup resistor. Implementing the circuit shown in Figure 7-7 allows the outputs to be pulled up to any logic rail. If a PMOS transistor is used make sure to pick a transistor with a low threshold voltage as this determines the output low voltage. This can also be done with a NMOS transistor, but the NMOS transistor inverts the logic. This implementation also allows the use of an external pull-up rail.

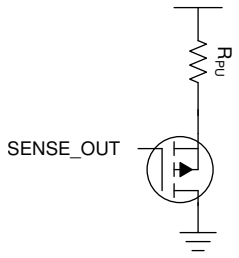


Figure 7-7. Additional Components for the PG Pin to be Pulled Up to Another Rail

7.1.7 Power-Good

7.1.7.1 Setting the Adjustable Power-Good Delay

The power-good delay time can be set in two ways: either by floating the DELAY pin or by connecting a capacitor from this pin to GND. When the DELAY pin is floating, the time defaults to $t_{(DLY\_FIX)}$. The delay time is set by the following equation if a capacitor is connected between the DELAY pin and GND.

$$t = t_{(DLY\_FIX)} + C_{DELAY}\left(\frac{V_{DLY(TH)}}{I_{DLY(CHARGE)}}\right) \quad (7)$$

7.2 Typical Application

Figure 7-8 shows a typical application circuit for the TPS7B87-Q1. TI recommends a low-ESR ceramic capacitor with a dielectric of type X5R or X7R.

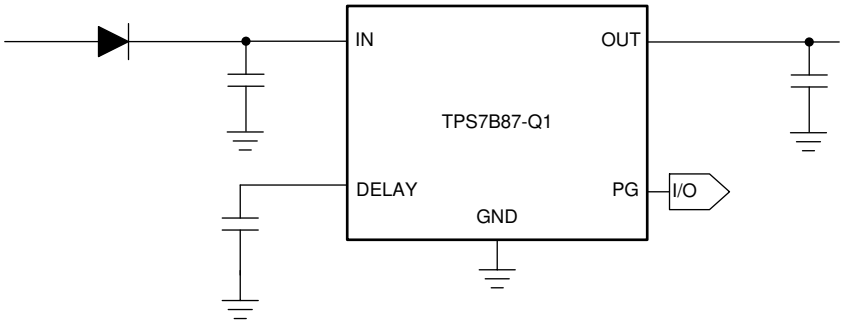


Figure 7-8. Typical Application Schematic for the TPS7B87-Q1

7.2.1 Design Requirements

For this design example, use the parameters listed in Table 7-1 as the input parameters.

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	6V to 40V
Output voltage	5V
Output current	350mA
Output capacitor	10µF
Power-good delay capacitor	100nF

7.2.2 Detailed Design Procedure

7.2.2.1 Input Capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommended value for the decoupling capacitor is 1µF. The voltage rating must be greater than the maximum input voltage.

7.2.2.2 Output Capacitor

The device requires an output capacitor to stabilize the output voltage. The capacitor value must be between 2.2µF and 200µF and the ESR range must be between 1mΩ and 2Ω. For this design, a low ESR, 10µF ceramic capacitor is used to improve transient performance.

7.2.3 Application Curves

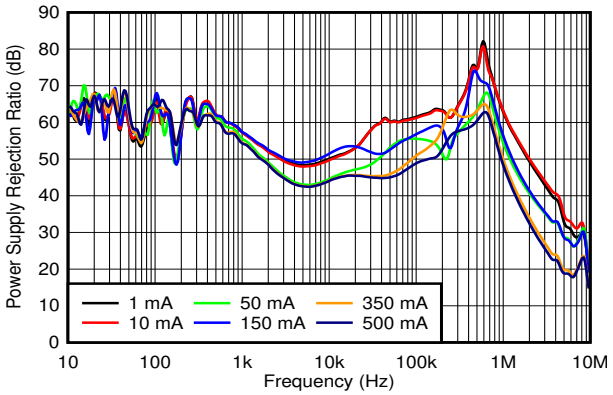


Figure 7-9. PSRR

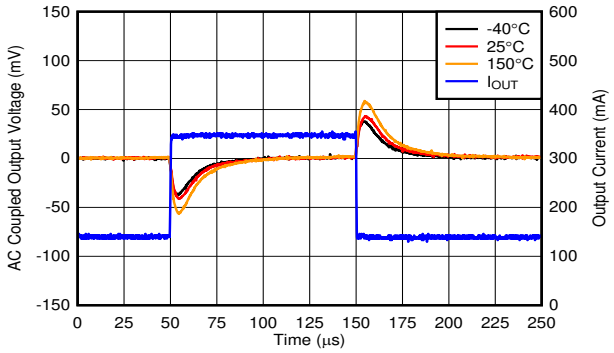


Figure 7-10. Transient Response

7.3 Power Supply Recommendations

This device is designed for operation from an input voltage supply with a range between 3V and 40V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B87-Q1, add an electrolytic capacitor with a value of 22µF and a ceramic bypass capacitor at the input.

7.4 Layout

7.4.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close as possible to each other, connected by a wide, component-side, copper surface. The use of vias and long traces to the input and output capacitors is strongly discouraged and negatively affects system performance. TI also recommends a ground reference plane either embedded in the PCB or located on the bottom side of the PCB opposite the components. This reference plane serves to reinforce the accuracy of the output voltage, shield noise, and behaves similarly to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

7.4.1.1 Package Mounting

Solder pad footprint recommendations for the TPS7B87-Q1 are available at the end of this document and at www.ti.com.

7.4.1.2 Board Layout Recommendations to Improve PSRR and Noise Performance

As depicted in Figure 7-11 and Figure 7-12 , place the input and output capacitors close to the device for the layout of the TPS7B87-Q1. To enhance the thermal performance, place as many vias as possible around the device. These vias improve the heat transfer between the different GND planes in the PCB.

To improve AC performance such as PSRR, output noise, and transient response, use a board design with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must connect directly to the GND pin of the device.

For stable operation and to maximize system performance, minimize the equivalent series inductance (ESL) and the equivalent series resistance (ESR). Place each capacitor as close as possible to the device and on the same side of the PCB as the regulator.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. Use of vias or long traces to connect the capacitors, can negatively affect system performance and even cause instability.

If possible, and to provide the maximum performance specified in this document, use the same layout pattern used for the TPS7B87-Q1 evaluation board, available at www.ti.com.

7.4.2 Layout Examples

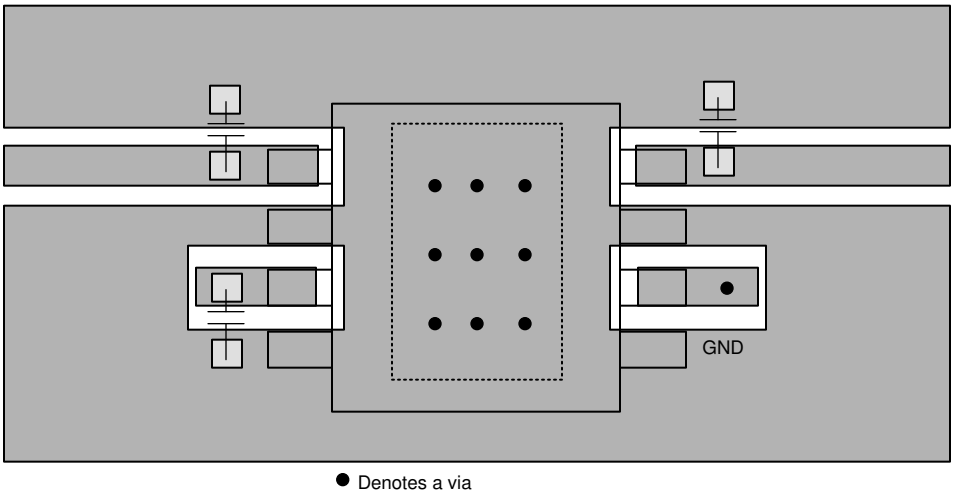


Figure 7-11. DDA Package Fixed Output

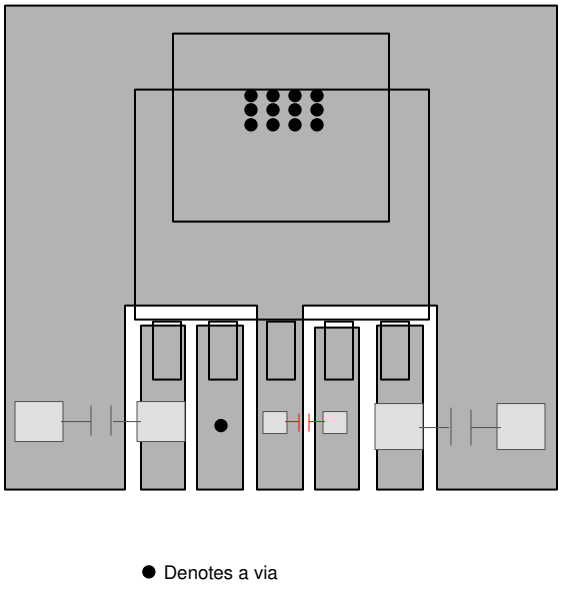


Figure 7-12. KVU Package Fixed Output

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

Table 8-1. Device Nomenclature (1)

PRODUCT	V_{OUT}
TPS7B87**xx**Q**yyy**RQ1	**xx** is the nominal output voltage (for example, 33 = 3.3V V; 50 = 5.0V). **yyy** is the package designator. **Q** indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard. **Q1** indicates that this device is an automotive grade (AEC-Q100) device. For the DDA package, this device potentially ships with multiple leadframes. The reel packaging label provides ASO information to distinguish which leadframe is used. ASO : FMX label denotes material from the new manufacturing site and ASO : ASE label denotes material from the legacy manufacturing site.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from April 31, 2021 to June 30, 2025 (from Revision A (April 2021) to Revision B (November 2025)) — **Page**

- Update the *Thermal Information*table to include the thermal information for the DDA package from the multiple manufacturing sites (ASE, FMX)....4
- Changed *Power-Good (PG)* section....15
- Updated the *Device nomenclature*to include a note that describes the method to distinguish the DDA material from different assembly sites. 26

- Updated the mechanical drawings from DDA0008E-C01 to DDA0008B-C01.....28

Changes from Revision * (December 2020) to Revision A (April 2021) **Page**

- Added *Functional Safety-Capable* bullet to *Features* list.....1
- Updated pin functions table to reflect pin 4 of the HSOIC (DDA) package as an NC pin..... 3

10 Mechanical, Packaging, and Orderable Information

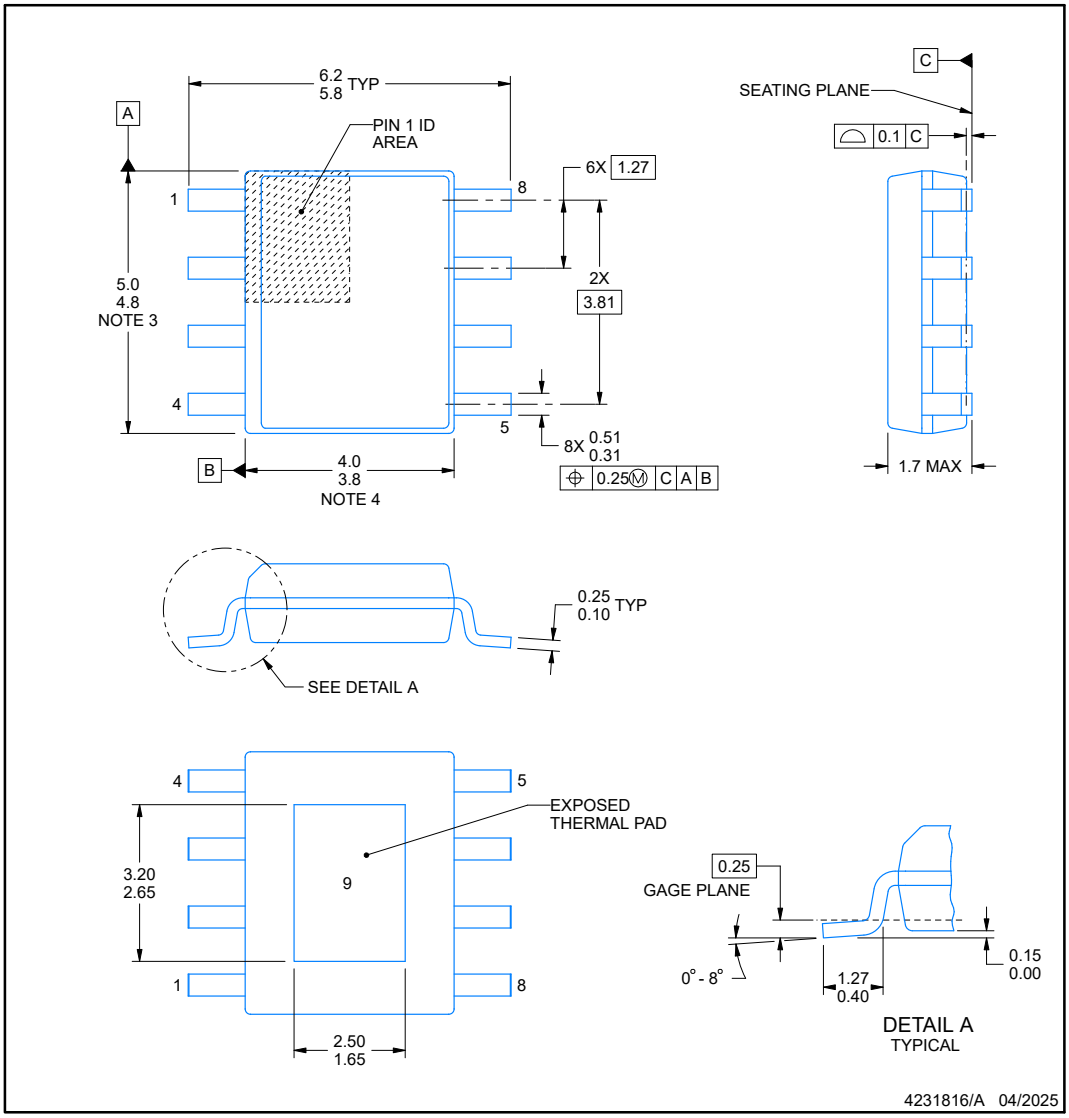
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Mechanical Data

PACKAGE OUTLINE

DDA0008B-C01 **PowerPAD™ SOIC - 1.7 mm max height**

PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

NOTES:

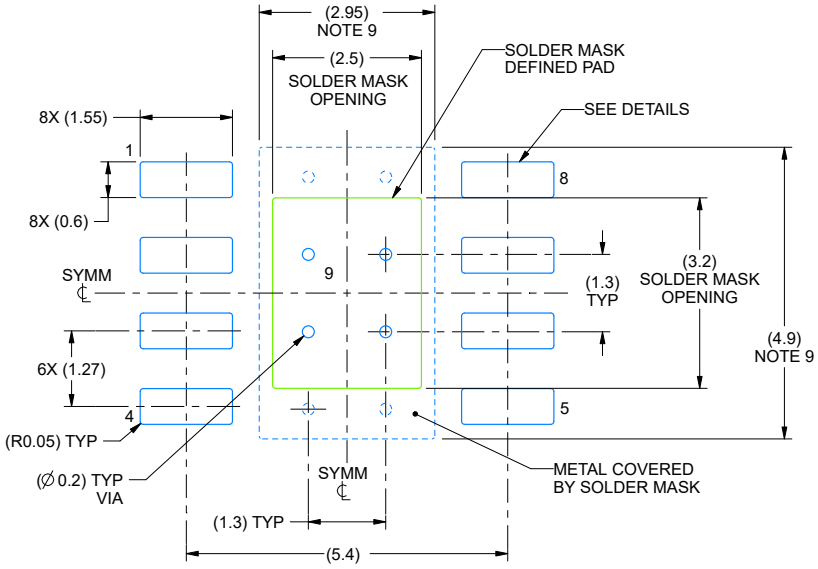
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.

EXAMPLE BOARD LAYOUT

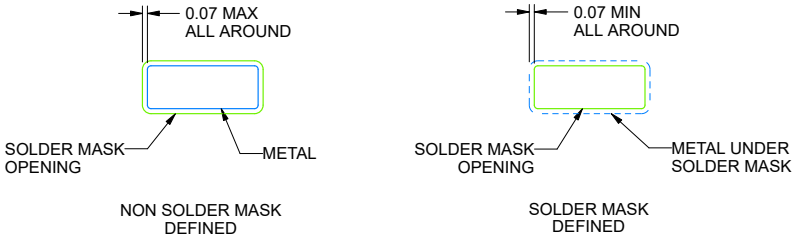
DDA0008B-C01

PowerPAD ™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4231816/A 04/2025

NOTES: (continued)

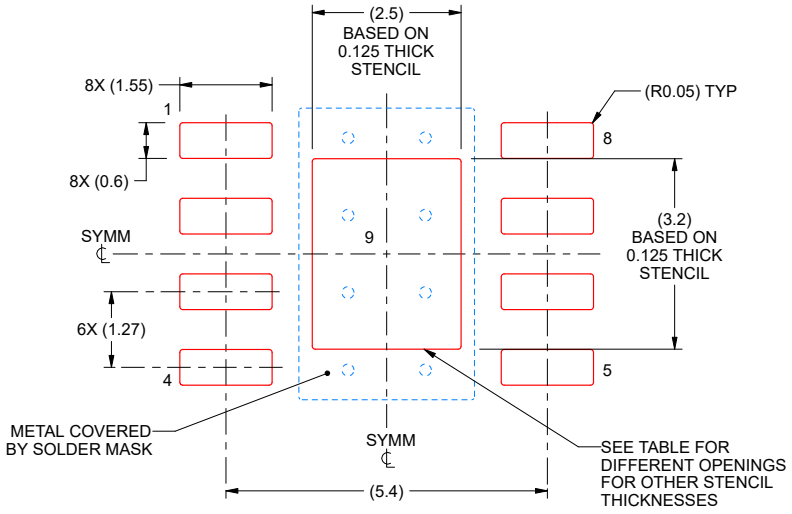
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B-C01

PowerPAD ™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.8 X 3.58
0.125	2.5 X 3.2 (SHOWN)
0.150	2.28 X 2.92
0.175	2.11 X 2.7

4231816/A 04/2025

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7B8733QDDARQ1	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	7B8733
TPS7B8733QDDARQ1.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	7B8733
TPS7B8733QKVURQ1	Active	Production	TO-252 (KVU) | 5	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 150	7B8733
TPS7B8733QKVURQ1.A	Active	Production	TO-252 (KVU) | 5	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 150	7B8733
TPS7B8733QKVURQ1R2	Active	Production	TO-252 (KVU) | 5	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 150	7B8733
TPS7B8733QKVURQ1R2.A	Active	Production	TO-252 (KVU) | 5	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 150	7B8733
TPS7B8750QDDARQ1	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	7B8750
TPS7B8750QDDARQ1.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	7B8750
TPS7B8750QKVURQ1	Active	Production	TO-252 (KVU) | 5	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 150	7B8750
TPS7B8750QKVURQ1.A	Active	Production	TO-252 (KVU) | 5	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 150	7B8750
TPS7B8750QKVURQ1R2	Active	Production	TO-252 (KVU) | 5	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 150	7B8750
TPS7B8750QKVURQ1R2.A	Active	Production	TO-252 (KVU) | 5	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 150	7B8750

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

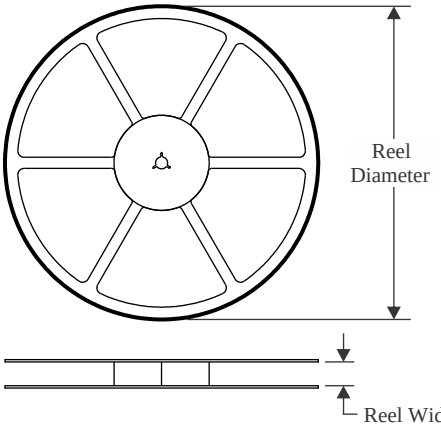
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

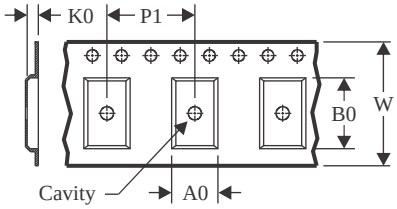
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

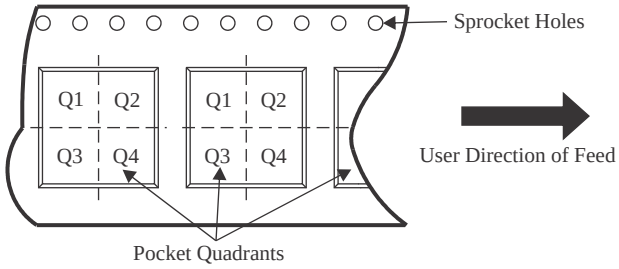


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

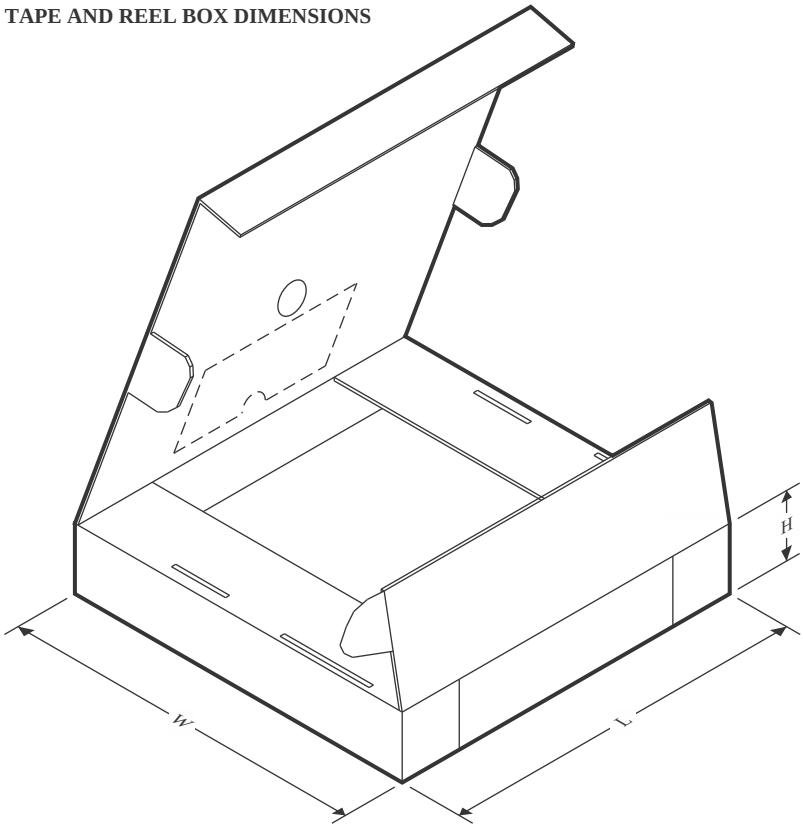
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B8733QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q3
TPS7B8733QKVURQ1R2	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TPS7B8750QDDARQ1	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TPS7B8750QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q3
TPS7B8750QKVURQ1R2	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

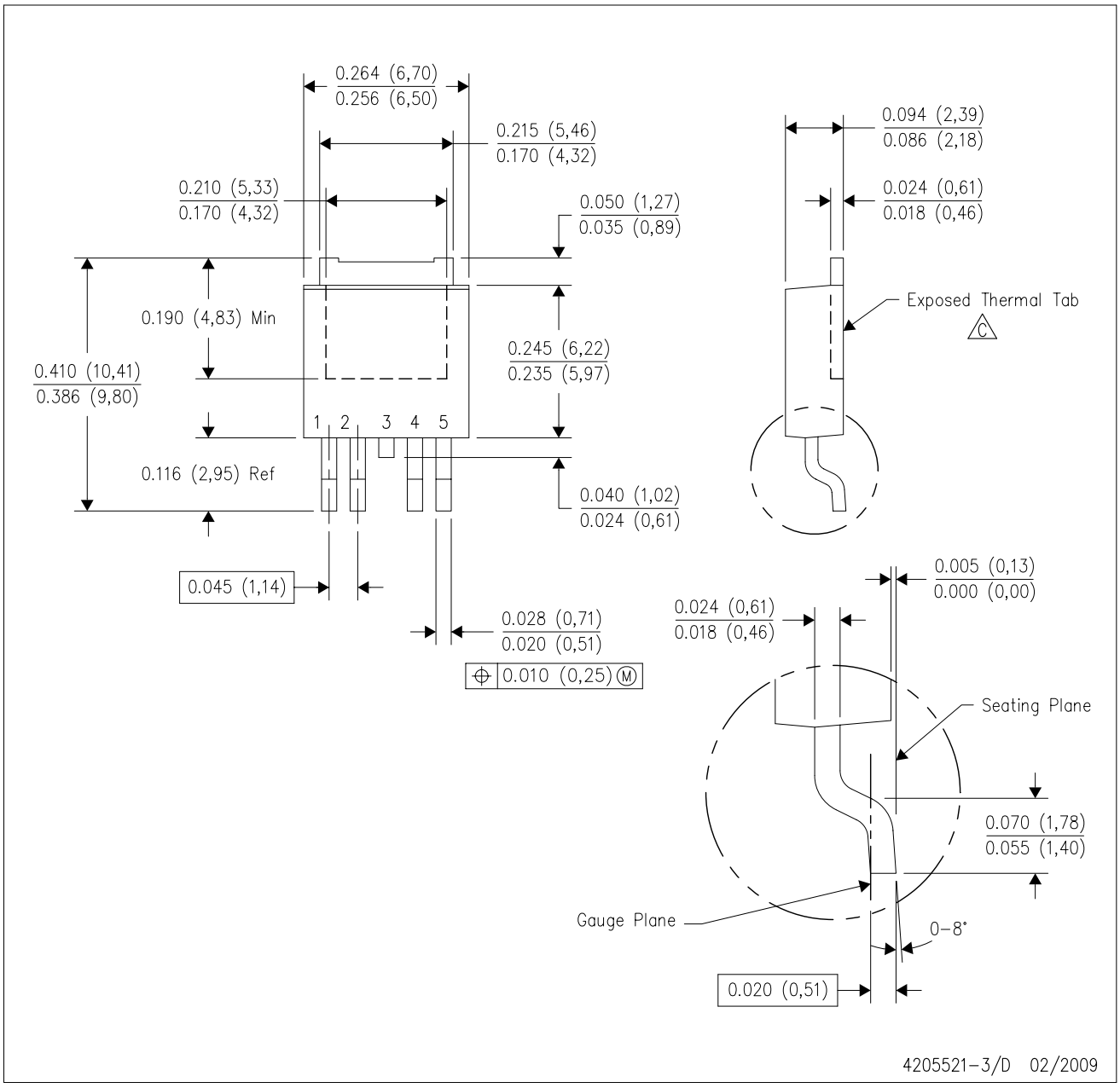
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B8733QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0
TPS7B8733QKVURQ1R2	TO-252	KVU	5	2500	340.0	340.0	38.0
TPS7B8750QDDARQ1	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
TPS7B8750QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0
TPS7B8750QKVURQ1R2	TO-252	KVU	5	2500	340.0	340.0	38.0

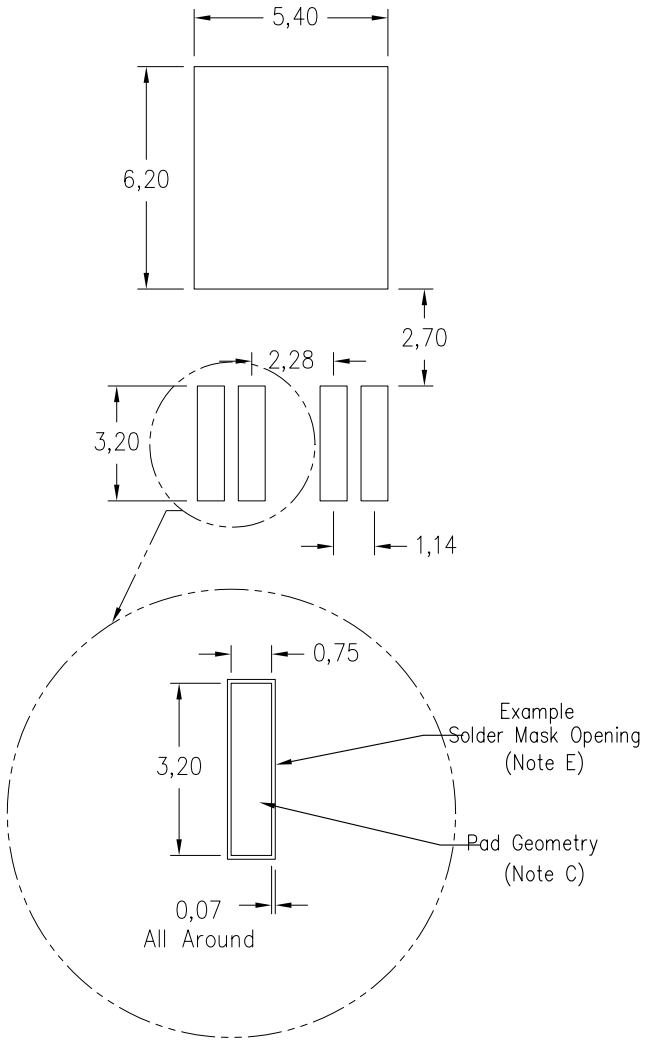
KVU (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



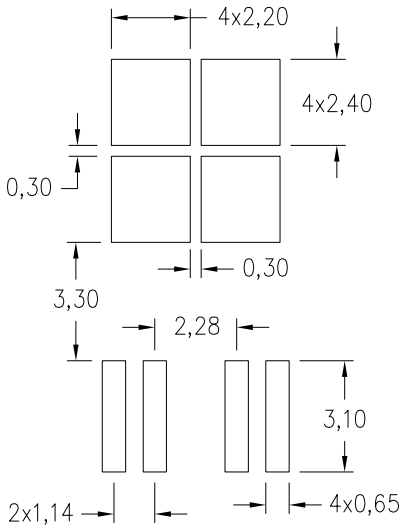
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the exposed thermal tab.
D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
E. Falls within JEDEC TO–252 variation AD.

KVU (R–PSFM–G5) PLASTIC FLANGE MOUNT PACKAGE

Example Board Layout



Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



63% solder coverage on center pad

4211592–3/B 03/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is an alternate information source for PCB land pattern designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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