













TPS7B81

SBVS402 - APRIL 2020

TPS7B81 150-mA, 40-V, Ultra-Low-I_Q, Low-Dropout Regulator

Features

Wide input voltage range: 3 V to 40 V

Output current: 150 mA

Ultra-low quiescent current (I_O):

2.7 µA typical at light loads

4.5 µA maximum at light loads

Accuracy: 1.5% over line, load, and temperature

Typical dropout voltage: 180 mV at 100 mA

Wide enable voltage range: 2 V to V_{IN} (40 V max)

Input voltage transient tolerance: 45 V

Fixed 5-V and 3.3-V output options

Current limit and thermal shutdown protection

Stable with a wide range of capacitors (1 µF to 200 µF)⁽¹⁾

Junction temperature range: -40°C to +150°C

High thermal performance packages:

DGN (8-pin HVSSOP), R_{0.IA} = 63.9°C/W

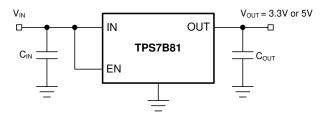
DRV (6-pin WSON), $R_{\theta JA} = 72.8$ °C/W

See the output capacitor requirements in the Recomended Operation Conditions table

Applications

- Smoke and heat detectors
- **Thermostats**
- Motion detectors (PIR, uWave, and so forth)
- Cordless power tools
- Appliance battery packs
- Motor drives

Typical Application Schematic



3 Description

The TPS7B81 is a low-dropout (LDO) linear regulator that operates from input voltages up to 40 V and can supply up to 150 mA in current. With only 2.7 µA of quiescent current at light loads, the device is an excellent choice for wide input supply designs and high cell count battery applications that need very low standby power consumption. The 45-V transient provides additional tolerance headroom applications where inductive kickback may be present, thereby reducing external circuitry for voltage suppression.

With integrated short-circuit and overcurrent limiting, the TPS7B81 protects the system during fault conditions. In addition to the low standby power consumption, the very low dropout voltage in light load conditions helps maintain regulation even when powered by depleted batteries.

The TPS7B81 is available in thermally enhanced, 8pin HVSSOP and 6-pin WSON packages. Both packages offer high thermal conductivity, and their small size supports compact design, making them well suited for space-limited applications such as power tools or motor drive modules and battery packs.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)		
TPS7B81	HVSSOP (8)	3.00 mm × 3.00 mm		
	WSON (6)	2.00 mm × 2.00 mm		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Quiescent Current vs Ambient Temperature $(V_{OUT} = 3.3 V)$

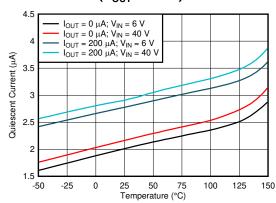






Table of Contents

1	Features 1	7.4 Device Functional Modes	11
2	Applications 1	8 Application and Implementation	12
3	Description 1	8.1 Application Information	12
4	Revision History2	8.2 Typical Application	15
5	Pin Configuration and Functions3	9 Power Supply Recommendations	16
6	Specifications4	10 Layout	17
•	6.1 Absolute Maximum Ratings4	10.1 Layout Guidelines	17
	6.2 ESD Ratings	10.2 Layout Example	17
	6.3 Recommended Operating Conditions	11 Device and Documentation Support	18
	6.4 Thermal Information	11.1 Receiving Notification of Documentation Updat	es 18
	6.5 Electrical Characteristics5	11.2 Support Resources	18
	6.6 Typical Characteristics	11.3 Trademarks	18
7	Detailed Description	11.4 Electrostatic Discharge Caution	18
-	7.1 Overview	11.5 Glossary	18
	7.2 Functional Block Diagram	12 Mechanical, Packaging, and Orderable	
	7.3 Feature Description	Information	18

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

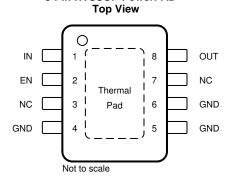
DATE	REVISION	NOTES
April 2020	*	Initial release.



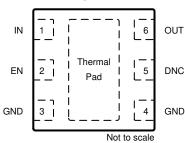
www.ti.com

5 Pin Configuration and Functions

DGN Package 8-Pin HVSSOP PowerPAD™



DRV Package 6-Pin WSON PowerPAD™ Top View



Pin Functions

	PIN			
NAME	N	0.	1/0	DESCRIPTION
NAIVIE	DGN	DRV		
DNC	_	5	_	Do not connect to a biased voltage. Tie this pin to ground or leave floating.
EN	EN 2 2		1	Enable input pin. Drive EN greater than V_{IH} to turn on the regulator. Drive EN less than V_{IL} to put the low-dropout (LDO) into shutdown mode.
GND 4, 5, 6 3,4		_	Ground reference	
IN	1	1	I	Input power-supply pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground as listed in the <i>Recommended Operating Conditions</i> table and the <i>Input Capacitor</i> section. Place the input capacitor as close to the output of the device as possible.
NC	3, 7	_	_	Not internally connected
OUT 8 6		0	Regulated output voltage pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground; see the <i>Recommended Operating Conditions</i> table and the <i>Output Capacitor</i> section. Place the output capacitor as close to output of the device as possible.	
Thermal page	b		_	Connect the thermal pad to a large-area GND plane for improved thermal performance.

TEXAS INSTRUMENTS

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)(2)

		MIN	MAX	UNIT
V _{IN}	Unregulated input voltage (3)	-0.3	45	V
V _{EN}	Enable input voltage ⁽³⁾	-0.3	V _{IN}	V
V _{OUT}	Regulated output	-0.3	7	V
TJ	Junction temperature	-40	150	°C
T _{stg}	Storage temperature	-40	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2) All voltage values are with respect to GND.

6.2 ESD Ratings

			VALUE	UNIT
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 $^{(1)}$	±2000	.,	
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	V

⁽¹⁾ JEDEC document JEP155 states that 2-kV HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{IN}	Unregulated input voltage	3	40	V
V _{EN}	Enable input voltage	0	V_{IN}	V
C _{OUT}	Output capacitor requirements ⁽¹⁾	1	200	μF
ESR	Output capacitor ESR requirements ⁽²⁾	0.001	5	Ω
T _A	Ambient temperature	-40	125	°C
TJ	Junction temperature	-40	150	°C

⁽¹⁾ The output capacitance range specified in the table is the effective capacitance value.

6.4 Thermal Information

		TPS7	7B81	
	THERMAL METRIC ⁽¹⁾	DGN (HVSSOP)	DRV (WSON)	UNIT
		8 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.9	72.8	°C/W
R ₀ JC(top)	Junction-to-case (top) thermal resistance	50.2	85.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.6	37.4	°C/W
ΨЈТ	Junction-to-top characterization parameter	1.8	2.7	°C/W
ΨЈВ	Junction-to-board characterization parameter	22.3	37.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12.1	13.8	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

⁽³⁾ Absolute maximum voltage, can withstand 45 V for 200 ms.

⁽²⁾ JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

⁽²⁾ Relevant ESR value at f = 10 kHz



www.ti.com

6.5 Electrical Characteristics

over operating ambient temperature range, $T_J = -40$ °C to +150°C, $V_{IN} = 14$ V, and 10- μ F ceramic output capacitor (unless otherwise noted)

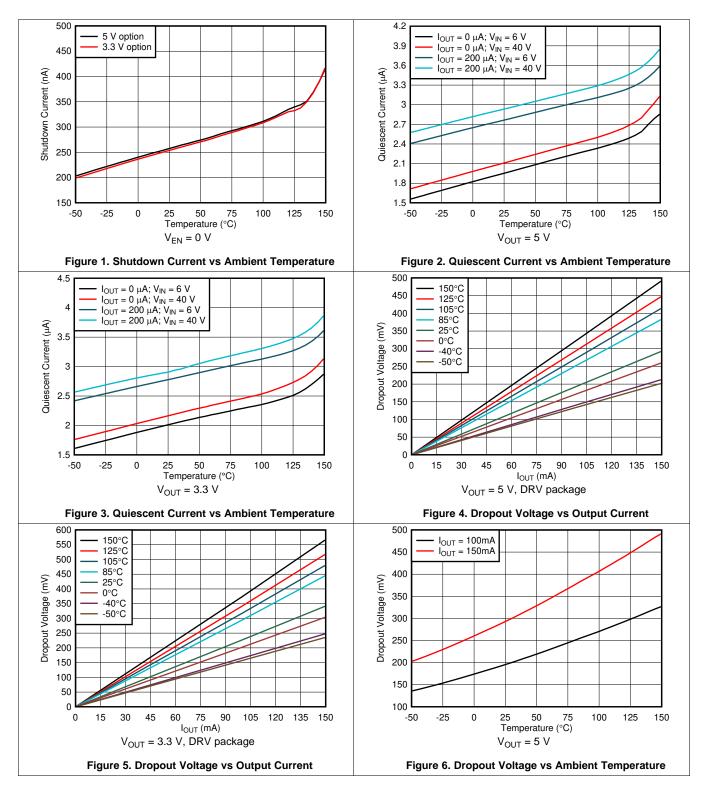
	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY	VOLTAGE AND CURREN	IT (IN)						
V _{IN}	Input voltage				V _{OUT(Nom)} + V _(Dropout)		40	V
I _(SD)	Shutdown current	EN = 0 V				0.3	1	μΑ
		$V_{IN} = 6 V \text{ to } 40$	$V, EN \ge 2 V, I_{OUT} = 0 mA$			1.9	3.5	
$I_{(Q)}$	Quiescent current	V = 6 \/ to 40	V, EN ≥ 2 V, I _{OUT} = 0.2 mA	DGN package		2.7	6.5	μΑ
		VIN = 0 V 10 40	v, LIV = 2 v, I _{OUT} = 0.2 IIIA	DRV package		2.7	4.5	
$V_{(IN,}$	V _{IN} undervoltage	Ramp V _{IN} down	until the output turns off				2.7	V
UVLO)	detection	Hysteresis				200		mV
ENABLE	INPUT (EN)							
V_{IL}	Logic-input low level						0.7	V
V_{IH}	Logic-input high level							V
I _{EN}	Enable current					10		nA
REGULA	TED OUTPUT (OUT)				1			
V _{OUT}	Regulated output	$V_{IN} = V_{OUT} + V_{OUT}$ $I_{OUT} = 1 \text{ mA to}$	$V_{IN} = V_{OUT} + V_{(Dropout)}$ to 40 V, $I_{OUT} = 1$ mA to 150 mA				1.5%	
V _{(Line-} Reg)	Line regulation	V _{IN} = 6 V to 40	V _{IN} = 6 V to 40 V, I _{OUT} = 10 mA				10	mV
V _{(Load-}	Load regulation	V _{IN} = 14 V. I _{QUIT} = 1 mA to 150 mA		DGN package			20	mV
Reg)	Load regulation	V _{IN} = 14 V, 1 _{OUT}	OUT = 1 mA to 150 mA DRV package				10	IIIV
			I _{OUT} = 150 mA	DGN package		270	540	mV
		V _{OUT} = 5 V		DRV package		325	585	
		V001 = 3 V	I _{OUT} = 100 mA	DGN package		180	350	
$V_{(Dropout)}$	Dropout voltage			DRV package		200	390	
			I _{OUT} = 150 mA	DGN package			650	
		$V_{OUT} = 3.3 V$	1001 = 100 111/1	DRV package		345	675	
			$I_{OUT} = 100 \text{ mA}$			255	450	
I _{OUT}	Output current	V _{OUT} in regulation 5.8 V for the fixed	on, $V_{IN} = 7 \text{ V}$ for the fixed 5-1 ed 3.3-V option	V option, $V_{IN} =$	0		150	mA
I _(CL)	Output current limit	V _{OUT} short to 90	V _{OUT} short to 90% × V _{OUT}			510	690	mA
PSRR	Power-supply ripple rejection	$V_{(Ripple)} = 0.5 V_1$ 2.2 μ F	PP, I _{OUT} = 10 mA, frequency	= 100 Hz, C _{OUT} =		60		dB
OPERAT	ING TEMPERATURE RAN	IGE			•		'	
T _(SD)	Junction shutdown temperature					175		°C
T _(HYST)	Hysteresis of thermal shutdown					20		°C

SBVS402 – APRIL 2020 www.ti.com

TEXAS INSTRUMENTS

6.6 Typical Characteristics

at $T_J = -40$ °C to +150°C, $V_{IN} = 14$ V, and $V_{EN} \ge 2$ V (unless otherwise noted)

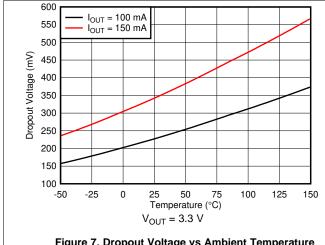




www.ti.com

Typical Characteristics (continued)

at $T_J = -40$ °C to +150°C, $V_{IN} = 14$ V, and $V_{EN} \ge 2$ V (unless otherwise noted)

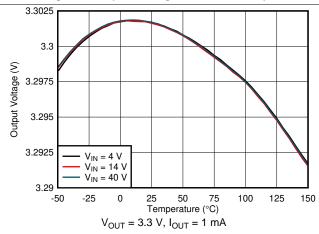


5 Output Voltage (V) 4.995 4.99 4.985 I_{OUT} = 1 mA I_{OUT} = 150 mA 4.98 100 125 150 -50 Temperature (°C) $V_{OUT} = 5 V$

5.005

Figure 7. Dropout Voltage vs Ambient Temperature





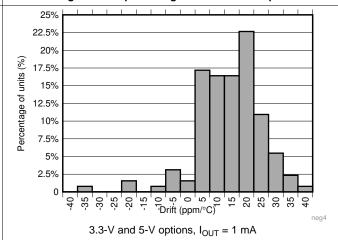
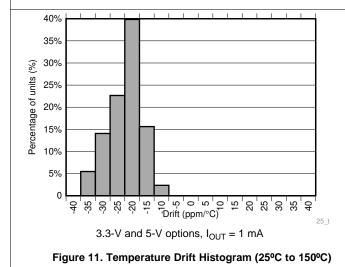


Figure 9. Output Voltage vs Ambient Temperature

Figure 10. Temperature Drift Histogram (-40°C to +25°C)



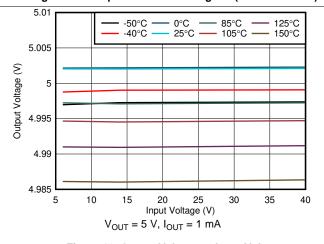
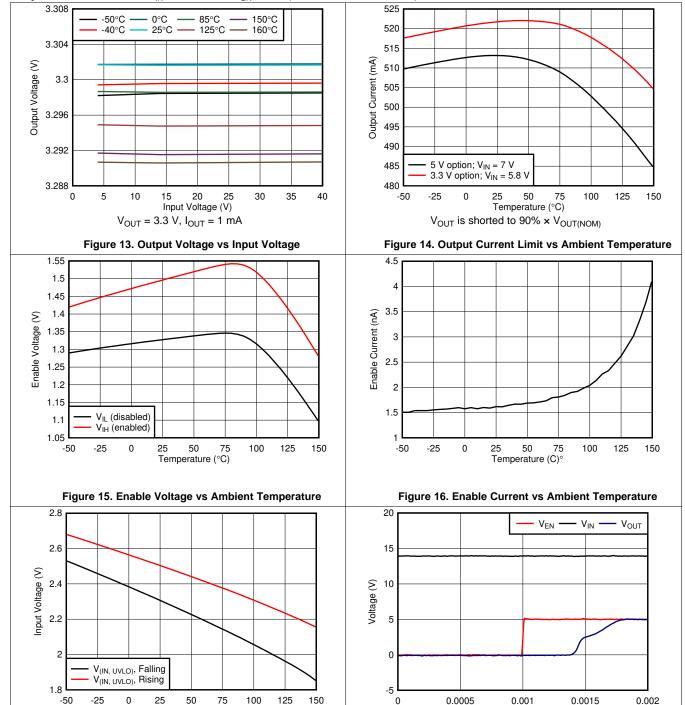


Figure 12. Output Voltage vs Input Voltage

TEXAS INSTRUMENTS

Typical Characteristics (continued)

at $T_J = -40$ °C to +150°C, $V_{IN} = 14$ V, and $V_{EN} \ge 2$ V (unless otherwise noted)



Submit Documentation Feedback

Temperature (°C)

Figure 17. UVLO vs Ambient Temperature

Copyright © 2020, Texas Instruments Incorporated

 $\label{eq:time} \mbox{Time (s)} $$V_{OUT} = 5 \ V, \ C_{IN} = 1 \ \mu\mbox{F}, \ C_{OUT} = 1 \ \mu\mbox{F}$

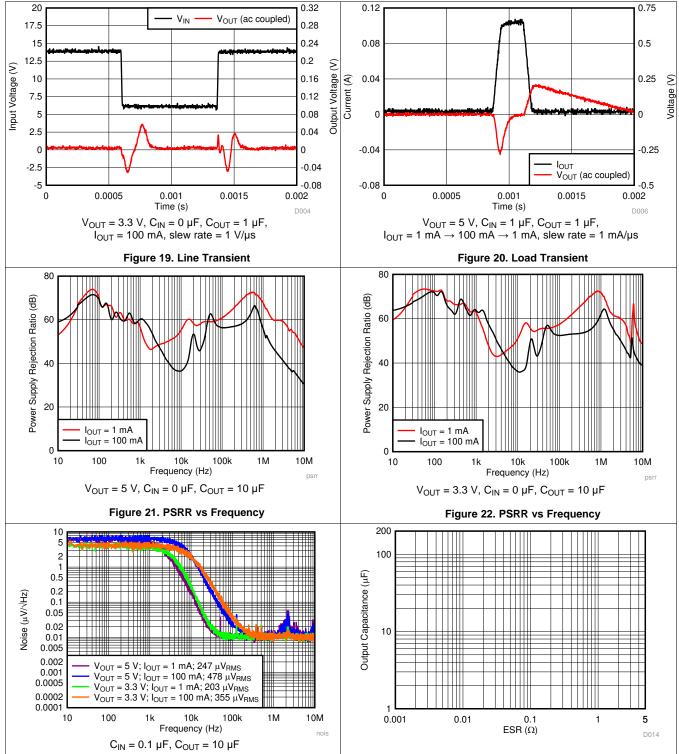
Figure 18. Startup With Enable



www.ti.com

Typical Characteristics (continued)

at $T_J = -40$ °C to +150°C, $V_{IN} = 14$ V, and $V_{EN} \ge 2$ V (unless otherwise noted)



Product Folder Links: *TPS7B81*

Figure 23. Noise vs Frequency

Figure 24. Output Capacitance vs ESR Stability

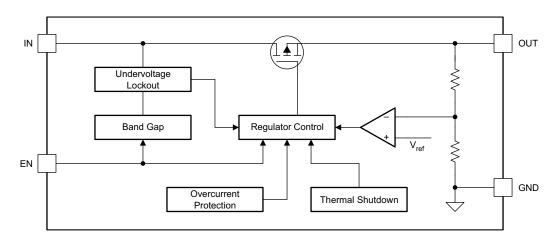
TEXAS INSTRUMENTS

7 Detailed Description

7.1 Overview

The TPS7B81 is a 40-V, 150-mA, low-dropout (LDO) linear regulator with ultra-low quiescent current. This voltage regulator consumes only 3 µA of quiescent current at light load, and is quite suitable for always-on applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Device Enable (EN)

The EN pin is a high-voltage-tolerant pin. A high input activates the device and turns the regulation on. Connect this pin to an external microcontroller or a digital circuit to enable and disable the device, or connect to the IN pin for self-bias applications.

7.3.2 Undervoltage Shutdown

This device has an integrated undervoltage lockout (UVLO) circuit to shut down the output if the input voltage (V_{IN}) falls below an internal UVLO threshold $(V_{(UVLO)})$. This feature ensures that the regulator does not latch into an unknown state during low-input-voltage conditions. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up with a normal power-up sequence when the input voltage is above the required level.

7.3.3 Current Limit

This device features current-limit protection to keep the device in a safe operating area when an overload or output short-to-ground condition occurs. This feature protects the device from excessive power dissipation. For example, during a short-circuit condition on the output, the fault protection limits the current through the pass element to $I_{(LIM)}$ to protect the device from excessive power dissipation.

7.3.4 Thermal Shutdown

This device incorporates a thermal shutdown (TSD) circuit as protection from overheating. For continuous normal operation, the junction temperature must not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature falls below the TSD trip point minus the thermal shutdown hysteresis, the output turns on again.



www.ti.com

7.4 Device Functional Modes

7.4.1 Operation With V_{IN} Lower Than 3 V

The device normally operates with input voltages above 3 V. The device can also operate at lower input voltages; the maximum UVLO voltage is 2.7 V. The device does not operate at input voltages below the actual UVLO voltage.

7.4.2 Operation With V_{IN} Larger Than 3 V

When V_{IN} is greater than 3 V, if V_{IN} is also higher than the output set value plus the device dropout voltage, V_{OUT} is equal to the set value. Otherwise, V_{OUT} is equal to V_{IN} minus the dropout voltage.

Table 1. Device Functional Mode Comparison

OPERATING MODE		PARAMETER						
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{(Dropout)}$ and $V_{IN} \ge 3 \text{ V}$	$V_{EN} > V_{IH}$	I _{OUT} < I _{CL}	T _J < 160°C				
Dropout mode	$3V \le V_{IN} < V_{OUT(nom)} + V_{(Dropout)}$	$V_{EN} > V_{IH}$	I _{OUT} < I _{CL}	T _J < 160°C				
Disabled mode (any true condition disables the device)	V _{IN} < V _(IN, UVLO)	V _{EN} < V _{IL}	_	T _J > 160°C				

SBVS402 – APRIL 2020 www.ti.com

TEXAS INSTRUMENTS

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7B81 is a 150-mA, 40-V, low-dropout (LDO) linear regulator with ultralow quiescent current. The PSpice transient model is available for download on the product folder and can be used to evaluate the basic functionality of the device.

8.1.1 Power Dissipation

Circuit reliability demands that proper consideration is given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Equation 1 approximates P_D :

$$P_{D} = (V_{IN} - V_{OUT}) \times I_{OUT}$$
 (1)

An important note is that power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. According to Equation 2, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance $(R_{\theta JA})$ of the combined PCB, device package, and the temperature of the ambient air (T_A) . This equation is rearranged for output current in Equation 3.

$$T_{J} = T_{A} + R_{\theta JA} \times P_{D} \tag{2}$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})]$$
(3)

Unfortunately, this thermal resistance $(R_{\theta JA})$ is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance $(R_{\theta JCbot})$ plus the thermal resistance contribution by the PCB copper.

Figure 25 through Figure 28 illustrate the functions of $R_{\theta JA}$ and ψ_{JB} versus copper area and thickness. These plots are generated with a 101.6-mm x 101.6-mm x 1.6-mm PCB of two and four layers. For the four-layer board, inner planes use a 1-oz copper thickness. Outer layers are simulated with both 1-oz and 2-oz copper thicknesses. A 2 x 1 array of thermal vias with a 300- μ m drill diameter and a 25- μ m copper (Cu) plating is located beneath the thermal pad of the device. The thermal vias connect the top layer, the bottom layer and, in the case of the 4-layer board, the first inner GND plane. The copper plane of each layer is of an equal area.

www.ti.com

Application Information (continued)

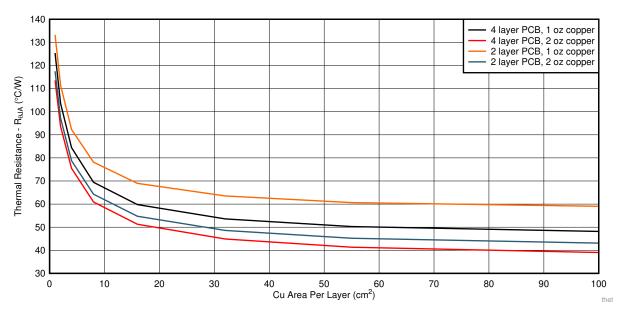


Figure 25. $R_{\theta JA}$ versus Cu Area for the WSON (DRV) Package

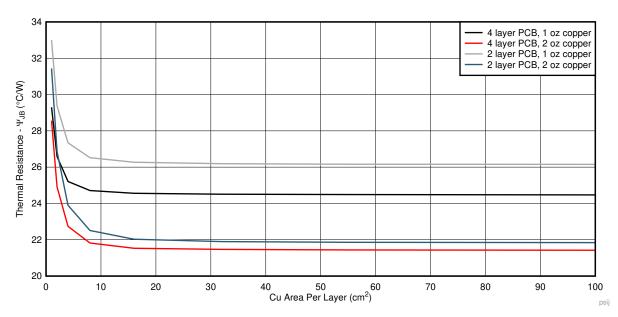


Figure 26. ψ_{JB} versus Cu Area for the WSON (DRV) Package

TEXAS INSTRUMENTS

Application Information (continued)

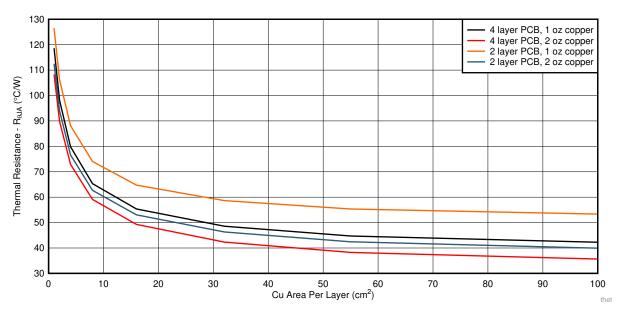


Figure 27. $R_{\theta JA}$ versus Cu Area for the HVSSOP (DGN) Package

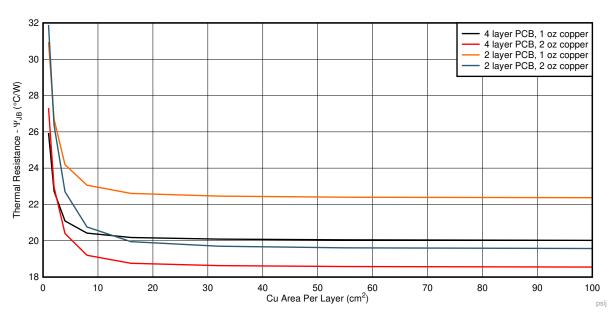


Figure 28. ψ_{JB} versus Cu Area for the HVSSOP (DGN) Package

SBVS402 - APRIL 2020

Application Information (continued)

8.1.1.1 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistance, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{IT} and Ψ_{IB}) are used in accordance with Equation 4 and given in the *Thermal Information* table.

$$\Psi_{JT}$$
: $T_J = T_T + \Psi_{JT} \times P_D$
 Ψ_{JB} : $T_J = T_B + \Psi_{JB} \times P_D$

where:

- P_D is the power dissipated as explained in Equation 1
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package

8.2 Typical Application

Figure 29 shows a typical application circuit for the TPS7B81. Different external component values can be used. depending on the end application. An application may require a larger output capacitor during fast load steps to prevent a large drop on the output voltage. TI recommends using a low-equivalent series resistance (ESR) ceramic capacitor with an X5R- or X7R-type dielectric.

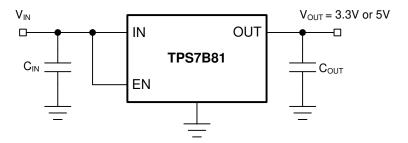


Figure 29. Typical Application Schematic

8.2.1 Design Requirements

Use the parameters listed in Table 2 for this design example.

Table 2. Design Requirements Parameters

PARAMETER	VALUE		
Input voltage range	3 V to 40 V		
Output voltage	5 V or 3.3 V		
Output current	150 mA maximum		

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current

8.2.2.1 Input Capacitor

Although an input capacitor is not required for stability, good analog design practice is to connect a 10-µF to 22μF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple rejection, and PSRR. The voltage rating must be greater than the maximum input voltage.

SBVS402 – APRIL 2020 www.ti.com

TEXAS INSTRUMENTS

8.2.2.2 Output Capacitor

To ensure the stability of the TPS7B81, the device requires an output capacitor with a value in the range from 1 μ F to 200 μ F and with an ESR range between 0.001 Ω and 5 Ω . TI recommends selecting a ceramic capacitor with low ESR to improve the load transient response.

8.2.3 Application Curve

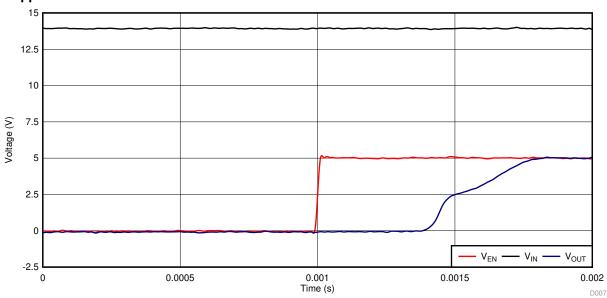


Figure 30. Power-Up Waveform (5 V)

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 3 V to 40 V. The input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B81, TI recommends adding a capacitor with a value greater than or equal to 10 µF with a 0.1-µF bypass capacitor in parallel at the input.

10 Layout

www.ti.com

10.1 Layout Guidelines

Layout is an important step for LDO power supplies, especially for high-voltage and large output current supplies. If the layout is not carefully designed, the regulator can fail to deliver enough output current because of thermal limitations. To improve the thermal performance of the device, and to maximize the current output at high ambient temperature, spread the copper under the thermal pad as far as possible and put enough thermal vias on the copper under the thermal pad. Figure 31 shows an example layout.

10.2 Layout Example

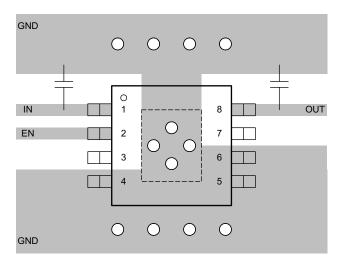


Figure 31. Example Layout Diagram

SBVS402 – APRIL 2020 www.ti.com



11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com 9-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
TPS7B8133DGNR	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	26BX
TPS7B8133DGNR.A	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	26BX
TPS7B8133DRVR	Active	Production	WSON (DRV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	26DH
TPS7B8133DRVR.A	Active	Production	WSON (DRV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	26DH
TPS7B8150DGNR	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	26CX
TPS7B8150DGNR.A	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	26CX
TPS7B8150DRVR	Active	Production	WSON (DRV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	26EH
TPS7B8150DRVR.A	Active	Production	WSON (DRV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	26EH

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

www.ti.com 9-Nov-2025

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS7B81:

Automotive: TPS7B81-Q1

NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

www.ti.com 3-Apr-2025

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B8133DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7B8133DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7B8150DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7B8150DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

www.ti.com 3-Apr-2025



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B8133DGNR	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7B8133DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7B8150DGNR	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7B8150DRVR	WSON	DRV	6	3000	210.0	185.0	35.0



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4206925/F





PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature
- number SLUA271 (www.ti.com/lit/slua271).

 5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



INSTRUMENTS www.ti.com

PowerPAD[™] HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-187.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
- 9. Size of metal pad may vary due to creepage requirement.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 11. Board assembly site may have different recommendations for stencil design.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025