TPS7B4254-Q1 Automotive, 150mA, 40V, Voltage-Tracking LDO With 4mV Tracking Tolerance

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
  - Device HBM ESD classification level 3A
  - Device CDM ESD classification level C6
- Wide input voltage range: –40V to 45V (max)
- Output voltage adjust range: 2V to 40V
- Output current capability: 150mA
- Very low output-tracking tolerance: ±4mV
- Low-dropout voltage: 160mV for I_{OUT} = 100mA
- Low quiescent current ($I_{(Q)}$):
  - < 4µA when ADJ = low
  - 60µA typical at light load
- Extremely wide ESR range:
  - 10µF to 500µF ceramic output capacitor
  - ESR range from 1mΩ to 20Ω
- Reverse polarity protection
- Current-limit and thermal-shutdown protection
- Output short-circuit-proof to ground and supply
- Inductive clamp at OUT pin
- 8-pin HSOIC PowerPAD™ package with exposed thermal pad
- For a newer drop-in alternative in the HSOIC package, see the TPS7B4258-Q1 device.

2 Applications

- Powertrain pressure sensors
- Powertrain temperature sensors
- Powertrain exhaust sensors
- Powertrain fluid concentration sensors
- Body control modules (BCM)
- Zone control module
- HVAC control module

3 Description

For automotive off-board sensors and low-current off-board modules, the power supply is through a long cable from the main board. In such cases, protection is required in the power devices for the off-board loads to prevent the onboard components from damage during a short to GND or short to battery caused by a broken cable. Off-board sensors require a power supply as consistent as that for onboard components to secure high accuracy of data acquisition.

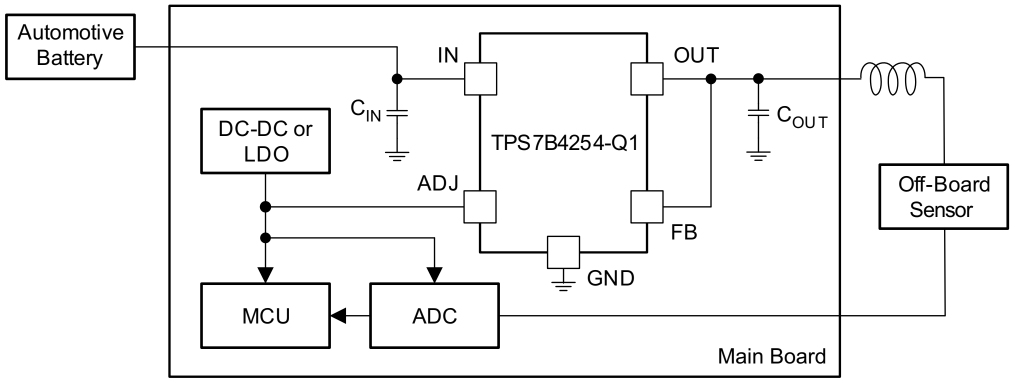
The TPS7B4254-Q1 is designed for automotive applications with a 45V load dump. The device can either be used as one tracking low-dropout (LDO) regulator or as a voltage tracker to build one closed power loop for off-board sensors with an onboard main supply. The output of the device is accurately regulated by a reference voltage at the ADJ pin.

To provide an accurate power supply to the off-board modules, the device offers a 4mV ultra-low tracking tolerance between the ADJ and FB pins across temperature. The back-to-back PMOS topology eliminates the need for an external diode under a reverse-polarity condition. The TPS7B4254-Q1 also includes thermal shutdown, inductive clamp, overload, and short-to-battery protection to prevent damage to onboard components during extreme conditions.

Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE(2)
TPS7B4254-Q1	DDA (HSOIC PowerPAD, 8)	4.9mm × 6mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

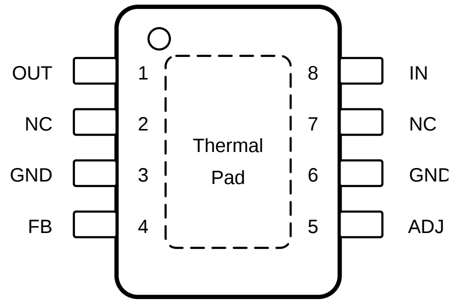


Typical Application Schematic

Table of Contents

1 Features.....1
2 Applications.....1
3 Description.....1
4 Pin Configuration and Functions.....4
5 Specifications.....5
5.1 Absolute Maximum Ratings.....5
5.2 ESD Ratings.....5
5.3 Recommended Operating Conditions.....5
5.4 Thermal Information.....6
5.5 Electrical Characteristics.....6
5.6 Typical Characteristics.....7
6 Detailed Description.....11
6.1 Overview.....11
6.2 Functional Block Diagram.....11
6.3 Feature Description.....11
6.4 Device Functional Modes.....14
7 Application and Implementation.....15
7.1 Application Information.....15
7.2 Typical Applications.....15
7.3 Power Supply Recommendations.....17
7.4 Layout.....17
8 Device and Documentation Support.....18
8.1 Device Support.....18
8.2 Documentation Support.....18
8.3 Receiving Notification of Documentation Updates.....18
8.4 Support Resources.....18
8.5 Trademarks.....18
8.6 Electrostatic Discharge Caution.....18
8.7 Glossary.....18
9 Revision History.....18
10 Mechanical, Packaging, and Orderable Information.....19
10.1 Mechanical Data.....20

4 Pin Configuration and Functions



NC – No internal connection

Figure 4-1. DDA Package 8-Pin HSOP With Exposed Thermal Pad Top View

Table 4-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
ADJ	5	I	Connect the reference to this pin. A low signal disables the device and a high signal enables the device. The reference voltage can be connected directly or by a voltage divider for lower output voltages. To compensate for line influences, connect a capacitor close to the device pin.
FB	4	I	This pin is the feedback pin, which can connect to the external resistor divider to select the output voltage.
GND	3, 6	G	Ground reference
IN	8	I	This pin is the device supply. To compensate for line influences, connect a capacitor close to the device pin.
NC	2, 7	NC	Not internally connected.
OUT	1	O	Block to GND with a capacitor close to the device pins with respect to the capacitance and ESR requirements listed in the *Output Capacitor* section.
Exposed thermal pad		—	Connect the thermal pad to the GND pin or leave the pad floating.

(1) I = input, O = output, G = ground, NC = no internal connection

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Unregulated input voltage	IN[(2)]	–40	45	V
Regulated output voltage	OUT[(2) (3)]	–1	45	V
Voltage difference between the input and output	IN – OUT	–40	45	V
Reference voltage	ADJ[(2)]	–0.3	45	V
Feedback input voltage for the tracker	FB[(2)]	–1	45	V
Reference voltage minus the input voltage	ADJ – IN[(4)]		18	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the GND pin.
(3) An internal diode is connected between the OUT and GND pins with 600mA dc current capability for inductive clamp protection.
(4) When the (ADJ – IN) voltage is higher than 18V, the (ADJ – OUT) voltage must be maintained lower than 18V, otherwise the device can be damaged.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(1)]	All pins except NC	±4000	V
			NC pins	±2000	
		Charged-device model (CDM), per AEC Q100-011		±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
V_{IN}	Unregulated input voltage[(2)]	4	40	V
V_{ADJ}	Reference input voltage	2	18	V
V_{FB}	Feedback input voltage for the tracker	2	18	V
V_{OUT}	Regulated output voltage	2	40	V
C_{OUT}	Output capacitor requirements[(3)]	10	500	µF
	Output ESR requirements[(4)]	0.001	20	Ω
T_J	Operating junction temperature	–40	150	°C

(1) Within the functional range the device operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related *Electrical Characteristics* table.
(2) $V_{IN} > V_{ADJ} + V_{DROPOUT}$
(3) The minimum output capacitance requirement is applicable for a worst-case capacitance tolerance of 30%. When a resistor divider is connected between the OUT and FB pins (the output voltage is higher than reference voltage), a 47nF feedforward capacitor is required to be connected between the OUT and FB pins for loop stability, and the ESR range of the output capacitor is required to be from 0.001 to 10Ω.
(4) Relevant ESR value at f = 10kHz

5.4 Thermal Information

THERMAL METRIC[1]		TPS7B4254-Q1 DDA (HSOIC) 8 PINS		UNIT
		ASO: ASE[2]	ASO: FMX[2]	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.4	42.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.1	57.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27	17.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.2	5.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26.9	17.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.4	7.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) See nomenclature table for more information regarding ASO.

5.5 Electrical Characteristics

V_{IN} = 13.5V, V_{ADJ} ≥ 2V, T_J = –40°C to 150°C, over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN(UVLO)}$	IN undervoltage detection	V_{IN} rising			3.65	V
		V_{IN} falling			2.8	V
ΔV_{OUT}	Output voltage tracking accuracy[1]	I_{OUT} = 100µA to 150mA, V_{IN} = 4 to 40V $V_{ADJ} < V_{IN} – 1V$ $2V < V_{ADJ} < 18V$	–4		4	mV
$\Delta V_{OUT(\Delta IO)}$	Load regulation, steady-state	I_{OUT} = 0.1 to 150mA, V_{ADJ}= 5V			4	mV
$\Delta V_{OUT(\Delta VI)}$	Line regulation, steady-state	I_{OUT} = 10mA, V_{IN} = 6 to 40V, V_{ADJ} = 5V			4	mV
PSRR	Power-supply ripple rejection	f_{rip} = 100Hz, V_{rip} = 0.5 VPP, C_{OUT} = 10µF, I_{OUT} = 100mA		70		dB
$V_{DROPOUT}$	Dropout voltage ($V_{DROPOUT} = V_{IN} – V_{OUT}$)	I_{OUT} = 100mA, $V_{IN} = V_{ADJ}$ ≥ 4V[2]		160	260	mV
$I_{OUT(LIM)}$	Output current limitation	V_{ADJ} = 5V, OUT short to GND	151	450	520	mA
$I_{R(IN)}$	Reverse current at IN	V_{IN} = 0V, V_{OUT} = 40V, V_{ADJ} = 5V	–2		0	µA
$I_{R(–IN)}$	Reverse current at negative IN	V_{IN} = –40V, V_{OUT} = 0V, V_{ADJ} = 5V	–10			µA
T_{SD}	Thermal shutdown temperature			175		°C
T_{SD_hys}	Thermal shutdown hysteresis			15		°C
I_Q	Current consumption	4V ≤ V_{IN} ≤ 40V, V_{ADJ} = 0V		2	4	µA
		4V ≤ V_{IN} ≤ 40V, V_{ADJ} = 5V, I_{OUT} < 100µA		60	100	µA
		4V ≤ V_{IN} ≤ 40V, V_{ADJ} = 5V, I_{OUT} < 150mA		210	260	µA
$I_{Q(DROPOUT)}$	Current consumption in dropout region	$V_{IN} = V_{ADJ}$ = 5V, I_{OUT} = 100µA		70	140	µA
I_{ADJ}	Reference input current	$V_{ADJ} = V_{FB}$ = 5V			5.5	µA
$V_{ADJ(LOW)}$	Reference low signal valid	V_{OUT} = 0V	0		0.7	V
$V_{ADJ(HIGH)}$	Reference high signal valid	$\lvert V_{OUT} – V_{ADJ}\rvert$ < 4mV	2		18	V
I_{FB}	FB bias current	$V_{ADJ} = V_{FB}$ = 5V			0.5	µA

(1) The tracking accuracy is specified when the FB pin is directly connected to the OUT pin which means $V_{ADJ} = V_{OUT}$, external resistor divider variance is not included.
(2) Measured when the output voltage, V_{OUT}, has dropped 10mV from the nominal value.

5.6 Typical Characteristics

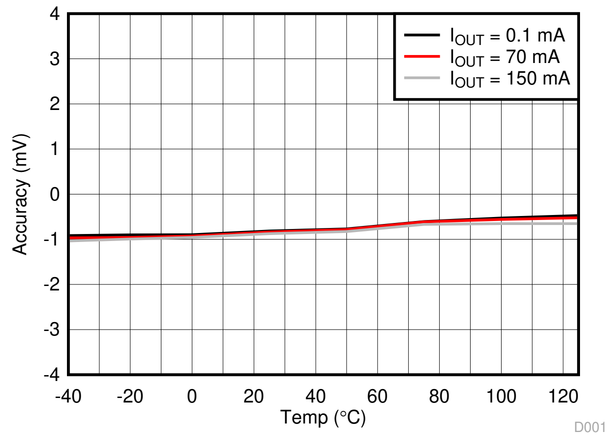


Figure 5-1. Tracking Accuracy vs Ambient Temperature

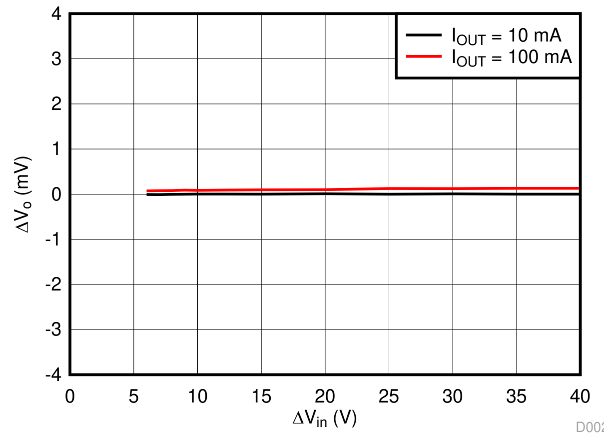


Figure 5-2. Line Regulation

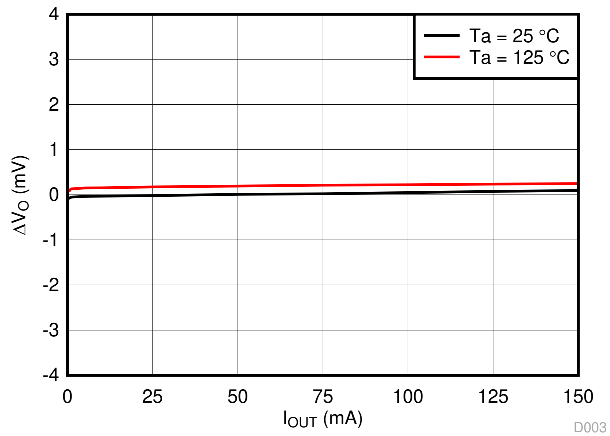
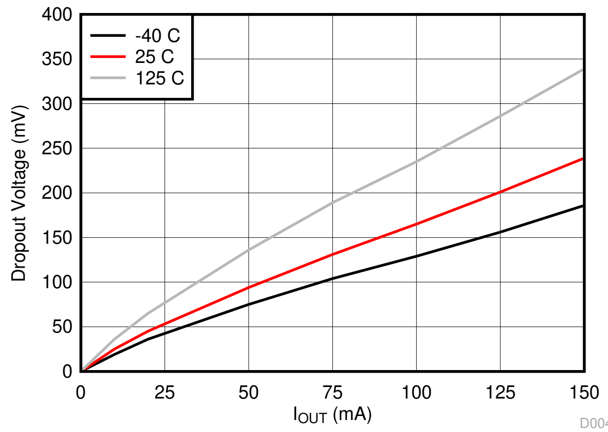
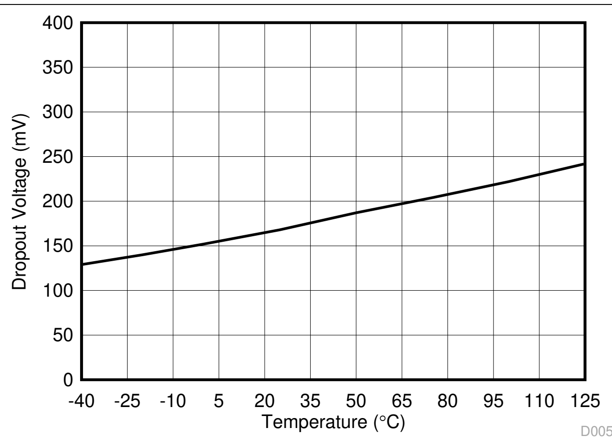


Figure 5-3. Load Regulation



$V_{IN} = V_{ADJ} = 4V$

Figure 5-4. Dropout Voltage vs Output Current



$V_{IN} = V_{ADJ} = 4V$ $I_{OUT} = 100mA$

Figure 5-5. Dropout Voltage vs Ambient Temperature

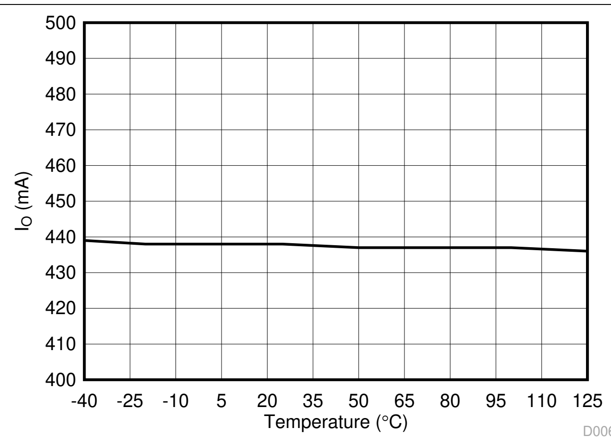


Figure 5-6. Current Limit ($I_{OUT(LIM)}$) vs Ambient Temperature

5.6 Typical Characteristics (continued)

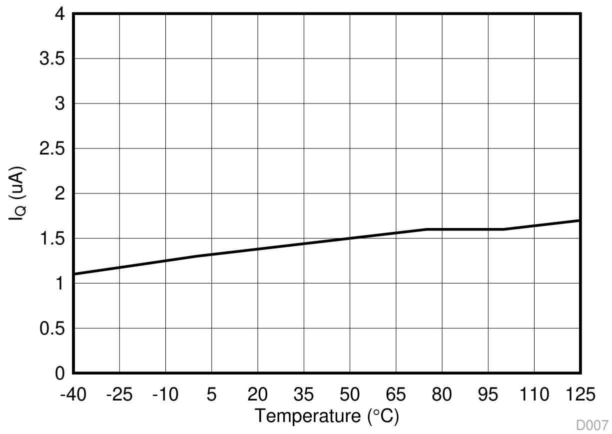


Figure 5-7. Shutdown Current vs Ambient Temperature

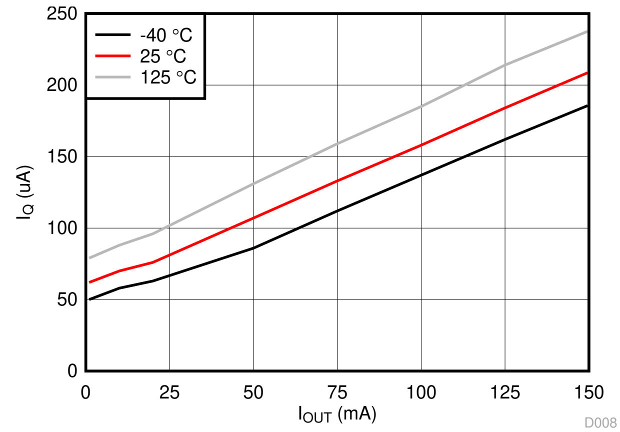


Figure 5-8. Quiescent Current vs Output Current

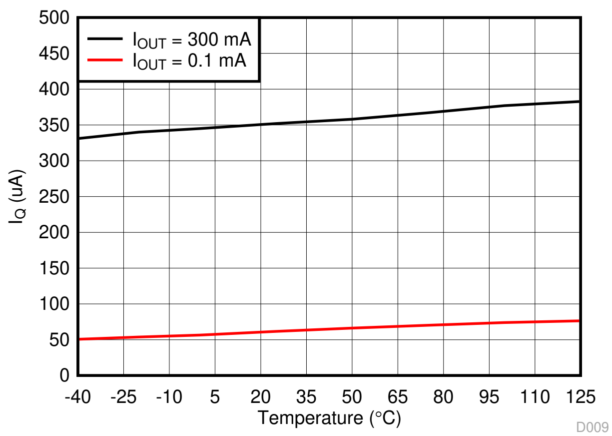
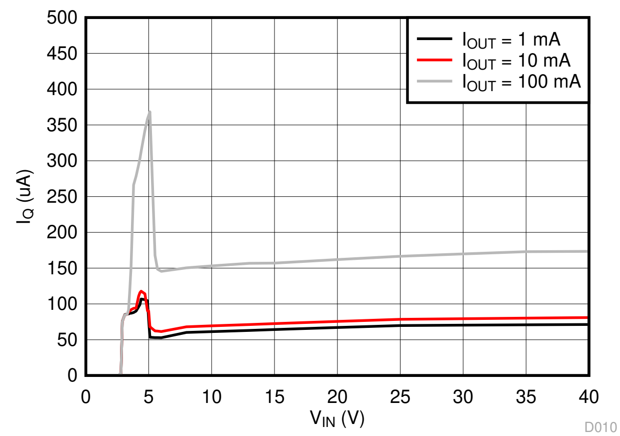
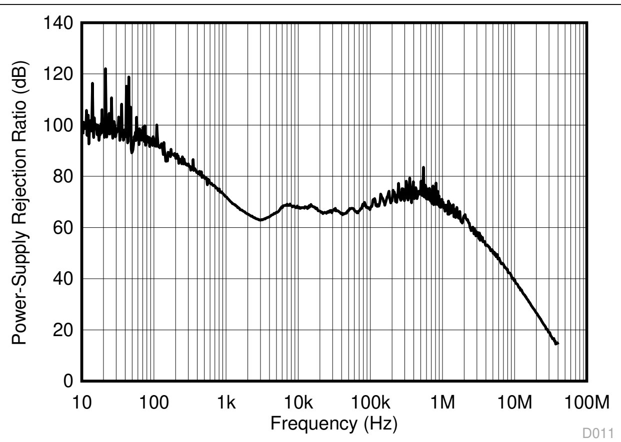


Figure 5-9. Quiescent Current vs Ambient Temperature



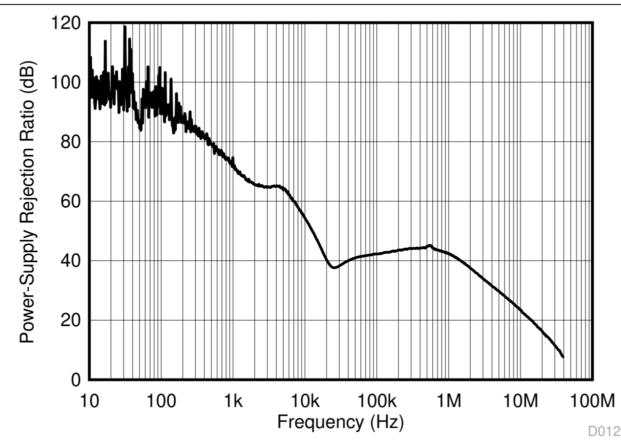
V_{ADJ} = 5V

Figure 5-10. Quiescent Current vs Input Voltage



C_{OUT} = 10µF I_{OUT} = 1mA T_A = 25°C
V_{IN} = 14V V_{ADJ} = 5V

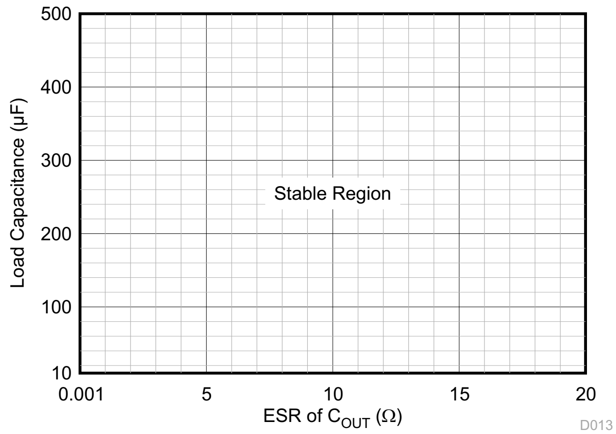
Figure 5-11. PSRR



C_{OUT} = 10µF I_{OUT} = 100mA T_A = 25°C
V_{IN} = 14V V_{ADJ} = 5V

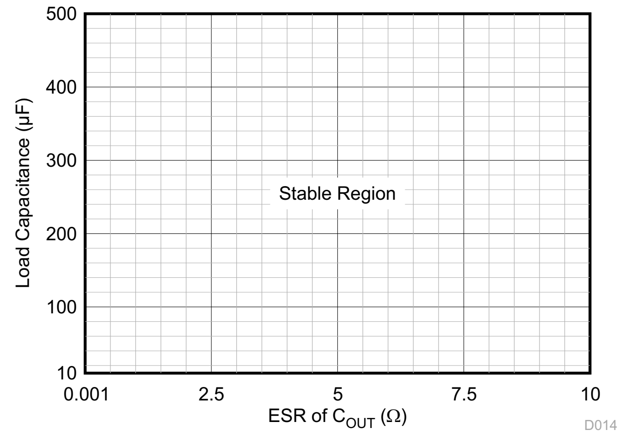
Figure 5-12. PSSR

5.6 Typical Characteristics (continued)



$V_{FB} = V_{OUT}$

Figure 5-13. ESR Stability vs Load Capacitance



$V_{FB} < V_{OUT}$

Figure 5-14. ESR Stability vs Load Capacitance

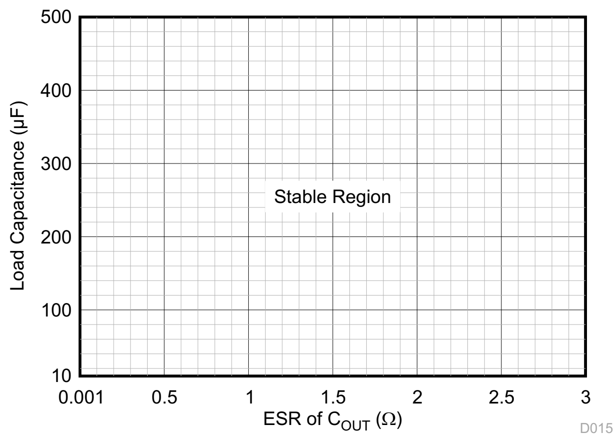
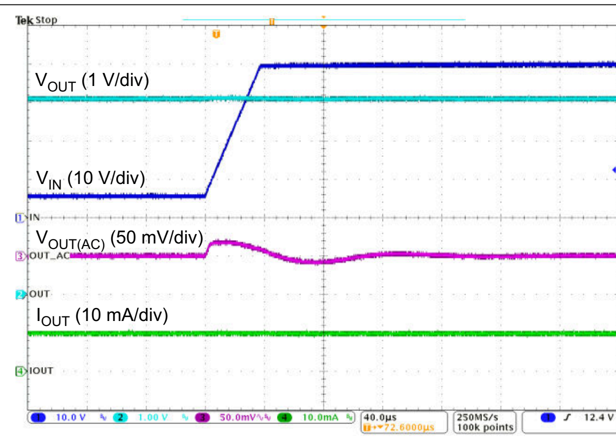
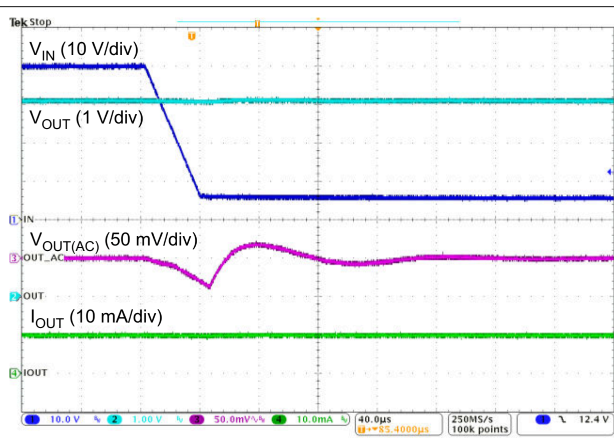


Figure 5-15. ESR Stability vs Load Capacitance (Multiple Output Capacitors in parallel)



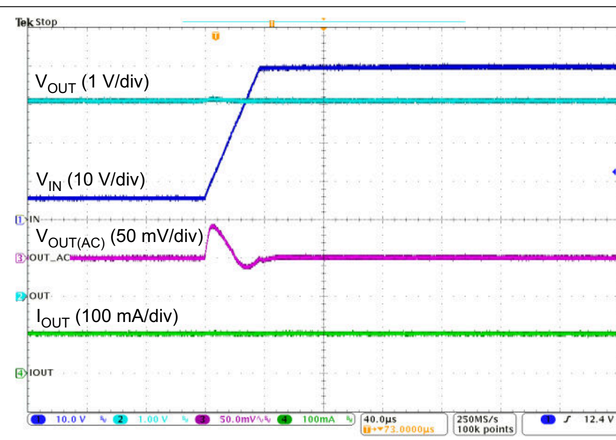
V_{IN} = 6 to 40V V_{ADJ} = 5V C_{OUT} = 10µF
I_{OUT} = 10mA 40µs/div

Figure 5-16. 6V to 40V Line Transient



V_{IN} = 40 to 6V V_{ADJ} = 5V C_{OUT} = 10µF
I_{OUT} = 10mA 40µs/div

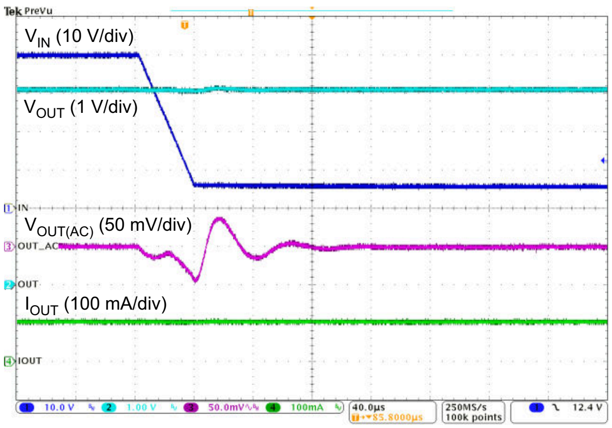
Figure 5-17. 40V to 6V Line Transient



V_{IN} = 6 to 40V V_{ADJ} = 5V C_{OUT} = 10µF
I_{OUT} = 100mA 40µs/div

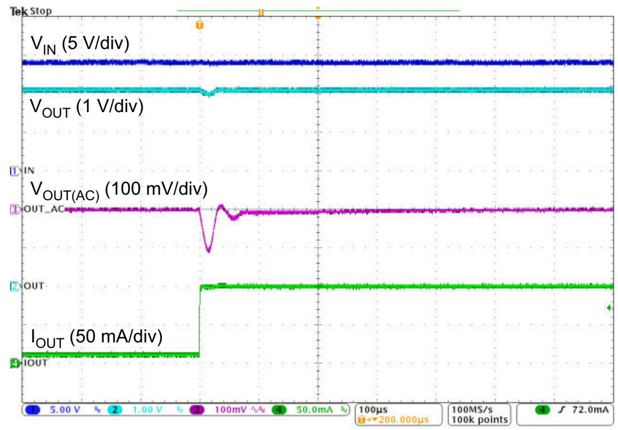
Figure 5-18. 6V to 40V Line Transient

5.6 Typical Characteristics (continued)



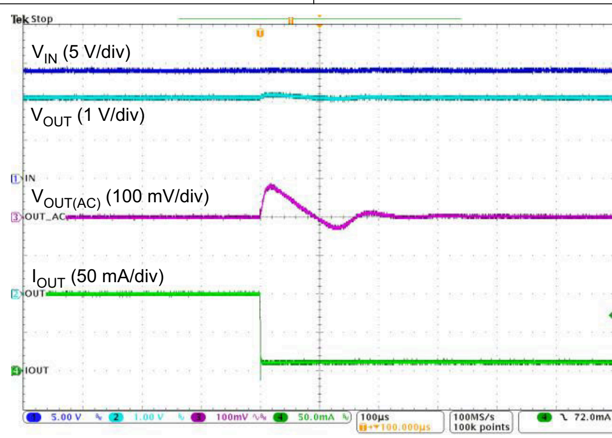
V_{IN} = 40 to 6V V_{ADJ} = 5V C_{OUT} = 10µF
I_{OUT} = 100mA 40µs/div

Figure 5-19. 40V to 6V Line Transient



V_{IN} = 14V V_{ADJ} = 5V C_{OUT} = 10µF
I_{OUT} = 10mA to 100mA 100µs/div

Figure 5-20. 10V to 100mA Load Transient



V_{IN} = 14V V_{ADJ} = 5V C_{OUT} = 10µF
I_{OUT} = 100mA to 10mA 100µs/div

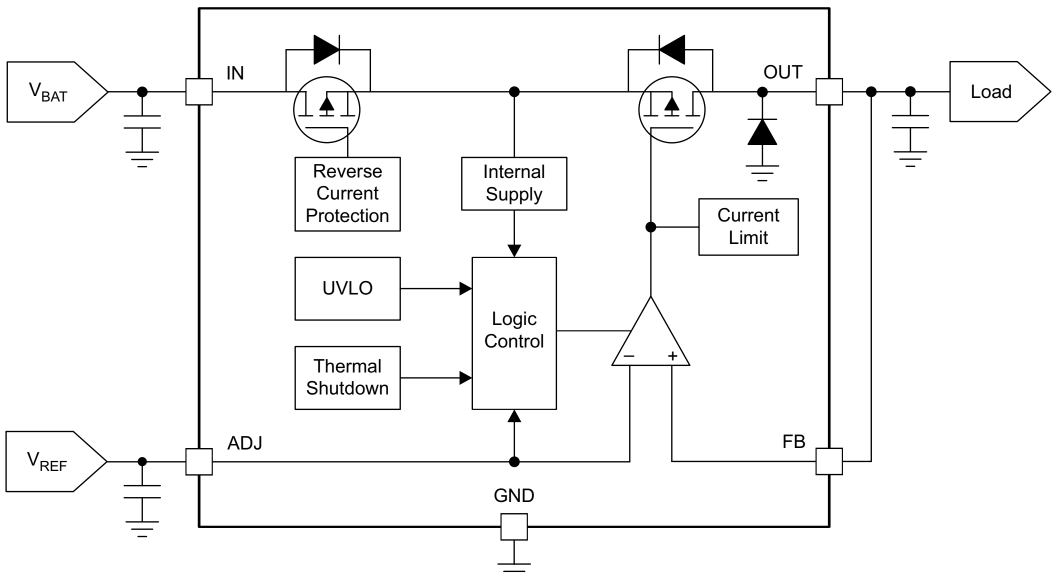
Figure 5-21. 100mA to 10mA Load Transient

6 Detailed Description

6.1 Overview

The TPS7B4254-Q1 device is a monolithic integrated low-dropout voltage tracker with an ultralow tracking tolerance. Key protection circuits are integrated in the device, including output current limitation, reverse polarity protection, inductive load clamp, output short-to-battery protection, and thermal shutdown in case of an overtemperature event.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Short-Circuit and Overcurrent Protection

The TPS7B4254-Q1 device features integrated fault protection, which makes the device a convinient choice for automotive applications. To keep the device in a safe area of operation during certain fault conditions, internal current-limit protection is used to limit the maximum output current. This protection protects the device from excessive power dissipation. For example, during a short-circuit condition on the output, the current through the pass element is limited to $I_{OUT(LIM)}$ to protect the device from excessive power dissipation.

6.3.2 Integrated Inductive Clamp Protection

During output turnoff, the cable inductance continues to source the current from the output of the device. The device integrates an inductive clamp at the OUT pin to help to dissipate the inductive energy stored in the cable. An internal diode is connected between the OUT and GND pins with a dc-current capability of 600mA for inductive clamp protection.

6.3.3 OUT Short-to-Battery and Reverse-Polarity Protection

The TPS7B4254-Q1 device can withstand a short to battery on the output, as shown in Figure 6-1. Therefore, no damage to the device occurs.

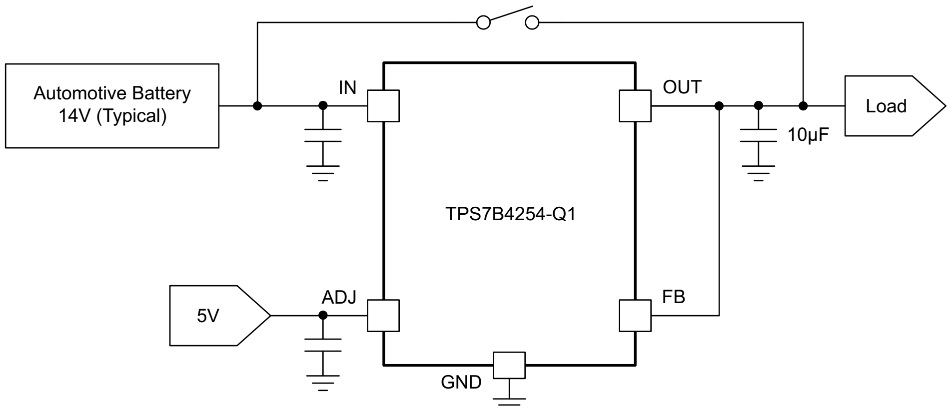


Figure 6-1. OUT Short to Battery, $V_{IN} = V_{BAT}$

A short to the battery can also occur when the device is powered by an isolated supply at lower voltage, as shown in Figure 6-2. In this case, the TPS7B4254-Q1 supply-input voltage is set to 7V when a short to battery (14V typical) occurs on the OUT pin, which operates at 5V. The internal back-to-back PMOS remains on for 1ms, during which the input voltage of the TPS7B4254-Q1 device charges up to the battery voltage. A diode connected between the output of the dc-dc converter and the input of the TPS7B4254-Q1 device is required in case the other loads connected behind the dc-dc converter cannot withstand the voltage of an automotive battery. To achieve a lower dropout voltage, TI recommends using a Schottky diode. This diode can be eliminated if the output of the dc-dc converter and the loads the converter powers, are able to withstand the automotive battery voltage.

The internal back-to-back PMOS is switched to OFF when reverse polarity or a short to battery occurs for 1ms. After that, the reverse current that flows out through the IN pin is less than 10µA. Meanwhile, a special ESD structure implemented at the input helps the device withstand –40V.

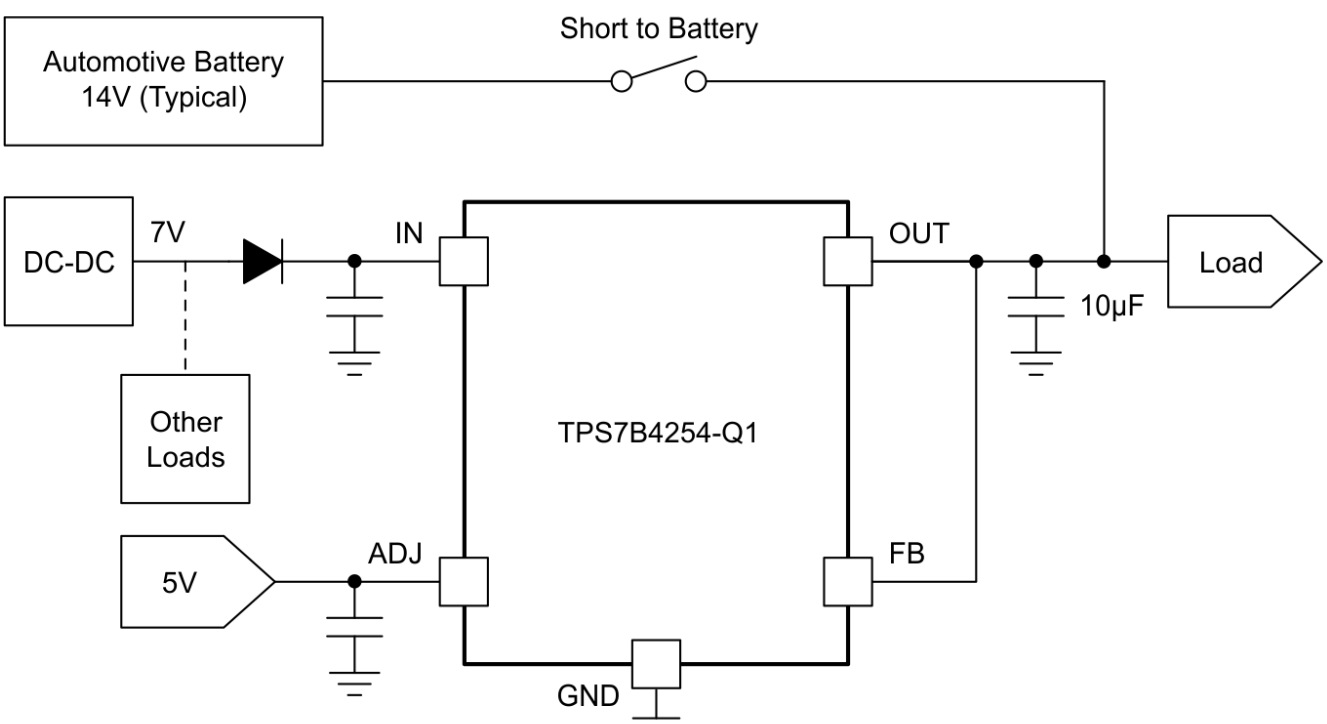


Figure 6-2. OUT Short to Battery, VIN < V_{BAT}

In most cases, the output of the TPS7B4254-Q1 device is shorted to the battery through an automotive cable. The parasitic inductance on the cable results in LC oscillation at the output of the TPS7B4254-Q1 device when the short to battery occurs. The peak voltage at the output of the TPS7B4254-Q1 device must be lower than the absolute-maximum voltage rating (45V) during LC oscillation.

6.3.4 Undervoltage Shutdown

The device has an internally fixed undervoltage-shutdown threshold. Undervoltage shutdown activates when the input voltage on IN drops below UVLO. This activation prevents the regulator from getting latched into an unknown state during a low input-supply voltage. If the input voltage has a negative transient that drops below the UVLO threshold and then recovers, the regulator shuts down and then powers up with a standard power-up sequence when the input voltage is above the required level.

6.3.5 Thermal Protection

The device incorporates a thermal shutdown (TSD) circuit as a protection from overheating. During continuous normal operation, the junction temperature must not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature decreases to 15°C (typical) lower than the TSD trip point, the output turns on.

Note

The purpose of the internal protection circuitry of the TPS7B4254-Q1 device is to protect against overload conditions and is not intended as a replacement for proper heat-sinking. Continuously running the device into thermal shutdown degrades device reliability.

6.3.6 Regulated Output (OUT)

The OUT pin is the regulated output based on the required voltage. The output has current limitation. During initial power up, the regulator has an incorporated soft-start feature to control the initial current through the pass element.

6.3.7 Adjustable Output Voltage (FB and ADJ)

6.3.7.1 OUT Voltage Equal to the Reference Voltage

With the reference voltage applied directly at the ADJ pin and the FB pin connected to the OUT pin, the voltage at the OUT pin equals to the reference voltage at the ADJ pin, as shown in Figure 6-3.

$$V_{OUT} = V_{ADJ} \tag{1}$$

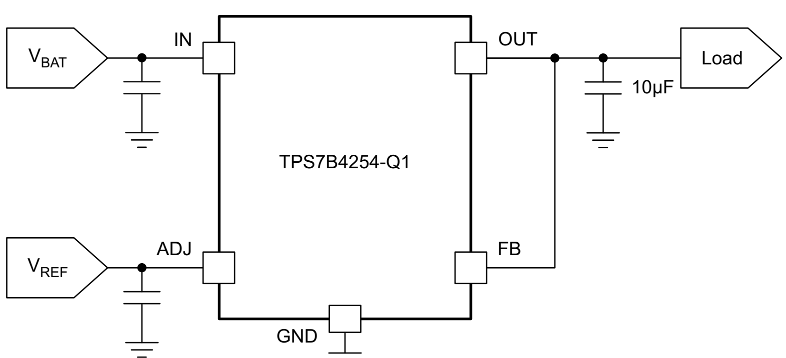


Figure 6-3. OUT Voltage Equal to the Reference Voltage

6.3.7.2 OUT Voltage Higher Than Reference Voltage

By using an external resistor divider connected between the OUT and FB pins, an output voltage higher than reference voltage can be generated as shown in Figure 6-4. Use Equation 2 to calculate the value of the output voltage. The recommended range for R1 and R2 is from 10kΩ to 100kΩ.

$$V_{OUT} = V_{ADJ} \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

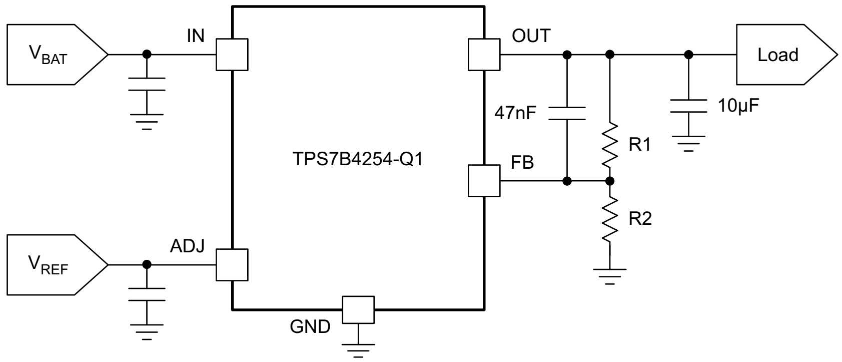


Figure 6-4. OUT Voltage Higher Than the Reference Voltage

6.3.7.3 Output Voltage Lower Than Reference Voltage

By using an external resistor divider connected at the ADJ pin, an output voltage lower than reference voltage can be generated as shown in Figure 6-5. Use Equation 3 to calculate the output voltage. The recommended value for both R1 and R2 is less than 100kΩ.

$$V_{OUT} = V_{REF} \times \frac{R2}{R1 + R2} \quad (3)$$

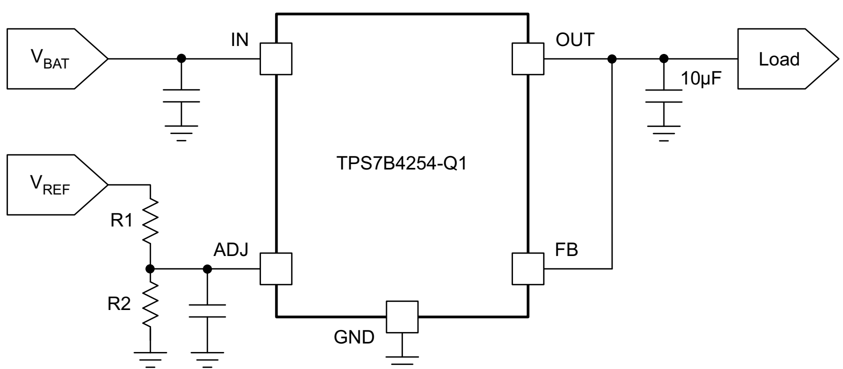


Figure 6-5. OUT Voltage Lower Than the Reference Voltage

6.4 Device Functional Modes

6.4.1 Operation With V_{IN} < 4V

The maximum UVLO voltage is 3.65V, and the device generally operates at an input voltage above 4V. The device can also operate at a lower input voltage; no minimum UVLO voltage is specified. At an input voltage below the actual UVLO voltage, the device does not operate.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS7B4254-Q1 device is a 150mA low-dropout tracking regulator with ultralow tracking tolerance. The PSpice transient model is available for download on the product folder and can be used to evaluate the basic function of the device.

7.2 Typical Applications

7.2.1 Application With Output Voltage Equal to the Reference Voltage

Figure 7-1 shows a typical application circuit for the TPS7B4254-Q1 device. Different values of external components can be used, depending on the end application. Some applications require a larger output capacitor during fast load steps to prevent a large drop on the output voltage. TI recommends using a low-ESR ceramic capacitor with a dielectric of type X5R or X7R.

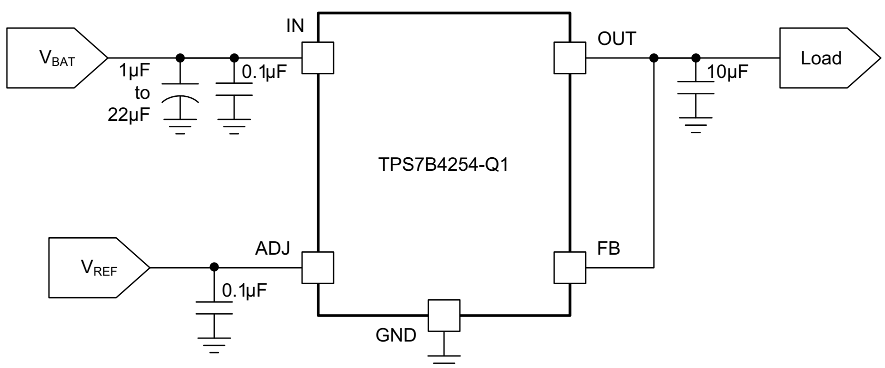


Figure 7-1. Output Voltage Equals the Reference Voltage

7.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 7-1 as the design parameters.

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	4V to 40V
Output voltage	2V to 40V
ADJ voltage	2V to 18V
Output capacitor	10 µF to 500 µF
Output capacitor ESR range	0.001Ω to 20Ω

7.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Reference voltage
- Output current

- Current limit

7.2.1.2.1 Input Capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommended value for the decoupling capacitor is 10µF with a 0.1µF ceramic bypass capacitor in parallel. The voltage rating must be greater than the maximum input voltage.

7.2.1.2.2 Output Capacitor

For stable operation, the TPS7B4254-Q1 device requires an output capacitor with a value in the range from 10µF to 500µF and with an ESR range from 0.001Ω to 20Ω when the FB pin is directly connected to the OUT pin. TI recommends selecting a ceramic capacitor with low ESR to improve the load transient response.

To achieve an output voltage higher than the reference voltage, a resistor divider is connected between the OUT pin and the FB pin. In this case, a 47nF feedforward capacitor must be connected between the OUT and FB pins for loop stability. The ESR of the output capacitor must be from 0.001Ω to 10Ω.

When multiple capacitors (two or more) are connected in parallel at the OUT pin, the ESR range of each output capacitor must be from 0.001Ω to 3Ω for loop stability.

In case the FB pin is shorted to ground, the TPS7B4254-Q1 device functions as a power switch with no need for the output capacitor.

7.2.1.3 Application Curve

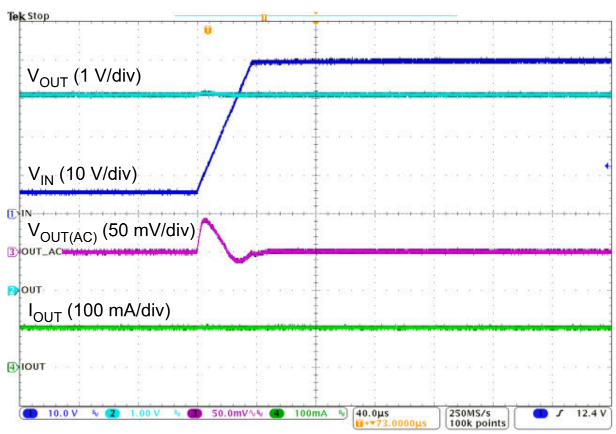


Figure 7-2. 6V to 40V Line Transient

7.2.2 High-Accuracy LDO

With an accurate voltage rail, the TPS7B4254-Q1 device can be used as an LDO with ultrahigh-accuracy output voltage by configuring the device as shown in Figure 7-3.

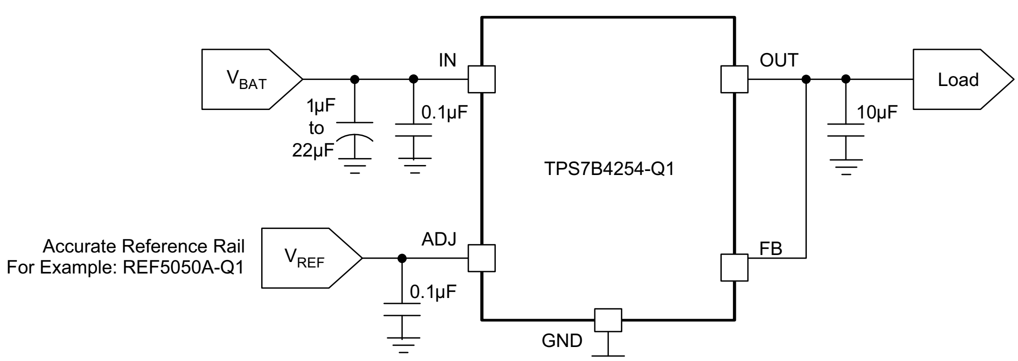


Figure 7-3. High-Accuracy LDO Application

For example, assume the reference voltage is a 5V rail with 0.1% accuracy. Because the tracking accuracy between the ADJ and OUT pins is specified below 4mV across temperature, the output accuracy of the TPS7B4254-Q1 device can be calculated with Equation 4.

$$\text{Accuracy of } V_{OUT} = \frac{V_{ADJ} \times 0.1\,\% + 4\text{ mV}}{V_{OUT}} \times 100\,\% = \frac{5 \times 0.1\,\% + 0.004}{5} \times 100\,\% = 0.18\,\% \tag{4}$$

7.3 Power Supply Recommendations

The device is designed to operate with an input voltage supply from 4V to 40V. This input supply must be well regulated. If the input supply is more than a few inches away from the TPS7B4254-Q1, TI recommends adding an electrolytic capacitor with a value of 10µF and a ceramic bypass capacitor at the input.

7.4 Layout

7.4.1 Layout Guidelines

For the layout of the TPS7B4254-Q1 device, place the input and output capacitors close to the devices as shown in the *Functional Block Diagram*. To enhance the thermal performance, TI recommends surrounding the device with some vias. Minimize equivalent series inductance (ESL) and ESR to maximize performance and ensure stability. Place every capacitor as close as possible to the device and on the same side of the PCB as the regulator.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. TI strongly discourages the use of vias and long traces for the path between the output capacitor and the OUT pins because vias can negatively impact system performance and even cause instability.

7.4.2 Layout Example

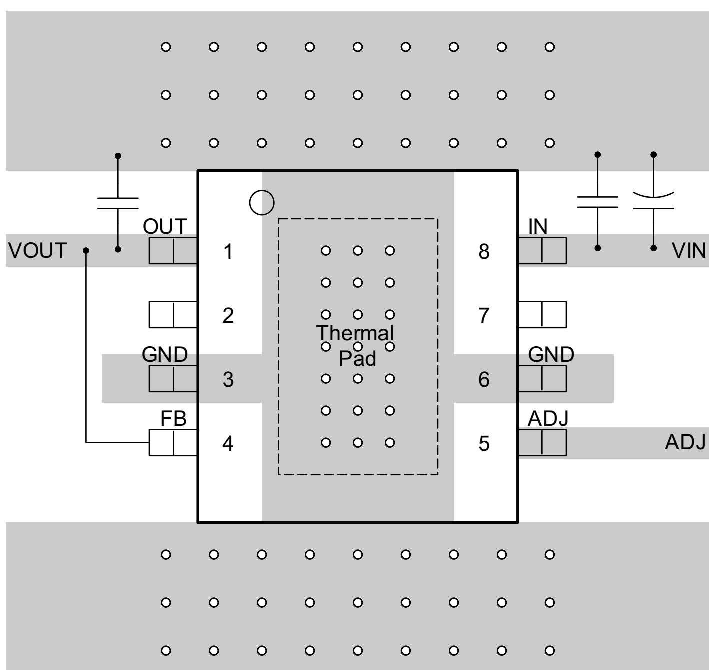


Figure 7-4. TPS7B4254-Q1 Layout Example

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

Table 8-1. Device Nomenclature

PRODUCT	V_{OUT}
TPS7B4254QyyyRQ1	**Q** indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard. **yyy** is the package designator (DDA = HSOIC). **Q1** indicates that this device is an automotive grade (AEC-Q100) device. This device potentially ships with multiple leadframes. The reel packaging label provides ASO information to distinguish which leadframe is used. ASO : FMX label denotes material from the new manufacturing site and ASO : ASE label denotes material from the legacy manufacturing site.

8.1.2 Development Support

For the TPS7B4254-Q1 PSpice Transient Model, go to .

8.2 Documentation Support

8.2.1 Related Documentation

- Texas Instruments, *TPS7B4254-Q1 Functional Safety FIT Rate, FMD and Pin FMA*, datasheet

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2016) to Revision C (November 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed *SO* to *HSOIC* throughout document	1
• Changed automotive-specific bullets in *Features* section	1
• Updated the *Thermal Information* table to include the thermal information for the DDA package from the multiple manufacturing sites (ASE, FMX)	6
• Updated the Device Nomenclature section to include a note that describes the method to distinguish the DDA material from different assembly sites	18
• Updated the mechanical drawings from DDA0008J to DDA0008J-C02	20

Changes from Revision A (May 2016) to Revision B (June 2016)	Page
• Changed MIN values for V_{ADJ}, V_{FB}, and V_{OUT} in the *Recommended Operating Conditions* table	5

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

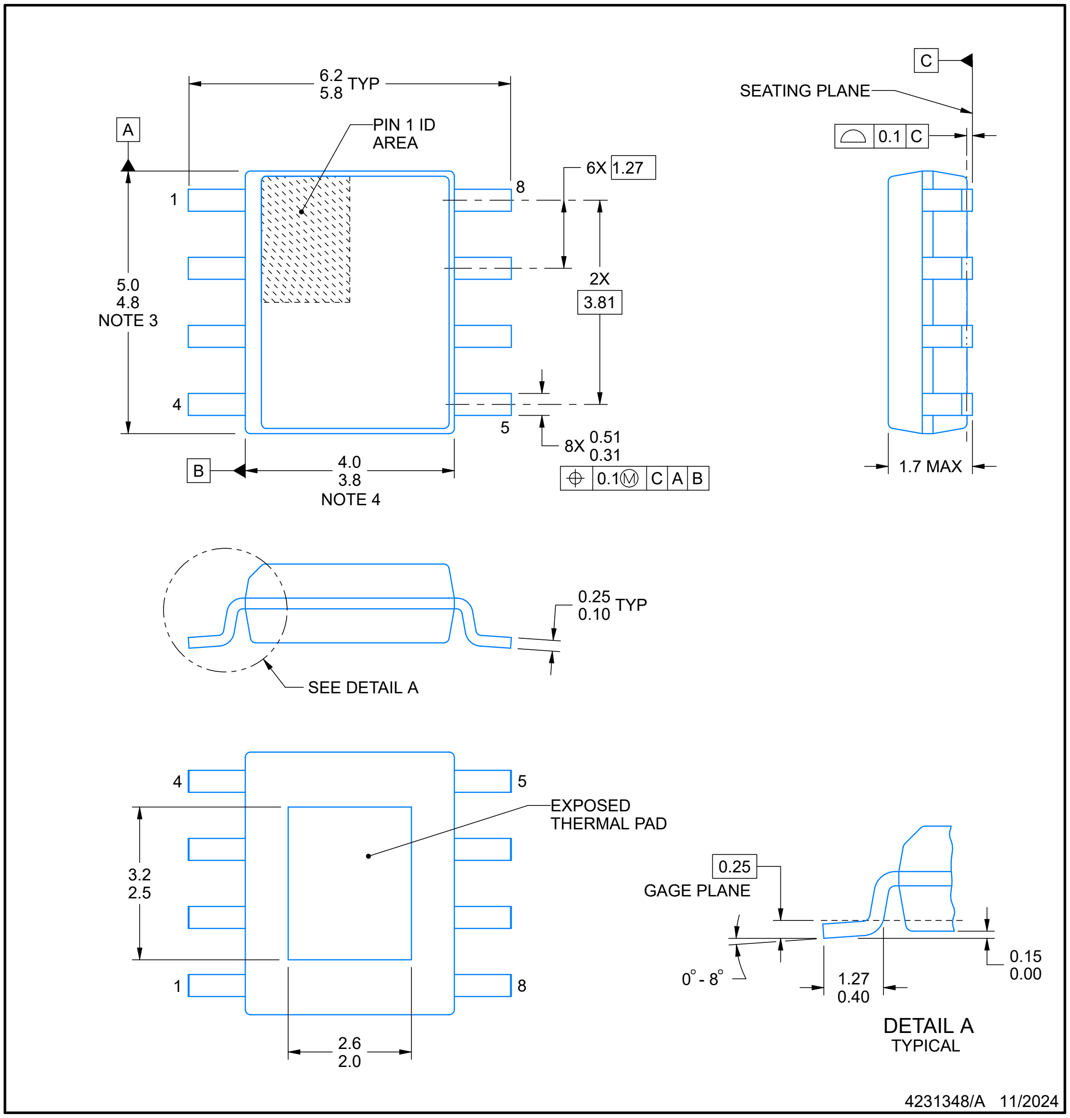
10.1 Mechanical Data

PACKAGE OUTLINE

DDA0008J-C02

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

NOTES:

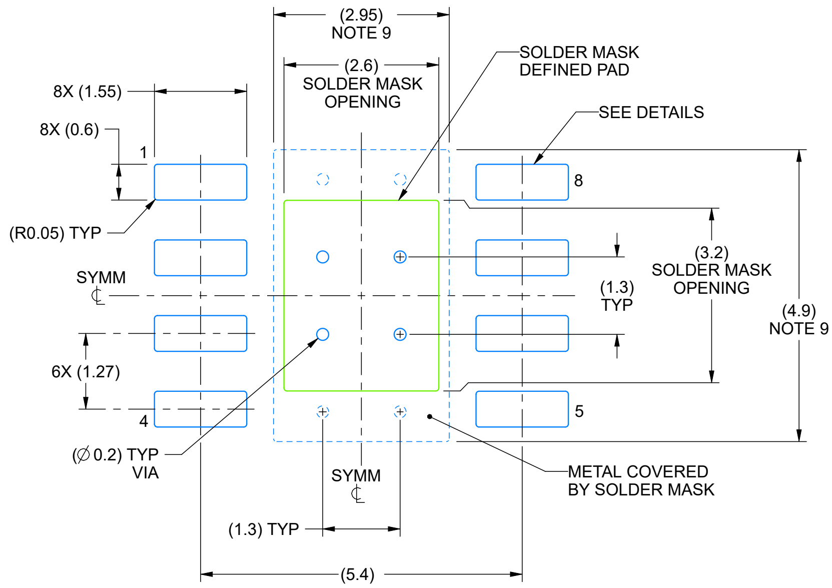
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.

www.ti.com

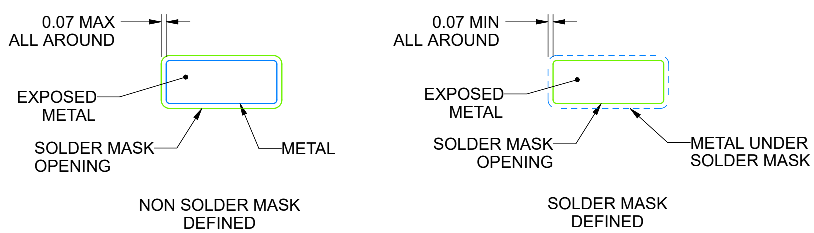
EXAMPLE BOARD LAYOUT

DDA0008J-C02 **PowerPAD ™ SOIC - 1.7 mm max height**

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X



SOLDER MASK DETAILS

4231348/A 11/2024

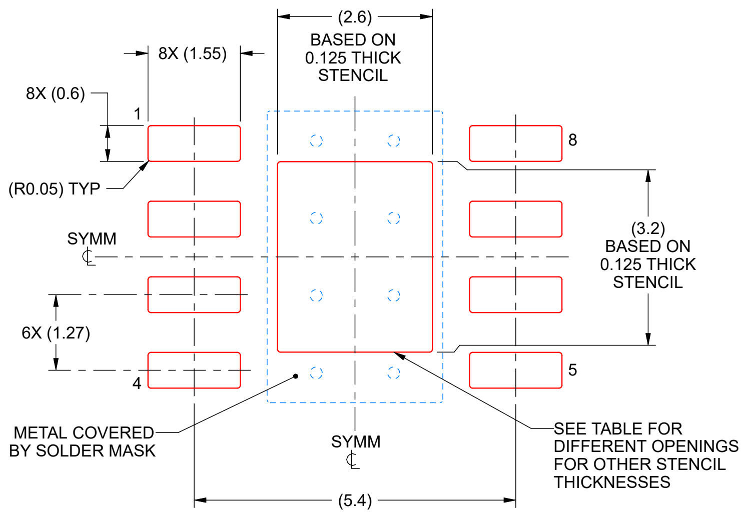
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DDA0008J-C02 **PowerPAD ™ SOIC - 1.7 mm max height**

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 3.58
0.125	2.6 X 3.2 (SHOWN)
0.150	2.37 X 2.92
0.175	2.20 X 2.70

4231348/A 11/2024

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

www.ti.com

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7B4254QDDARQ1	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	4254
TPS7B4254QDDARQ1.A	Active	Production	null (null) |	2500 | LARGE T&R	-	NIPDAUAG	Level-2-260C-1 YEAR	See TPS7B4254QDDARQ1	4254

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

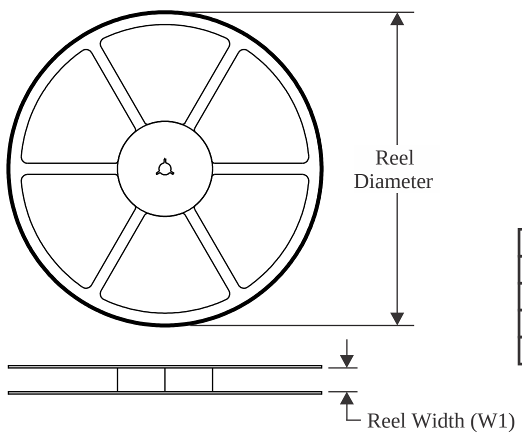
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

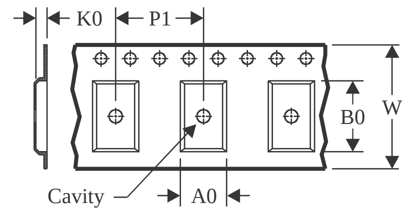
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

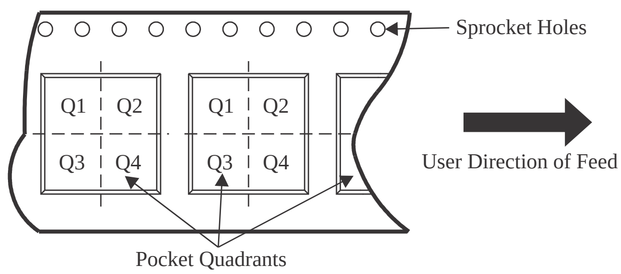


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

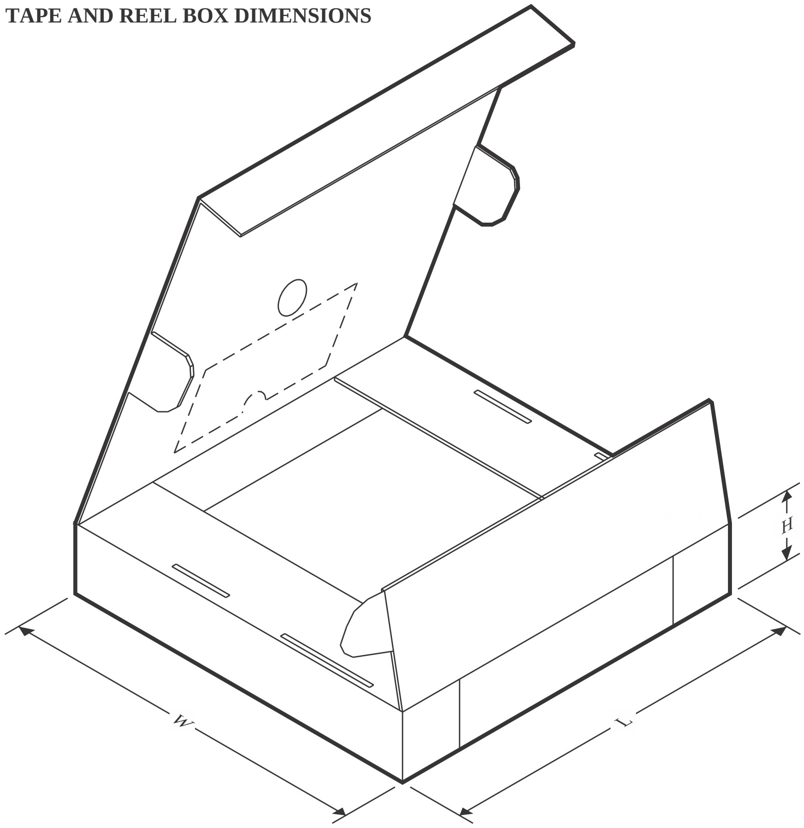
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B4254QDDARQ1	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B4254QDDARQ1	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0