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ULTRALOW-NOISE, HIGH-PSRR, FAST, RF, 250-mA LOW-DROPOUT LINEAR REGULATORS

FEATURES

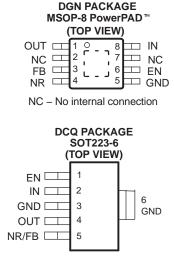
- 250-mA Low-Dropout Regulator With Enable
- Available in Fixed and Adjustable (1.2 V to 5.5 V) Versions
- High PSRR (60 dB at 10 kHz)
- Ultralow Noise (32 μVrms, TPS79428)
- Fast Start-Up Time (50 μs)
- Stable With a 2.2-µF Ceramic Capacitor
- Excellent Load/Line Transient Response
- Very Low Dropout Voltage (155 mV at Full Load)
- Available in MSOP-8 and SOT223-6 Packages

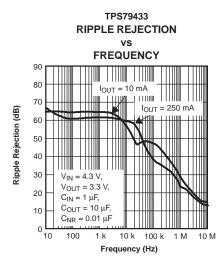
APPLICATIONS

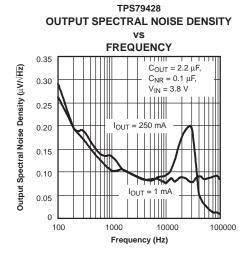
- RF: VCOs, Receivers, ADCs
- Audio
- Bluetooth™, Wireless LAN
- Cellular and Cordless Telephones
- Handheld Organizers, PDAs

DESCRIPTION

The TPS794xx family of low-dropout (LDO) linear voltage regulators features high power-supply rejection ratio (PSRR), ultralow-noise, fast start-up, and excellent line and load transient responses in small outline, MSOP-8 PowerPAD™ and SOT223-6 packages. Each device in the family is stable with a small 2.2-µF ceramic capacitor on the output. The family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (for example, 155 mV at 250 mA). Each device achieves fast start-up times (approximately 50 μs with a 0.001-μF bypass capacitor) while consuming low quiescent current (170 µA typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than μA. The TPS79428 exhibits approximately 32 μV_{RMS} of output voltage noise at 2.8 V output with a 0.1-μF bypass capacitor. Applications with analog components that are noise-sensitive, such as portable RF electronics, benefit from the high PSRR and low noise features as well as the fast response time.







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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

| PRODUCT | V _{OUT} ⁽²⁾ |
|-----------------------------|--|
| TPS794 xx<i>yyyz</i> | XX is nominal output voltage (for example, 28 = 2.8 V, 285 = 2.85 V, 01 = Adjustable). YYY is package designator. Z is package quantity. |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (2) Output voltages from 1.3 V to 5.0 V in 100 mV increments are available; minimum order quantities may apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS

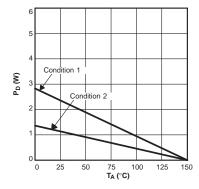
over operating temperature range unless otherwise noted(1)

| | VALUE |
|---|-------------------------------|
| V _{IN} range | -0.3 V to 6 V |
| V _{EN} range | -0.3 V to $V_{IN} + 0.3$ V |
| V _{OUT} range | -0.3 V to 6 V |
| Peak output current | Internally limited |
| ESD rating, HBM | 2 kV |
| ESD rating, CDM | 500 V |
| Continuous total power dissipation | See Dissipation Ratings Table |
| Junction temperature range, T _J | -40°C to +150°C |
| Storage temperature range, T _{stg} | −65°C to +150°C |

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PACKAGE DISSIPATION RATINGS

| PACKAGE | AIR FLOW (CFM) | R _{θJC} (°C/W) | R _{θJA} (°C/W) | T _A ≦ 25°C POWER RATING | T _A = 70°C POWER RATING | T _A = 85°C POWER RATING |
|---------|-------------------|----------------------------|----------------------------|---------------------------------------|---------------------------------------|---------------------------------------|
| | 0 | 8.47 | 55.09 | 2.27 W | 1.45 W | 1.18 W |
| DGN | 150 | 8.21 | 49.97 | 2.50 W | 1.60 W | 1.30 W |
| | 250 | 8.20 | 48.10 | 2.60 W | 1.66 W | 1.35 W |



| CONDITIONS | PACKAGE | PCB AREA | θЈА |
|------------|---------|----------------------------------|---------|
| 1 | SOT223 | 4in ² Top Side Only | 53°C/W |
| 2 | SOT223 | 0.5in ² Top Side Only | 110°C/W |

Figure 1. SOT223 Power Dissipation



ELECTRICAL CHARACTERISTICS

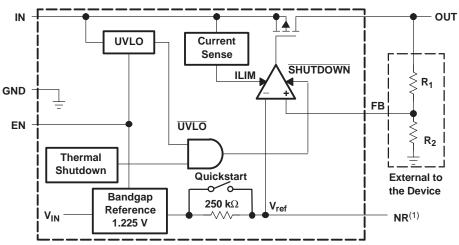
Over recommended operating temperature range (T $_J$ = -40°C to 125°C), V_{EN} = V_{IN} , V_{IN} = $V_{OUT(nom)}$ + 1 $V^{(1)}$, I_{OUT} = 1mA, C_{OUT} = 10 μ F, C_{NR} = 0.01 μ F, unless otherwise noted. Typical values are at 25°C.

| PARAMETER | | | TEST COND | MIN | TYP | MAX | UNIT | | |
|--|--|--|--|--|------------------|-------------------------|-----------------------|-------------------|--|
| Input voltag | je, V _{IN} ⁽¹⁾ | | | 2.7 | | 5.5 | V | | |
| Continuous | output current, I _{OUT} | | | | 0 | | 250 | mA | |
| | Output voltage range | TPS79401 | | | 1.225 | | 5.5 – V _{DO} | V | |
| Output voltage | A | TPS79401 ⁽²⁾ | $0 \mu A \le I_{OUT} \le 250 \text{ mA}, V_{OUT}$ | 0.97(V _{OUT}) | V _{OUT} | 1.03(V _{OUT}) | V | | |
| Voltage Accuracy | | Fixed V _{OUT} | $0 \mu A \le I_{OUT} \le 250 \text{ mA}, V_{OUT}$ | $_{\Gamma}$ + 1 V \leq V _{IN} \leq 5.5 V ⁽¹⁾ | -3.0 | | +3.0 | % | |
| Output volta | age line regulation (ΔV _{OUT} % | ₀ /ΔV _{IN}) ⁽¹⁾ | V_{OUT} + 1 V \leq V _{IN} \leq 5.5 V | | | 0.05 | 0.12 | %/V | |
| Load regulation (ΔV _{OUT} %/ΔI _{OUT}) | | $0 \ \mu A \le I_{OUT} \le 250 \ mA$ | | | 10 | | mV | | |
| | | TPS79428 | I _{OUT} = 250 mA | | | 155 | 210 | | |
| $V_{IN} = V_{OUT(nom)} - 0.1 V$ | | TPS79430 | I _{OUT} = 250 mA | | | 155 | 210 | mV | |
| | | TPS79433 | I _{OUT} = 250 mA | | | 145 | 200 | | |
| Output current limit | | | V _{OUT} = 0 V | | | 925 | | mA | |
| Ground pin current | | | $0 \ \mu A \le I_{OUT} \le 250 \ mA$ | | 170 | 220 | μΑ | | |
| Shutdown current ⁽⁴⁾ | | | $V_{EN} = 0 \text{ V}, 2.7 \text{ V} \le V_{IN} \le 5.5$ | 5 V | | 0.07 | 1 | μΑ | |
| FB pin current | | | V _{FB} = 1.225 V | | | | 1 | μΑ | |
| | | | f = 100 Hz, I _{OUT} = 250 mA | | 65 | | | | |
| Power-supp | oly ripple rejection | TPS79428 | f = 10 kHz, I _{OUT} = 250 mA | | 60 | | dB | | |
| | | | f = 100 kHz, I _{OUT} = 250 mA | | 40 | | | | |
| | | | | $C_{NR} = 0.001 \ \mu F$ | | 55 | | | |
| 0.44!- | | TD070400 | BW = 100 Hz to 100 kHz, | $C_{NR} = 0.0047 \mu F$ | | 36 | | μV _{RMS} | |
| Output nois | se voltage | TPS79428 | $I_{OUT} = 250 \text{ mA}$ | C _{NR} = 0.01 μF | | 33 | | | |
| | | | | $C_{NR} = 0.1 \mu F$ | | 32 | | | |
| | | | | C _{NR} = 0.001 μF | | 50 | | | |
| Time, start- | up | TPS79428 | $R_L=14~\Omega,~C_{OUT}=1~\mu F$ | $C_{NR} = 0.0047 \mu F$ | | 70 | | μs | |
| | | | | $C_{NR} = 0.01 \mu F$ | | 100 | | 1 | |
| High-level enable input voltage | | $2.7 \text{ V} \le V_{IN} \le 5.5 \text{ V}$ | 1.7 | | V_{IN} | V | | | |
| Low-level enable input voltage | | $2.7~\textrm{V} \leq \textrm{V}_{\textrm{IN}} \leq 5.5~\textrm{V}$ | 0 | | 0.7 | V | | | |
| EN pin current | | V _{EN} = 0 | 1 | | 1 | μΑ | | | |
| UVLO thres | shold | | V _{CC} rising | 2.25 | | 2.65 | V | | |
| UVLO hyste | eresis | | | | 100 | | mV | | |

Minimum V_{IN} is 2.7 V or V_{OUT} + V_{DO}, whichever is greater.
 Tolerance of external resistors not included in this specification.
 Dropout is not measured for the TPS79418 and TPS79425 since minimum V_{IN} = 2.7 V.
 For adjustable versions, this applies only after V_{IN} is applied; then V_{EN} transitions high to low.

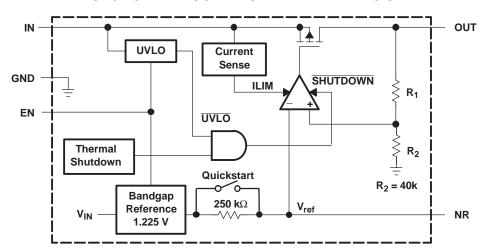


FUNCTIONAL BLOCK DIAGRAM—ADJUSTABLE VERSION



(1) Not Available on DCQ (SOT223) options.

FUNCTIONAL BLOCK DIAGRAM—FIXED VERSION

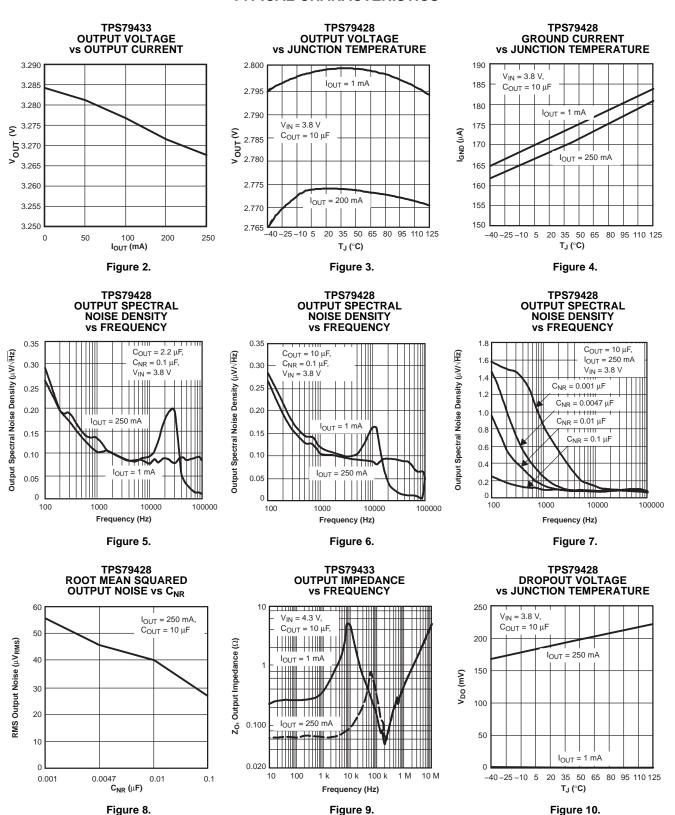


Terminal Functions

| | TERMINA | L | |
|------|---------------|-----------------|--|
| NAME | DGN (MSOP) | DCQ (SOT223) | DESCRIPTION |
| NR | 4 | 5 | Connecting an external capacitor to this pin bypasses noise generated by the internal bandgap, which improves power-supply rejection and reduces output noise. |
| EN | 6 | 1 | The EN terminal is an input that enables or shuts down the device. When EN is a logic high, the device is enabled. When the device is a logic low, the device is in shutdown mode. |
| FB | 3 | 5 | Feedback input voltage for the adjustable device. |
| GND | 5, PAD | 3, 6 | Regulator ground |
| IN | 8 | 2 | Unregulated input to the device. |
| NC | 2, 7 | | No internal connection. |
| OUT | 1 | 4 | Regulator output |

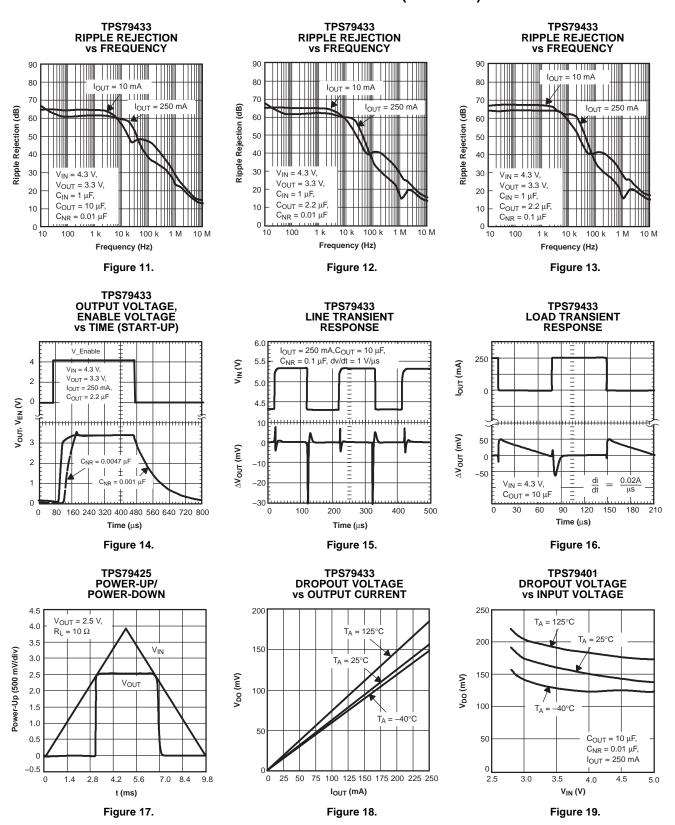


TYPICAL CHARACTERISTICS





TYPICAL CHARACTERISTICS (continued)





TYPICAL CHARACTERISTICS (continued)

TPS79428 TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT

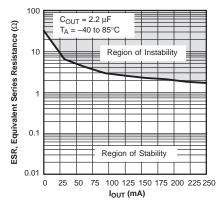


Figure 20.

TPS79428 TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT

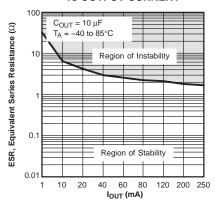


Figure 21.



APPLICATION INFORMATION

The TPS794xx family of low-dropout (LDO) regulators has been optimized for use in noise-sensitive equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (265 μA typically), and an enable input to reduce supply currents to less than 1 μA when the regulator is turned off.

A typical application circuit is shown in Figure 22.

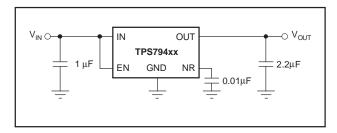


Figure 22. Typical Application Circuit

EXTERNAL CAPACITOR REQUIREMENTS

A 1-µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS794xx, is required for stability and improves transient response, noise rejection, and ripple rejection. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like most low-dropout regulators, the TPS794xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 1 $\mu\text{F}.$ Any

1 μF or larger ceramic capacitor is suitable.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS794xx has an NR pin which is connected to the voltage reference through a 250-k Ω internal resistor. The 250-k Ω internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low-pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In

order for the regulator to operate properly, the current flow out of the NR pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor, thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current. The bypass capacitor should be no more than 0.1- μF in order to ensure that it is fully charged during the quickstart time provided by the internal switch shown in the Functional Block Diagram.

For example, the TPS79430 exhibits only 33 μV_{RMS} of output voltage noise using a 0.1- μF ceramic bypass capacitor and a 10- μF ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases because of the RC time constant at the bypass pin that is created by the internal 250-k Ω resistor and external capacitor.

BOARD LAYOUT RECOMMENDATION TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac measurements such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT} , with each ground plane connected only at the ground pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the ground pin of the device.

REGULATOR MOUNTING

The tab of the SOT223-6 package is electrically connected to ground. For best thermal performance, the tab of the surface-mount version should be soldered directly to a circuit-board copper area. Increasing the copper area improves heat dissipation.

Solder pad footprint recommendations for the devices are presented in Application Report SBFA015, Solder Pad Recommendations for Surface-Mount Devices, available from the TI web site (www.ti.com).



PROGRAMMING THE TPS79401 ADJUSTABLE LDO REGULATOR

The output voltage of the TPS79401 adjustable regulator is programmed using an external resistor divider as shown in Figure 23. The output voltage is calculated using Equation 1:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \tag{1}$$

where:

 V_{REF} = 1.2246 V typ (the internal reference voltage)

Resistors R_1 and R_2 should be chosen for approximately 40- μ A divider current. Lower value resistors can be used for improved noise performance, but the device wastes more power. Higher values should be avoided, as leakage current at FB increases the output voltage error.

The recommended design procedure is to choose $R_2=30.1\,k\Omega$ to set the divider current at 40 μ A, $C_1=15$ pF for stability, and then calculate R_1 using Equation 2:

$$R_{1} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_{2}$$
 (2)

In order to improve the stability of the adjustable version, it is suggested that a small compensation capacitor be placed between OUT and FB.

The approximate value of this capacitor can be calculated as Equation 3:

$$C_1 = \frac{(3 \times 10^{-7}) \times (R_1 + R_2)}{(R_1 \times R_2)}$$
(3)

The suggested value of this capacitor for several resistor ratios is shown in the table within Figure 23. If this capacitor is not used (such as in a unity-gain configuration), then the minimum recommended output capacitor is 2.2 μ F instead of 1 μ F.

REGULATOR PROTECTION

The TPS794xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS794xx features internal current limiting and thermal protection. During normal operation, the TPS794xx limits output current to approximately 2.8 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

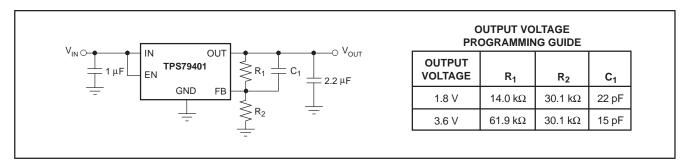


Figure 23. TPS79401 Adjustable LDO Regulator Programming



THERMAL INFORMATION

The amount of heat that an LDO linear regulator generates is directly proportional to the amount of power it dissipates during operation. All integrated circuits have a maximum allowable junction temperature (T_Jmax) above which normal operation is not assured. A system designer must design the operating environment so that the operating junction temperature (T_J) does not exceed the maximum junction temperature (T_Jmax). The two main environmental variables that a designer can use to improve thermal performance are air flow and external heatsinks. The purpose of this information is to aid the designer in determining the proper operating environment for a linear regulator that is operating at a specific power level.

In general, the maximum expected power (P_Dmax) consumed by a linear regulator is computed as shown in Equation 4:

$$P_{D} max = (V_{IN(avg)} - V_{OUT(avg)}) \times I_{OUT(avg)} + V_{I(avg)} \times I_{Q}$$
(4)

where:

- V_{IN(avg)} is the average input voltage
- V_{OUT(avg)} is the average output voltage
- I_{OUT(avg)} is the average output current
- I_O is the quiescent current

For most TI LDO regulators, the quiescent current is insignificant compared to the average output current; therefore, the term $V_{\text{IN}(avg)} \times I_{\text{Q}}$ can be neglected. The operating junction temperature is computed by adding the ambient temperature (T_A) and the increase in temperature due to the regulator's power dissipation. The temperature rise is computed by multiplying the maximum expected power dissipation by the sum of the thermal resistances between the junction and the case (R_{OJC}), the case to heatsink $(R_{\Theta CS})$, and the heatsink to ambient $(R_{\Theta SA})$. Thermal resistances are measures of how effectively an object dissipates heat. Typically, the larger the device, the more surface area available for power dissipation and the lower the object's thermal resistance.

Figure 24 illustrates these thermal resistances for a SOT223 package mounted in a JEDEC low-K board.

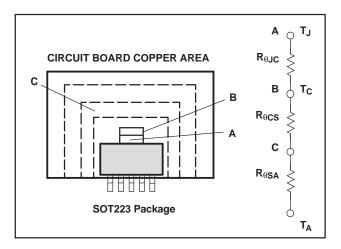


Figure 24. Thermal Resistances

Equation 5 summarizes the computation:

$$T_J = T_A + P_D \max \times (R_{\theta JC} + R_{\theta CS} + R_{\theta SA})$$
 (5)

The $R_{\Theta JC}$ is specific to each regulator as determined by its package, lead frame, and die size provided in the regulator's data sheet. The $R_{\Theta SA}$ is a function of the type and size of heatsink. For example, black body radiator type heatsinks can have $R_{\Theta CS}$ values ranging from 5°C/W for very large heatsinks to 50°C/W for very small heatsinks. The $R_{\Theta CS}$ is a function of how the package is attached to the heatsink. For example, if a thermal compound is used to attach a heatsink to a SOT223 package, $R_{\Theta CS}$ of 1°C/W is reasonable.

Even if no external black body radiator type heatsink is attached to the package, the board on which the regulator is mounted provides some heatsinking through the pin solder connections. Some packages, like the DDPAK and SOT223 packages, use a copper plane underneath the package or the circuit board ground plane for additional heatsinking to improve their thermal performance. Computer-aided thermal modeling can be used to compute very accurate approximations of an integrated circuit's performance in different operating thermal environments (for example, different types of circuit boards, different types and sizes of heatsinks, different air flows, etc.). Using these models, the three thermal resistances can be combined into one thermal resistance between junction and ambient $(R_{\Theta,JA})$. This $R_{\Theta,JA}$ is valid only for the specific operating environment used in the computer model.



Equation 5 simplifies into Equation 6:

$$T_{J} = T_{A} + P_{D} \max \times R_{\theta J A}$$
 (6)

Rearranging Equation 6 gives Equation 7:

$$R_{\theta JA} = \frac{T_J - T_A}{P_D max} \tag{7}$$

Using Equation 6 and the computer model generated curves shown in Figure 25, a designer can quickly heatsink compute required thermal the resistance/board area for а given ambient temperature, power dissipation, and operating environment.

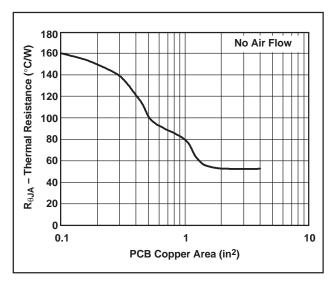


Figure 25. SOT223 Thermal Resistance vs PCB Copper Area

SOT223 POWER DISSIPATION

The SOT223 package provides an effective means of managing power dissipation in surface-mount

applications. The SOT223 package dimensions are provided in the *Mechanical Data* section at the end of the data sheet. The addition of a copper plane directly underneath the SOT223 package enhances the thermal performance of the package.

To illustrate, the TPS79425 in a SOT223 package was chosen. For this example, the average input voltage is 3.3 V, the output voltage is 2.5 V, the average output current is 1 A, the ambient temperature 55°C, no air flow is present, and the operating environment is the same as documented below. Neglecting the quiescent current, the maximum average power is Equation 8:

$$P_D \max = (3.3 - 2.5)V \times 1A = 800 mW$$
 (8)

Substituting T_J max for T_J into Equation 4 gives Equation 9:

$$R_{\theta JA} \max = (125 - 55)^{\circ}C/800 \,\text{mW} = 87.5^{\circ}C/W$$
 (9)

From Figure 25, $R_{\theta JA}$ vs PCB Copper Area, the ground plane needs to be $0.55~\text{in}^2$ for the part to dissipate 800 mW. The operating environment used to construct Figure 25 consisted of a board with 1 oz. copper planes. The package is soldered to a 1 oz. copper pad on the top of the board. The pad is tied through thermal vias to the 1 oz. ground plane.

From the data in Figure 25 and rearranging equation 6, the maximum power dissipation for a different ground plane area and a specific ambient temperature can be computed, as shown in Figure 26.

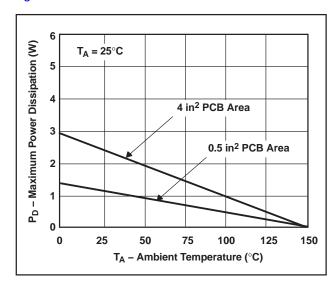


Figure 26. SOT223 Maximum Power Dissipation vs Ambient Temperature

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PACKAGING INFORMATION

| Orderable part number | Status | Material type | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material | MSL rating/ Peak reflow | Op temp (°C) | Part marking (6) |
|-----------------------|----------|---------------|-------------------|-----------------------|-----------------|--------------------------------|----------------------------|--------------|------------------|
| TPS79401DCQ | Obsolete | Production | SOT-223 (DCQ) 6 | - | - | Call TI | Call TI | -40 to 85 | PS79401 |
| TPS79401DCQR | Active | Production | SOT-223 (DCQ) 6 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PS79401 |
| TPS79401DCQR.A | Active | Production | SOT-223 (DCQ) 6 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PS79401 |
| TPS79401DGNR | Active | Production | HVSSOP (DGN) 8 | 2500 LARGE T&R | Yes | Call TI Nipdauag Nipdau | Level-1-260C-UNLIM | -40 to 85 | AXL |
| TPS79401DGNR.A | Active | Production | HVSSOP (DGN) 8 | 2500 LARGE T&R | Yes | Call TI | Level-1-260C-UNLIM | -40 to 85 | AXL |
| TPS79401DGNT | Obsolete | Production | HVSSOP (DGN) 8 | - | - | Call TI | Call TI | -40 to 85 | AXL |
| TPS79418DCQ | Obsolete | Production | SOT-223 (DCQ) 6 | - | - | Call TI | Call TI | -40 to 85 | PS79418 |
| TPS79418DCQR | Active | Production | SOT-223 (DCQ) 6 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PS79418 |
| TPS79418DCQR.A | Active | Production | SOT-223 (DCQ) 6 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PS79418 |
| TPS79418DGNR | Active | Production | HVSSOP (DGN) 8 | 2500 LARGE T&R | Yes | Call TI Nipdau | Level-1-260C-UNLIM | -40 to 85 | AXM |
| TPS79418DGNR.A | Active | Production | HVSSOP (DGN) 8 | 2500 LARGE T&R | Yes | Call TI | Level-1-260C-UNLIM | -40 to 85 | AXM |
| TPS79418DGNT | Obsolete | Production | HVSSOP (DGN) 8 | - | - | Call TI | Call TI | -40 to 85 | AXM |
| TPS79425DCQ | Obsolete | Production | SOT-223 (DCQ) 6 | - | - | Call TI | Call TI | -40 to 85 | PS79425 |
| TPS79425DCQR | Active | Production | SOT-223 (DCQ) 6 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PS79425 |
| TPS79425DCQR.A | Active | Production | SOT-223 (DCQ) 6 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PS79425 |
| TPS79425DGNR | Active | Production | HVSSOP (DGN) 8 | 2500 LARGE T&R | Yes | Call TI Nipdau | Level-1-260C-UNLIM | -40 to 85 | AYB |
| TPS79425DGNR.A | Active | Production | HVSSOP (DGN) 8 | 2500 LARGE T&R | Yes | Call TI | Level-1-260C-UNLIM | -40 to 85 | AYB |
| TPS79425DGNT | Obsolete | Production | HVSSOP (DGN) 8 | - | - | Call TI | Call TI | -40 to 85 | AYB |
| TPS79428DCQ | Obsolete | Production | SOT-223 (DCQ) 6 | - | - | Call TI | Call TI | -40 to 85 | PS79428 |
| TPS79428DCQR | Active | Production | SOT-223 (DCQ) 6 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PS79428 |
| TPS79428DCQR.A | Active | Production | SOT-223 (DCQ) 6 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PS79428 |
| TPS79428DGNT | Active | Production | HVSSOP (DGN) 8 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AYC |
| TPS79428DGNT.A | Active | Production | HVSSOP (DGN) 8 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AYC |
| TPS79430DCQ | Active | Production | SOT-223 (DCQ) 6 | 78 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PS79430 |
| TPS79430DCQ.A | Active | Production | SOT-223 (DCQ) 6 | 78 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PS79430 |
| TPS79430DCQR | Active | Production | SOT-223 (DCQ) 6 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PS79430 |
| TPS79430DCQR.A | Active | Production | SOT-223 (DCQ) 6 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PS79430 |
| TPS79430DGNR | Active | Production | HVSSOP (DGN) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AYD |



-40 to 85

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AYE



TPS79433DGNT

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| Orderable part number | Status | Material type | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material | MSL rating/ Peak reflow | Op temp (°C) | Part marking (6) |
|-----------------------|----------|---------------|-------------------|-----------------------|-----------------|-------------------------------|----------------------------|--------------|------------------|
| | | | | | | (4) | (5) | | |
| TPS79430DGNR.A | Active | Production | HVSSOP (DGN) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AYD |
| TPS79430DGNT | Obsolete | Production | HVSSOP (DGN) 8 | - | - | Call TI | Call TI | -40 to 85 | AYD |
| TPS79433DCQ | Obsolete | Production | SOT-223 (DCQ) 6 | - | - | Call TI | Call TI | -40 to 85 | PS79433 |
| TPS79433DCQR | Active | Production | SOT-223 (DCQ) 6 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PS79433 |
| TPS79433DCQR.A | Active | Production | SOT-223 (DCQ) 6 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PS79433 |
| TPS79433DGNR | Active | Production | HVSSOP (DGN) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AYE |
| TPS79433DGNR.A | Active | Production | HVSSOP (DGN) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AYE |

⁽¹⁾ Status: For more details on status, see our product life cycle.

Obsolete

Call TI

Call TI

Production

HVSSOP (DGN) | 8

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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TAPE AND REEL INFORMATION





| A0 | Dimension designed to accommodate the component width |
|----|---|
| В0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|-----------------|--------------------|---|------|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| TPS79401DCQR | SOT-223 | DCQ | 6 | 2500 | 330.0 | 12.4 | 7.1 | 7.45 | 1.88 | 8.0 | 12.0 | Q3 |
| TPS79418DCQR | SOT-223 | DCQ | 6 | 2500 | 330.0 | 12.4 | 7.1 | 7.45 | 1.88 | 8.0 | 12.0 | Q3 |
| TPS79425DCQR | SOT-223 | DCQ | 6 | 2500 | 330.0 | 12.4 | 7.1 | 7.45 | 1.88 | 8.0 | 12.0 | Q3 |
| TPS79428DCQR | SOT-223 | DCQ | 6 | 2500 | 330.0 | 12.4 | 7.1 | 7.45 | 1.88 | 8.0 | 12.0 | Q3 |
| TPS79428DGNT | HVSSOP | DGN | 8 | 250 | 180.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS79430DCQR | SOT-223 | DCQ | 6 | 2500 | 330.0 | 12.4 | 7.1 | 7.45 | 1.88 | 8.0 | 12.0 | Q3 |
| TPS79430DGNR | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS79433DCQR | SOT-223 | DCQ | 6 | 2500 | 330.0 | 12.4 | 7.1 | 7.45 | 1.88 | 8.0 | 12.0 | Q3 |
| TPS79433DGNR | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |



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*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS79401DCQR | SOT-223 | DCQ | 6 | 2500 | 346.0 | 346.0 | 29.0 |
| TPS79418DCQR | SOT-223 | DCQ | 6 | 2500 | 346.0 | 346.0 | 41.0 |
| TPS79425DCQR | SOT-223 | DCQ | 6 | 2500 | 346.0 | 346.0 | 41.0 |
| TPS79428DCQR | SOT-223 | DCQ | 6 | 2500 | 358.0 | 335.0 | 35.0 |
| TPS79428DGNT | HVSSOP | DGN | 8 | 250 | 213.0 | 191.0 | 35.0 |
| TPS79430DCQR | SOT-223 | DCQ | 6 | 2500 | 346.0 | 346.0 | 29.0 |
| TPS79430DGNR | HVSSOP | DGN | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TPS79433DCQR | SOT-223 | DCQ | 6 | 2500 | 346.0 | 346.0 | 29.0 |
| TPS79433DGNR | HVSSOP | DGN | 8 | 2500 | 353.0 | 353.0 | 32.0 |

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TPS79430DCQ | DCQ | SOT-223 | 6 | 78 | 532.13 | 8.63 | 3.6 | 3.68 |
| TPS79430DCQ.A | DCQ | SOT-223 | 6 | 78 | 532.13 | 8.63 | 3.6 | 3.68 |



PLASTIC SMALL OUTLINE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.



PLASTIC SMALL OUTLINE



- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC SMALL OUTLINE



- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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$\textbf{PowerPAD}^{^{\text{\tiny{TM}}}}\,\textbf{VSSOP - 1.1 mm max height}$

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-187.



SMALL OUTLINE PACKAGE



- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
- 9. Size of metal pad may vary due to creepage requirement.



SMALL OUTLINE PACKAGE



- 10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 11. Board assembly site may have different recommendations for stencil design.



PowerPAD[™] HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
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SMALL OUTLINE PACKAGE



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SMALL OUTLINE PACKAGE



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- 11. Board assembly site may have different recommendations for stencil design.



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