# TPS736 Capacitor-Free, NMOS, 400mA, Low-Dropout Regulator With Reverse Current Protection

## 1 Features

- Stable with no output capacitor or any value or type of capacitor
- Input voltage range of 1.7V to 5.5V
- Ultra-low dropout voltage: 75mV typ
- Excellent load transient response—with or without optional output capacitor
- NMOS topology delivers low reverse leakage current
- Low noise: 30$\mu V_{RMS}$ typ (10Hz to 100kHz)
- 0.5% initial accuracy
- 1% overall accuracy over line, load, and temperature
- Less than 1µA max $I_Q$ in shutdown mode
- Thermal shutdown and specified min/max current limit protection
- Available in multiple output voltage versions:
  - Fixed outputs of 1.20V to 5.0V
  - Adjustable output from 1.20V to 5.5V
  - Custom outputs available

## 2 Applications

- Portable-, battery-powered equipment
- Post-regulation for switching supplies
- Noise-sensitive circuitry such as VCOs
- Point of load regulation for DSPs, FPGAs, ASICs, and microprocessors

## 3 Description

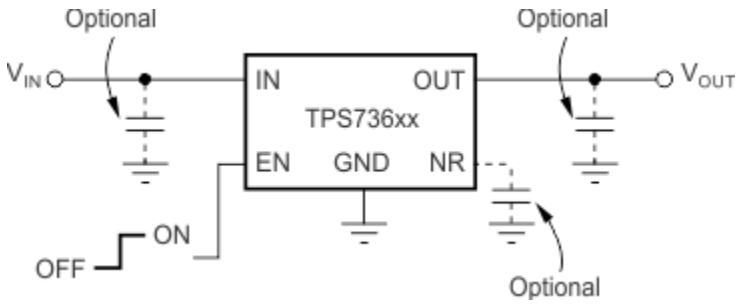
The TPS736 low-dropout (LDO) linear voltage regulator uses a new topology: an NMOS pass transistor in a voltage-follower configuration. This topology is stable using output capacitors with low ESR, and even allows operation without a capacitor. The device also provides high reverse blockage (low reverse current) and ground pin current that is nearly constant over all output current values.

The TPS736 uses an advanced BiCMOS process to yield high precision while delivering very low dropout voltages and low ground pin current. Current consumption, when not enabled, is under 1µA and designed for portable applications. The extremely low output noise (30$\mu V_{RMS}$ with 0.1µF $C_{NR}$) is designed for powering VCOs. This device is protected by thermal shutdown and foldback current limit.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| TPS736 | DBV (SOT-23, 5) | 2.9mm × 2.8mm |
| | DCQ (SOT-223, 6) | 6.5mm × 7.06mm |
| | DRB (VSON, 8) | 3mm × 3mm |

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Typical Application Circuit for Fixed-Voltage Versions**

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# Table of Contents




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# 4 Pin Configuration and Functions

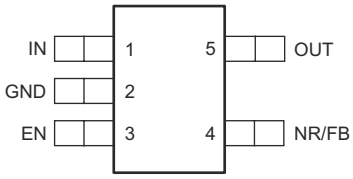


**Figure 4-1. DBV Package, 5-Pin SOT-23 (Top View)**

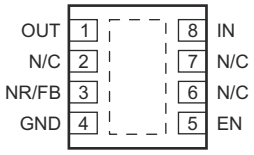


**Figure 4-2. DRB Package, 8-Pin VSON (Top View)**

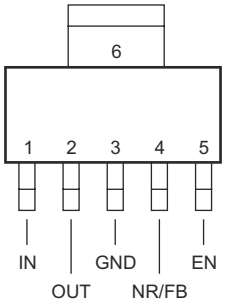


**Figure 4-3. DCQ Package, 6-Pin SOT-223 (Top View)**

**Table 4-1. Pin Functions**

| PIN | | | | TYPE[1] | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| | SOT-23 | SOT-223 | VSON | | |
| EN | 3 | 5 | 5 | I | Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. See the *Enable Pin and Shutdown* section for more details. EN can be connected to IN if not used. |
| FB | 4 | 4 | 3 | I | Adjustable-voltage version only. This pin is the input to the control loop error amplifier, and sets the output voltage of the device. |
| GND | 2 | 3, 6 | 4, Pad | — | Ground. |
| IN | 1 | 1 | 8 | I | Input supply. |
| NR | 4 | 4 | 3 | — | Fixed-voltage versions only. Connecting an external capacitor to this noise reduction pin bypasses noise generated by the internal band gap, reducing output noise to very low levels. |
| OUT | 5 | 2 | 1 | O | Output of the regulator. There are no output capacitor requirements for stability. |

(1) I = Input; O = Output

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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)[1]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | Input, $V_{IN}$ | –0.3 | 6 | V |
| | Enable, $V_{EN}$ | –0.3 | 6 | |
| | Output, $V_{OUT}$ | –0.3 | 5.5 | |
| | $V_{NR}$, $V_{FB}$ | –0.3 | 6 | |
| Current | Maximum output, $I_{OUT}$ | Internally limited | | |
| Output short-circuit duration | | Indefinite | | |
| Continuous total power dissipation | $P_{DISS}$ | See *Thermal Information* | | |
| Temperature | Operating junction, $T_J$ | –55 | 150 | °C |
| | Storage, $T_{stg}$ | –65 | 150 | |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1] | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins[2] | ±500 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input supply voltage | 1.7 | | 5.5 | V |
| $I_{OUT}$ | Output current | 0 | | 400 | mA |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |

## 5.4 Thermal Information

| THERMAL METRIC[1] | | TPS736 New silicon | | | UNIT |
|---|---|---|---|---|---|
| | | DRB (VSON) | DCQ (SOT-223) | DBV (SOT-23) | |
| | | 8 PINS | 6 PINS | 5 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 49.4 | 76 | 185.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 76.6 | 46.6 | 82.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 22.0 | 18.1 | 53.1 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 3.8 | 8.6 | 21.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 22.0 | 17.6 | 52.7 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 3.8 | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.


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## 5.5 Thermal Information

| THERMAL METRIC[1] [2] | | TPS736 Legacy silicon[3] | | | UNIT |
|---|---|---|---|---|---|
| | | DRB (VSON) | DCQ (SOT-223) | DBV (SOT-23) | |
| | | 8 PINS | 6 PINS | 5 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance[4] | 52.8 | 118.7 | 221.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance[5] | 60.4 | 64.9 | 74.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance[6] | 28.4 | 65.0 | 51.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter[7] | 2.1 | 14.0 | 2.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter[8] | 28.6 | 63.8 | 51.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance[9] | 12.0 | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.
(3) Thermal data for the DRB, DCQ, and DBV packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
(a) i. DRB: The exposed pad is connected to the PCB ground layer through a 2×2 thermal via array.
ii. DCQ: The exposed pad is connected to the PCB ground layer through a 3×2 thermal via array.
iii. DBV: There is no exposed pad with the DBV package.
(b) i. DRB: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
ii. DCQ: Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage.
iii. DBV: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
(c) These data are generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3in × 3in copper area. To understand the effects of the copper area on thermal performance, see the Power Dissipation section of this data sheet.
(4) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(5) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(6) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(7) The junction-to-top characterization parameter, $\psi_{JT}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain $R_{\theta JA}$ using a procedure described in JESD51-2a (sections 6 and 7).
(8) The junction-to-board characterization parameter, $\psi_{JB}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain $R_{\theta JA}$ using a procedure described in JESD51-2a (sections 6 and 7).
(9) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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## 5.6 Electrical Characteristics

Over operating temperature range ($T_J$ = –40°C to 125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5V(1) , $I_{OUT}$ = 10mA, $V_{EN}$ = 1.7V, and $C_{OUT}$ = 0.1µF (unless otherwise noted). Typical values are at $T_J$ = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage range(1) (2) | | | 1.7 | | 5.5 | V |
| $V_{FB}$ | Internal reference (TPS73601) | $T_J$ = 25°C | | 1.198 | 1.204 | 1.210 | V |
| $V_{OUT}$ | Output voltage range (TPS73601)(3) | | | $V_{FB}$ | | 5.5 - $V_{DO}$ | V |
| | Accuracy(1) (4) | Nominal | $T_J$ = 25°C | –0.5 | | 0.5 | % |
| | | over $V_{IN}$, $I_{OUT}$, and T | $V_{OUT}$ + 0.5V ≤ $V_{IN}$ ≤ 5.5V; 10mA ≤ $I_{OUT}$ ≤ 400mA | –1 | ±0.5 | 1 | |
| $\Delta V_{OUT(\Delta VIN)}$ | Line regulation (1) | $V_{OUT(nom)}$ + 0.5V ≤ $V_{IN}$ ≤ 5.5V | | | 0.01 | | %/V |
| $\Delta V_{OUT(\Delta IOUT)}$ | Load regulation | 1mA ≤ $I_{OUT}$ ≤ 400mA | | | 0.002 | | %/mA |
| | | 10mA ≤ $I_{OUT}$ ≤ 400mA | | | 0.0005 | | |
| $V_{DO}$ | Dropout voltage(5) ($V_{IN}$ = $V_{OUT(nom)}$ - 0.1V) | $I_{OUT}$ = 400mA | | | 75 | 200 | mV |
| $Z_{O(DO)}$ | Output impedance in dropout | 1.7V ≤ $V_{IN}$ ≤ $V_{OUT}$ + $V_{DO}$ | | | 0.25 | | Ω |
| $I_{CL}$ | Output current limit | $V_{OUT}$ = 0.9 × $V_{OUT(nom)}$ | legacy silicon | 400 | 650 | 800 | mA |
| | | 3.6V ≤ $V_{IN}$ ≤ 4.2V, 0°C ≤ $T_J$ ≤ 70°C | | 500 | | 800 | |
| | | $V_{OUT}$ = 0.9 × $V_{OUT(nom)}$ | new silicon | 500 | | 800 | |
| $I_{SC}$ | Short-circuit current | $V_{OUT}$ = 0V | | | 450 | | mA |
| $I_{REV}$ | Reverse leakage current(6) (-$I_{IN}$) | $V_{EN}$ ≤ 0.5V, 0V ≤ $V_{IN}$ ≤ $V_{OUT}$ | | | 0.1 | 10 | µA |
| $I_{GND}$ | Ground pin current | $I_{OUT}$ = 10mA ($I_Q$), legacy silicon | | | 400 | 550 | µA |
| | | $I_{OUT}$ = 10mA ($I_Q$), new silicon | | | 400 | 630 | |
| $I_{GND}$ | Ground pin current | $I_{OUT}$ = 400mA | | | 800 | 1000 | µA |
| $I_{SHDN}$ | Shutdown current ($I_{GND}$) | $V_{EN}$ ≤ 0.5V, $V_{OUT}$ ≤ $V_{IN}$ ≤ 5.5V, –40°C ≤ $T_J$ ≤ 100°C, legacy silicon | | | 0.02 | 1 | µA |
| | | $V_{EN}$ ≤ 0.5V, $V_{OUT}$ ≤ $V_{IN}$ ≤ 5.5V, new silicon | | | 0.02 | 1 | |
| $I_{FB}$ | Feedback pin current (TPS73601) | | | | 0.1 | 0.3 | µA |
| PSRR | Power-supply rejection ratio (ripple rejection) | f = 100Hz, $I_{OUT}$ = 400mA | | | 58 | | dB |
| | | f = 10kHz, $I_{OUT}$ = 400mA | | | 37 | | |
| $V_N$ | Output noise voltage, BW = 10Hz to 100kHz | $C_{OUT}$ = 10µF, no $C_{NR}$ | | | 27 × $V_{OUT}$ | | $\mu V_{RMS}$ |
| | | $C_{OUT}$ = 10µF, $C_{NR}$ =0.01µF | | | 8.5 × $V_{OUT}$ | | |
| $t_{STR}$ | Startup time | $V_{OUT}$ = 3V, $R_L$ = 30Ω, $C_{OUT}$ = 1µF, $C_{NR}$ = 0.01µF | | | 600 | | µs |
| $V_{EN(high)}$ | EN pin high (enabled) | | | 1.7 | | $V_{IN}$ | V |
| $V_{EN(low)}$ | EN pin low (shutdown) | | | 0 | | 0.5 | V |
| $I_{EN(high)}$ | Enable pin current (enabled) | $V_{EN}$ = 5.5V | | | 0.02 | 0.1 | µA |
| $T_{SD}$ | Thermal shutdown temperature | Shutdown, temperature increasing | | | 160 | | °C |
| | | Reset, temperature decreasing | | | 140 | | |
| $T_J$ | Operating junction temperature | | | –40 | | 125 | °C |

(1) Minimum $V_{IN}$ = $V_{OUT}$ + $V_{DO}$ or 1.7V, whichever is greater.
(2) For $V_{OUT(nom)}$ < 1.6V, when $V_{IN}$ ≤ 1.6V, the output locks to $V_{IN}$ and can result in a damaging over-voltage condition on the output. To avoid this situation, disable the device before powering down $V_{IN}$. (Legacy silicon only)
(3) TPS73601 is tested at $V_{OUT}$ = 2.5V.
(4) Tolerance of external resistors not included in this specification.
(5) $V_{DO}$ is not measured for output versions with $V_{OUT(nom)}$ < 1.8V, because minimum $V_{IN}$ = 1.7V.
(6) Fixed-voltage versions only; refer to *Application Information* section for more information.


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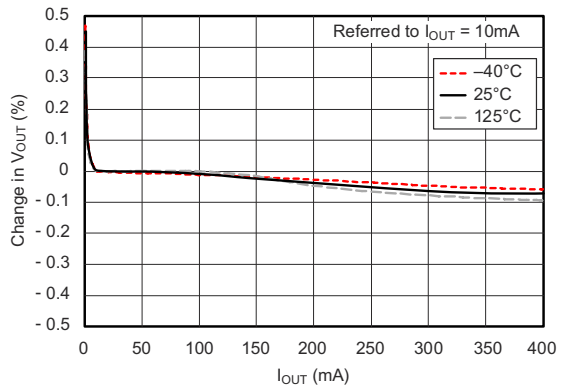
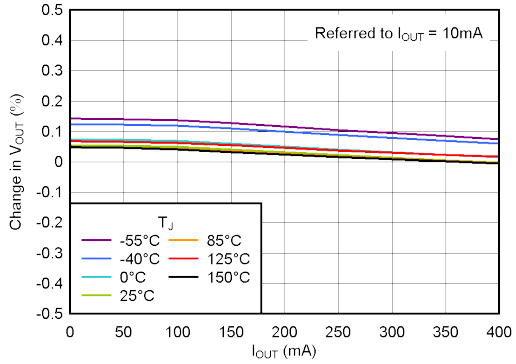
## 5.7 Typical Characteristics

For all voltage versions, at $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(nom)}$ + 0.5V, $I_{OUT}$ = 10mA, $V_{EN}$ = 1.7V, and $C_{OUT}$ = 0.1µF, unless otherwise noted.



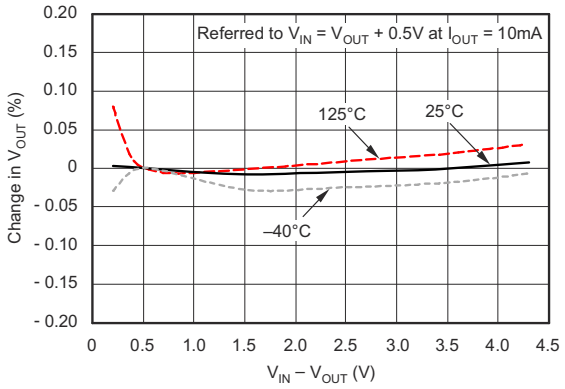

Legacy silicon

**Figure 5-1. Load Regulation**



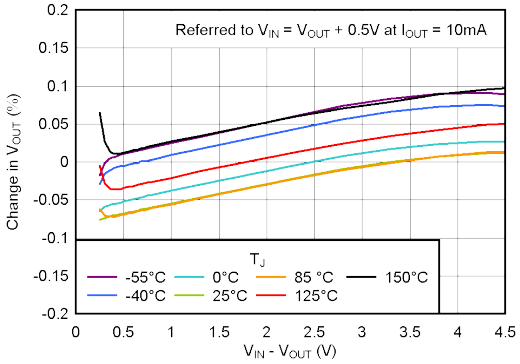

New silicon

**Figure 5-2. Load Regulation**



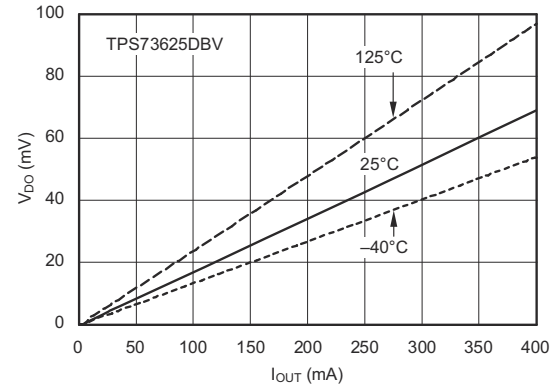

Legacy silicon

**Figure 5-3. Line Regulation**



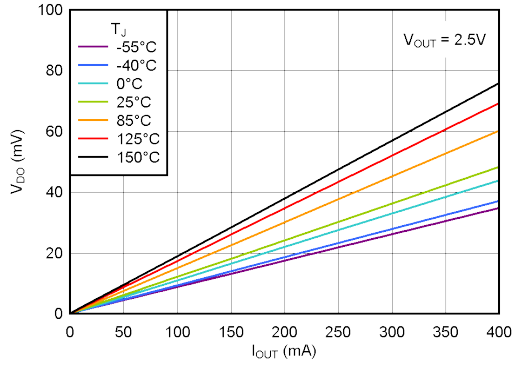

New silicon

**Figure 5-4. Line Regulation**




Legacy silicon

**Figure 5-5. Dropout Voltage vs Output Current**

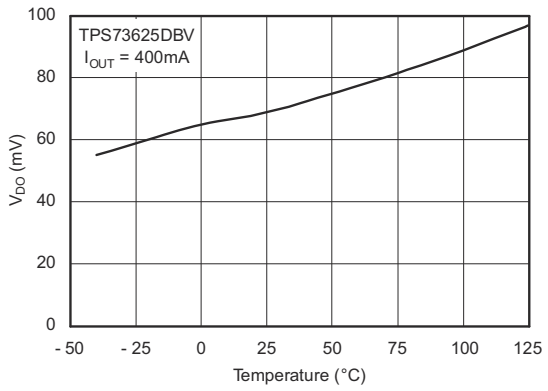



New silicon

**Figure 5-6. Dropout Voltage vs Output Current**

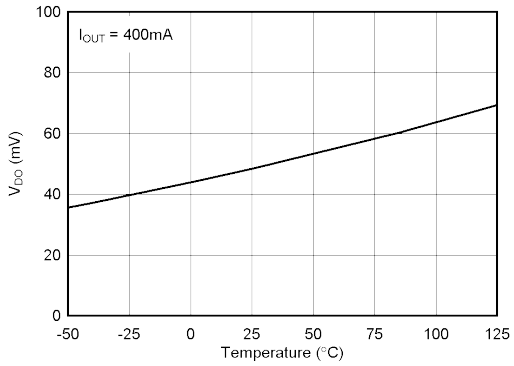
## 5.7 Typical Characteristics (continued)

For all voltage versions, at $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(nom)}$ + 0.5V, $I_{OUT}$ = 10mA, $V_{EN}$ = 1.7V, and $C_{OUT}$ = 0.1µF, unless otherwise noted.



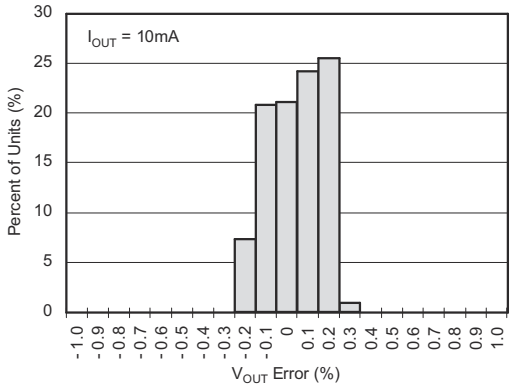

Legacy silicon

**Figure 5-7. Dropout Voltage vs Temperature**



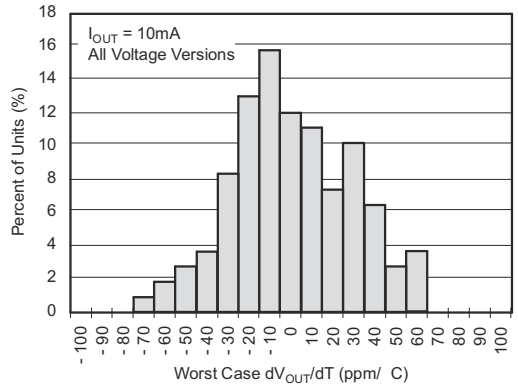

New silicon

**Figure 5-8. Dropout Voltage vs Temperature**



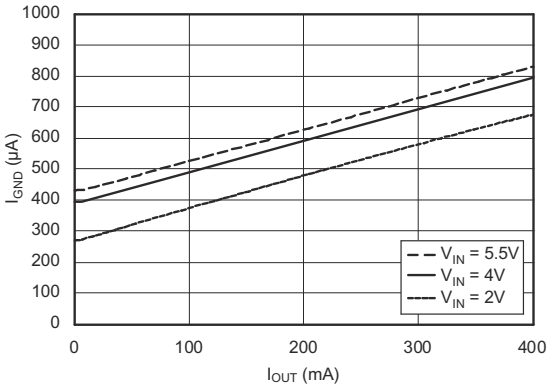

Legacy silicon

**Figure 5-9. Output Voltage Accuracy Histogram**



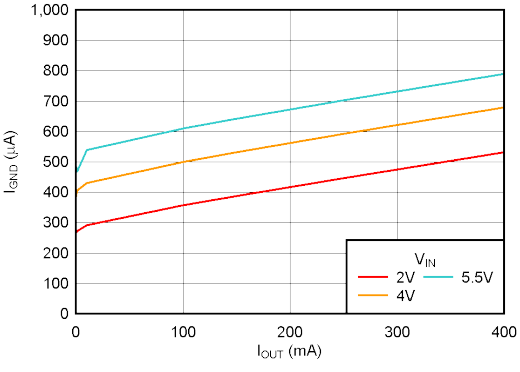

Legacy silicon

**Figure 5-10. Output Voltage Drift Histogram**




Legacy silicon

**Figure 5-11. Ground Pin Current vs Output Current**




New silicon

**Figure 5-12. Ground Pin Current vs Output Current**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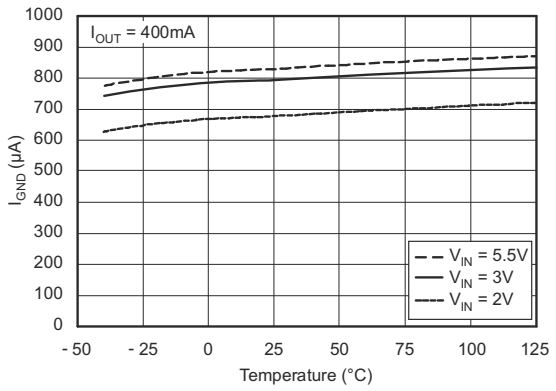
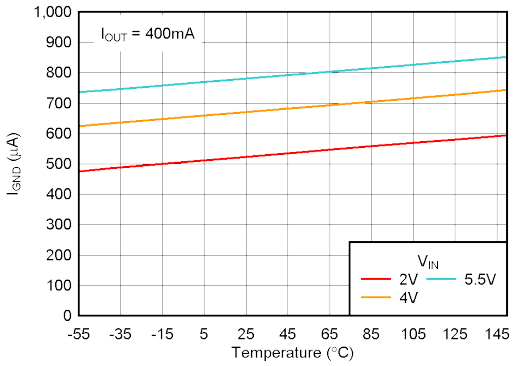
## 5.7 Typical Characteristics (continued)

For all voltage versions, at $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(nom)}$ + 0.5V, $I_{OUT}$ = 10mA, $V_{EN}$ = 1.7V, and $C_{OUT}$ = 0.1µF, unless otherwise noted.



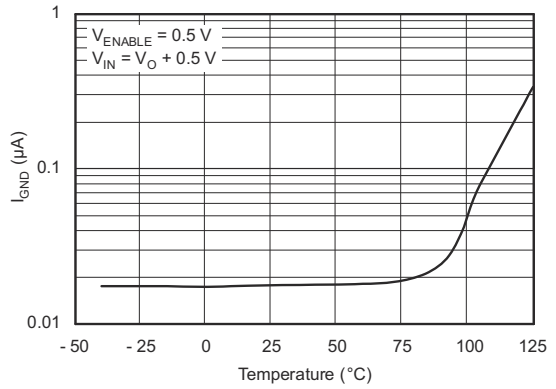

Legacy silicon

**Figure 5-13. Ground Pin Current vs Temperature**



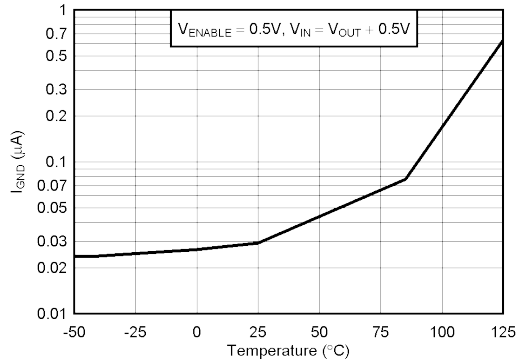

New silicon

**Figure 5-14. Ground Pin Current vs Temperature**



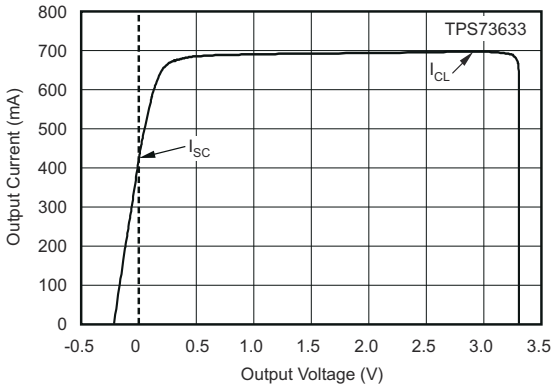

Legacy silicon

**Figure 5-15. Ground Pin Current In Shutdown vs Temperature**



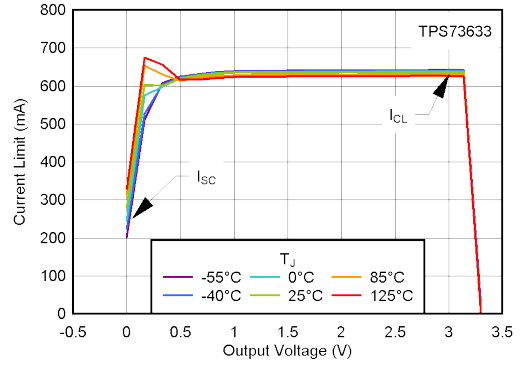

New silicon

**Figure 5-16. Ground Pin Current in Shutdown vs Temperature**




Legacy silicon

**Figure 5-17. Current Limit vs $V_{OUT}$ (Foldback)**




New silicon

**Figure 5-18. Current Limit vs $V_{OUT}$ (Foldback)**

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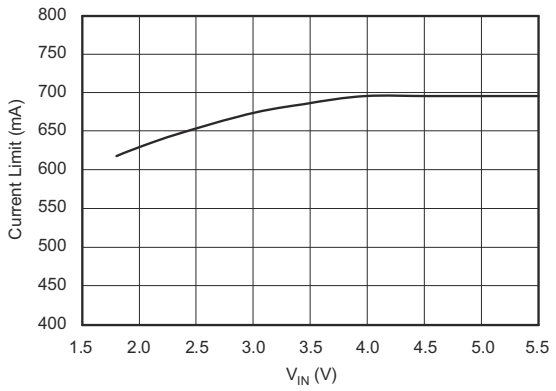
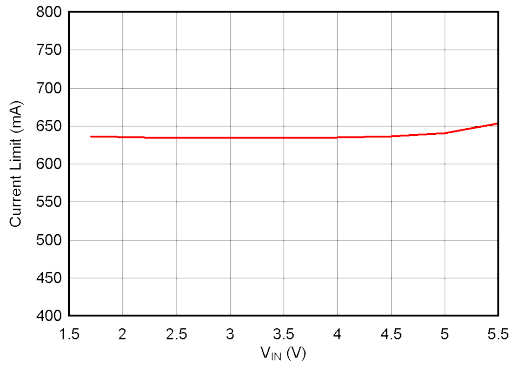
## 5.7 Typical Characteristics (continued)

For all voltage versions, at $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(nom)}$ + 0.5V, $I_{OUT}$ = 10mA, $V_{EN}$ = 1.7V, and $C_{OUT}$ = 0.1µF, unless otherwise noted.



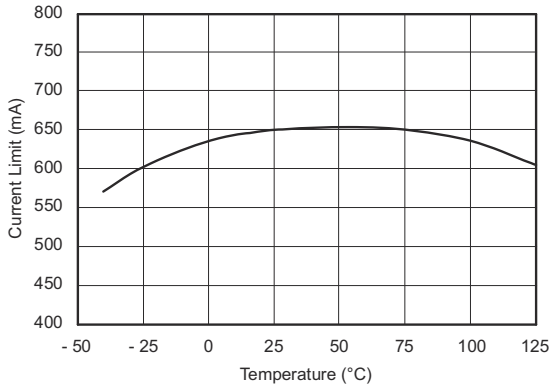

Legacy silicon

**Figure 5-19. Current Limit vs $V_{IN}$**



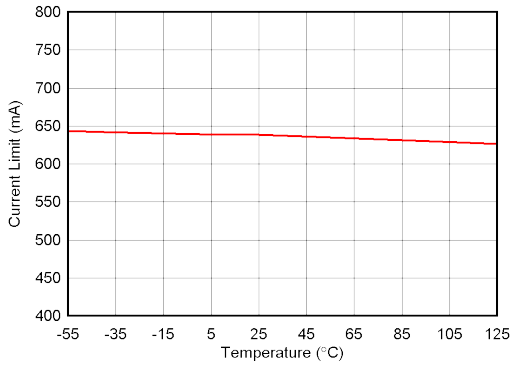

New silicon

**Figure 5-20. Current Limit vs $V_{IN}$**



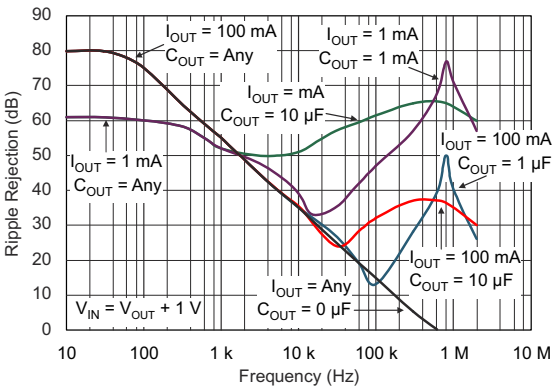

Legacy silicon

**Figure 5-21. Current Limit vs Temperature**



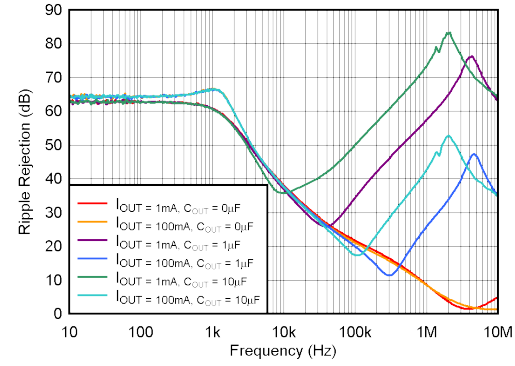

New silicon

**Figure 5-22. Current Limit vs Temperature**




Legacy silicon

**Figure 5-23. PSRR (Ripple Rejection) vs Frequency**




New silicon

**Figure 5-24. PSRR (Ripple Rejection) vs Frequency**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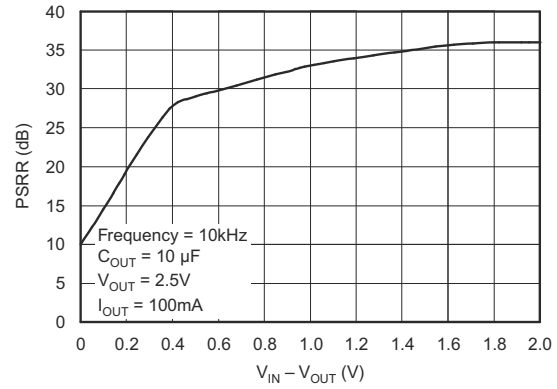
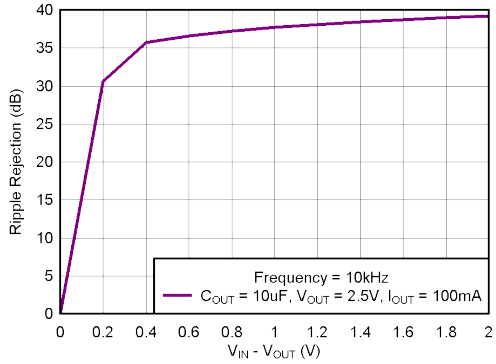
## 5.7 Typical Characteristics (continued)

For all voltage versions, at $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(nom)}$ + 0.5V, $I_{OUT}$ = 10mA, $V_{EN}$ = 1.7V, and $C_{OUT}$ = 0.1µF, unless otherwise noted.



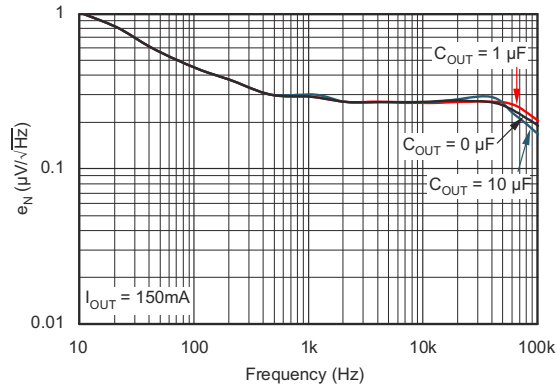

Legacy silicon

**Figure 5-25. PSRR (Ripple Rejection) vs $V_{IN}$ – $V_{OUT}$**



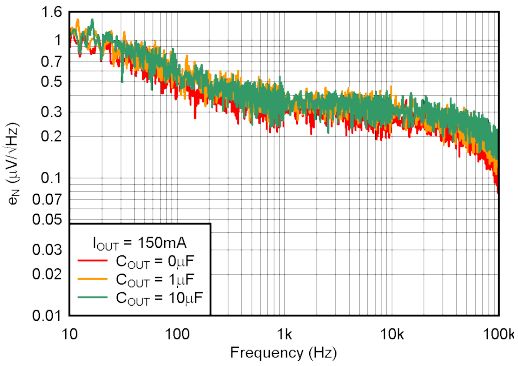

New silicon

**Figure 5-26. PSRR (Ripple Rejection) vs $V_{IN}$ – $V_{OUT}$**



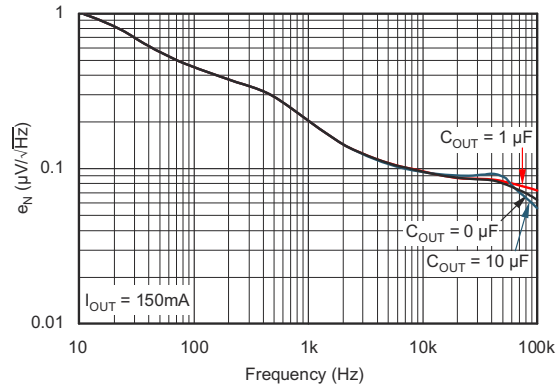

Legacy silicon

**Figure 5-27. Noise Spectral Density $C_{NR}$ = 0µF**



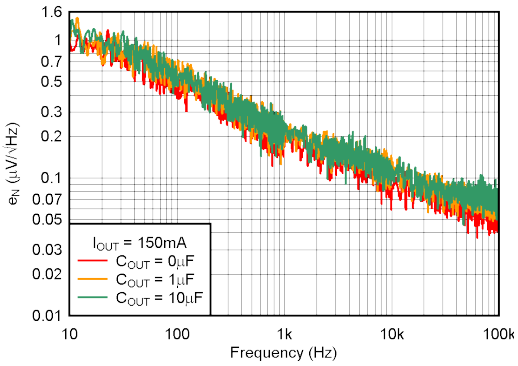

New silicon

**Figure 5-28. Noise Spectral Density $C_{NR}$ = 0µF**




Legacy silicon

**Figure 5-29. Noise Spectral Density $C_{NR}$ = 0.01µF**




New silicon

**Figure 5-30. Noise Spectral Density $C_{NR}$ = 0.01µF**

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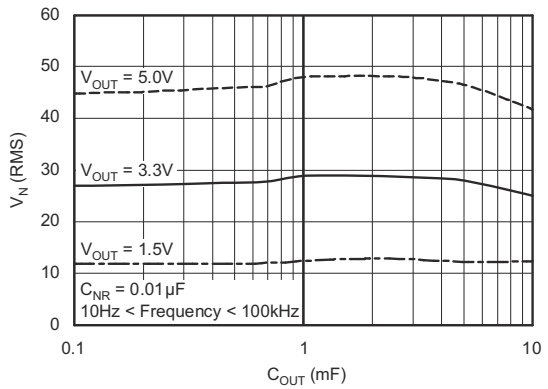
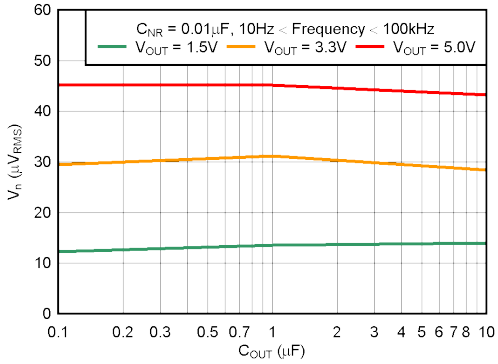
## 5.7 Typical Characteristics (continued)

For all voltage versions, at $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(nom)}$ + 0.5V, $I_{OUT}$ = 10mA, $V_{EN}$ = 1.7V, and $C_{OUT}$ = 0.1µF, unless otherwise noted.



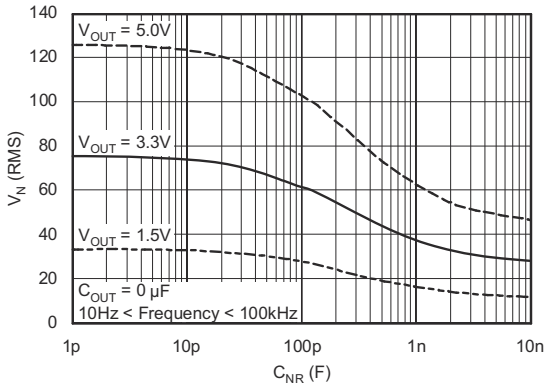

Legacy silicon

**Figure 5-31. RMS Noise Voltage vs $C_{OUT}$**



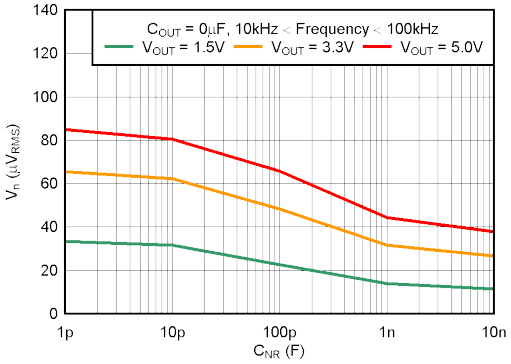

New silicon

**Figure 5-32. RMS Noise Voltage vs $C_{OUT}$**



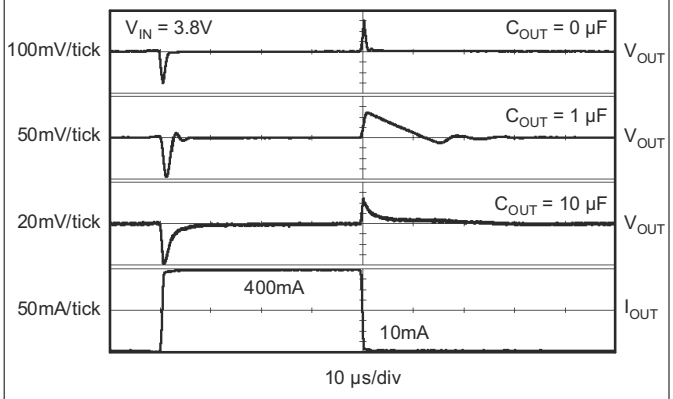

Legacy silicon

**Figure 5-33. RMS Noise Voltage vs $C_{NR}$**



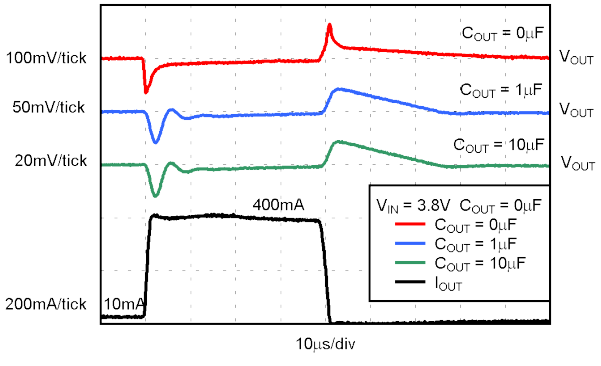

New silicon

**Figure 5-34. RMS Noise Voltage vs $C_{NR}$**




Legacy silicon

**Figure 5-35. TPS73633 Load Transient Response**




New silicon

**Figure 5-36. TPS73633 Load Transient Response**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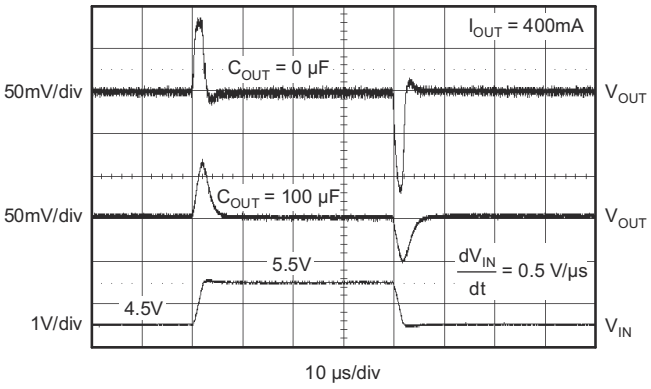
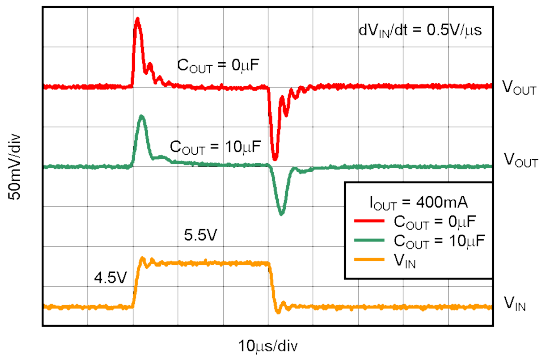
## 5.7 Typical Characteristics (continued)

For all voltage versions, at $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(nom)}$ + 0.5V, $I_{OUT}$ = 10mA, $V_{EN}$ = 1.7V, and $C_{OUT}$ = 0.1µF, unless otherwise noted.



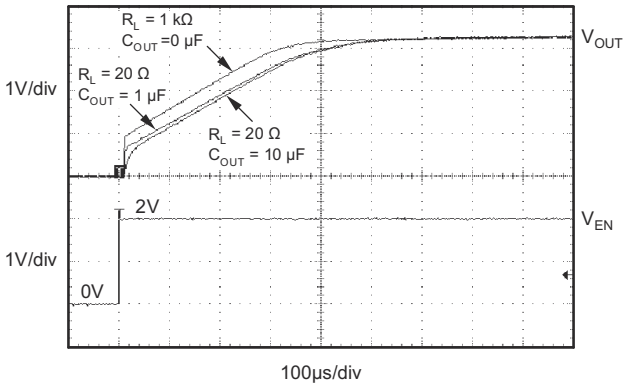

Legacy silicon

**Figure 5-37. TPS73633 Line Transient Response**



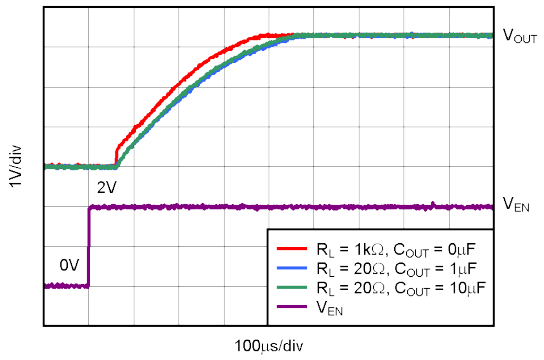

New silicon

**Figure 5-38. TPS73633 Line Transient Response**



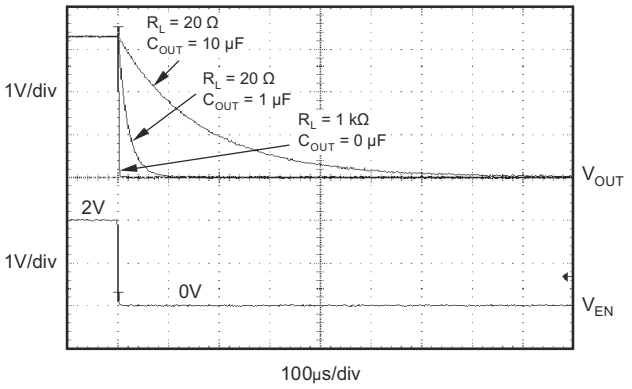

Legacy silicon

**Figure 5-39. TPS73633 Turn-On Response**



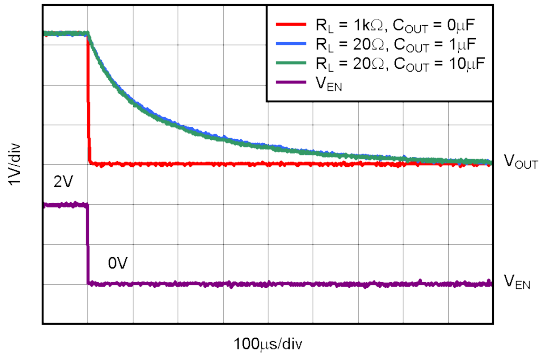

New silicon

**Figure 5-40. TPS73633 Turn-On Response**




Legacy silicon

**Figure 5-41. TPS73633 Turn-Off Response**




New silicon

**Figure 5-42. TPS73633 Turn-Off Response**

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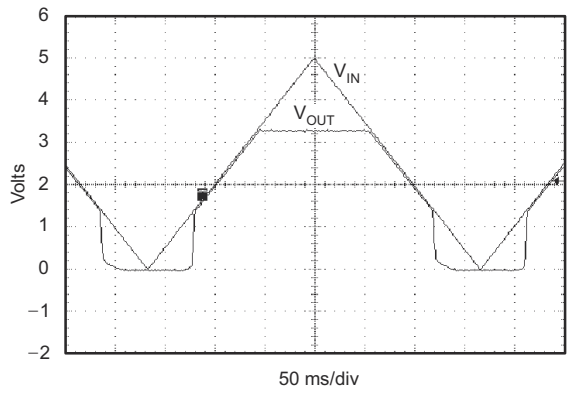
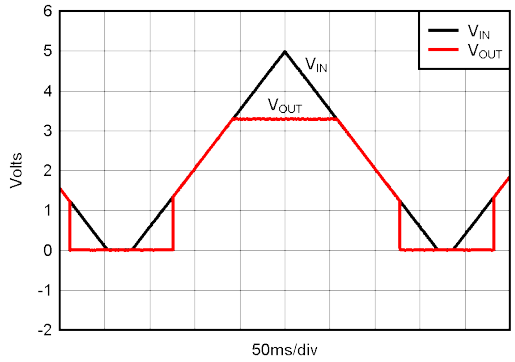
## 5.7 Typical Characteristics (continued)

For all voltage versions, at $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(nom)}$ + 0.5V, $I_{OUT}$ = 10mA, $V_{EN}$ = 1.7V, and $C_{OUT}$ = 0.1µF, unless otherwise noted.



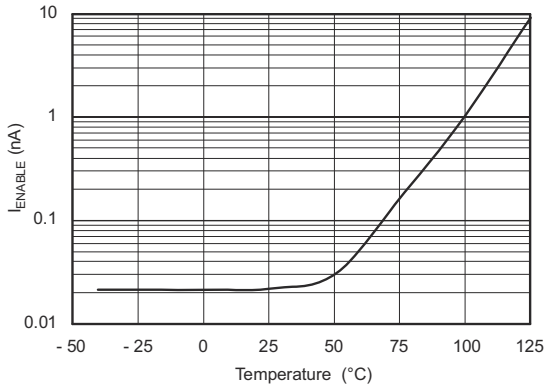

Legacy silicon

**Figure 5-43. TPS73633 Power-Up, Power-Down**



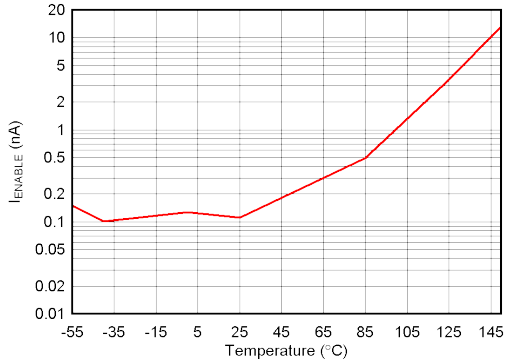

New silicon

**Figure 5-44. TPS73633 Power-Up, Power-Down**



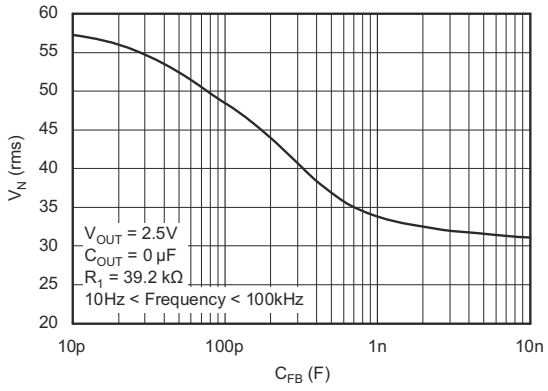

Legacy silicon

**Figure 5-45. $I_{ENABLE}$ vs Temperature**



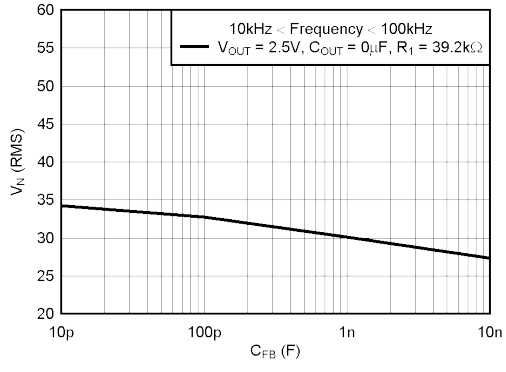

New silicon

**Figure 5-46. $I_{ENABLE}$ vs Temperature**




Legacy silicon

**Figure 5-47. TPS73601 RMS Noise Voltage vs $C_{FB}$**




New silicon

**Figure 5-48. TPS73601 RMS Noise Voltage vs $C_{FB}$**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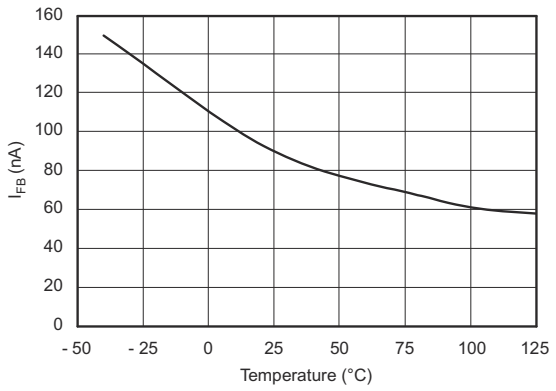
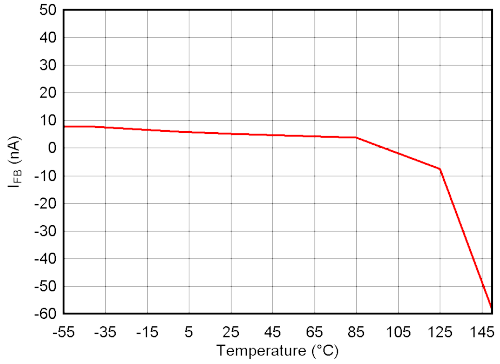
## 5.7 Typical Characteristics (continued)

For all voltage versions, at $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(nom)}$ + 0.5V, $I_{OUT}$ = 10mA, $V_{EN}$ = 1.7V, and $C_{OUT}$ = 0.1µF, unless otherwise noted.



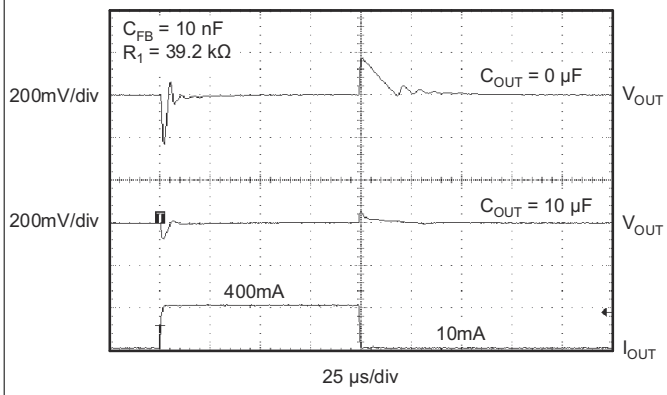

Legacy silicon

**Figure 5-49. TPS73601 $I_{FB}$ vs Temperature**



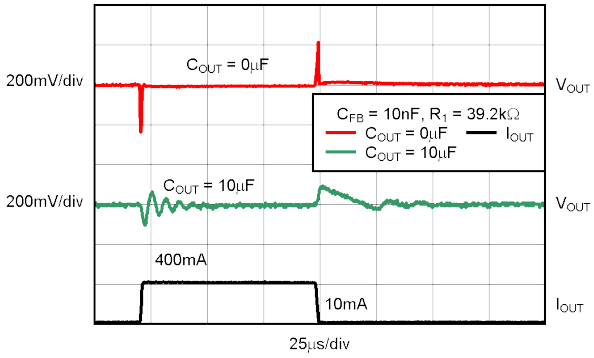

New silicon

**Figure 5-50. TPS73601 $I_{FB}$ vs Temperature**



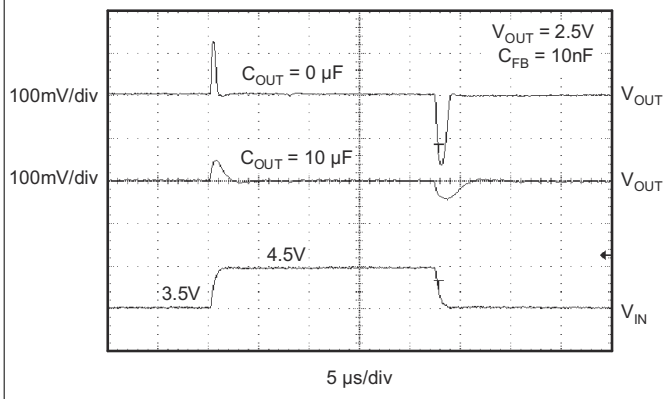

Legacy silicon

**Figure 5-51. TPS73601 Load Transient, Adjustable Version**



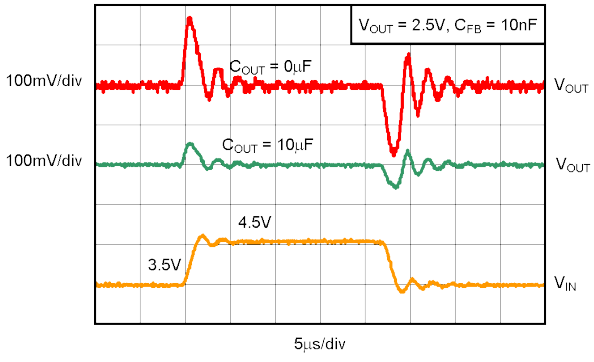

New silicon

**Figure 5-52. TPS73601 Load Transient, Adjustable Version**




Legacy silicon

**Figure 5-53. TPS73601 Line Transient, Adjustable Version**




New silicon

**Figure 5-54. TPS73601 Line Transient, Adjustable Version**

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# 6 Detailed Description

## 6.1 Overview

The TPS736 low-dropout linear regulator operates down to an input voltage of 1.7V and supports output voltages down to 1.2V while sourcing up to 400mA of load current. This linear regulator uses an NMOS pass transistor with an integrated 4MHz charge pump to provide a dropout voltage of less than 200mV at full load current. This unique architecture also permits stable regulation over a wide range of output capacitors. In fact, the TPS736 device does not require any output capacitor for stability. The increased insensitivity to the output capacitor value and type makes this linear regulator a good choice when powering a load where the effective capacitance is unknown.

The TPS736 also features a noise reduction (NR) pin that allows for additional reduction of the output noise. With a noise reduction capacitor of 0.01µF connected from the NR pin to GND, the TPS73615 output noise can be as low as 12.75µ$V_{RMS}$. The low noise output featured by the TPS736 makes the device well-suited for powering VCOs or any other noise sensitive load.

## 6.2 Functional Block Diagrams

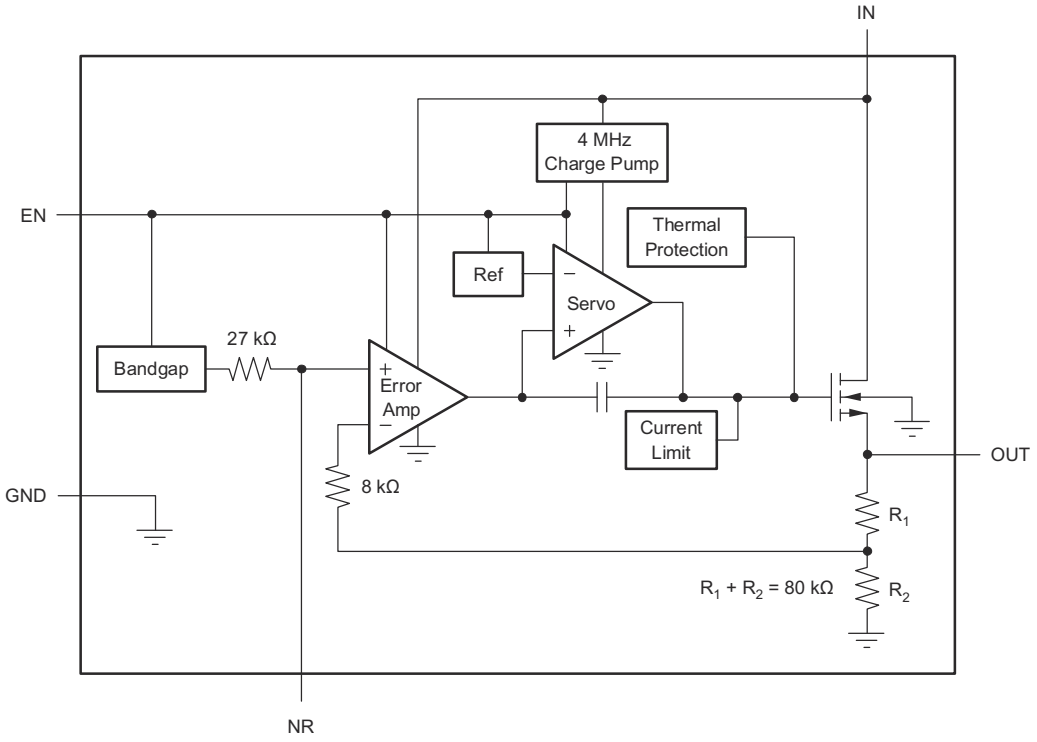


**Figure 6-1. Fixed-Voltage Version**


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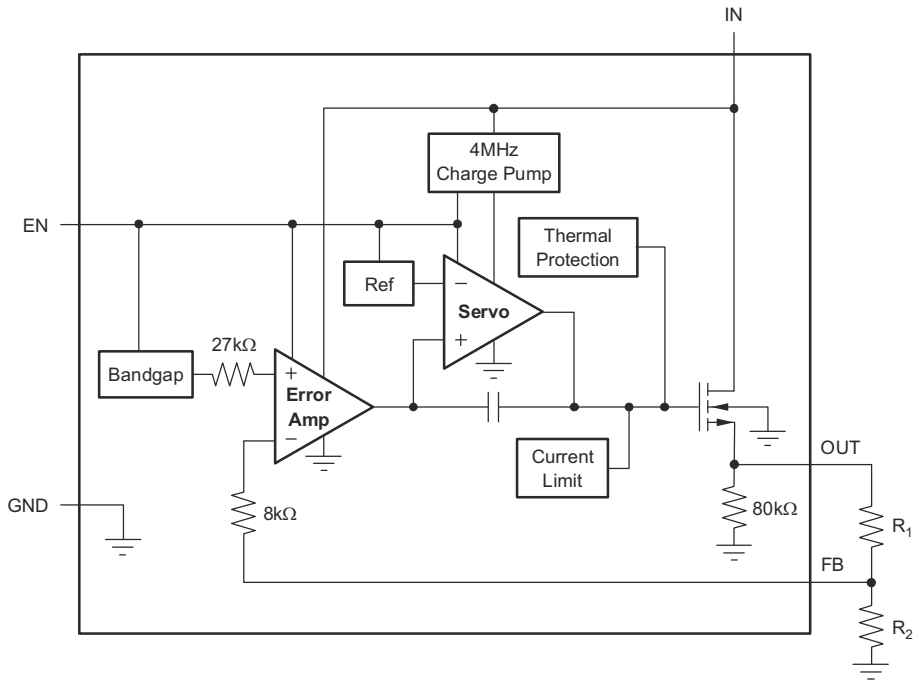


**Standard 1% Resistor Values for Common Output Voltages**

| $V_O$ | $R_1$ | $R_2$ |
|---|---|---|
| 1.2V | Short | Open |
| 1.5V | 23.2kΩ | 95.3kΩ |
| 1.8V | 28.0kΩ | 56.2kΩ |
| 2.5V | 39.2kΩ | 36.5kΩ |
| 2.8V | 44.2kΩ | 33.2kΩ |
| 3.0V | 46.4kΩ | 30.9kΩ |
| 3.3V | 52.3kΩ | 30.1kΩ |

NOTE: $V_{OUT} = (R_1 + R_2)/R_2 \times 1.204$; $R_1||R_2 \cong 19k\Omega$ for best accuracy.

**Figure 6-2. Adjustable-Voltage Version**

## 6.3 Feature Description

### *6.3.1 Output Noise*

A precision band-gap reference is used to generate the internal reference voltage, $V_{REF}$. This reference is the dominant noise source within the TPS736 and generates approximately $32\mu V_{RMS}$ (10Hz to 100kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by:

$$V_N = 32\mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32\mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \quad (1)$$

Since the value of $V_{REF}$ is 1.2V, this relationship reduces to:

$$V_N(\mu V_{RMS}) = 27\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (2)$$

for the case of no $C_{NR}$.

An internal 27kΩ resistor in series with the noise-reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise-reduction capacitor, $C_{NR}$, is connected from NR to ground. For $C_{NR}$ = 10nF, the total noise in the 10Hz to 100kHz bandwidth is reduced by a factor of approximately 3.2, giving the approximate relationship:

$$V_N(\mu V_{RMS}) = 8.5\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (3)$$

for $C_{NR}$ = 10nF.

This noise reduction effect is shown as *RMS Noise Voltage vs $C_{NR}$* in the *Typical Characteristics* section.

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The TPS73601 adjustable version does not have the NR pin available. However, connecting a feedback capacitor, $C_{FB}$, from the output to the feedback pin (FB) reduces output noise and improves load transient performance.

The TPS736 uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass transistor above $V_{OUT}$. The charge pump generates approximately 250µV of switching noise at approximately 4MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of $I_{OUT}$ and $C_{OUT}$.

### 6.3.2 Internal Current Limit

The TPS736 internal current limit helps protect the regulator during fault conditions. Foldback current limit helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when $V_{OUT}$ drops below 0.5V. See Figure 5-17 in the *Typical Characteristics* section.

Note from Figure 5-17 that approximately –0.2V of $V_{OUT}$ results in a current limit of 0mA. Therefore, if OUT is forced below –0.2V before EN goes high, the device can not start up. In applications that work with both a positive and negative voltage supply, the TPS736 must be enabled first.

### 6.3.3 Enable Pin and Shutdown

The enable pin (EN) is active high and is compatible with standard TTL-CMOS levels. $V_{EN}$ below 0.5V (max) turns the regulator off and drops the GND pin current to approximately 10nA. When EN is used to shutdown the regulator, all charge is removed from the pass transistor gate. A $V_{EN}$ above 1.7V (minimum) turns the regulator on and the output ramps back up to a regulated $V_{OUT}$ (see Figure 5-40).

When shutdown capability is not required, connect EN to $V_{IN}$. However, the pass transistor cannot be discharged using this configuration, and the pass transistor can be left on (enhanced) for a significant time after $V_{IN}$ has been removed. This scenario can result in reverse current flow (if the IN pin is low impedance) and faster ramp times upon power-up. In addition, for $V_{IN}$ ramp times slower than a few milliseconds, the output can overshoot upon power-up.

Current limit foldback can prevent device start-up under some conditions. See the *Internal Current Limit* section for more information.

### 6.3.4 Reverse Current

The NMOS pass transistor of the TPS736 provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass transistor is pulled low. To ensure that all charge is removed from the gate of the pass transistor, the EN pin must be driven low before the input voltage is removed. If this is not done, the pass transistor can be left on due to stored charge on the gate.

After the EN pin is driven low, no bias voltage is needed on any pin for reverse current blocking. Reverse current is specified as the current flowing out of the IN pin due to voltage applied on the OUT pin. There is additional current flowing into the OUT pin due to the 80kΩ internal resistor divider to ground (see Figure 6-1 and Figure 6-2).

For the TPS73601, reverse current can flow when $V_{FB}$ is more than 1.0V above $V_{IN}$.

## 6.4 Device Functional Modes

### 6.4.1 Normal Operation With $1.7V \le V_{IN} \le 5.5V$ and $V_{EN} \ge 1.7V$

The TPS736 requires an input voltage of at least 1.7V to function properly and attempt to maintain regulation. If the device output voltage is greater than 1.5V when the input voltage is at 1.7V, the device is operating in dropout and regulation cannot be maintained. Because of the NMOS architecture used in the TPS736, the dropout voltage is not a strong function of the input voltage.

When operating the device near 5.5V, take care to suppress any transient spikes that can exceed the 6.0V absolute maximum voltage rating. The device must never operate at a dc voltage greater than 5.5V.


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# 7 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

The TPS736 is an LDO regulator that uses an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features, combined with low noise and an enable input, make the TPS736 designed for portable applications. This regulator offers a wide selection of fixed output voltage versions and an adjustable output version. All versions have thermal and over-current protection, including foldback current limit.

## 7.2 Typical Application

Figure 7-1 shows the basic circuit connections for the fixed voltage models. Figure 7-2 gives the connections for the adjustable output version (TPS73601).

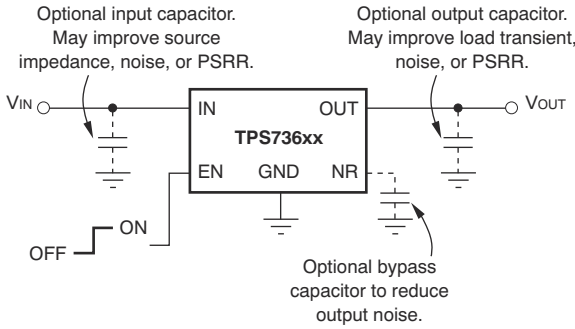


**Figure 7-1. Typical Application Circuit for Fixed-Voltage Versions**

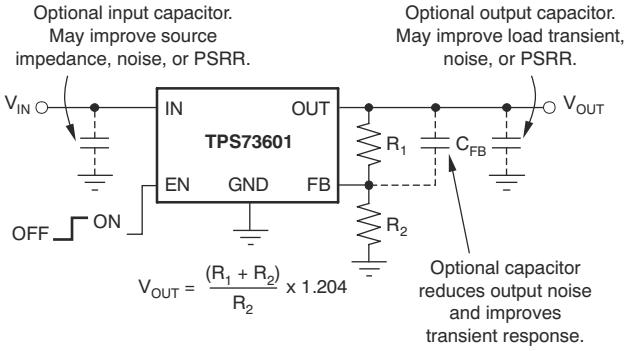


**Figure 7-2. Typical Application Circuit for Adjustable-Voltage Version**

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### 7.2.1 Design Requirements

For this design example, use the parameters listed below as the input parameters.

**Table 7-1. Design Parameters (Fixed-Voltage Version)**

| PARAMETER | DESIGN REQUIREMENT |
|---|---|
| Input voltage | 5V, ±3% |
| Output voltage | 3.3V, ±1% |
| Output current | 400mA (maximum), 20mA (minimum) |
| RMS noise, 10Hz to 100kHz | < 30$\mu V_{RMS}$ |
| Ambient temperature | 55°C (maximum) |

**Table 7-2. Design Parameters (Adjustable-Voltage Version)**

| PARAMETER | DESIGN REQUIREMENT |
|---|---|
| Input voltage | 5V, ±3%, provided by the dc/dc converter switching at 1MHz |
| Output voltage | 2.5V, ±1% |
| Output current | 0.4A (maximum), 10mA (minimum) |
| RMS noise, 10Hz to 100kHz | < 35$\mu V_{RMS}$ |
| Ambient temperature | 55°C (maximum) |

### 7.2.2 Detailed Design Procedure

The first step when designing with a linear regulator is to examine the maximum load current along with the input and output voltage requirements to determine if the device thermal and dropout voltage requirements can be met. At 0.4A, the dropout voltage of the TPS73633 is a maximum of 200mV over temperature; thus, the dropout headroom is sufficient for operation over both input and output voltage accuracy.

The maximum power dissipated in the linear regulator is the maximum voltage dropped across the pass transistor from the input to the output times the maximum load current. In this example, the maximum voltage drop across in the pass transistor is 5V + 3% (5.15V) minus 3.3V – 1% (3.267V) or 1.883V. The power dissipated in the pass transistor is calculated by taking this voltage drop multiplied by the maximum load current. For this example, the maximum power dissipated in the linear regulator is 942mW. Once the power dissipated in the linear regulator is known, the corresponding junction temperature rise can be calculated. To calculate the junction temperature rise above ambient, the power dissipated must be multiplied by the junction-to-ambient thermal resistance. For thermal resistance information see the *Thermal Protection* section. For this example, using the DRB package, the maximum junction temperature rise is calculated to be 45°C. The maximum junction temperature rise is calculated by adding junction temperature rise to the maximum ambient temperature. In this example, the maximum junction temperature is 100°C. Keep in mind the maximum junction temperate must be below 125°C for reliable operation. Addition ground planes, added thermal vias, and air flow all help to lower the maximum junction temperature. Using the DCQ or DBV packages are not recommended for this application due to the excessive junction temperature rise that is incurred.

To get the noise level below 30$\mu V_{RMS}$, a noise reduction capacitance ($C_{NR}$) of 10nF is selected along with an output capacitance of 10µF. Referencing the *Output Noise* section, the RMS noise can be calculated to be 28$\mu V_{RMS}$.

Use of an input capacitor is optional. However, in systems where the input supply is located several inches away from the LDO, a small 0.1µF input capacitor is recommended to negate the adverse effects that input supply inductance has on stability and ac performance.

In the same way as with designing with a fixed output voltage, the first step is to examine the maximum load current along with the input and output voltage requirements to determine if the device thermal and dropout voltage requirements are met. At 0.4A, the maximum dropout voltage is 200mV. Since the input voltage is 5V and the output voltage is 2.5V, there is more than sufficient voltage headroom to avoid dropout and maintain good PSRR.


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The maximum power dissipated in the linear regulator is the maximum voltage dropped across the pass transistor from the input to the output times the maximum load current. In this example, the maximum voltage drop across in the pass transistor is 5V + 3% (5.15 V) minus 2.5V – 1% (2.475V) or 2.675V. The power dissipated in the pass transistor is calculated by taking this voltage drop multiplied by the maximum load current. For this example, the maximum power dissipated in the linear regulator is 1.07W. Once the power dissipated in the linear regulator is known, the corresponding junction temperature rise can be calculated. To calculate the junction temperature rise above ambient, the power dissipated must be multiplied by the junction-to-ambient thermal resistance. For thermal resistance information, see the *Thermal Information* table. For this example, using the DRB package, the maximum junction temperature rise is calculated to be 51°C. The maximum junction temperature rise is calculated by adding junction temperature rise to the maximum ambient temperature. In this example, the maximum junction temperature is 106°C. Keep in mind the maximum junction temperate must be below 125°C for reliable operation. Addition ground planes, added thermal vias, and air flow all help to lower the maximum junction temperature. Using the DCQ or DBV packages are not recommended for this application due to the excessive junction temperature rise that is incurred.

$R_1$ and $R_2$ can be calculated for any output voltage using the formula shown in Figure 7-2. Sample resistor values for common output voltages are shown in Figure 6-2.

For best accuracy, make the parallel combination of $R_1$ and $R_2$ approximately equal to 19kΩ. This 19kΩ, in addition to the internal 8kΩ resistor, presents the same impedance to the error amplifier as the 27kΩ bandgap reference output. This impedance helps compensate for leakages into the error amplifier terminals.

Using the values in Figure 6-2 for a 2.5V output results in a value of 39.2kΩ for $R_1$ and 36.5kΩ for $R_2$.

To get the noise level below 35$\mu V_{RMS}$, a noise reduction capacitance ($C_{FF}$) of 10nF is selected. Figure 5-47 must be used as a reference when selecting optimal value for $C_{FF}$.

A 10µF, low equivalent series resistance (ESR) ceramic X5R capacitor was used on the output of this design to minimize the output voltage droop during a low transient. Use of an input capacitor is optional. However, in systems where the input supply is located several inches away from the LDO, a small 0.1µF input capacitor is recommended to negate the adverse effects that input supply inductance has on stability and ac performance. See the *Input and Output Capacitor Requirements* section for additional information about input and output capacitor selection.

#### 7.2.2.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1µF to 1µF, low ESR capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor can be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS736 does not require an output capacitor for stability and has maximum phase margin with no capacitor. The device is designed to be stable for all available types and values of capacitors. In applications where multiple low ESR capacitors are in parallel, ringing can occur when the product of $C_{OUT}$ and total ESR drops below 50nΩ × F. Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance meets this requirement.

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#### 7.2.2.2 Dropout Voltage

The TPS736 uses an NMOS pass transistor to achieve extremely low dropout. When ($V_{IN}$ – $V_{OUT}$) is less than the dropout voltage ($V_{DO}$), the NMOS pass transistor is in the linear region of operation and the input-to-output resistance is the $R_{DS(on)}$ of the NMOS pass transistor.

For large step changes in load current, the TPS736 requires a larger voltage drop from $V_{IN}$ to $V_{OUT}$ to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the dc dropout. Values of $V_{IN}$ – $V_{OUT}$ above this line provide normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom ($V_{IN}$ to $V_{OUT}$ voltage drop). Under worst-case conditions [full-scale instantaneous load change with ($V_{IN}$ – $V_{OUT}$) close to dc dropout levels], the TPS736 can take a couple of hundred microseconds to return to the specified regulation accuracy.

#### 7.2.2.3 Transient Response

The low open-loop output impedance provided by the NMOS pass transient in a voltage follower configuration allows operation without an output capacitor for many applications. As with any regulator, the addition of a capacitor (nominal value 1µF) from the OUT pin to ground reduces undershoot magnitude but increases the duration. In the adjustable version, the addition of a capacitor, $C_{FB}$, from the OUT pin to the FB pin also improves the transient response.

The TPS736 does not have active pull-down when the output is over-voltage. This feature allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This feature also results in an output overshoot of several percent if load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor $C_{OUT}$ and the internal/external load resistance. The rate of decay is given by:

Fixed voltage version

$$dV / dt = \frac{V_{OUT}}{C_{OUT} \times 80\ k\Omega \parallel R_{LOAD}} \quad (4)$$

Adjustable voltage version

$$dV / dt = \frac{V_{OUT}}{C_{OUT} \times 80\ k\Omega \parallel (R_1 + R_2) \parallel R_{LOAD}} \quad (5)$$


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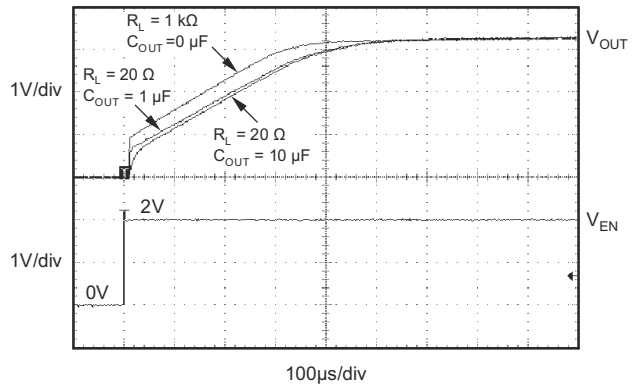
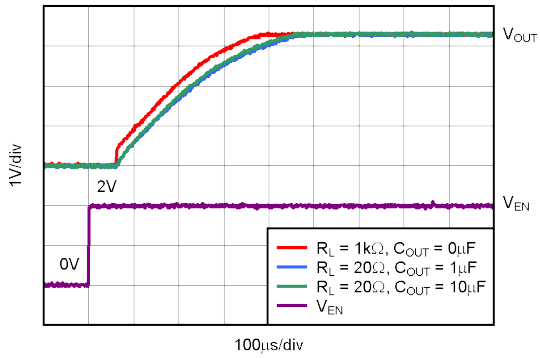
### 7.2.3 Application Curves



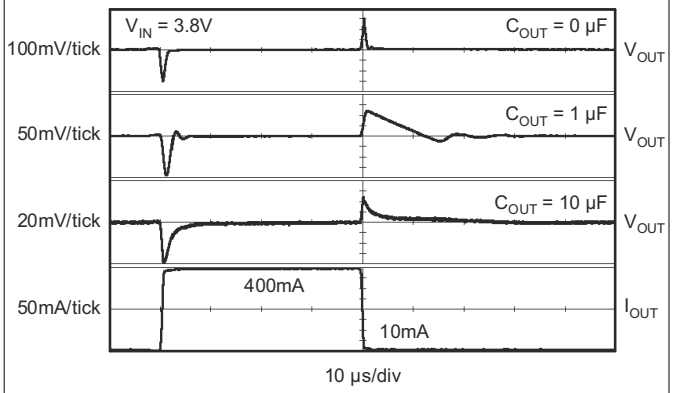

Legacy silicon

**Figure 7-3. TPS73633 Turn-On Response**



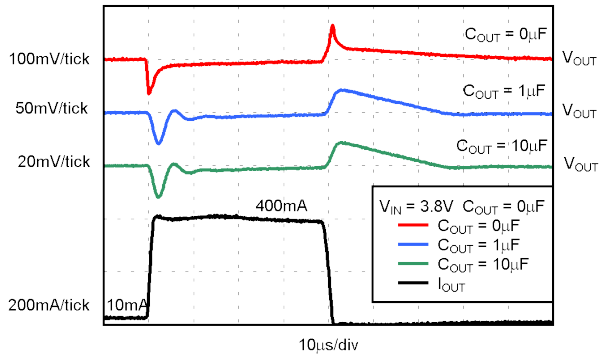

New silicon

**Figure 7-4. TPS73633 Turn-On Response**



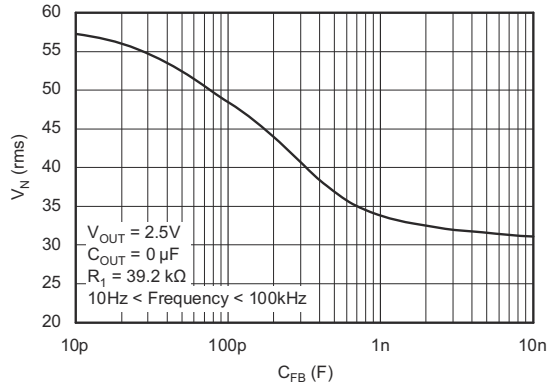

Legacy silicon

**Figure 7-5. TPS73633 Load Transient Response**



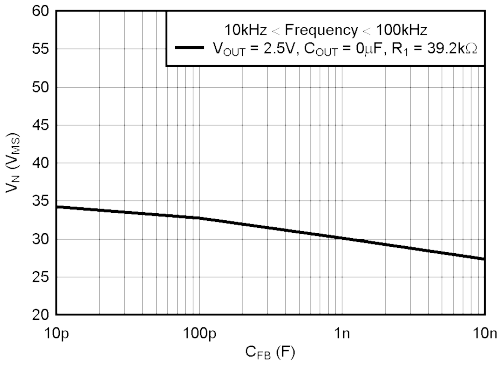

New silicon

**Figure 7-6. TPS73633 Load Transient Response**




Legacy silicon

**Figure 7-7. TPS73601 RMS Noise Voltage vs $C_{FB}$**




New silicon

**Figure 7-8. TPS73601 RMS Noise Voltage vs $C_{FB}$**

### 7.2.3 Application Curves (continued)

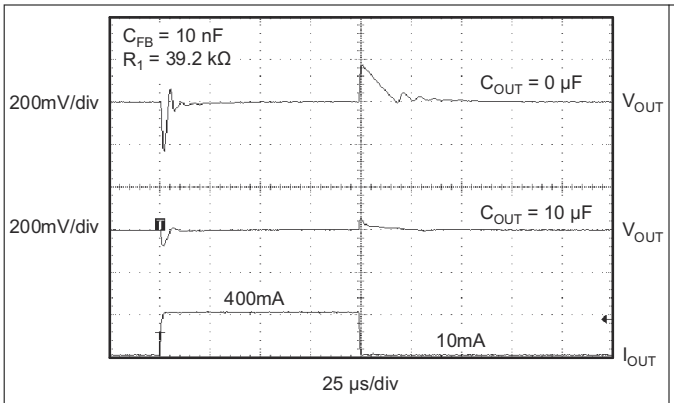



**Figure 7-9. TPS73601 Load Transient, Adjustable Version**

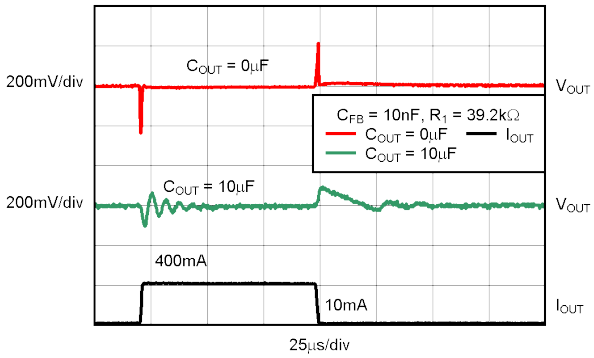



**Figure 7-10. TPS73601 Load Transient, Adjustable Version**

## 7.3 Power Supply Recommendations

This device is designed to operate with an input supply range of 1.7V to 5.5V. If the input supply is noisy, additional input capacitors with low ESR help improve output noise performance.

## 7.4 Layout

### 7.4.1 Layout Guidelines

To improve ac performance such as PSRR, output noise, and transient response, design the board with ground plane connections for $V_{IN}$ and $V_{OUT}$ capacitors, and the ground plane connected at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

#### 7.4.1.1 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are shown in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heat-sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation ($P_D$) is equal to the product of the output current times the voltage drop across the output pass transistor ($V_{IN}$ to $V_{OUT}$):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to provide the required output voltage.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#### 7.4.1.2 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This limits the dissipation of the regulator, protecting the device from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature must be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS736 has been designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TPS736 into thermal shutdown degrades device reliability.

### *7.4.2 Layout Examples*

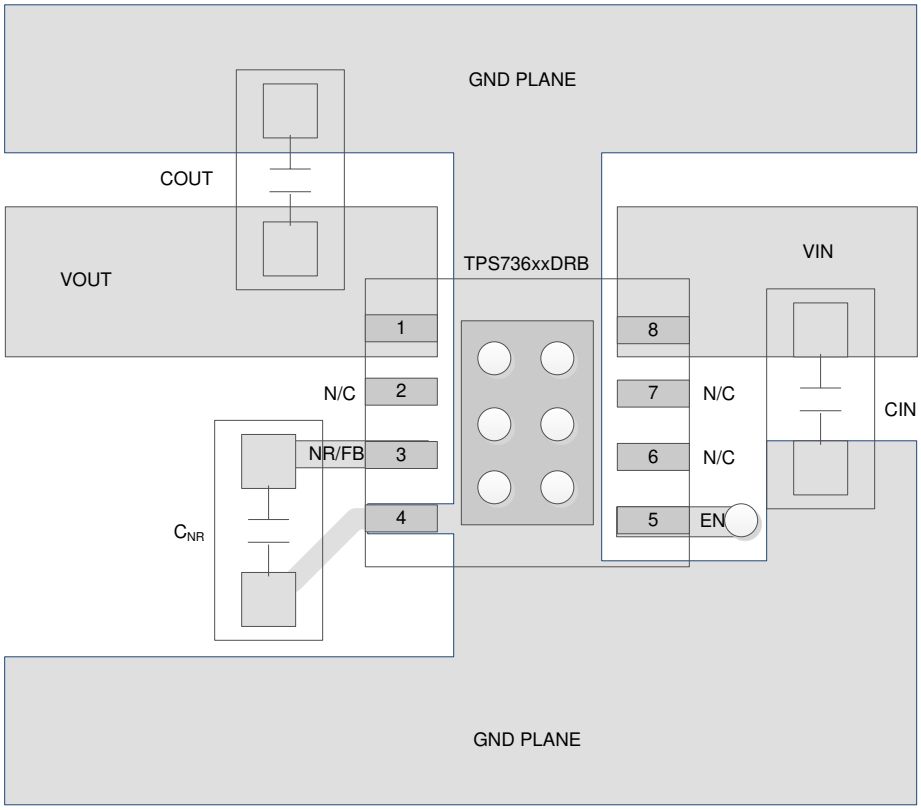


**Figure 7-11. Fixed Output Voltage Option Layout (DRB Package)**

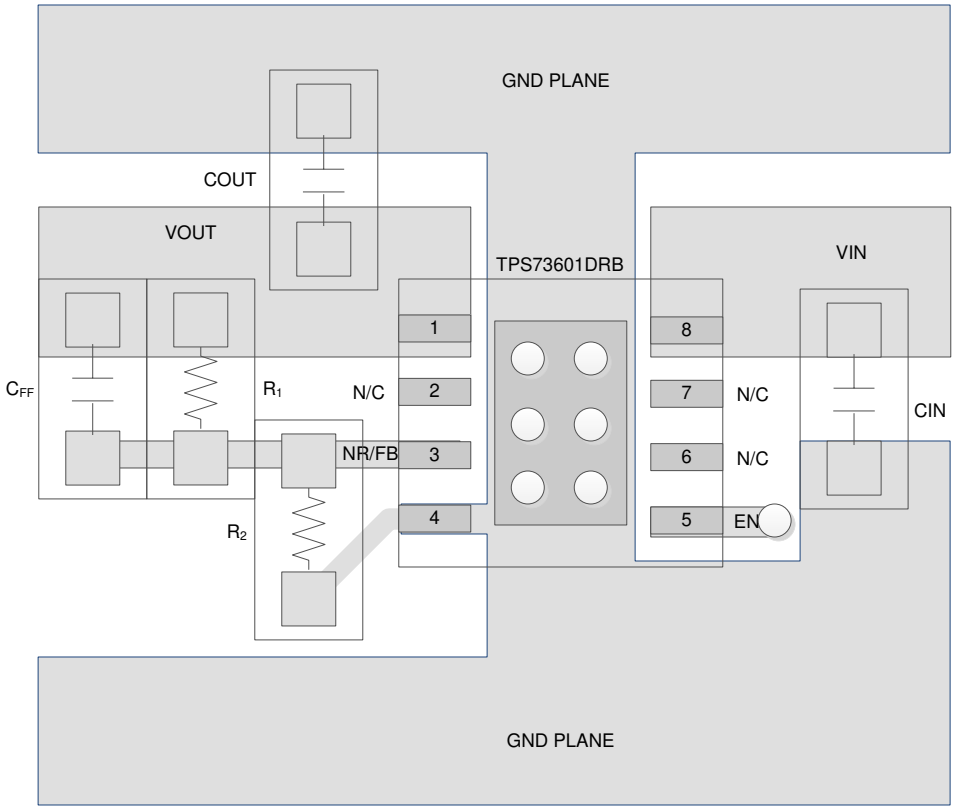


**Figure 7-12. Adjustable Output Voltage Option Layout (DRB Package)**

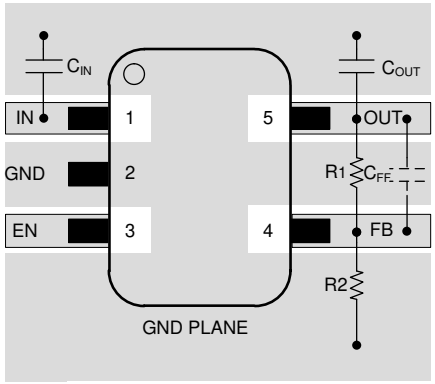


**Figure 7-13. Layout Example for the DBV Package Adjustable Version**


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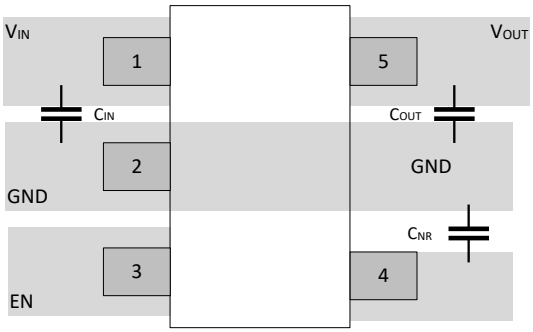


**Figure 7-14. Layout Example for the DBV Package Fixed Version**

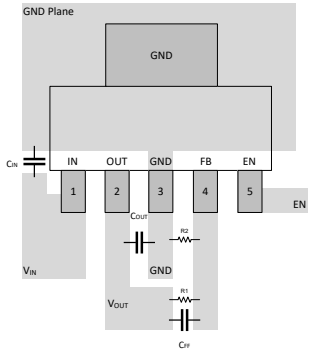


**Figure 7-15. Layout Example for the DCQ Package Adjustable Version**

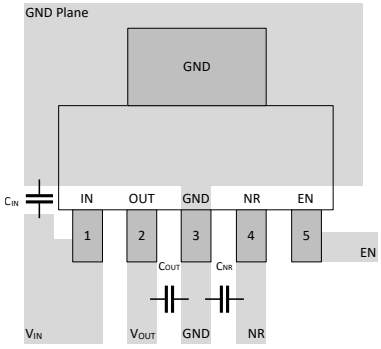


**Figure 7-16. Layout Example for the DCQ Package Fixed Version**

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# 8 Device and Documentation Support

## 8.1 Device Support

### *8.1.1 Development Support*

#### 8.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS736. The TPS73601DRBEVM-518 evaluation module (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

#### 8.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS736 is available through the product folders under *Simulation Models*.

### *8.1.2 Device Nomenclature*

**Table 8-1. Device Nomenclature**

| PRODUCT(1) | DESCRIPTION |
|---|---|
| TPS736**xxyyy z(M3)** | **xx** is the nominal output voltage (for example, 25 = 2.5V; 01 = Adjustable).<br>**yyy** is the package designator.<br>**z** is the package quantity.<br>**M3** is a suffix designator for devices that only use the latest manufacturing flow (CSO: RFB). Devices without this suffix ship with the *legacy silicon* (CSO: DLN) or the *new silicon* (CSO: RFB). The reel packaging label provides CSO information to distinguish which silicon is being used. Device performance for new and legacy silicon is denoted throughout the document. |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

## 8.2 Documentation Support

### *8.2.1 Related Documentation*

For related documentation see the following:

- Texas Instruments, *Regulating $V_{OUT}$ Below 1.2V Using an External Reference* application note
- Texas Instruments, *TPS73x01DRBEVM-518* user's guide

## 8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 8.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.


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### 8.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision W (May 2025) to Revision X (May 2025) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document | 1 |
| • Added new silicon ground pin current spec | 6 |

| Changes from Revision V (September 2024) to Revision W (May 2025) | Page |
|---|---|
| • Updated DRB (VSON) for DRB0008A package outline | 4 |
| • Added new silicon DBV thermals | 4 |
| • Changed discussion of EN and added information about EN turning the regulator on in *Enable Pin and Shutdown* section | 18 |
| • Deleted *Package Mounting* section | 25 |
| • Changed *legacy chip* to *legacy silicon* in *Device Nomenclature* table | 28 |

| Changes from Revision U (January 2015) to Revision V (September 2024) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document | 1 |
| • Added M3 devices to document and added the M3 new silicon *Thermal Information* table | 1 |
| • Changed max output current | 4 |
| • Changed VFB typical value | 6 |
| • Added new silicon current limit | 6 |
| • Added new silicon plots to *Typical Characteristics* section | 7 |
| • Changed *Output current* value from *500mA* to *400mA* in *Design Parameters (Fixed-Voltage Version)* table | 20 |
| • Changed *Detailed Design Procedure* section: Changed dropout voltage value from *0.5A* to *0.4A*, changed maximum dropout voltage from an estimation to *200mV* | 20 |
| • Added new silicon plots to *Application Curves* section | 23 |
| • Added *Layout Example for the DBV Package Adjustable Version* through *Layout Example for the DCQ Package Fixed Version* figures to *Layout Examples* section | 25 |
| • Added M3 information to *Device Nomenclature* section | 28 |

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS73601DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PJFQ |
| TPS73601DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PJFQ |
| TPS73601DBVR1G4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PJFQ |
| TPS73601DBVR1G4.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PJFQ |
| TPS73601DBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PJFQ |
| TPS73601DBVT.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PJFQ |
| TPS73601DBVTG4 | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PJFQ |
| TPS73601DBVTG4.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PJFQ |
| TPS73601DCQ | Obsolete | Production | SOT-223 (DCQ) \| 6 | - | - | Call TI | Call TI | -40 to 125 | PS73601 |
| TPS73601DCQG4 | Obsolete | Production | SOT-223 (DCQ) \| 6 | - | - | Call TI | Call TI | -40 to 125 | PS73601 |
| TPS73601DCQR | Active | Production | SOT-223 (DCQ) \| 6 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PS73601 |
| TPS73601DCQR.A | Active | Production | SOT-223 (DCQ) \| 6 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PS73601 |
| TPS73601DRBR | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PJFQ |
| TPS73601DRBR.A | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PJFQ |
| TPS73601DRBRG4 | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PJFQ |
| TPS73601DRBRM3 | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PJFQ |
| TPS73601DRBRM3.A | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PJFQ |
| TPS73601DRBT | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PJFQ |
| TPS73601DRBT.A | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PJFQ |
| TPS73601DRBTG4 | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PJFQ |
| TPS736125DRBR | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | T49 |
| TPS736125DRBR.A | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | T49 |
| TPS73615DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T44 |
| TPS73615DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T44 |
| TPS73615DBVT | Obsolete | Production | SOT-23 (DBV) \| 5 | - | - | Call TI | Call TI | -40 to 125 | T44 |
| TPS73615DCQ | Obsolete | Production | SOT-223 (DCQ) \| 6 | - | - | Call TI | Call TI | -40 to 125 | PS73615 |
| TPS73615DCQR | Active | Production | SOT-223 (DCQ) \| 6 | 2500 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | PS73615 |
| TPS73615DCQR.A | Active | Production | SOT-223 (DCQ) \| 6 | 2500 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | PS73615 |
| TPS73615DCQRG4 | Active | Production | SOT-223 (DCQ) \| 6 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PS73615 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS73615DCQRG4.A | Active | Production | SOT-223 (DCQ) \| 6 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PS73615 |
| TPS73615DRBR | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | T44 |
| TPS73615DRBR.A | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | T44 |
| TPS73616DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OCQ |
| TPS73616DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OCQ |
| TPS73616DBVT | Obsolete | Production | SOT-23 (DBV) \| 5 | - | - | Call TI | Call TI | -40 to 125 | OCQ |
| TPS73618DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T43 |
| TPS73618DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T43 |
| TPS73618DBVRG4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T43 |
| TPS73618DBVRG4.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T43 |
| TPS73618DBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T43 |
| TPS73618DBVT.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T43 |
| TPS73618DBVTG4 | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T43 |
| TPS73618DBVTG4.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T43 |
| TPS73618DCQR | Active | Production | SOT-223 (DCQ) \| 6 | 2500 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | PS73618 |
| TPS73618DCQR.A | Active | Production | SOT-223 (DCQ) \| 6 | 2500 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | PS73618 |
| TPS73619DRBR | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | BYY |
| TPS73619DRBR.A | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | BYY |
| TPS73619DRBT | Obsolete | Production | SON (DRB) \| 8 | - | - | Call TI | Call TI | -40 to 125 | BYY |
| TPS73625DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T42 |
| TPS73625DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T42 |
| TPS73625DBVRG4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T42 |
| TPS73625DBVRG4.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T42 |
| TPS73625DBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T42 |
| TPS73625DBVT.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T42 |
| TPS73625DBVTG4 | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T42 |
| TPS73625DBVTG4.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T42 |
| TPS73625DCQ | Obsolete | Production | SOT-223 (DCQ) \| 6 | - | - | Call TI | Call TI | -40 to 125 | PS73625 |
| TPS73625DCQR | Active | Production | SOT-223 (DCQ) \| 6 | 2500 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | PS73625 |
| TPS73625DCQR.A | Active | Production | SOT-223 (DCQ) \| 6 | 2500 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | PS73625 |
| TPS73630DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T45 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS73630DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T45 |
| TPS73630DBVRG4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T45 |
| TPS73630DBVRG4.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T45 |
| TPS73630DBVT | Obsolete | Production | SOT-23 (DBV) \| 5 | - | - | Call TI | Call TI | -40 to 125 | T45 |
| TPS73630DCQ | Obsolete | Production | SOT-223 (DCQ) \| 6 | - | - | Call TI | Call TI | -40 to 125 | PS73630 |
| TPS73630DCQR | Active | Production | SOT-223 (DCQ) \| 6 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PS73630 |
| TPS73630DCQR.A | Active | Production | SOT-223 (DCQ) \| 6 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PS73630 |
| TPS73632DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T53 |
| TPS73632DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T53 |
| TPS73632DBVRG4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T53 |
| TPS73632DBVRG4.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T53 |
| TPS73633DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T46 |
| TPS73633DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T46 |
| TPS73633DBVR1G4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T46 |
| TPS73633DBVR1G4.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T46 |
| TPS73633DBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T46 |
| TPS73633DBVT.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T46 |
| TPS73633DBVTG4 | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T46 |
| TPS73633DBVTG4.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T46 |
| TPS73633DCQ | Obsolete | Production | SOT-223 (DCQ) \| 6 | - | - | Call TI | Call TI | -40 to 125 | PS73633 |
| TPS73633DCQR | Active | Production | SOT-223 (DCQ) \| 6 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PS73633 |
| TPS73633DCQR.A | Active | Production | SOT-223 (DCQ) \| 6 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PS73633 |
| TPS73633DRBR | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | T46 |
| TPS73633DRBR.A | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | T46 |
| TPS73633DRBRM3 | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T46 |
| TPS73633DRBRM3.A | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T46 |
| TPS73633DRBT | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T46 |
| TPS73633DRBT.A | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T46 |
| TPS73633DRBTG4 | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T46 |
| TPS73643DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T54 |
| TPS73643DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T54 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS73643DBVRG4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T54 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS736 :**

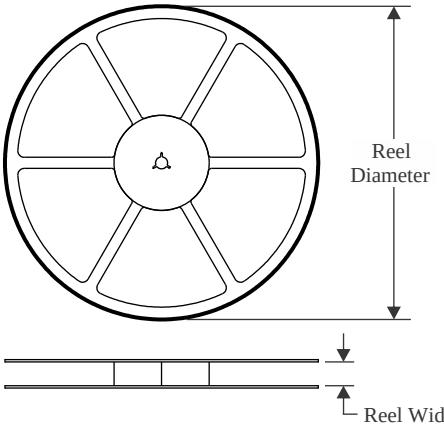
- Automotive : TPS736-Q1

NOTE: Qualified Version Definitions:

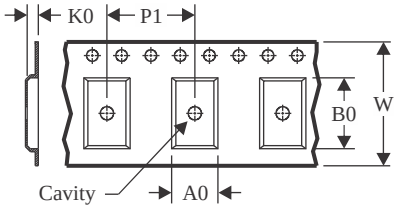
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

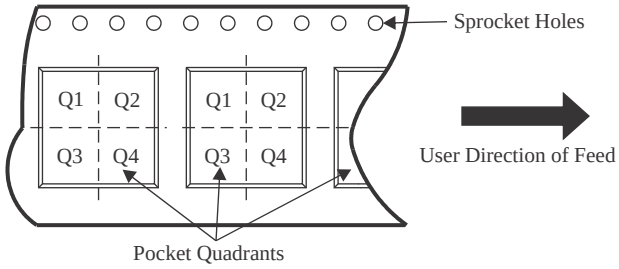



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

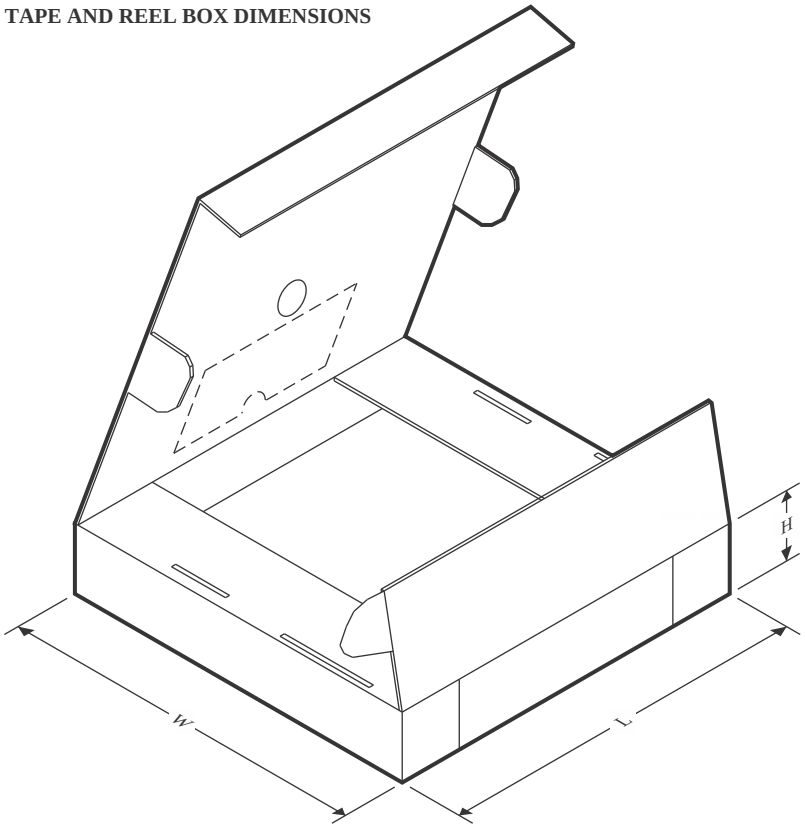



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS73601DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS73601DBVR1G4 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS73601DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS73601DBVTG4 | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS73601DCQR | SOT-223 | DCQ | 6 | 2500 | 330.0 | 12.4 | 7.05 | 7.4 | 1.9 | 8.0 | 12.0 | Q3 |
| TPS73601DRBR | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS73601DRBRM3 | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS73601DRBT | SON | DRB | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS736125DRBR | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS73615DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS73615DCQR | SOT-223 | DCQ | 6 | 2500 | 330.0 | 12.4 | 6.85 | 7.3 | 1.88 | 8.0 | 12.0 | Q3 |
| TPS73615DCQRG4 | SOT-223 | DCQ | 6 | 2500 | 330.0 | 12.4 | 7.1 | 7.45 | 1.88 | 8.0 | 12.0 | Q3 |
| TPS73615DRBR | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS73616DBVR | SOT-23 | DBV | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS73618DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS73618DBVRG4 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS73618DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS73618DBVTG4 | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS73618DCQR | SOT-223 | DCQ | 6 | 2500 | 330.0 | 12.4 | 6.85 | 7.3 | 1.88 | 8.0 | 12.0 | Q3 |
| TPS73619DRBR | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.0 | 8.0 | 12.0 | Q2 |
| TPS73625DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS73625DBVRG4 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS73625DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS73625DBVTG4 | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS73625DCQR | SOT-223 | DCQ | 6 | 2500 | 330.0 | 12.4 | 6.85 | 7.3 | 1.88 | 8.0 | 12.0 | Q3 |
| TPS73630DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS73630DBVRG4 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS73630DCQR | SOT-223 | DCQ | 6 | 2500 | 330.0 | 12.4 | 7.1 | 7.45 | 1.88 | 8.0 | 12.0 | Q3 |
| TPS73632DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS73632DBVRG4 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS73633DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS73633DBVR1G4 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS73633DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS73633DBVTG4 | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS73633DCQR | SOT-223 | DCQ | 6 | 2500 | 330.0 | 12.4 | 7.1 | 7.45 | 1.88 | 8.0 | 12.0 | Q3 |
| TPS73633DRBR | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS73633DRBRM3 | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS73633DRBT | SON | DRB | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS73643DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS73601DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS73601DBVR1G4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS73601DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS73601DBVTG4 | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS73601DCQR | SOT-223 | DCQ | 6 | 2500 | 366.0 | 364.0 | 50.0 |
| TPS73601DRBR | SON | DRB | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS73601DRBRM3 | SON | DRB | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS73601DRBT | SON | DRB | 8 | 250 | 210.0 | 185.0 | 35.0 |
| TPS736125DRBR | SON | DRB | 8 | 3000 | 353.0 | 353.0 | 32.0 |
| TPS73615DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS73615DCQR | SOT-223 | DCQ | 6 | 2500 | 356.0 | 356.0 | 36.0 |
| TPS73615DCQRG4 | SOT-223 | DCQ | 6 | 2500 | 346.0 | 346.0 | 29.0 |
| TPS73615DRBR | SON | DRB | 8 | 3000 | 353.0 | 353.0 | 32.0 |
| TPS73616DBVR | SOT-23 | DBV | 5 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS73618DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS73618DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS73618DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS73618DBVTG4 | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |

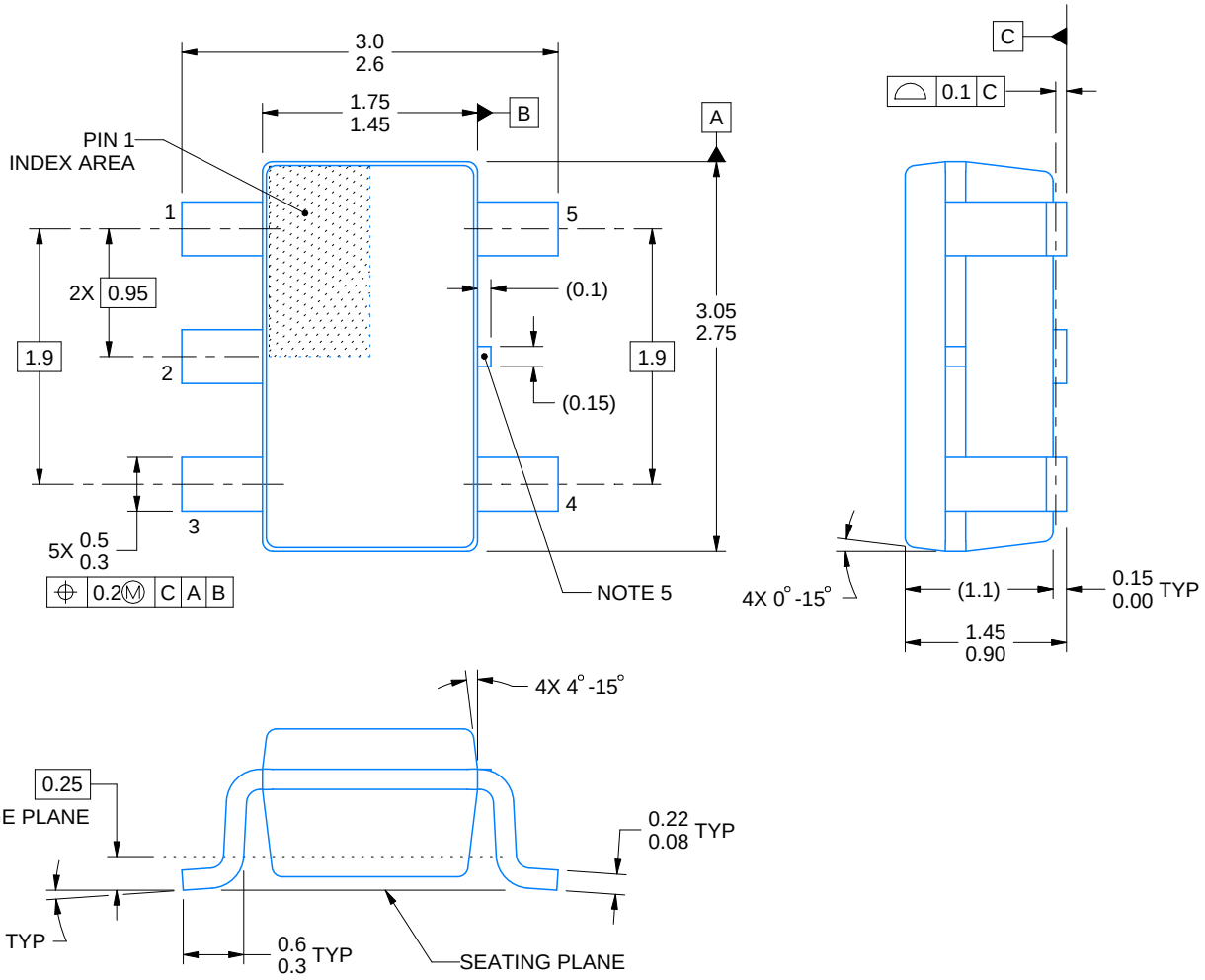
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS73618DCQR | SOT-223 | DCQ | 6 | 2500 | 356.0 | 356.0 | 36.0 |
| TPS73619DRBR | SON | DRB | 8 | 3000 | 367.0 | 367.0 | 38.0 |
| TPS73625DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS73625DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS73625DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS73625DBVTG4 | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS73625DCQR | SOT-223 | DCQ | 6 | 2500 | 356.0 | 356.0 | 36.0 |
| TPS73630DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS73630DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS73630DCQR | SOT-223 | DCQ | 6 | 2500 | 346.0 | 346.0 | 41.0 |
| TPS73632DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS73632DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS73633DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS73633DBVR1G4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS73633DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS73633DBVTG4 | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS73633DCQR | SOT-223 | DCQ | 6 | 2500 | 346.0 | 346.0 | 41.0 |
| TPS73633DRBR | SON | DRB | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS73633DRBRM3 | SON | DRB | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS73633DRBT | SON | DRB | 8 | 250 | 210.0 | 185.0 | 35.0 |
| TPS73643DBVR | SOT-23 | DBV | 5 | 3000 | 200.0 | 183.0 | 25.0 |

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

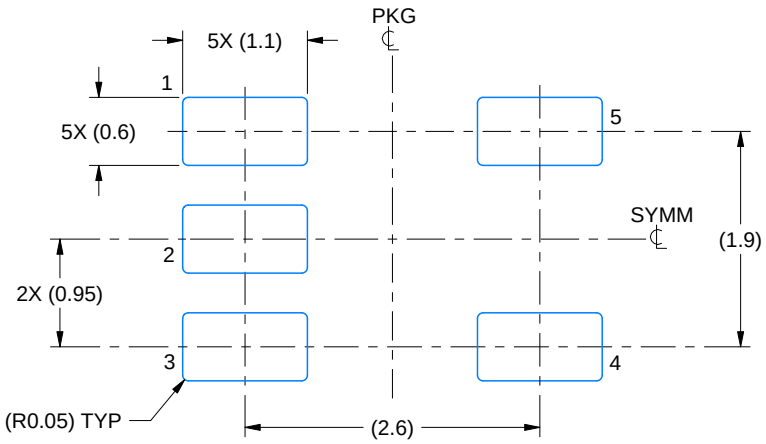
SMALL OUTLINE TRANSISTOR



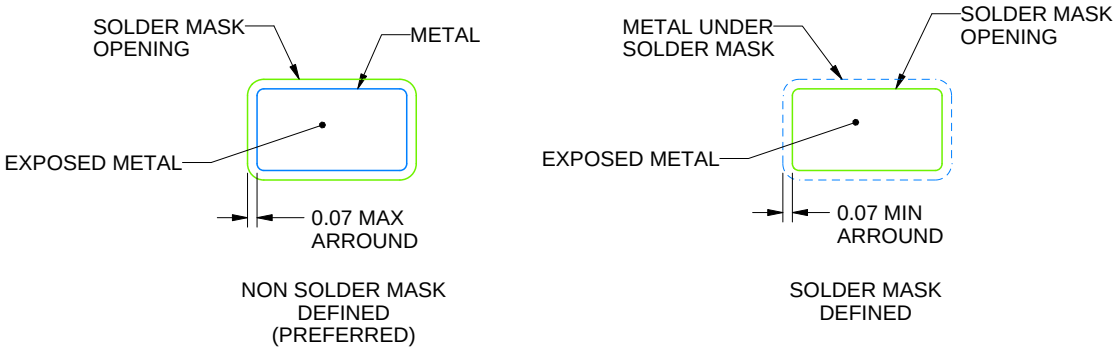

4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

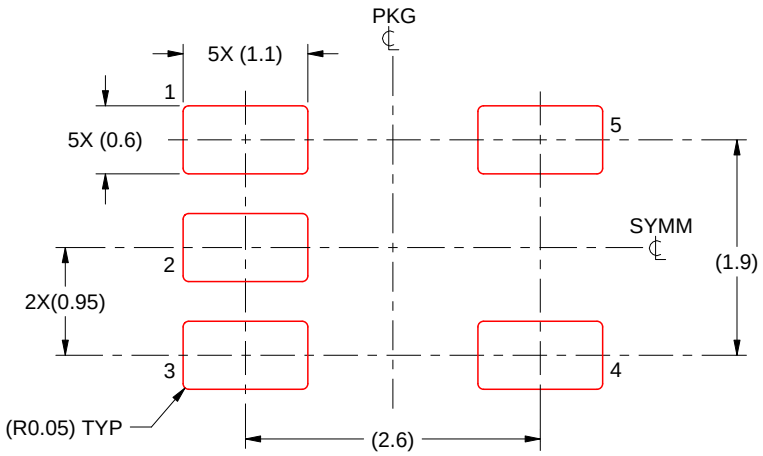



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

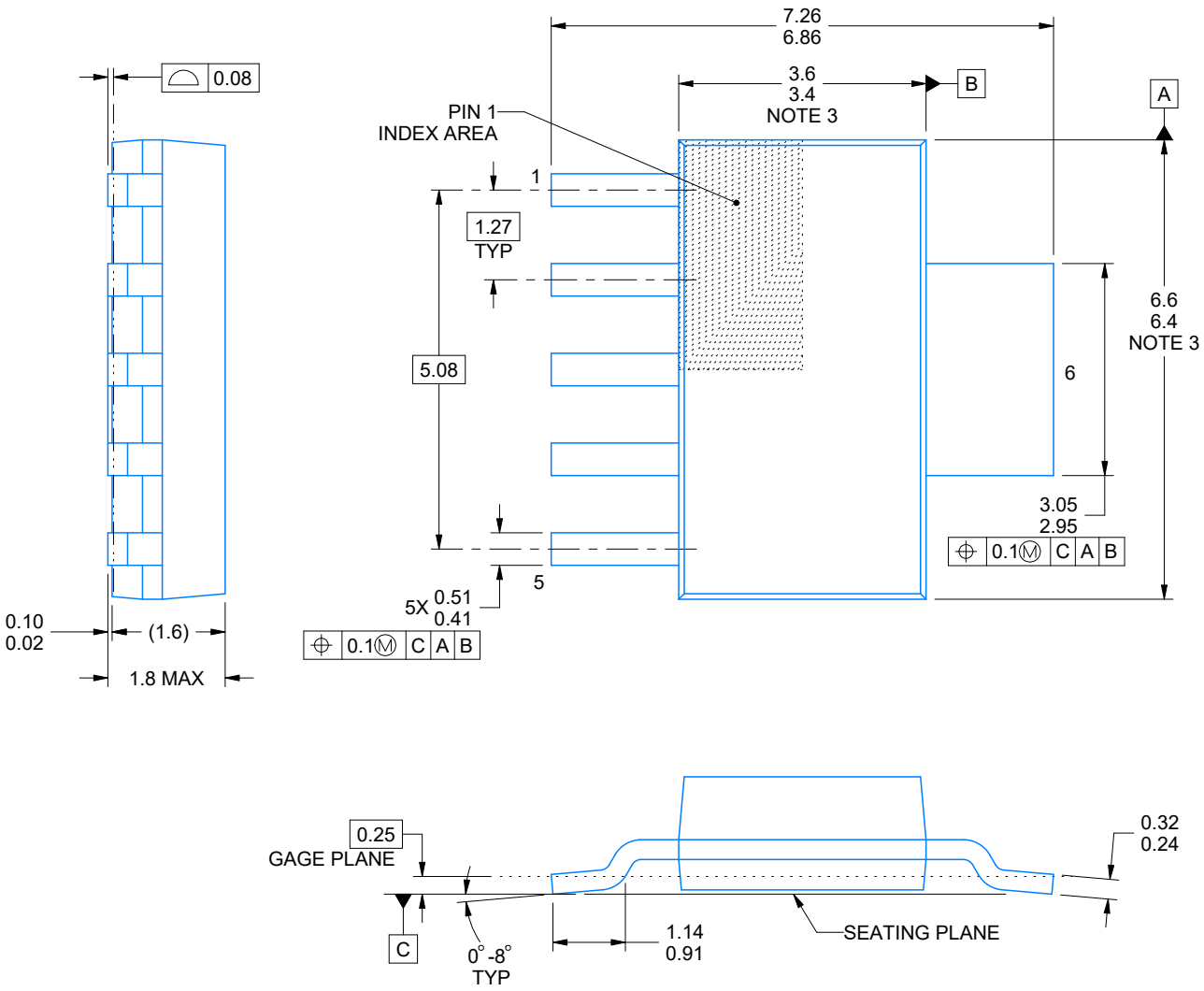
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DCQ0006A

## SOT - 1.8 mm max height

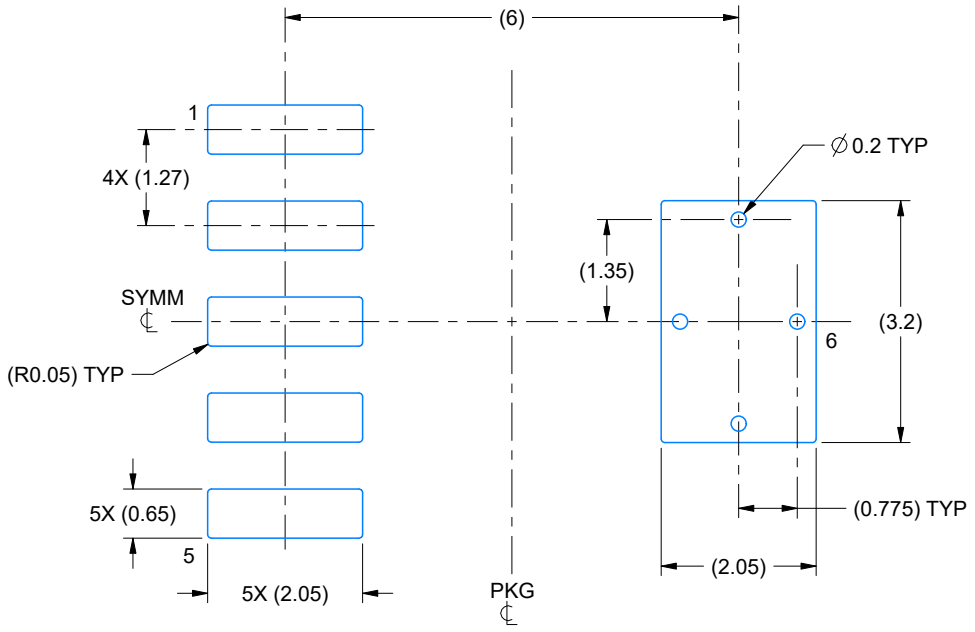
PLASTIC SMALL OUTLINE



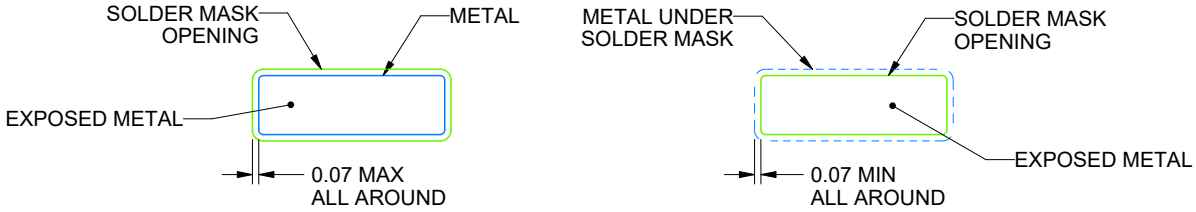

4214845/C 11/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

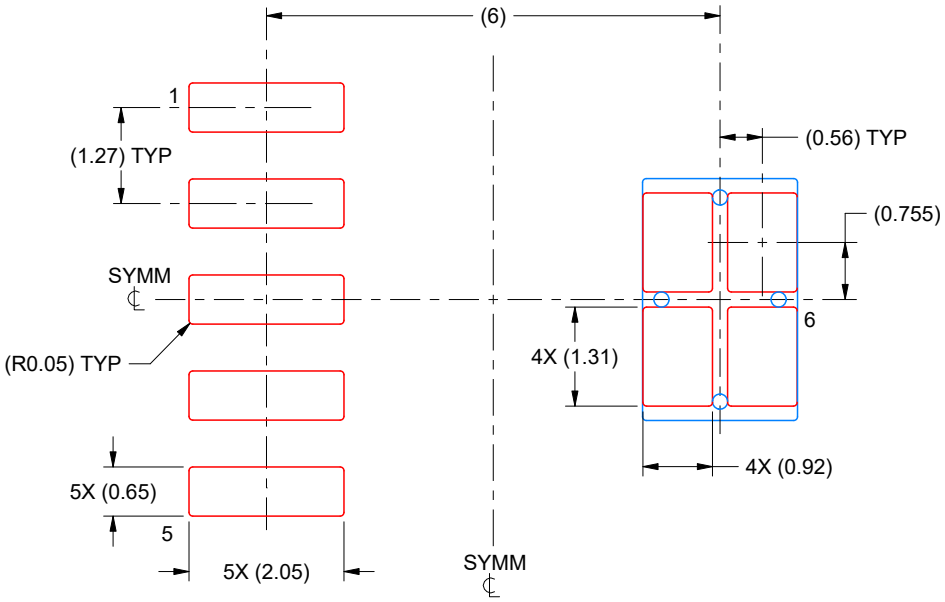



SOLDER MASK DETAILS

4214845/C 11/2021

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214845/C 11/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

# DRB 8

# VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

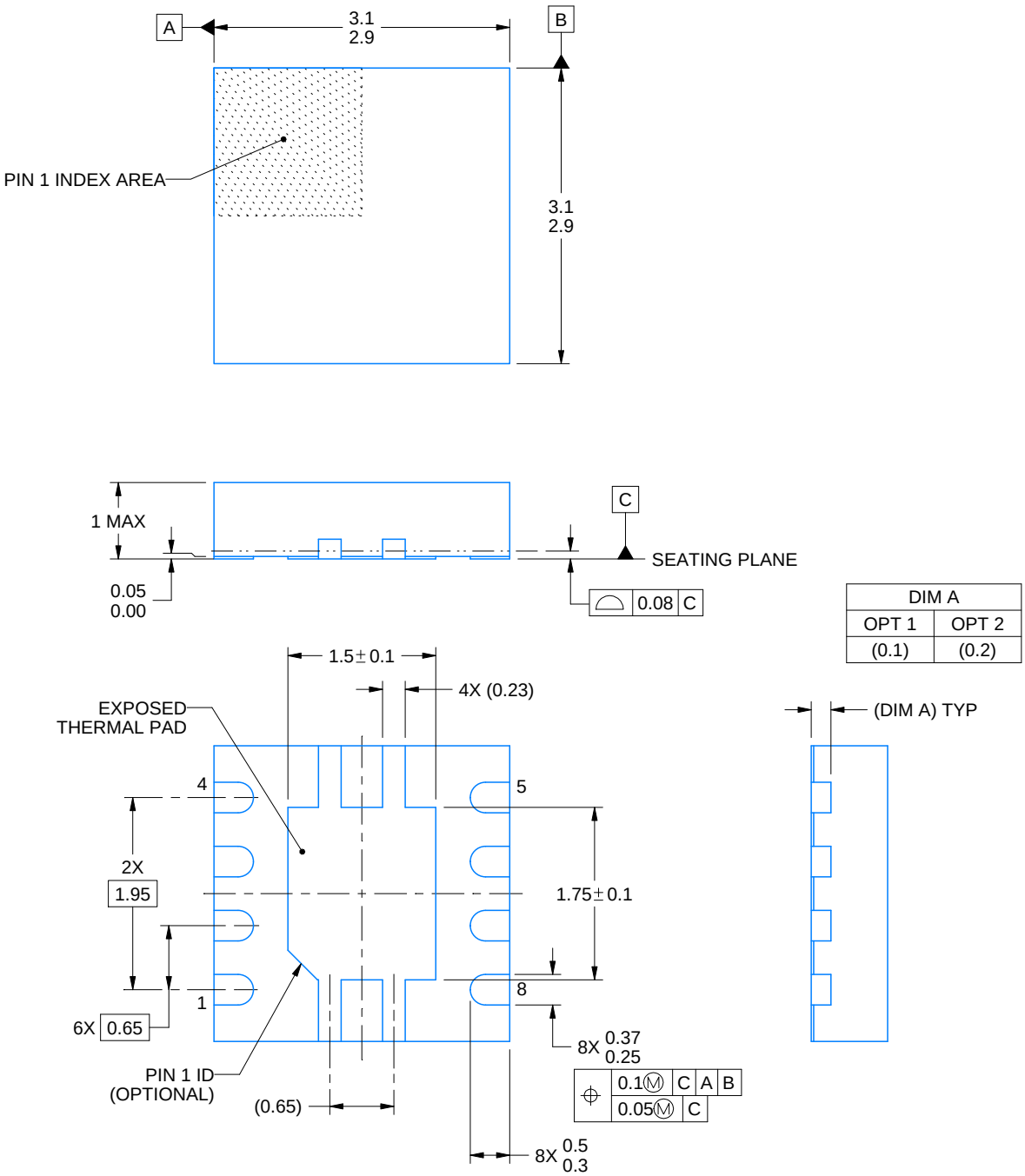
4203482/L

# PACKAGE OUTLINE

## DRB0008A

## VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




NOTES:

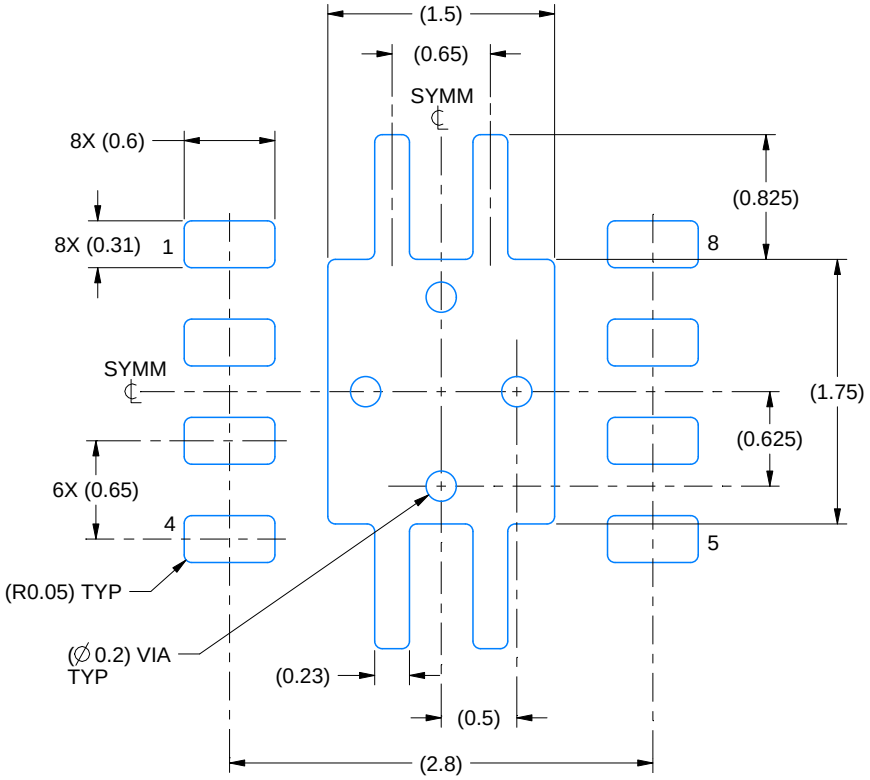
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

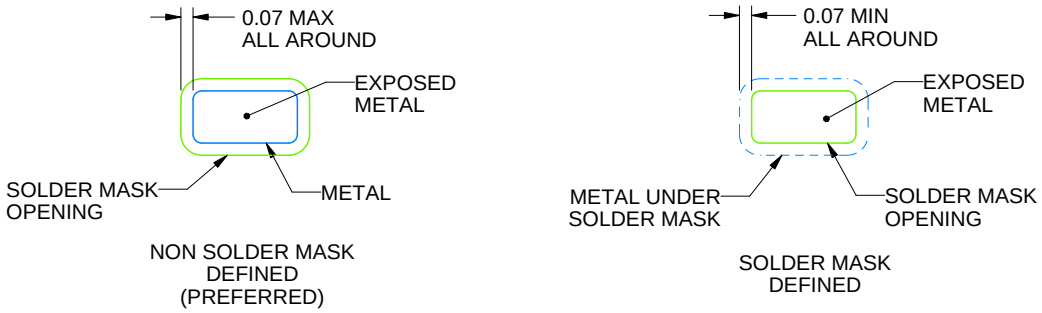
## DRB0008A

## VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

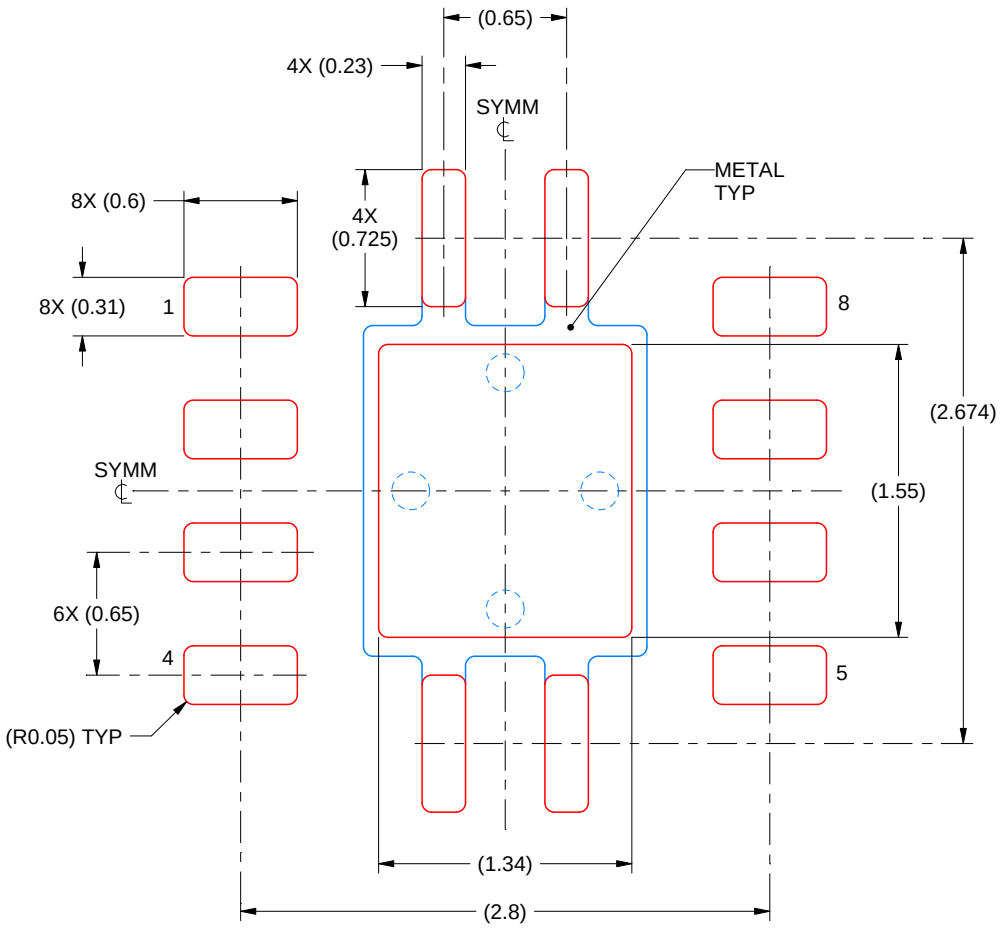



SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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