TPS732-Q1 Automotive, Cap-Free, NMOS, 250mA, Low-Dropout Regulator With Reverse-Current Protection

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 0: –40°C to 150°C, T_A
  - Device HBM classification level 2
  - Device CDM classification level C4B
  - Device MM classification level M2
- Stable with no output capacitor or any value or type of capacitor
- Input voltage range: 1.7V to 5.5V
- Ultra-low dropout voltage: 40mV typical at 250mA
- Excellent load transient response—with or without optional output capacitor
- NMOS topology provides low reverse leakage current
- Low noise: 30μV_{RMS} typical (10kHz to 100kHz)
- Initial accuracy: 0.5%
- 1% overall accuracy (line, load, and temperature)
- Less than 1μA maximum I_Q in shutdown mode
- Thermal shutdown and specified minimum and maximum current limit protection
- Available in multiple output voltage versions:
  - Fixed outputs of 1.2V, 1.5V, 1.6V, 1.8V, 2.5V, 3V, 3.3V, and 5V
  - Adjustable outputs from 1.2V to 5.5V
  - Custom outputs available

2 Applications

- Portable and battery-powered equipment
- Post-regulation for switching supplies
- Noise-sensitive circuitry such as VCOs
- Point of load regulation for DSPs, FPGAs, ASICs, and microprocessors

3 Description

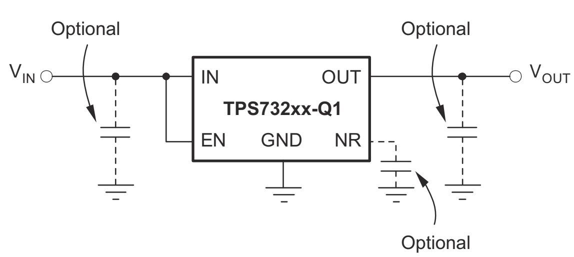
The TPS732-Q1 low-dropout (LDO) voltage regulator uses an NMOS topology consisting of an NMOS pass transient in a voltage-follower configuration. This topology is stable using output capacitors with low ESR, and even allows operation without a capacitor. The topology also provides high reverse blockage (low reverse current) and ground pin current that is nearly constant over all values of output current.

The TPS732-Q1 uses an advanced BiCMOS process to yield high precision while delivering low dropout voltages and low ground pin current. Current consumption, when not enabled, is under 1μA and designed for portable applications. The extremely low output noise (30μV_{RMS} with 0.1μF C_{NR}) is designed for powering VCOs. This device is protected by thermal shutdown and foldback current limit.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS732-Q1	DBV (SOT-23, 5)	2.9mm × 2.8mm
	DCQ (SOT-223, 6)	6.5mm × 7.06mm
	DRB (VSON, 8)	3mm × 3mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit for Fixed Voltage Versions

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4 Pin Configuration and Functions

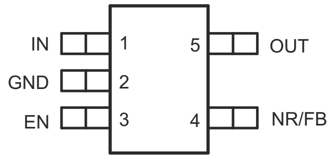


Figure 4-1. DBV Package 5-Pin SOT-23 Top View

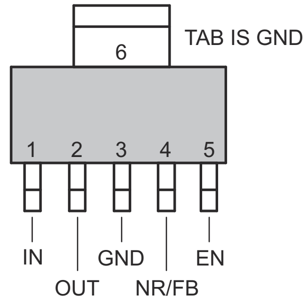
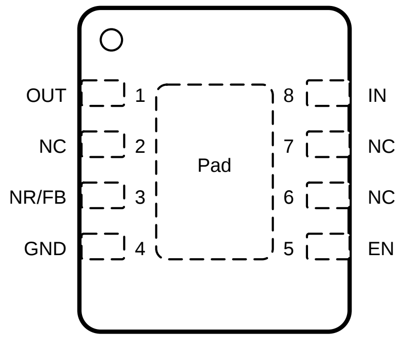


Figure 4-2. DCQ Package, 6-Pin SOT-223 (Top View)



NC: No internal connection

Figure 4-3. DRB Package 8-Pin VSON With Exposed Thermal Pad Top View

Table 4-1. Pin Functions

PIN				TYPE(1)	DESCRIPTION
NAME	NO.				
	SOT-23	SOT-223	VSON		
EN	3	5	5	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. See the *Shutdown* section for more details. EN can be connected to IN if not used.
FB(2)	4	4	3	I	Input to the control loop error amplifier, and is used to set the output voltage of the device.
GND	2	3, 6	4	—	Ground
IN	1	1	8	I	Unregulated input supply
NR(3)	4	4	3	—	Connecting an external capacitor to this pin bypasses noise generated by the internal band gap. This bypass allows output noise to be reduced to low levels.
OUT	5	2	1	O	Output of the regulator. There are no output capacitor requirements for stability.
Pad	—	—	Pad	—	Ground
NC	—	—	2, 6, 7	—	No internal connection

(1) I = Input; O = Output.
(2) Adjustable voltage versions only.
(3) Fixed voltage versions only.

5 Specifications

5.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage	Input, V_{IN}	–0.3	6	V
	Enable, V_{EN}	–0.3	6	
	Output, V_{OUT}	–0.3	5.5	
	V_{NR}, V_{FB}	–0.3	6	
Current	Maximum output, I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P_{DISS}	See *Thermal Information*		
Temperature	Operating junction, T_J	–55	150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	
		Machine model (MM) (legacy silicon only)	±200	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	1.7		5.5	V
I_{OUT}	Output current	0		250	mA
T_J	Operating junction temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC[1]		TPS732-Q1 New silicon			UNIT
		DRB (VSON)	DCQ (SOT-223)	DBV (SOT-23)	
		8 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.4	76	185.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76.6	46.6	82.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.0	18.1	53.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.8	8.6	21.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	22.0	17.6	52.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.8	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Thermal Information

THERMAL METRIC[1]		TPS732-Q1 Legacy silicon		UNIT
		DBV (SOT-23)	DRB (VSON)	
		5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180	47.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64	83	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35	–	°C/W
ψ_{JT}	Junction-to-top characterization parameter	–	2.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	–	17.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	12.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.6 Electrical Characteristics

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5V[1] , I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted). Typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{FB}	Internal reference (TPS73201-Q1)	T_J = 25°C		1.198	1.204	1.210	V
V_{OUT}	Output voltage range (TPS73201-Q1) [2]			V_{FB}		5.5 - V_{DO}	V
	Accuracy[1]	Nominal	T_J = 25°C	–0.5		0.5	%
		V_{IN}, I_{OUT}, and T	V_{OUT} + 0.5V ≤ V_{IN} ≤ 5.5V; 10mA ≤ I_{OUT} ≤ 250mA	–1	±0.5	1	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	($V_{OUT(nom)}$ + 0.5V) ≤ V_{IN} ≤ 5.5V			0.06		%/V
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	1mA ≤ I_{OUT} ≤ 250mA			0.002		%/mA
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	10mA ≤ I_{OUT} ≤ 250mA			0.0008		%/mA
V_{DO}	Dropout voltage[3] (V_{IN} = $V_{OUT(NOM)}$ - 0.1V)	I_{OUT} = 250mA			40	150	mV
$Z_{O(DO)}$	Output impedance in dropout	1.7V ≤ V_{IN} ≤ V_{OUT} + V_{DO}			0.25		Ω
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(nom)}$		250	425	600	mA
I_{SC}	Short-circuit current	V_{OUT} = 0V			300		mA
I_{REV}	Reverse leakage current[4] (-I_{IN})	V_{EN} ≤ 0.5V, 0V ≤ V_{IN} ≤ V_{OUT}			0.1	10	µA
I_{GND}	Ground pin current	I_{OUT} = 10mA (I_Q), legacy silicon			400	550	µA
		I_{OUT} = 10mA (I_Q), new silicon			400	630	
I_{GND}	Ground pin current	I_{OUT} = 250mA			650	950	µA
I_{SHDN}	Shutdown current (I_{GND})	V_{EN} ≤ 0.5V, V_{OUT} ≤ V_{IN} ≤ 5.5V			0.02	1	µA
I_{FB}	Feedback pin current (TPS73201)				0.1	0.45	µA
PSRR	Power-supply rejection ratio (ripple rejection)	f = 100Hz, I_{OUT} = 250mA			58		dB
		f = 10kHz, I_{OUT} = 250mA			37		
V_N	Output noise voltage, BW = 10Hz to 100kHz	C_{OUT} = 10µF, no C_{NR}			27 × V_{OUT}		μV_{RMS}
		C_{OUT} = 10µF, C_{NR} =0.01µF			8.5 × V_{OUT}		
$V_{EN(high)}$	EN pin high (enabled)			1.7		V_{IN}	V
$V_{EN(low)}$	EN pin low (shutdown)			0		0.5	V
$I_{EN(high)}$	Enable pin current (enabled)	V_{EN} = 5.5V			0.02	0.1	µA
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing			160		°C
		Reset, temperature decreasing			140		

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 1.7V, whichever is greater.
(2) TPS73201-Q1 is tested at V_{OUT} = 2.5V.
(3) V_{DO} is not measured for output versions with $V_{OUT(nom)}$ < 1.8V, because minimum V_{IN} = 1.7V.
(4) Fixed-voltage versions only; refer to *Application Information* section for more information.

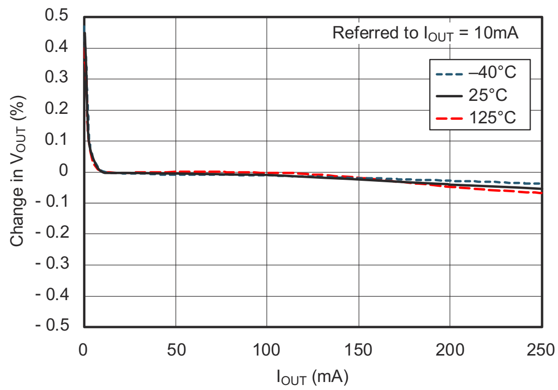
5.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STR}	Start-up time	V_{OUT} = 3V, R_L = 30Ω, C_{OUT} = 1µF, C_{NR} = 0.01µF		600		µs

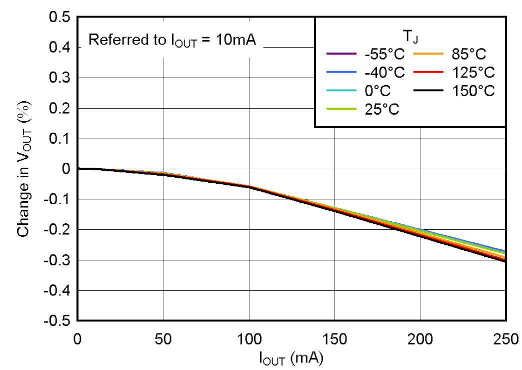
5.8 Typical Characteristics

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



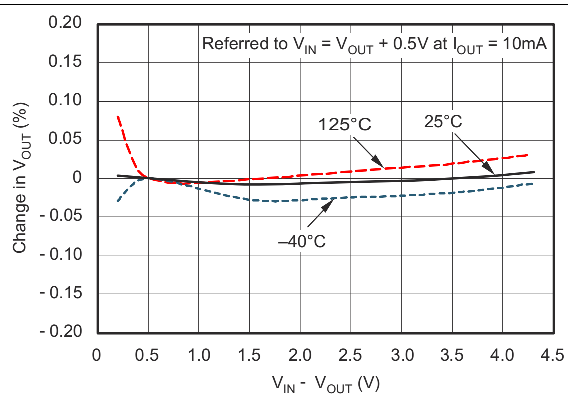
Legacy silicon

Figure 5-1. Load Regulation



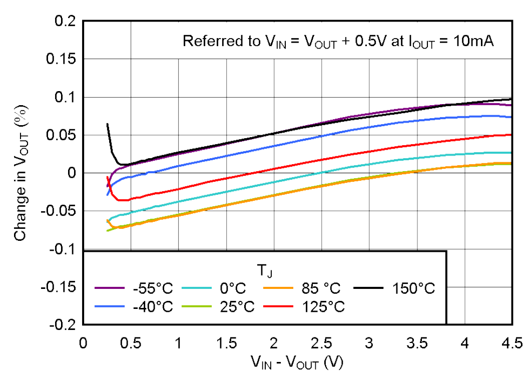
New silicon

Figure 5-2. Load Regulation



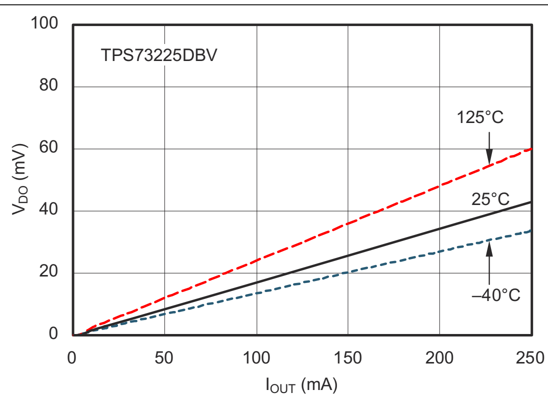
Legacy silicon

Figure 5-3. Line Regulation



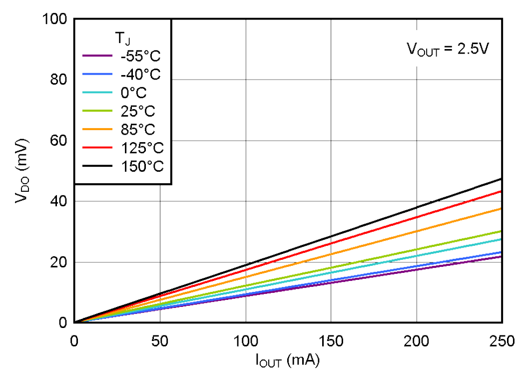
New silicon

Figure 5-4. Line Regulation



Legacy silicon

Figure 5-5. Dropout Voltage vs Output Current



New silicon

Figure 5-6. Dropout Voltage vs Output Current

5.8 Typical Characteristics (continued)

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)

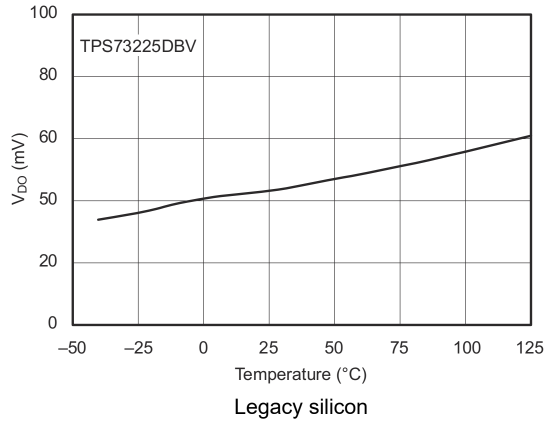


Figure 5-7. Dropout Voltage vs Temperature

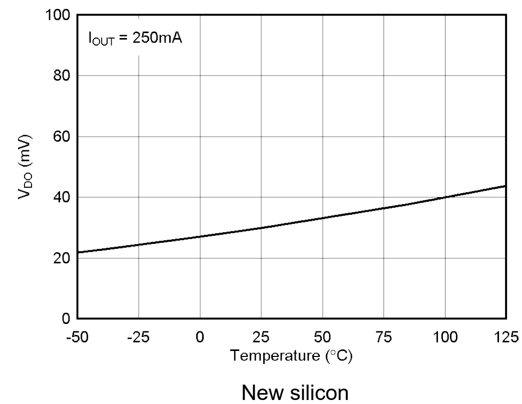


Figure 5-8. Dropout Voltage vs Temperature

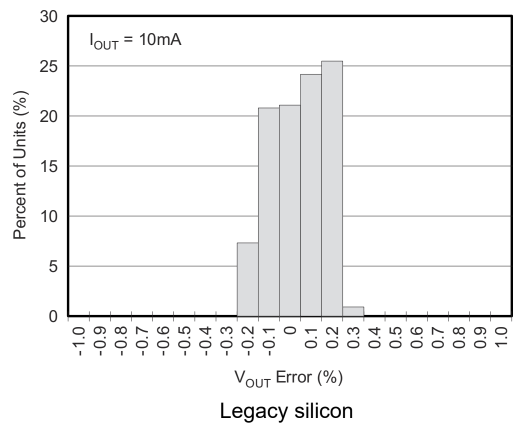


Figure 5-9. Output Voltage Accuracy Histogram

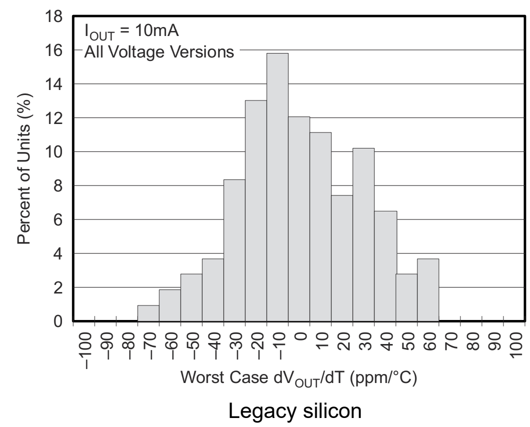


Figure 5-10. Output Voltage Drift Histogram

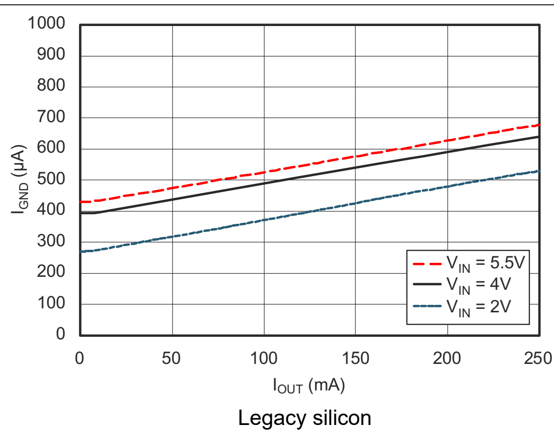


Figure 5-11. Ground Pin Current vs Output Current

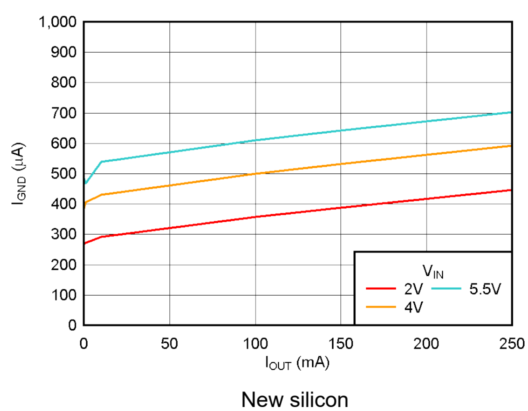
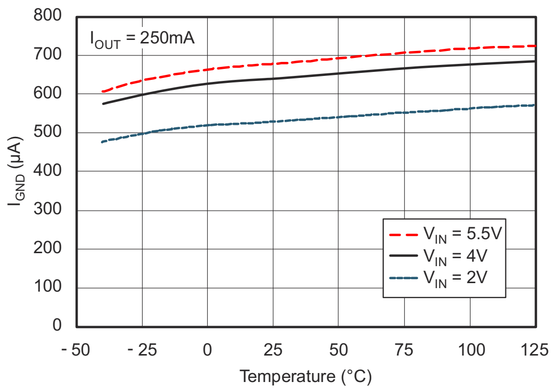


Figure 5-12. Ground Pin Current vs Output Current

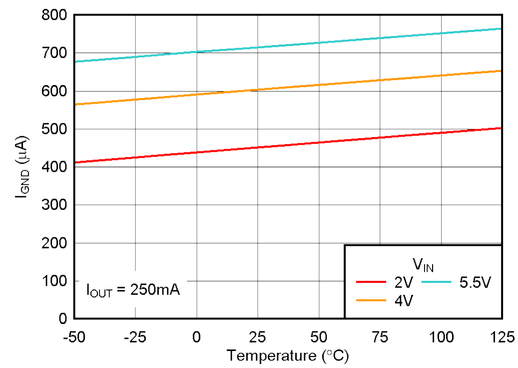
5.8 Typical Characteristics (continued)

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



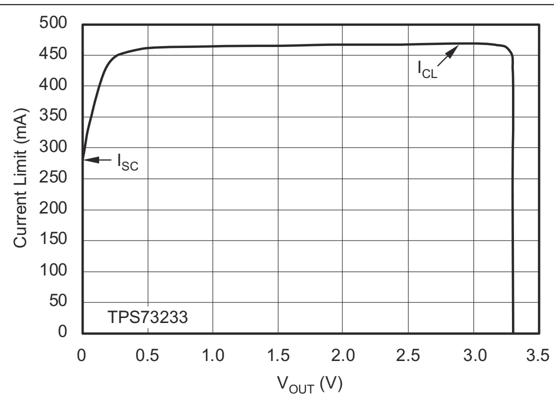
Legacy silicon

Figure 5-13. Ground Pin Current vs Temperature



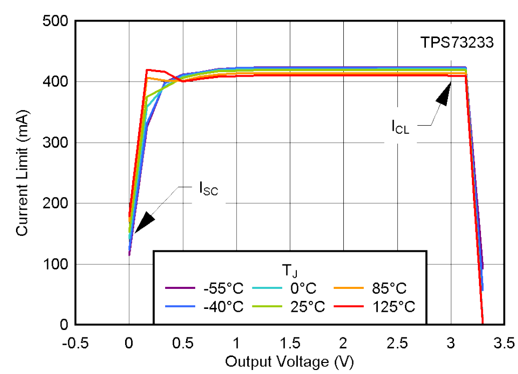
New silicon

Figure 5-14. Ground Pin Current vs Temperature



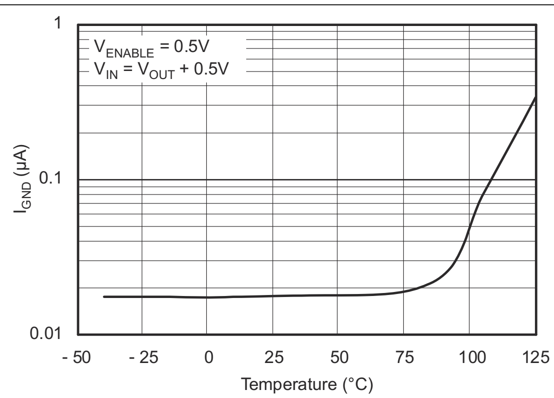
Legacy silicon

Figure 5-15. Current Limit vs V_{OUT} (FOLDBACK)



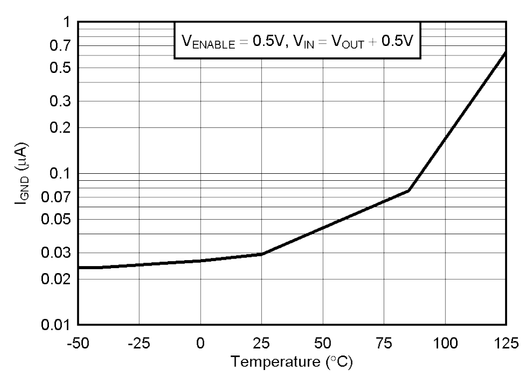
New silicon

Figure 5-16. Current Limit vs V_{OUT} (Foldback)



Legacy silicon

Figure 5-17. Ground Pin Current in Shutdown vs Temperature

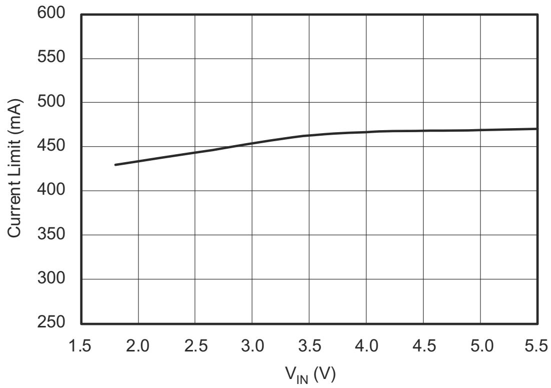


New silicon

Figure 5-18. Ground Pin Current in Shutdown vs Temperature

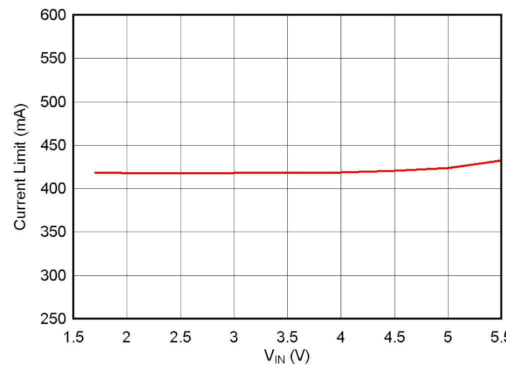
5.8 Typical Characteristics (continued)

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



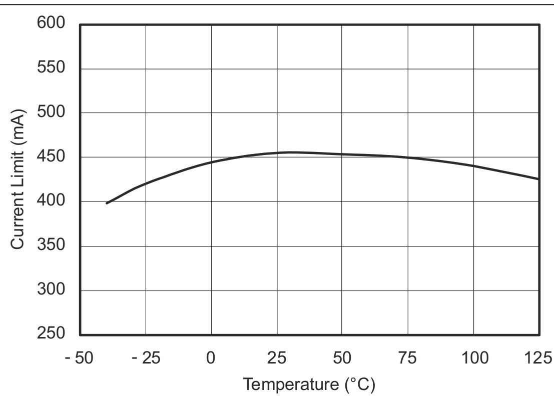
Legacy silicon

Figure 5-19. Current Limit vs V_{IN}



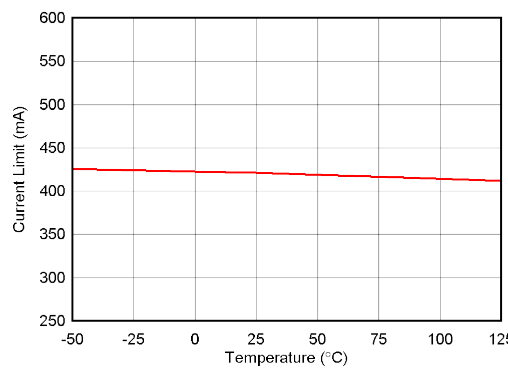
New silicon

Figure 5-20. Current Limit vs V_{IN}



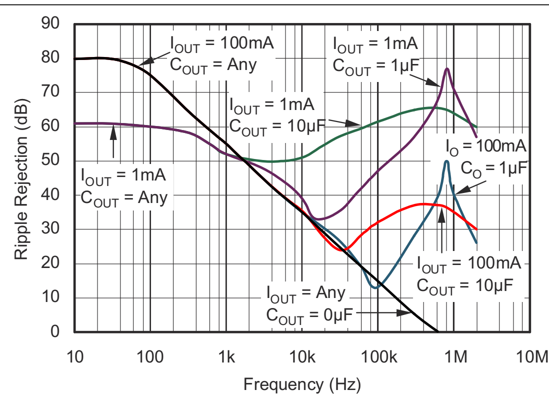
Legacy silicon

Figure 5-21. Current Limit vs Temperature



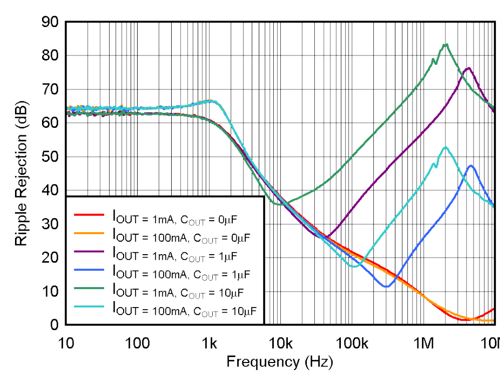
New silicon

Figure 5-22. Current Limit vs Temperature



Legacy silicon

Figure 5-23. PSRR (Ripple Rejection) vs Frequency

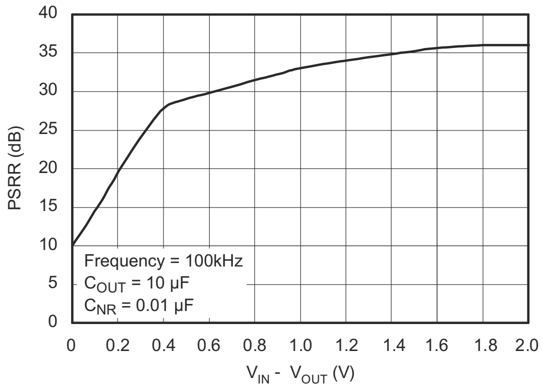


New silicon

Figure 5-24. PSRR (Ripple Rejection) vs Frequency

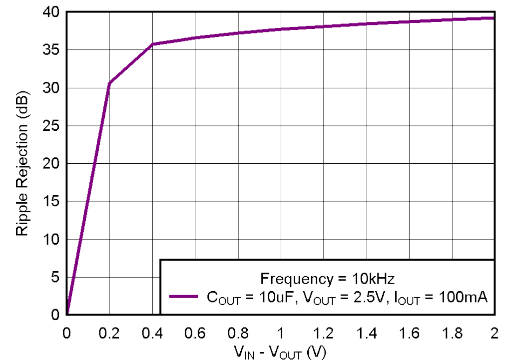
5.8 Typical Characteristics (continued)

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



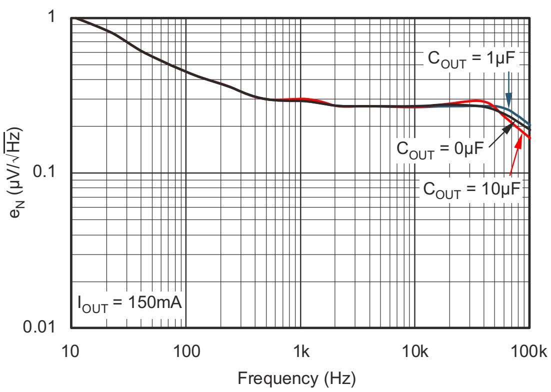
Legacy silicon

Figure 5-25. PSRR (Ripple Rejection) vs V_{IN} – V_{OUT}



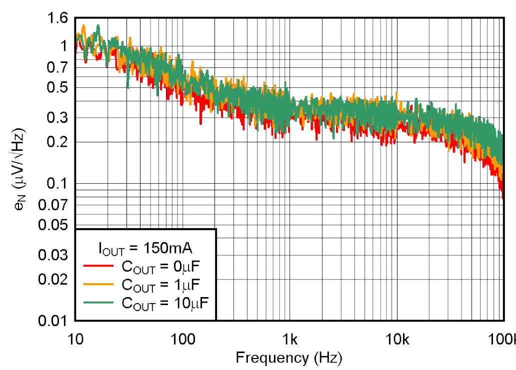
New silicon

Figure 5-26. PSRR (Ripple Rejection) vs (V_{IN} – V_{OUT})



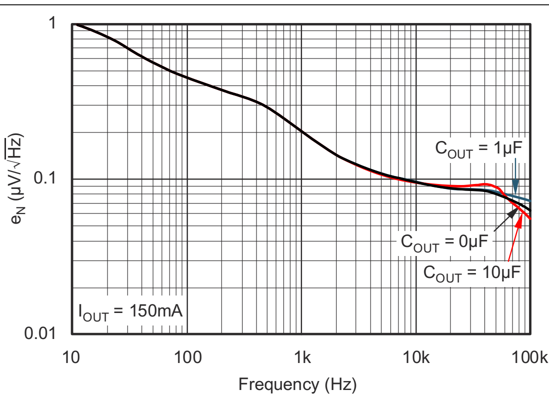
Legacy silicon

Figure 5-27. Noise Spectral Density vs C_{NR} = 0µF



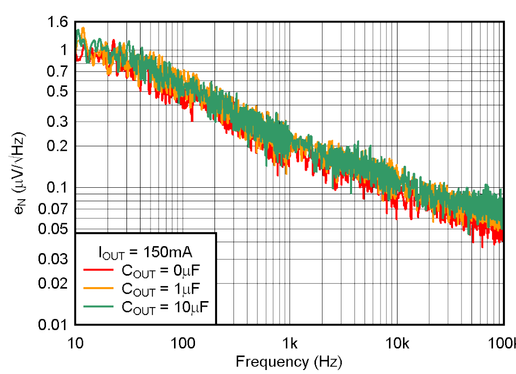
New silicon

Figure 5-28. Noise Spectral Density C_{NR} = 0µF



Legacy silicon

Figure 5-29. Noise Spectral Density vs C_{NR} = 0.01µF

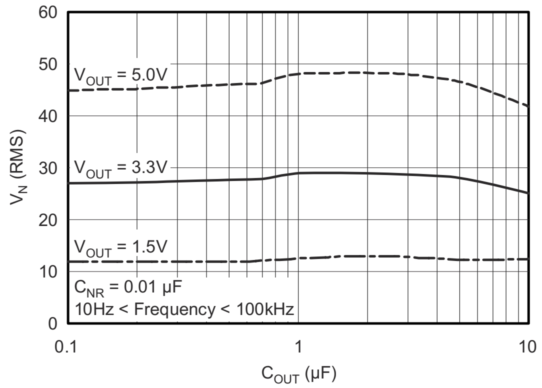


New silicon

Figure 5-30. Noise Spectral Density C_{NR} = 0.01µF

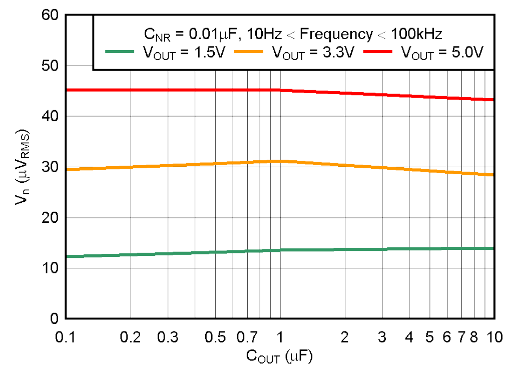
5.8 Typical Characteristics (continued)

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



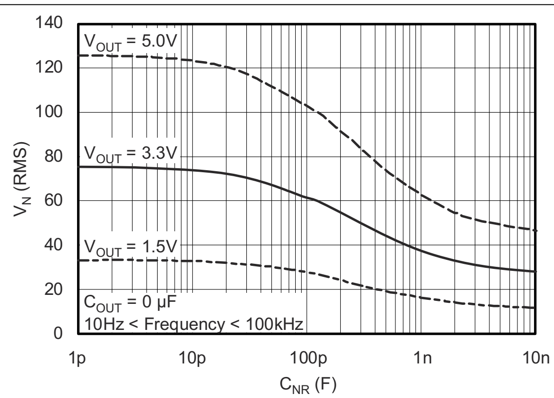
Legacy silicon

Figure 5-31. RMS Noise Voltage vs C_{OUT}



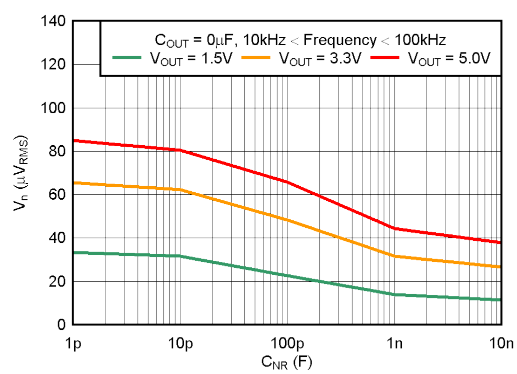
New silicon

Figure 5-32. RMS Noise Voltage vs C_{OUT}



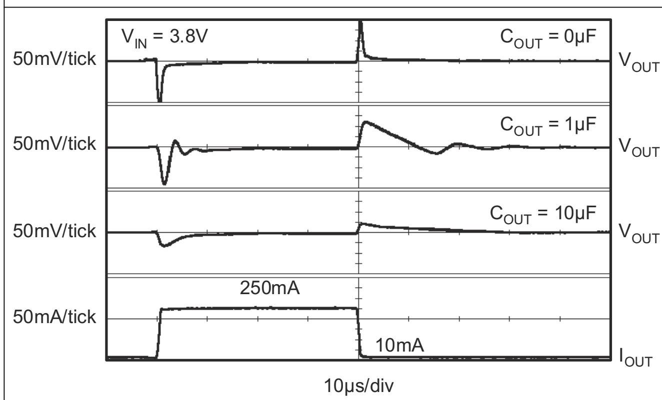
Legacy silicon

Figure 5-33. RMS Noise Voltage vs C_{NR}



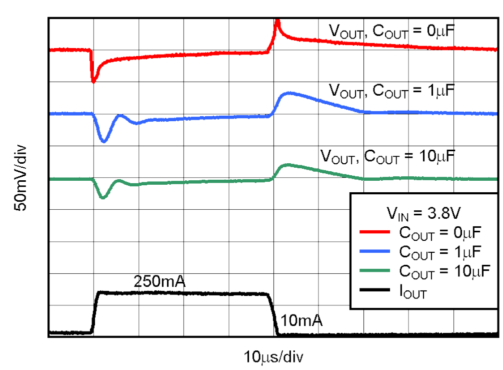
New silicon

Figure 5-34. RMS Noise Voltage vs C_{NR}



Legacy silicon

Figure 5-35. TPS73233-Q1 – Load Transient Response

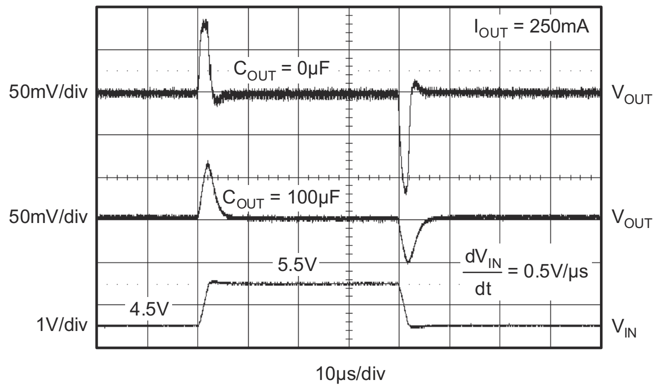


New silicon

Figure 5-36. TPS73233-Q1 Load Transient Response

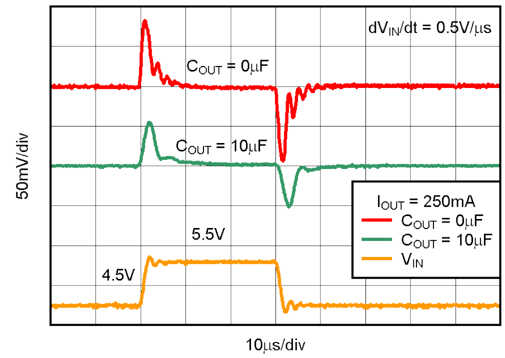
5.8 Typical Characteristics (continued)

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



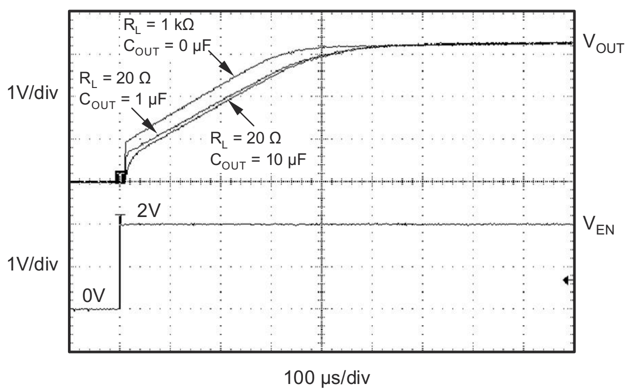
Legacy silicon

Figure 5-37. TPS73233-Q1 – Line Transient Response



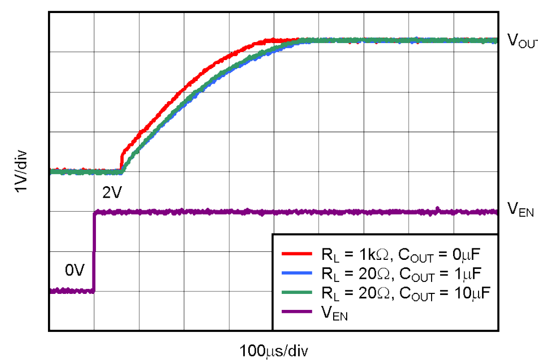
New silicon

Figure 5-38. TPS73233-Q1 Line Transient Response



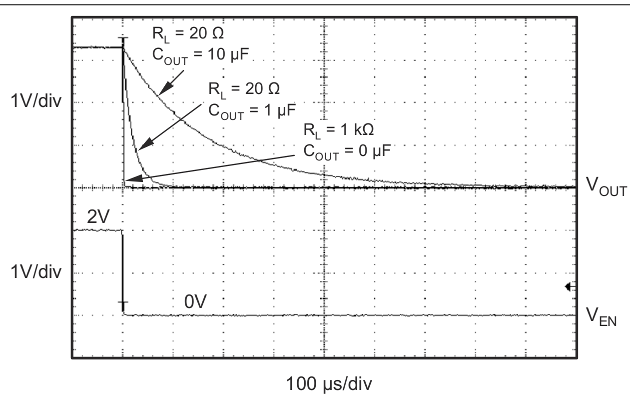
Legacy silicon

Figure 5-39. TPS73233-Q1 – Turn-On Response



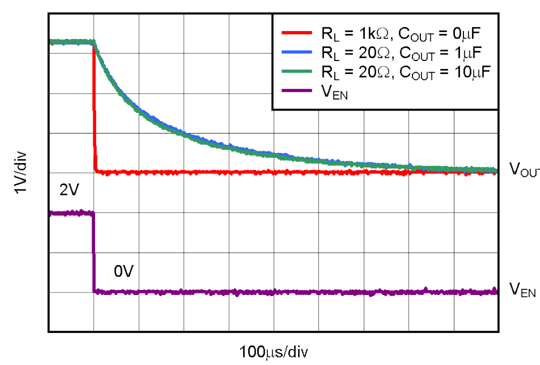
New silicon

Figure 5-40. TPS73233-Q1 Turn-On Response



Legacy silicon

Figure 5-41. TPS73233-Q1 – Turn-Off Response

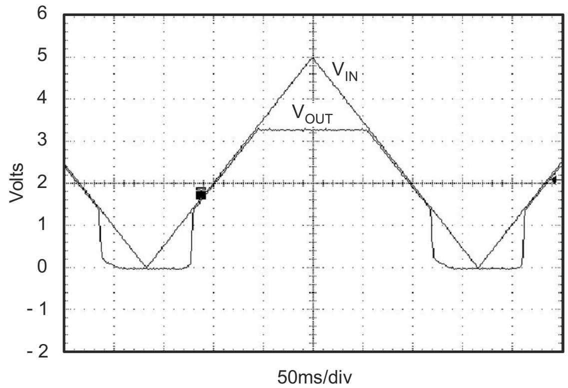


New silicon

Figure 5-42. TPS73233-Q1 Turn-Off Response

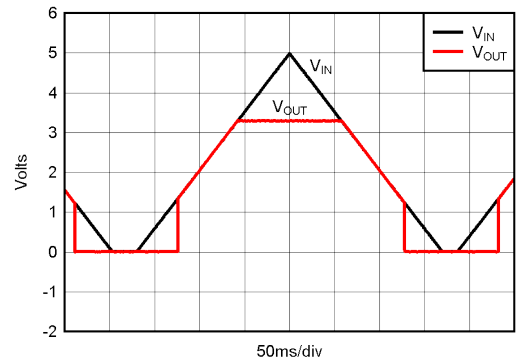
5.8 Typical Characteristics (continued)

for all voltage versions at T_J = 25°C, $V_{IN} = V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



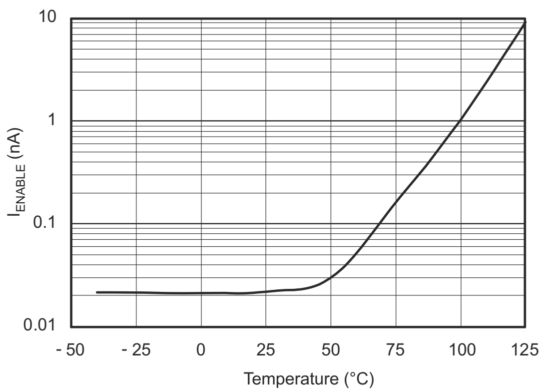
Legacy silicon

Figure 5-43. TPS73233-Q1 – Power-Up and Power-Down



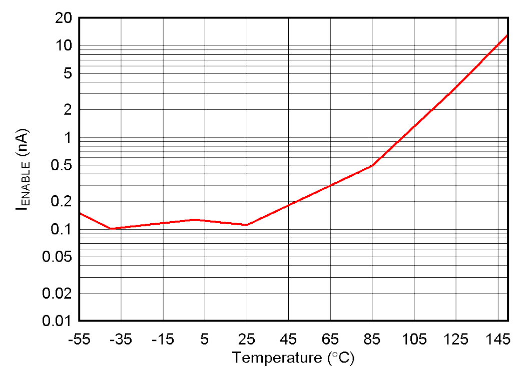
New silicon

Figure 5-44. TPS73233-Q1 Power-Up and Power-Down



Legacy silicon

Figure 5-45. I_{ENABLE} vs Temperature



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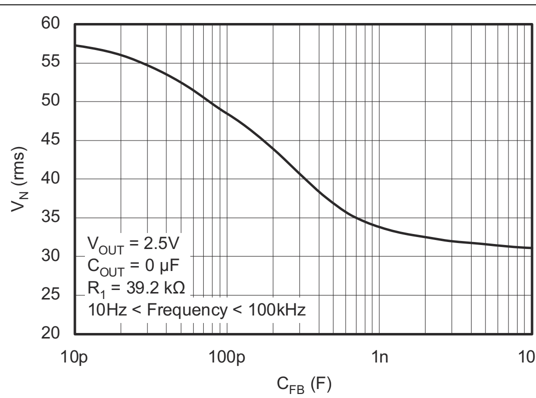
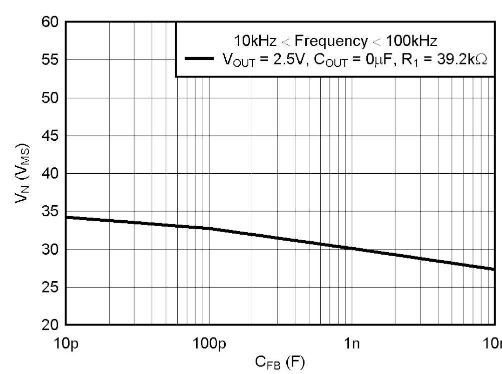
New silicon

Figure 5-46. I_{ENABLE} vs Temperature



Legacy silicon

Figure 5-47. TPS73201-Q1 – RMS Noise Voltage vs C_{ADJ}

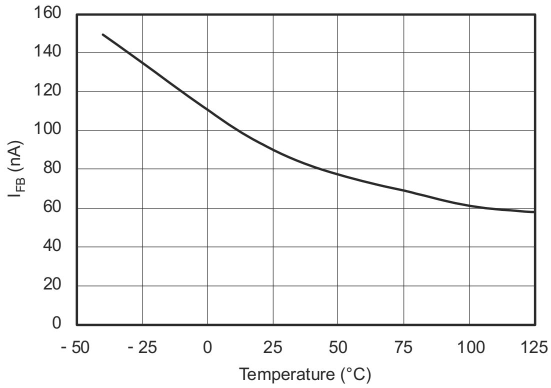


New silicon

Figure 5-48. TPS73201-Q1 RMS Noise Voltage vs C_{FB}

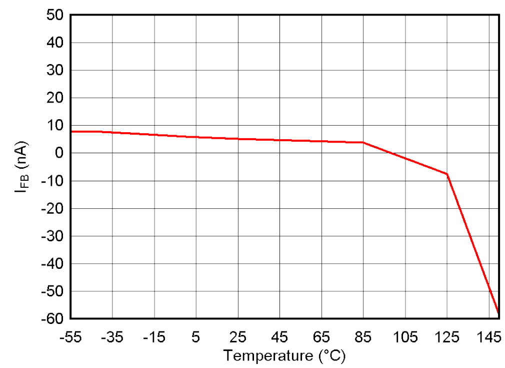
5.8 Typical Characteristics (continued)

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



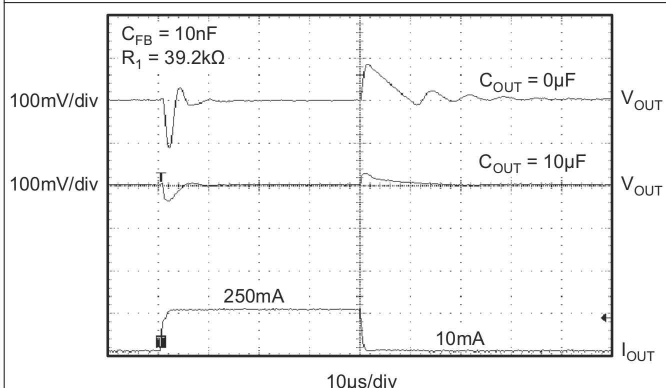
Legacy silicon

Figure 5-49. TPS73201-Q1 – I_{FB} vs Temperature



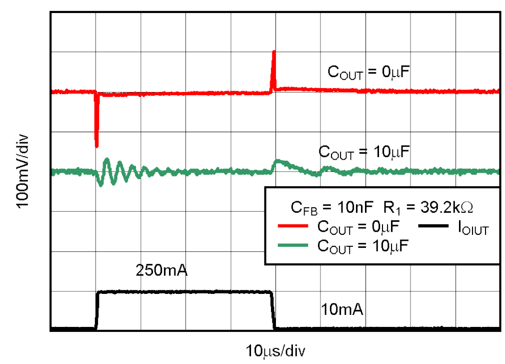
New silicon

Figure 5-50. TPS73201-Q1 I_{FB} vs Temperature



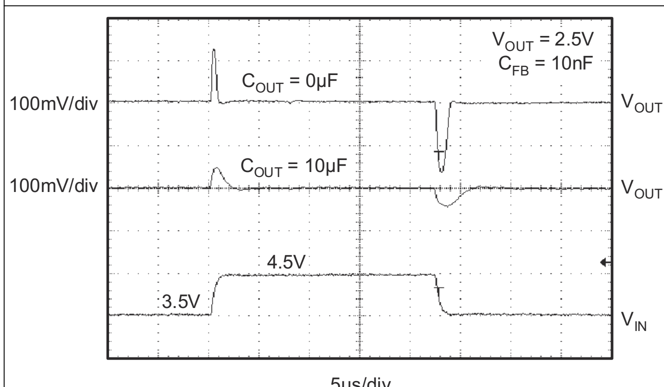
Legacy silicon

Figure 5-51. TPS73201-Q1 – Load Transient, Adjustable Version



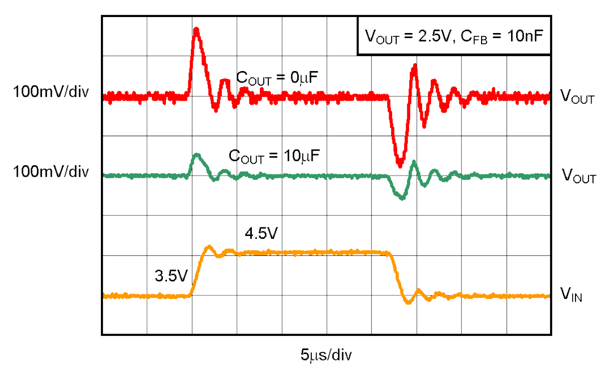
New silicon

Figure 5-52. TPS73201-Q1 Load Transient, Adjustable Version



Legacy silicon

Figure 5-53. TPS73201-Q1 – Line Transient, Adjustable Version



New silicon

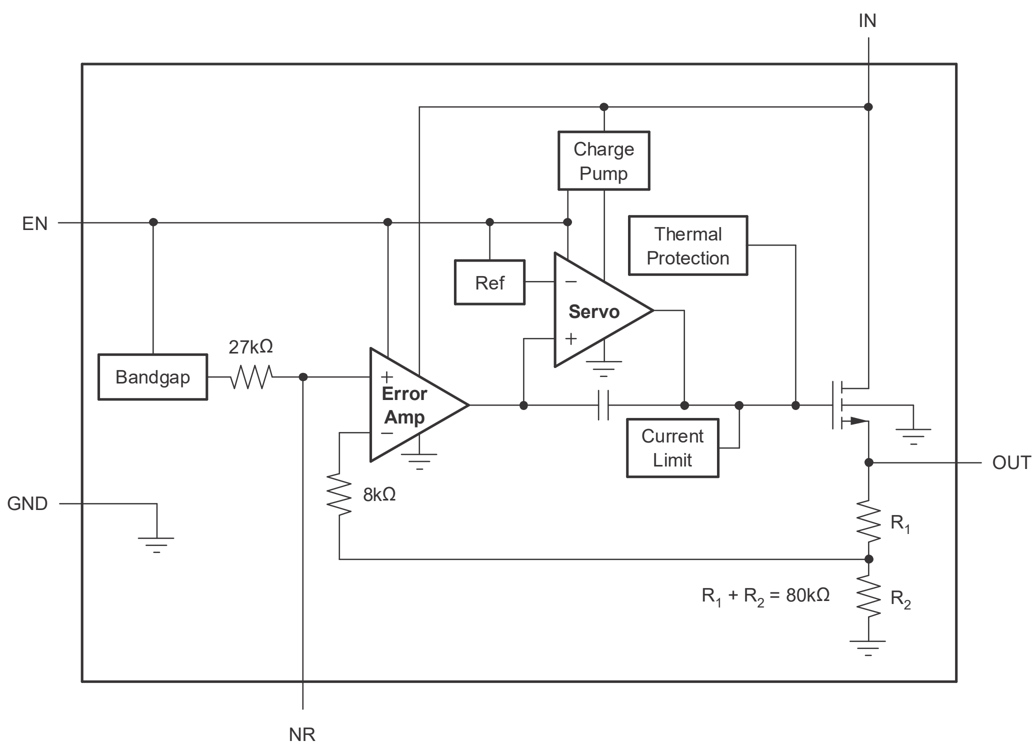
Figure 5-54. TPS73201-Q1 Line Transient, Adjustable Version

6 Detailed Description

6.1 Overview

The TPS732-Q1 low-dropout linear regulator devices operate with an input voltage down to 1.7V and support output voltages down to 1.2V while sourcing up to 250mA of load current. These linear regulators use an NMOS pass element with an integrated 4MHz charge pump to provide a dropout voltage of less than 150mV at full load current. This unique architecture also permits stable regulation over a wide range of output capacitors. In fact, the TPS732-Q1 family of devices does not require any output capacitor for stability. The increased insensitivity to the output capacitor value and type makes this family of linear regulators an ideal choice when powering a load where the effective capacitance is unknown. The TPS732-Q1 family of devices also features a noise reduction (NR) pin that allows for additional reduction of the output noise. The low noise output featured by the TPS732-Q1 family makes the device well-suited for powering VCOs or any other noise-sensitive load.

6.2 Functional Block Diagram



Fixed voltage version.

6.3 Feature Description

6.3.1 Internal Current Limit

The TPS732-Q1 internal current limit helps protect the regulator during fault conditions. Foldback helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5V. See Figure 5-15.

6.3.2 Shutdown

The enable pin is active high and is compatible with standard TTL-CMOS levels. V_{EN} below 0.5V (maximum) turns the regulator off and drops the ground pin current to approximately 10nA. When shutdown capability is not required, the Enable pin can be connected to V_{IN}. When a pullup resistor is used, and operation down to 1.8V is required, use pullup resistor values below 50kΩ.

6.3.3 Dropout Voltage

The TPS732-Q1 family of devices uses an NMOS pass transistor to achieve extremely low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the NMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS\text{-}ON}$ of the NMOS pass element.

For large step changes in load current, the TPS732-Q1 family of devices requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the dc dropout. Values of V_{IN} – V_{OUT} above this line provide normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom (V_{IN} to V_{OUT} voltage drop). Under worst-case conditions [full-scale instantaneous load change with (V_{IN} – V_{OUT}) close to dc dropout levels], the TPS732-Q1 family of devices can take a couple of hundred microseconds to return to the specified regulation accuracy.

6.3.4 Transient Response

The low open-loop output impedance provided by the NMOS pass element in a voltage follower configuration allows operation without an output capacitor for many applications. As with any regulator, the addition of a capacitor (nominal value 1µF) from the output pin to ground reduces undershoot magnitude but increase duration. In the adjustable version, the addition of a capacitor, C_{FB}, from the output to the adjust pin also improves the transient response.

The TPS732-Q1 family of devices does not have active pulldown when the output is over-voltage. This allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This also results in an output overshoot of several percent if the load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor C_{OUT} and the internal and external load resistance. The rate of decay is given by Equation 1 and Equation 2:

Fixed voltage version:

$$ {}^{dV}\!/_{dt} = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega} \tag{1} $$

Adjustable voltage version:

$$ {}^{dV}\!/_{dt} = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \,||\, (R_1 + R_2)} \tag{2} $$

6.3.5 Reverse Current

The NMOS pass element of the TPS732-Q1 family of devices provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass device is pulled low. To verify that all charge is removed from the gate of the pass element, the enable pin must be driven low before the input voltage is removed. If this is not done, the pass element can be left on due to stored charge on the gate.

After the enable pin is driven low, no bias voltage is needed on any pin for reverse current blocking. Note that reverse current is specified as the current flowing out of the IN pin due to voltage applied on the OUT pin. There is additional current flowing into the OUT pin due to the 80kΩ internal resistor divider to ground (see the *Functional Block Diagram* and Figure 7-3).

For the TPS73201-Q1, reverse current can flow when V_{FB} is more than 1V above V_{IN}.

6.3.6 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This limits the dissipation of the regulator, protecting the device from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature must be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS732-Q1 family of devices is designed to protect against overload conditions. The protection circuitry is not intended to replace proper heatsinking. Continuously running the TPS732-Q1 family of devices into thermal shutdown degrades device reliability.

6.4 Device Functional Modes

6.4.1 Normal Operation

The TPS732-Q1 family of devices require an input voltage of at least 1.7V to function properly and attempt to maintain regulation.

When operating the device near 5.5V, take care to suppress any transient spikes that can exceed the 6V absolute maximum voltage rating. The device must never operate at a DC voltage greater than 5.5V.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS732-Q1 belongs to a family of new generation LDO regulators that use an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features, combined with low noise and an enable input, make the TPS732-Q1 family of devices ideal for portable applications. This regulator family offers a wide selection of fixed output voltage versions and an adjustable output version. All versions have thermal and overcurrent protection, including foldback current limit.

7.2 Typical Application

Figure 7-1 shows the basic circuit connections for the fixed voltage models. Figure 7-2 gives the connections for the adjustable output version (TPS73201-Q1).

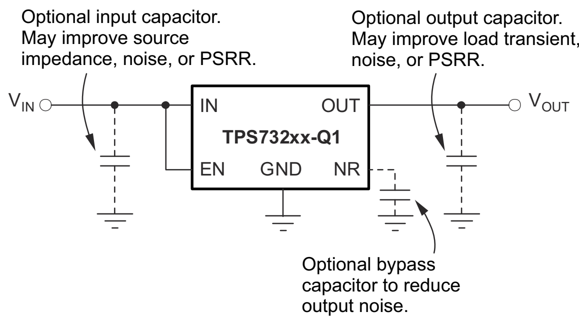


Figure 7-1. Typical Application Circuit for Fixed-Voltage Versions

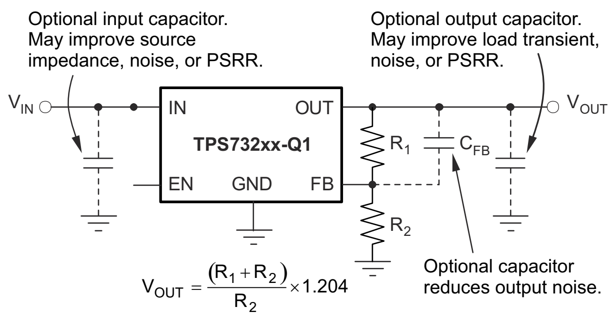
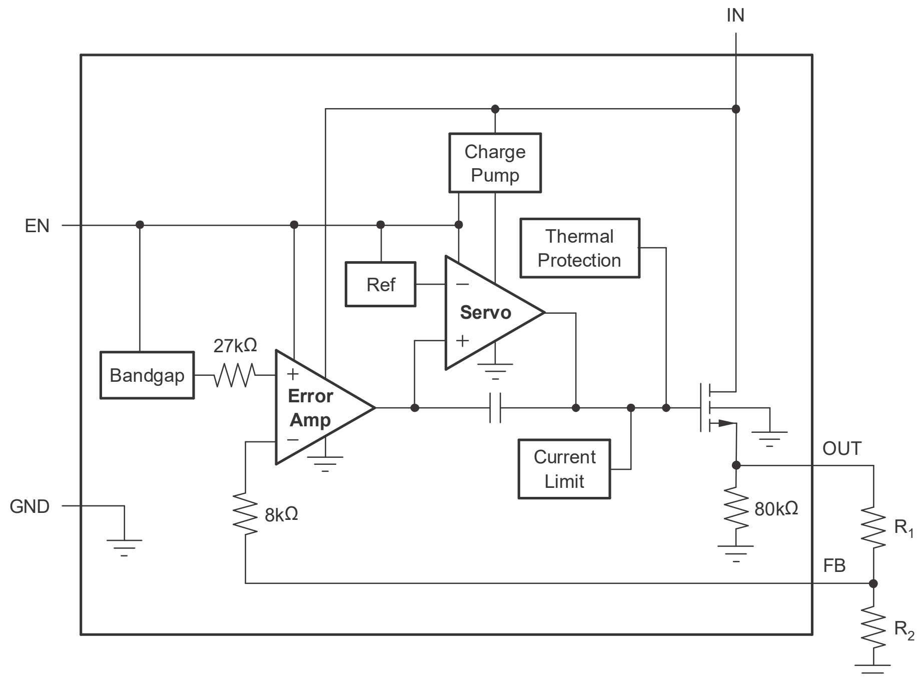


Figure 7-2. Typical Application Circuit for Adjustable-Voltage Versions

7.2.1 Design Requirements

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 7-2. Sample resistor values for common output voltages are shown in Figure 7-3. For best accuracy, make the parallel combination of R_1 and R_2 approximately 19kΩ.



$V_{OUT} = (R_1 + R_2) / R_2 \times 1.204$
$R_1 \,||\, R_2 \cong 19k\Omega$ for best accuracy.

Figure 7-3. Adjustable Voltage Version

Table 7-1. Standard 1% Resistor Values for Common Output Voltages

V_{OUT}	R_1	R_2
1.2V	Short	Open
1.5V	23.2kΩ	95.3kΩ
1.8V	28kΩ	56.2kΩ
2.5V	39.2kΩ	36.5kΩ
2.8V	44.2kΩ	33.2kΩ
3V	46.4kΩ	30.9kΩ
3.3V	52.3kΩ	30.1kΩ
5V	78.7kΩ	24.9kΩ

7.2.2 Detailed Design Procedure

7.2.2.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1μF to 1μF low ESR capacitor across the input supply near the regulator. This counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor can be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS732-Q1 family of devices does not require an output capacitor for stability and has maximum phase margin with no capacitor. The devices are designed to be stable for all available types and values of capacitors. In applications where $V_{IN} – V_{OUT}$ < 0.5V and multiple low ESR capacitors are in parallel, ringing can occur when the product of C_{OUT} and total ESR drops below 50nF×Ω. Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance meets this requirement.

7.2.2.2 Output Noise

A precision band-gap reference is used to generate the internal reference voltage, V_{REF}. This reference is the dominant noise source within the TPS732-Q1 family of devices and generates approximately 32μV_{RMS} (10Hz to 100kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by:

$$V_N = 32\mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32\mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \tag{3}$$

Because the value of V_{REF} is 1.2V, this relationship reduces to:

$$V_N(\mu V_{RMS}) = 27\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \tag{4}$$

where

- C_{NR} does not exist

An internal 27kΩ resistor in series with the noise reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise reduction capacitor, C_{NR}, is connected from NR to ground. For C_{NR} = 10nF, the total noise in the 10Hz to 100kHz bandwidth is reduced by a factor of approximately 3.2, giving the approximate relationship:

$$V_N(\mu V_{RMS}) = 8.5\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \tag{5}$$

where

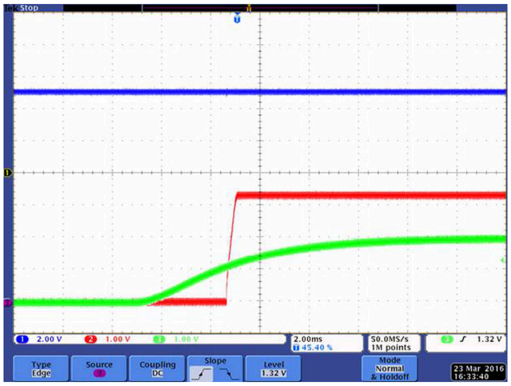
- C_{NR} = 10nF

This noise reduction effect is shown as *RMS Noise Voltage vs C_{NR}* in *Typical Characteristics*.

The TPS73201-Q1 adjustable version does not have the noise-reduction pin available. However, connecting a feedback capacitor, C_{FB}, from the output to the FB pin reduces output noise and improve load transient performance.

The TPS732-Q1 family of devices uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass element above V_{OUT}. The charge pump generates approximately 250μV of switching noise at approximately 2MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT}.

7.2.3 Application Curves



Legacy silicon

Figure 7-4. Start-Up

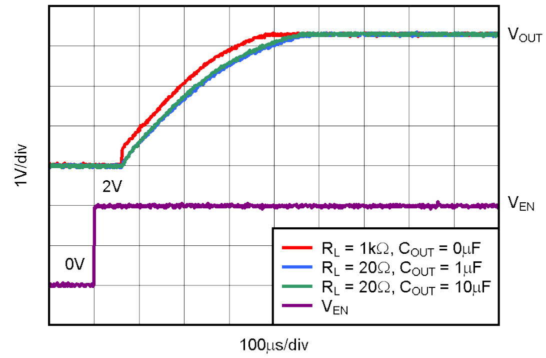


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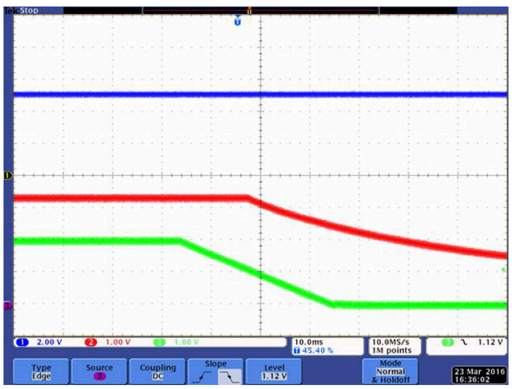
Figure 7-5. Start-up



Legacy silicon

Figure 7-6. Shutdown

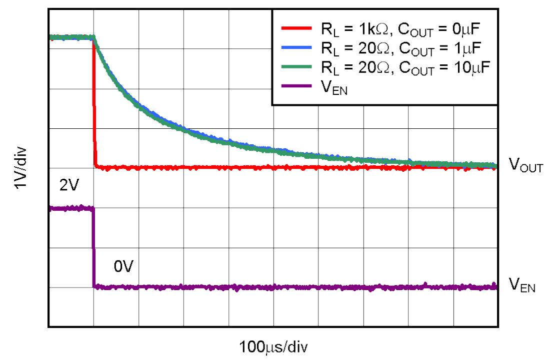


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Figure 7-7. Shutdown

7.3 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range from 1.7V to 5.5V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

7.4 Layout

7.4.1 Layout Guidelines

To improve ac performance such as PSRR, output noise, and transient response, design the PCB with ground plane connections for V_{IN} and V_{OUT} capacitors, and the ground plane connected at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

7.4.1.1 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improve the heat-sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{6}$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to provide the required output voltage.

7.4.2 Layout Examples

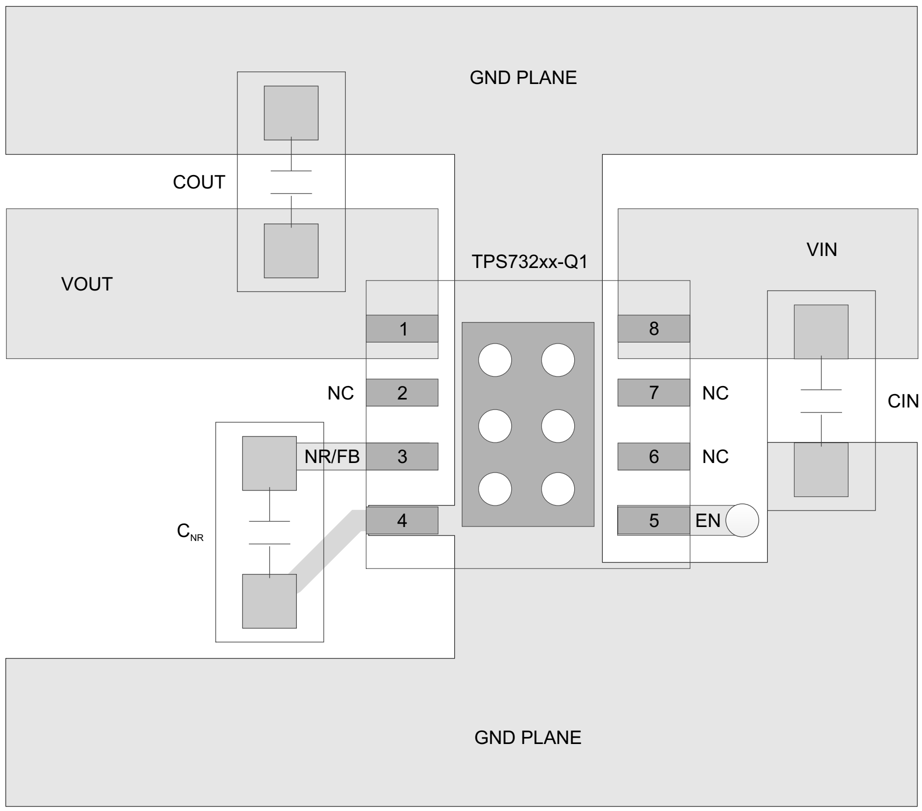


Figure 7-8. Fixed Output Voltage Option Layout (DRB Package)

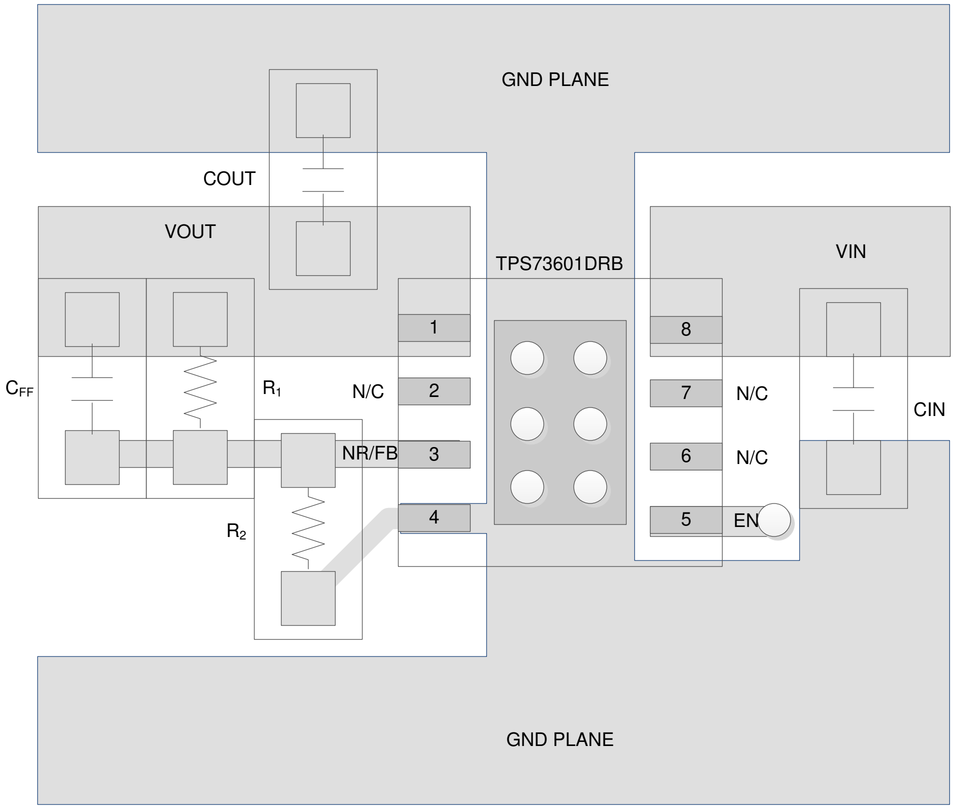


Figure 7-9. Adjustable Output Voltage Option Layout (DRB Package)

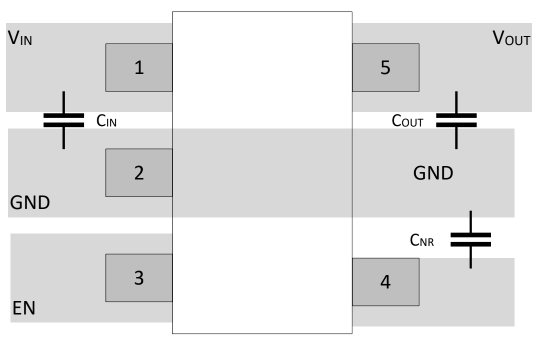


Figure 7-10. Layout Example for the DBV Package (Fixed Version)

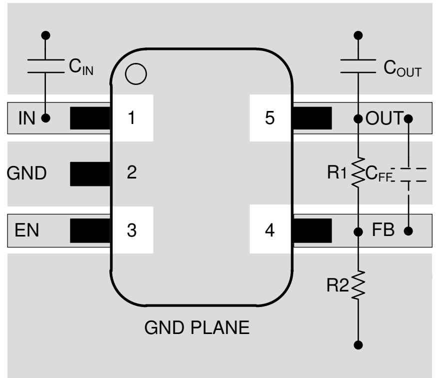


Figure 7-11. Layout Example for the DBV Package (Adjustable Version)

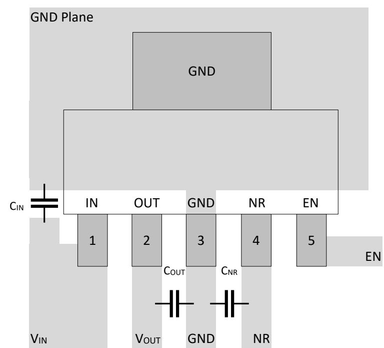


Figure 7-12. Layout Example for the DCQ Package (Fixed Version)

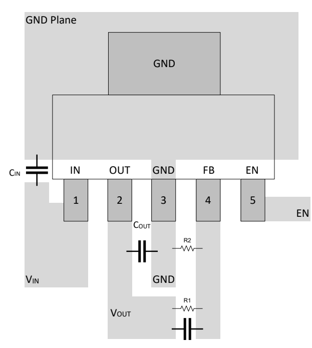


Figure 7-13. Layout Example for the DCQ Package (Adjustable Version)

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

Table 8-1. Ordering Information

PRODUCT	DESCRIPTION(1)
TPS732**xxQyyyz(M3)Q1**	**xx** is the nominal output voltage (for example, 25 = 2.5 V, 01 = Adjustable (2)). **Q** indicates that the device is a grade-1 device in accordance with the AEC-Q100 standard. **yyy** is the package designator. **z** is the package quantity. **M3** is a suffix designator for devices that only use the latest manufacturing flow (CSO: RFB). Devices without this suffix can ship with the *legacy silicon* (CSO: DLN) or the *new silicon* (CSO: RFB). The reel packaging label provides CSO information to distinguish which silicon is being used. Device performance for new and legacy silicon is denoted throughout the document. **Q1** indicates that this device is an automotive grade (AEC-Q100) device.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.
(2) For fixed 1.20V operation, tie FB to OUT.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (December 2024) to Revision H (July 2025) **Page**

- Updated DRB (VSON) for DRB0008A package outline........ 4
- Added new silicon DBV thermals........ 4
- Added new silicon ground pin current spec........ 6
- Deleted *Package Mounting* section........ 22

Changes from Revision F (April 2016) to Revision G (December 2024) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document........ 1
- Changed entire document to align with current family format........ 1
- Added M3 devices to document........ 1

Changes from Revision E (August 2013) to Revision F (April 2016) **Page**

- Added *Device Information* table, *Table of Contents*, *Specifications* section, *ESD Ratings* table, *Recommended Operating Conditions* table, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS73201QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJOQ
TPS73201QDBVRQ1.A	Active	Production	null (null) |	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See TPS73201QDBVRQ1	PJOQ
TPS73201QDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	PSAQ
TPS73201QDRBRQ1.A	Active	Production	null (null) |	3000 | LARGE T&R	-	NIPDAU	Level-3-260C-168 HR	See TPS73201QDRBRQ1	PSAQ
TPS73218QDCQRM3Q1	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	73218Q
TPS73218QDCQRM3Q1.A	Active	Production	null (null) |	2500 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	See TPS73218QDCQRM3Q1	73218Q
TPS73218QDCQRQ1	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	73218Q
TPS73218QDCQRQ1.A	Active	Production	null (null) |	2500 | LARGE T&R	-	NIPDAU	Level-3-260C-168 HR	See TPS73218QDCQRQ1	73218Q
TPS73250QDCQRQ1	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	73250Q
TPS73250QDCQRQ1.A	Active	Production	null (null) |	2500 | LARGE T&R	-	NIPDAU	Level-3-260C-168 HR	See TPS73250QDCQRQ1	73250Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

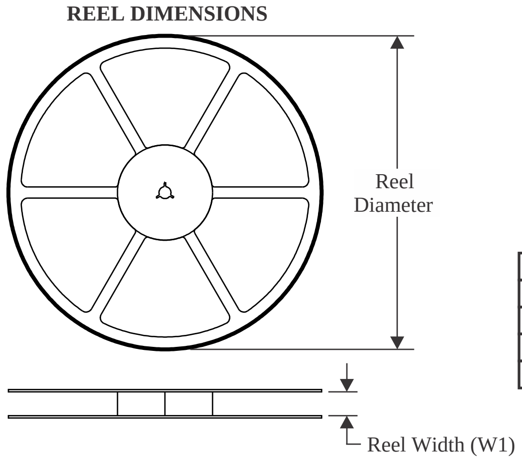
OTHER QUALIFIED VERSIONS OF TPS732-Q1 :

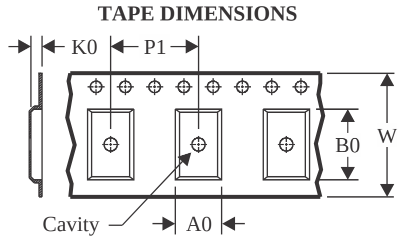
- Catalog : TPS732

NOTE: Qualified Version Definitions:

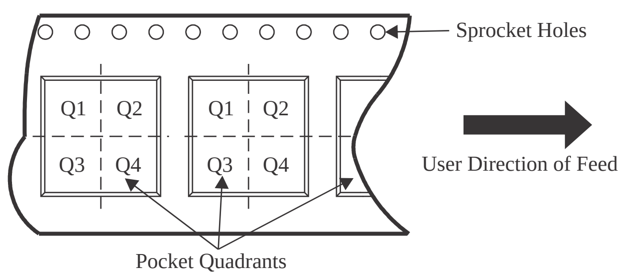
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION





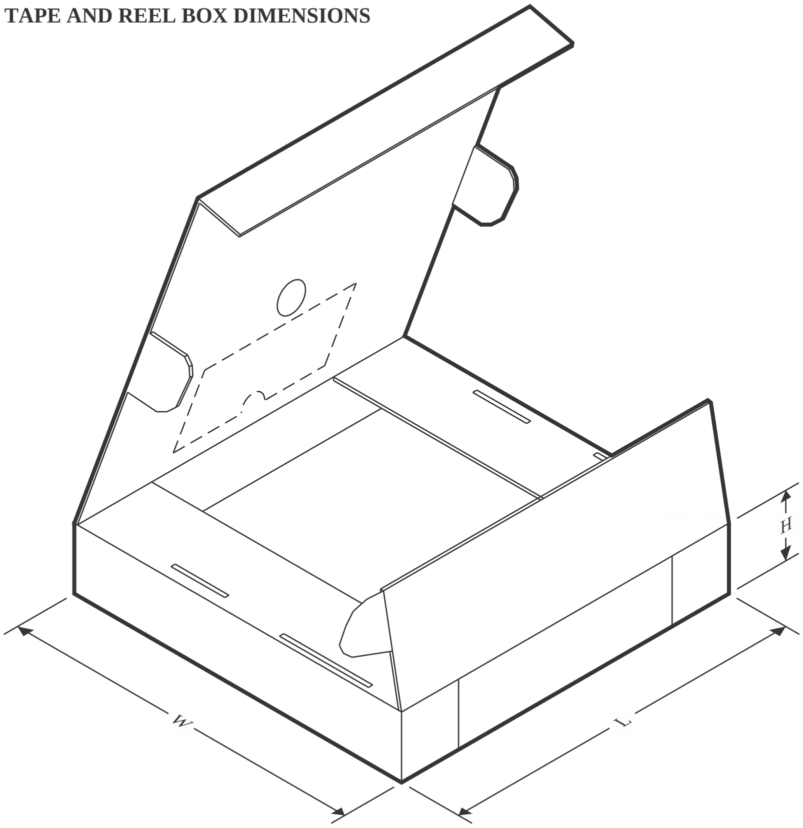
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

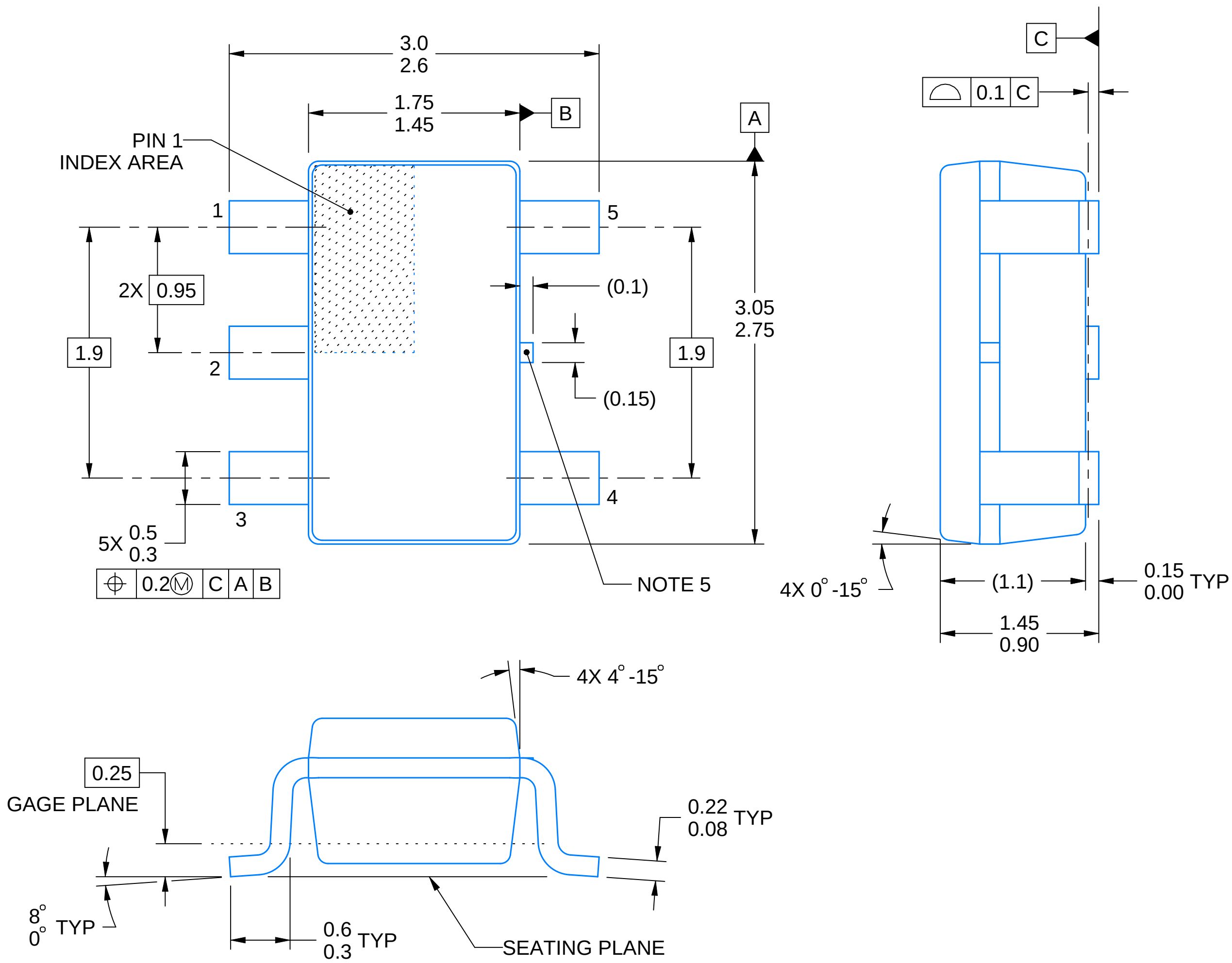
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73201QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73201QDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73218QDCQRQ1	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73250QDCQRQ1	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

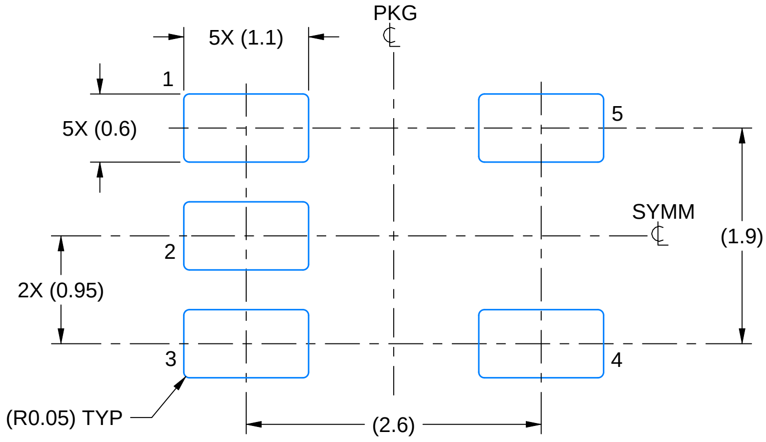
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73201QDBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS73201QDRBRQ1	SON	DRB	8	3000	353.0	353.0	32.0
TPS73218QDCQRQ1	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS73250QDCQRQ1	SOT-223	DCQ	6	2500	346.0	346.0	29.0



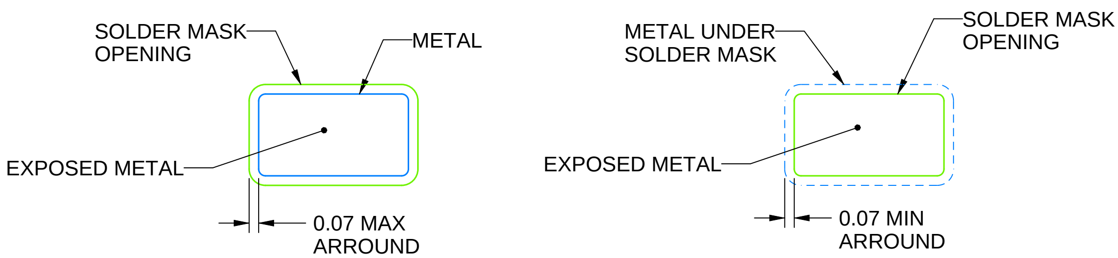
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)

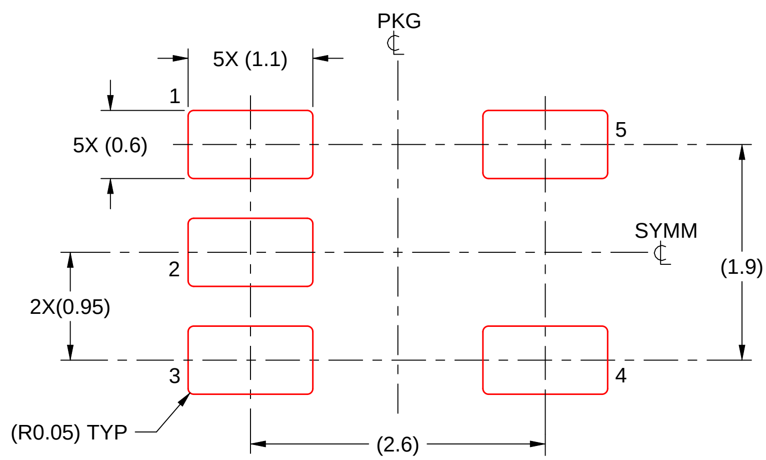
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

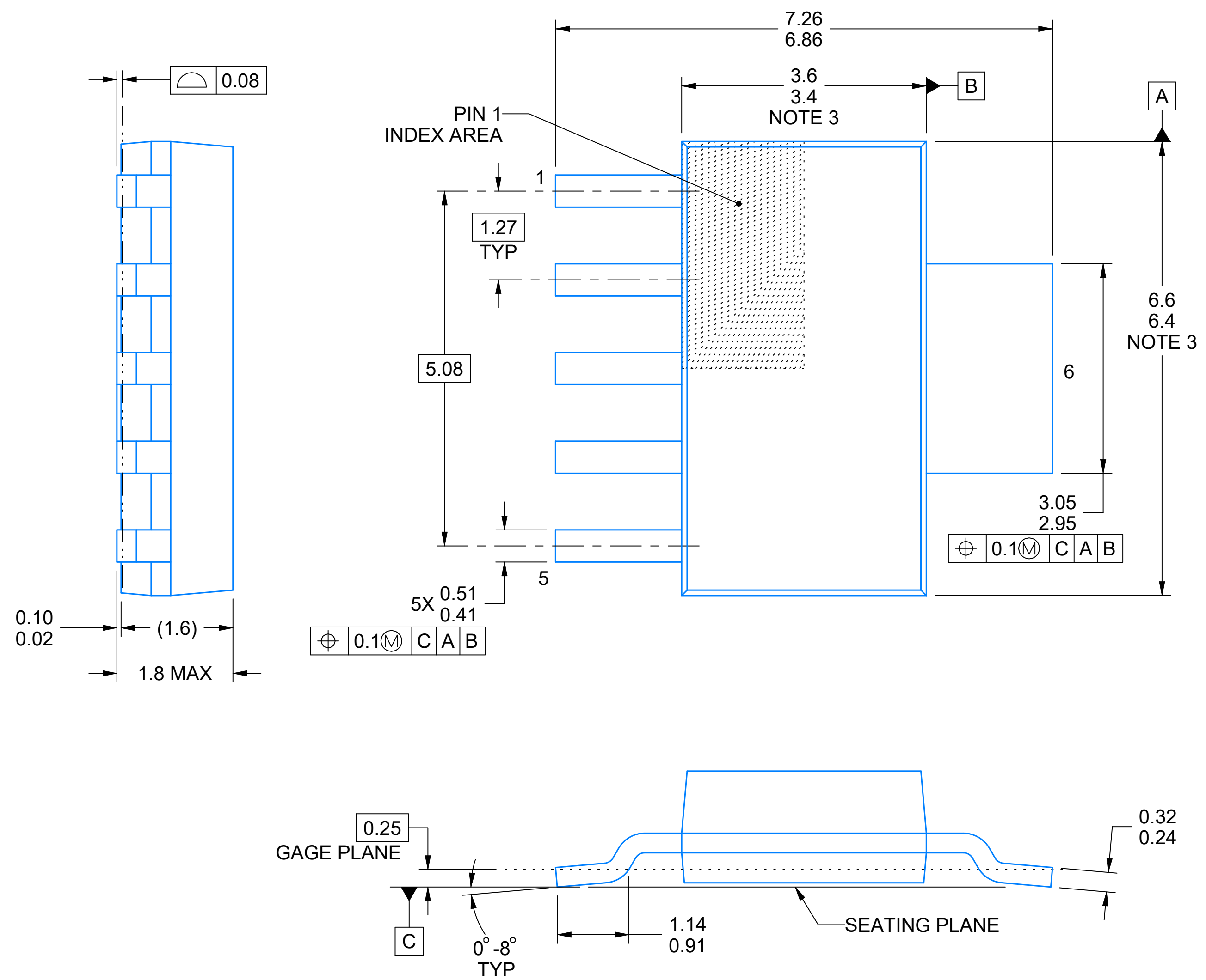


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

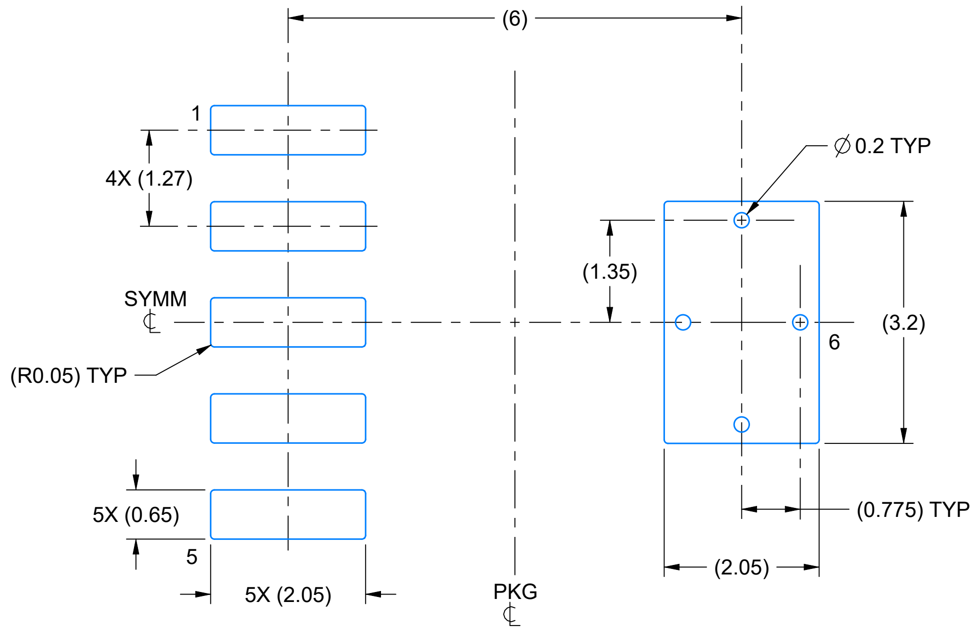
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



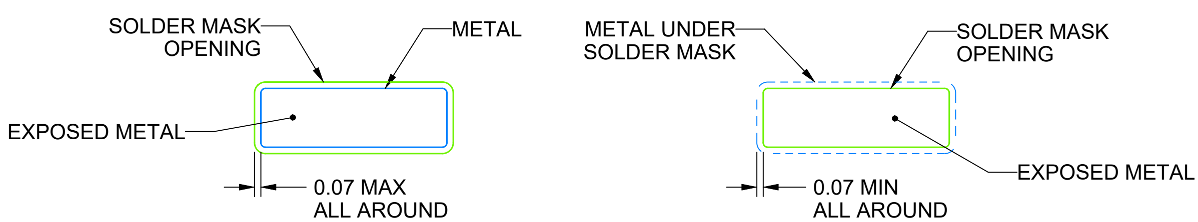
4214845/C 11/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

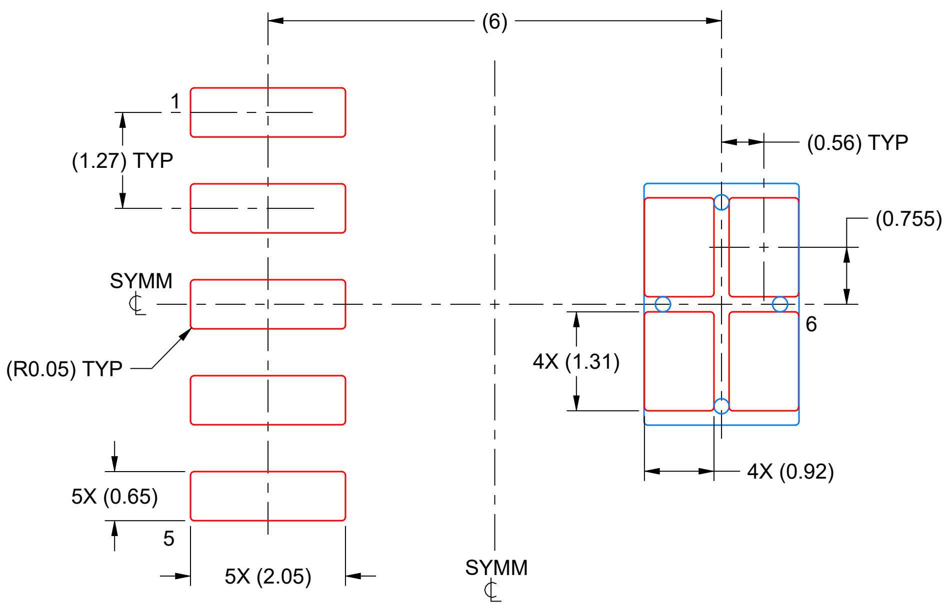


SOLDER MASK DETAILS

4214845/C 11/2021

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214845/C 11/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

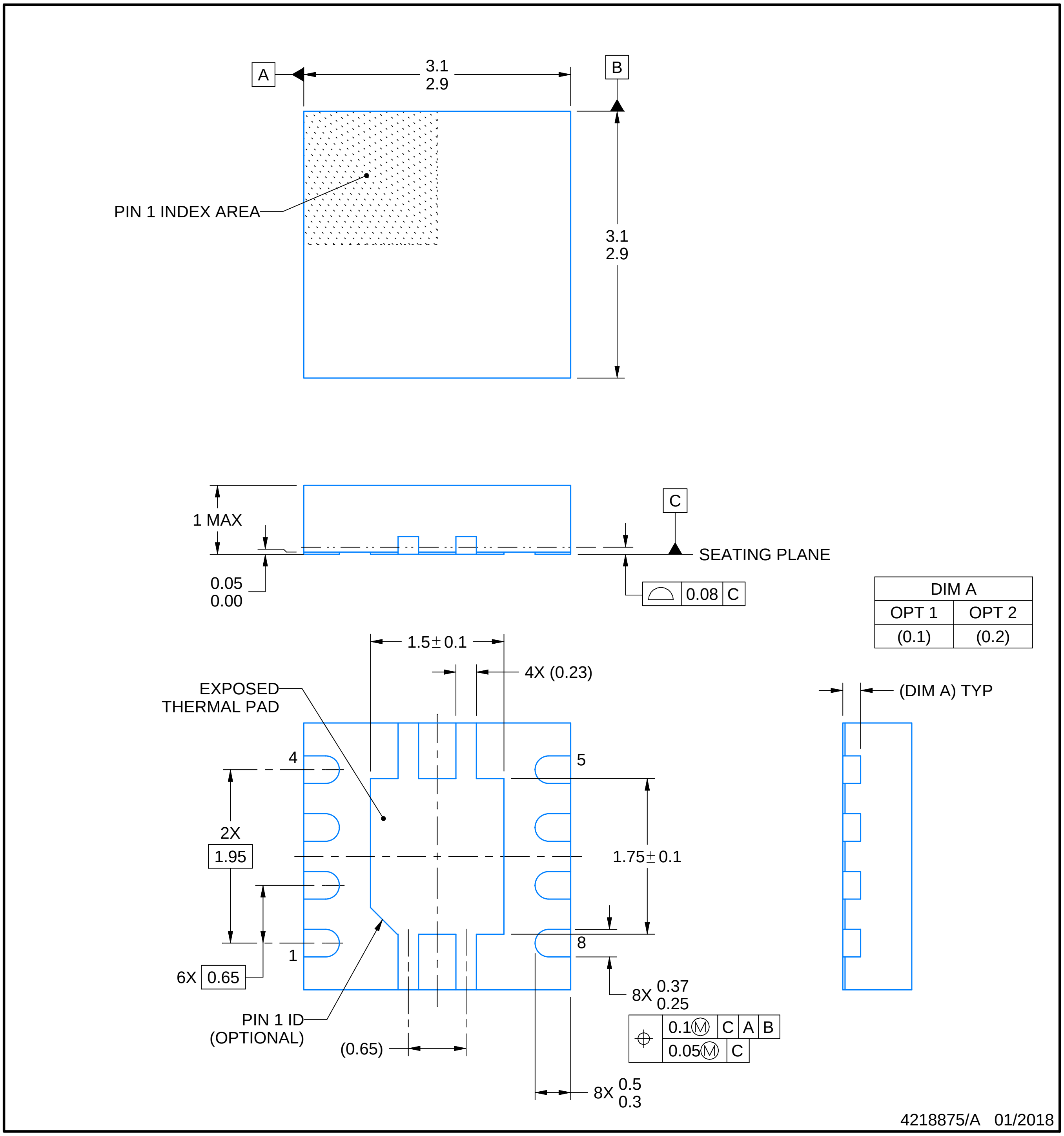
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DRB0008A

PACKAGE OUTLINE

VSON - 1 mm max height

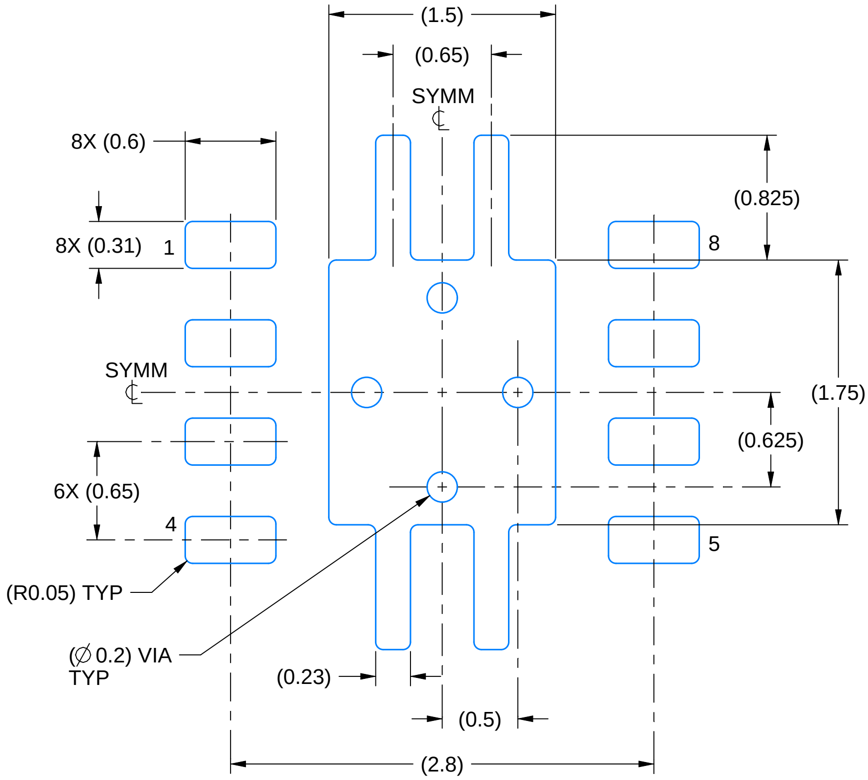
PLASTIC SMALL OUTLINE - NO LEAD



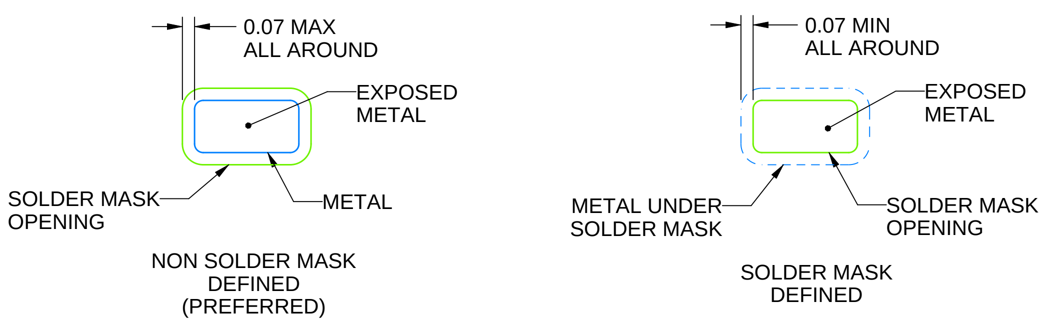
DIM A	
OPT 1	OPT 2
(0.1)	(0.2)

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

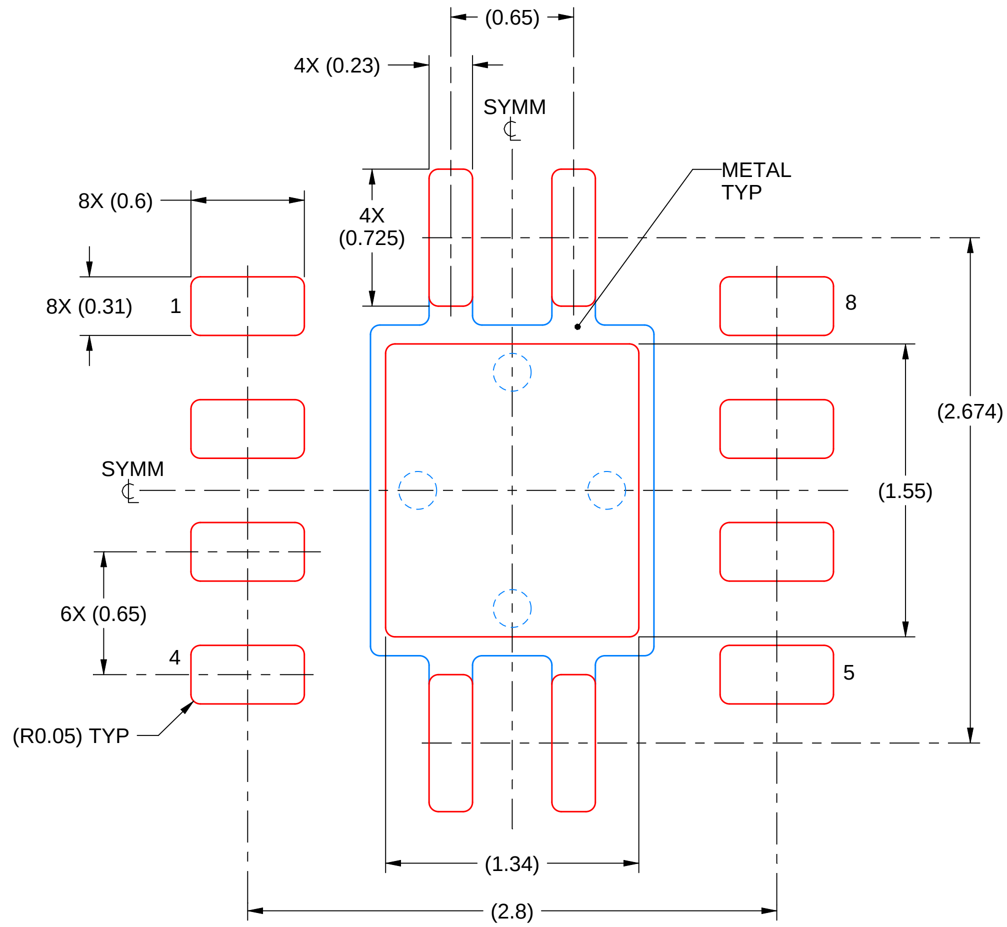


SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.